NEC Electronics Inc.

μPB100474
1,024 x 4-Bit
100K ECL RAM

Description

NEC's μPB100474 is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with open-emitter, noninverted outputs. It is available in a 24-pin cerdip, 24-pin ceramic LCC, or 24-pin ceramic flatpack package.

Features

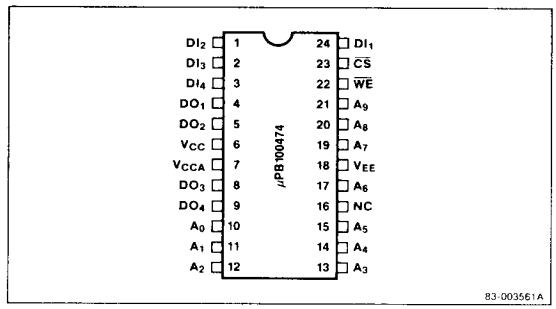
- 1024-word by 4-bit organization
- 100K interface ECL
- Full voltage and temperature compensation
- Noninverted, open emitter outputs
- Fast access times
- 24-pin cerdip, ceramic LCC, and ceramic flatpack packaging

Ordering Information

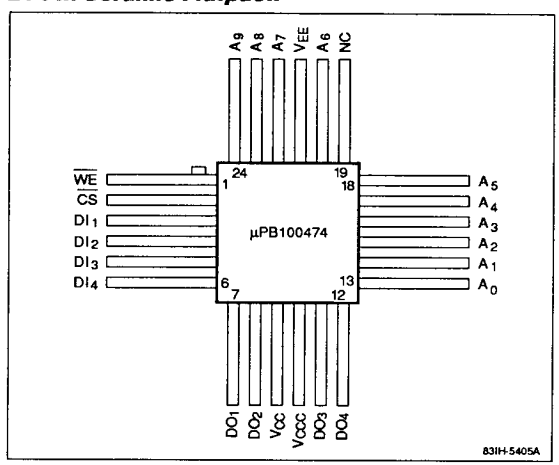
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474B-6	6 ns	−450 mA	24-pin ceramic flatpack
B-8	8 ns	−220 mA	
B-10	10 ns		
B-15	15 ns		
μPB100474D-8	8 ns	−220 mA	24-pin cerdip
D-10	10 ns		
D-15	15 ns		
μPB100474K-4.5	4.5 ns	−450 mA	24-pin ceramic LCC
K-6	6 ns		

Pin Configurations

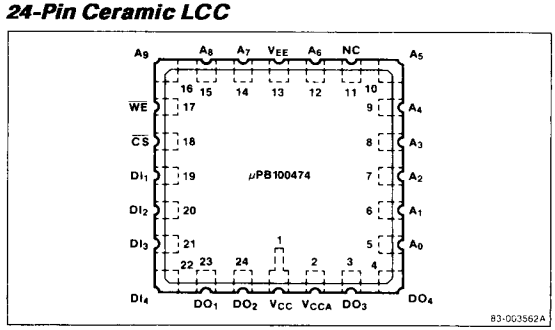
24-Pin Cerdip



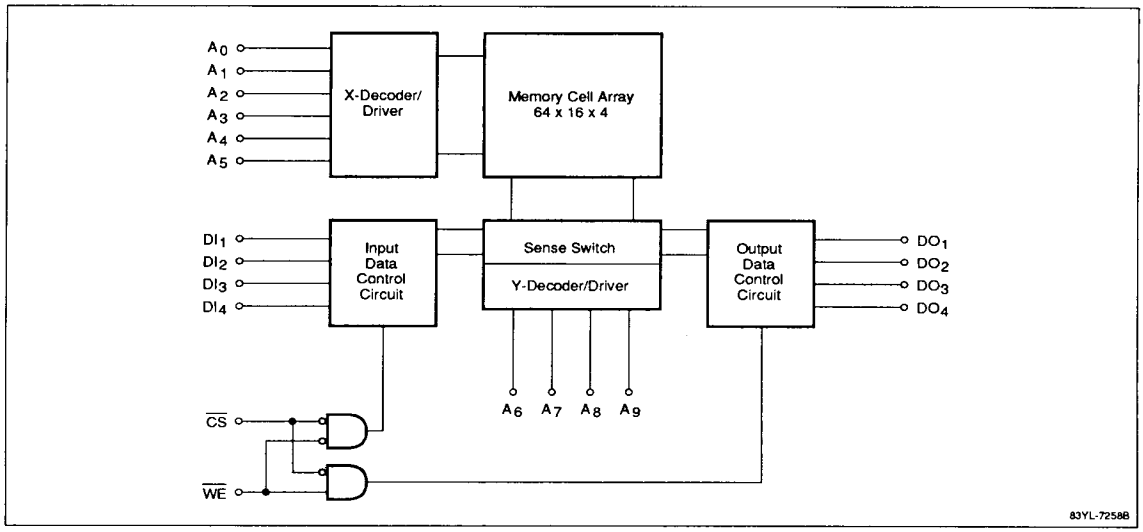
24-Pin Ceramic Flatpack



24-Pin Ceramic LCC



Block Diagram



Pin Identification

Symbol	Function
A_0 - A_9	Addresses
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 V to +0.5
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	−30 mA to +0.1
Storage temperature, T_{STG}	−65 to +150 °C
Storage temperature under bias, T_{STG} (Bias)	−55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	t_{AA} = 8/10/15 ns; all inputs and outputs open
		−450			mA	t_{AA} = 4.5/6 ns; all inputs and outputs open (Note 2)

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 ms.

(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90 °C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

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Figure 1. Loading Conditions Test Circuit

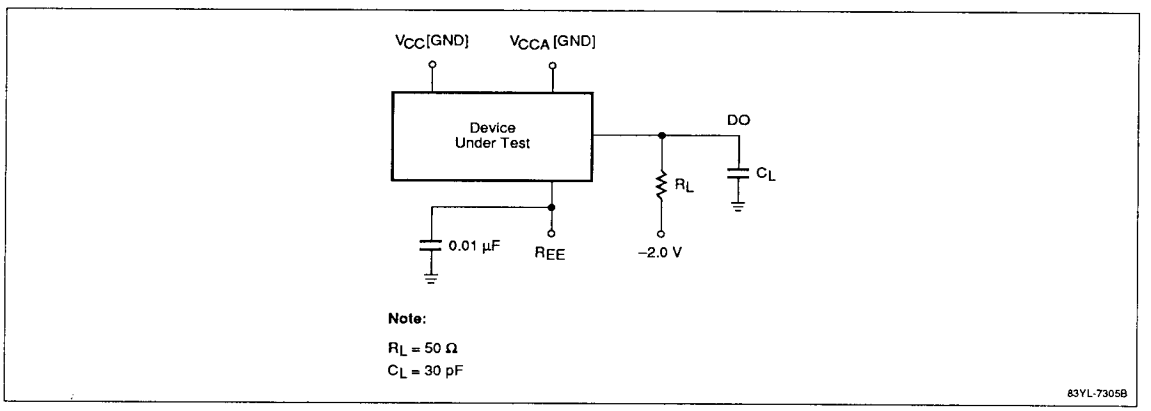
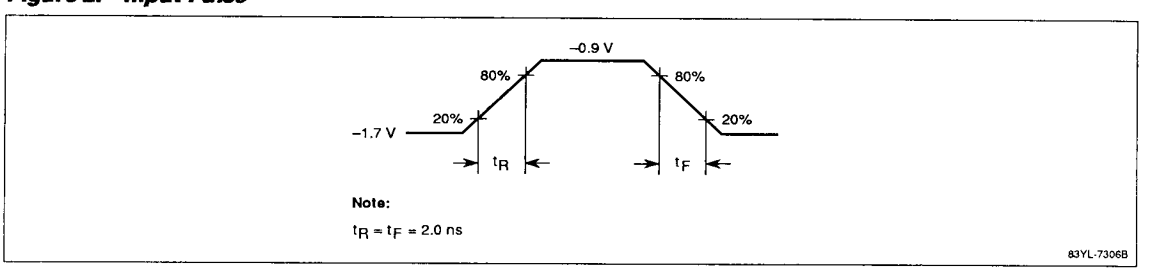


Figure 2. Input Pulse



AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

Parameter	Symbol	μPB100474-4.5		μPB100474-6		μPB100474-8		μPB100474-10		μPB100474-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Operation												
Chip select access time	t_{ACS}		4		4		5		6		8	ns
Chip select recovery time	t_{RCS}		4		4		5		6		8	ns
Address access time	t_{AA}		4.5		6		8		10		15	ns
Write Operation												
Write pulse width	t_W	4.5		6		6		10		15		ns
Data setup time	t_{WSD}	1		1		1		2		2		ns
Data hold time	t_{WHD}	1		1		1		2		2		ns
Address setup time	t_{WSA}	1		1		1		3		3		ns
Address hold time	t_{WHA}	2		2		1		2		2		ns
Chip select setup time	t_{WSCS}	1		1		1		2		2		ns
Chip select hold time	t_{WHCS}	1		1		1		2		2		ns
Write disable time	t_{WS}		4		4		5		6		8	ns
Write recovery time	t_{WR}		4.5		6		8		10		10	ns

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

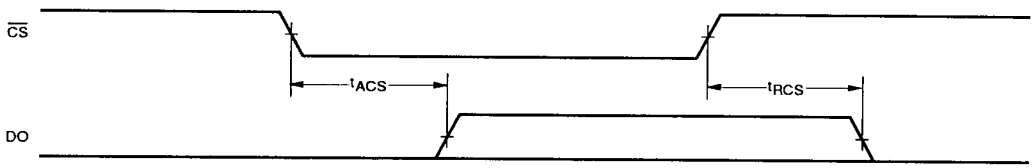
(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

(3) See figures 1 and 2 for loading conditions and input pulse timing. For the μPB100474-4.5/-6, C_L = 5 pF. For the μPB100474-8/10/15, C_L = 30 pF.

(4) Output rise and fall times = 2 ns (typ).

Timing Waveforms

Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.
[2] $\overline{WE} = V_{IH}$.

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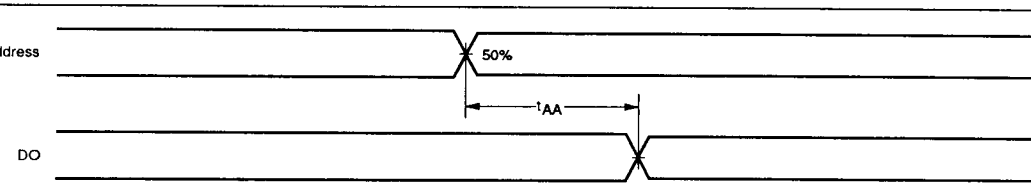
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.
[2] $\overline{WE} = V_{IH}$.

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Timing Waveforms (cont)

Write Cycle