

May 1995

54F/74F540 • 54F/74F541 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'F540 and 'F541 are similar in function to the 'F240 and 'F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

Features

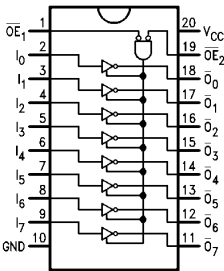
- TRI-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors

Commercial	Military	Package Number	Package Description
74F540PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F540DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F540SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F540SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F540FM (Note 2)	W20A	20-Lead Cerpack
	54F540LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F541PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F541DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F541SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F541SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F541FM (Note 2)	W20A	20-Lead Cerpack
	54F541LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

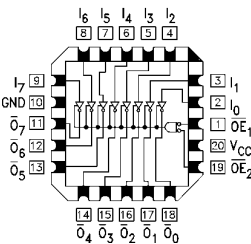
Pin Assignment for DIP, SOIC and Flatpak



'F540

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Pin Assignment for LCC

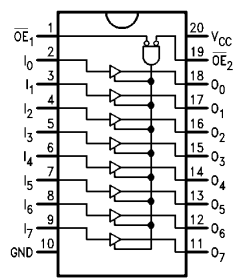


TL/F/9553-2

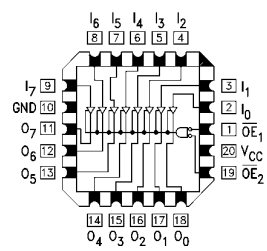
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54F/74F540 • 54F/74F541 Octal Buffer/Line Driver with TRI-STATE Outputs

Connection Diagrams (Continued)



'F541



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Unit Loading/Fan Out

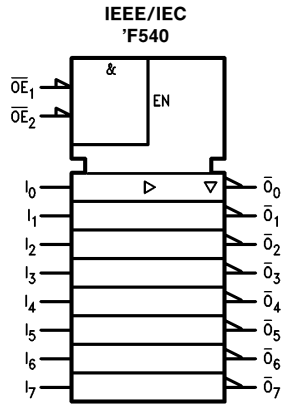
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA / -0.6 mA
I_n	Inputs	1.0/1.0	20 μA / -0.6 mA
$O_n, \overline{O}_n$	Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)

Truth Table

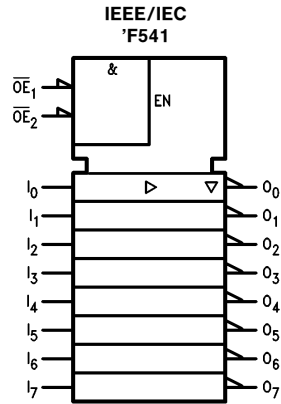
Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	'F540	'F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



TL/F/9553-3



TL/F/9553-6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.4 2.0 2.4 2.0 2.7			V	Min	I _{OH} = −3 mA I _{OH} = −12 mA I _{OH} = −3 mA I _{OH} = −15 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.55 0.55		V	Min	I _{OL} = 48 mA I _{OL} = 64 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0		μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0		μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75		μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6		mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50		μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50		μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−100	−225		mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500		μA	0.0V	V _{OUT} = 5.25V

DC Electrical Characteristics (Continued)

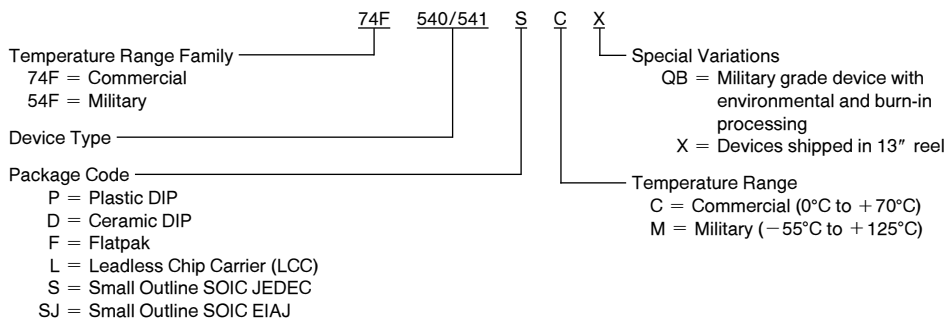
Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CCH}	Power Supply Current ('F540)	11	20		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F540)	53	75		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F540)	31	45		mA	Max	V _O = HIGH Z
I _{CCH}	Power Supply Current ('F541)	26	35		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F541)	55	75		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F541)	31	55		mA	Max	V _O = HIGH Z

AC Electrical Characteristics

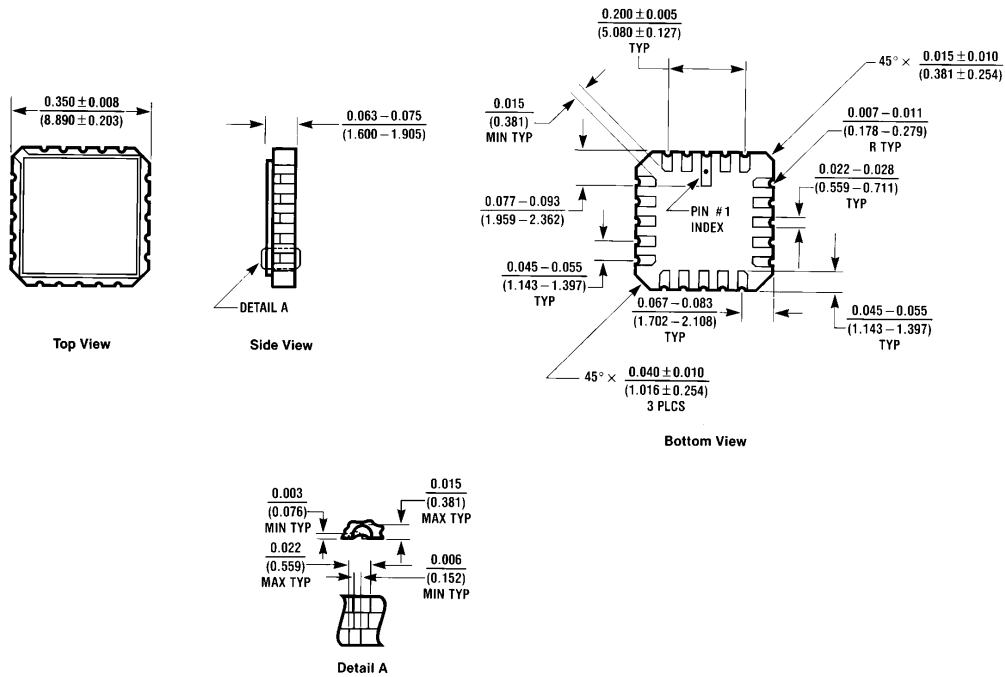
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Data to Output ('F540)	1.5 1.0	3.0 2.0	5.0 4.0	1.0 1.0	6.0 4.5	1.0 1.0	5.5 4.0	ns
t _{PZH} t _{PZL}	Output Enable Time ('F540)	2.5 3.5	4.9 5.8	8.0 10.0	2.5 3.5	9.0 11.0	2.5 3.5	8.5 10.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ('F540)	1.5 1.0	3.4 2.5	6.0 5.5	1.5 1.0	7.0 7.5	1.5 1.0	6.5 6.0	
t _{PLH} t _{PHL}	Propagation Delay Data to Output ('F541)	1.5 1.5	3.3 2.7	5.5 5.5			1.5 1.5	6.0 6.0	ns
t _{PZH} t _{PZL}	Output Enable Time ('F541)	3.0 3.5	5.8 6.1	8.0 8.5			2.5 3.0	9.5 9.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time ('F541)	1.5 1.5	3.4 2.9	6.0 5.5			1.5 1.5	6.5 6.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



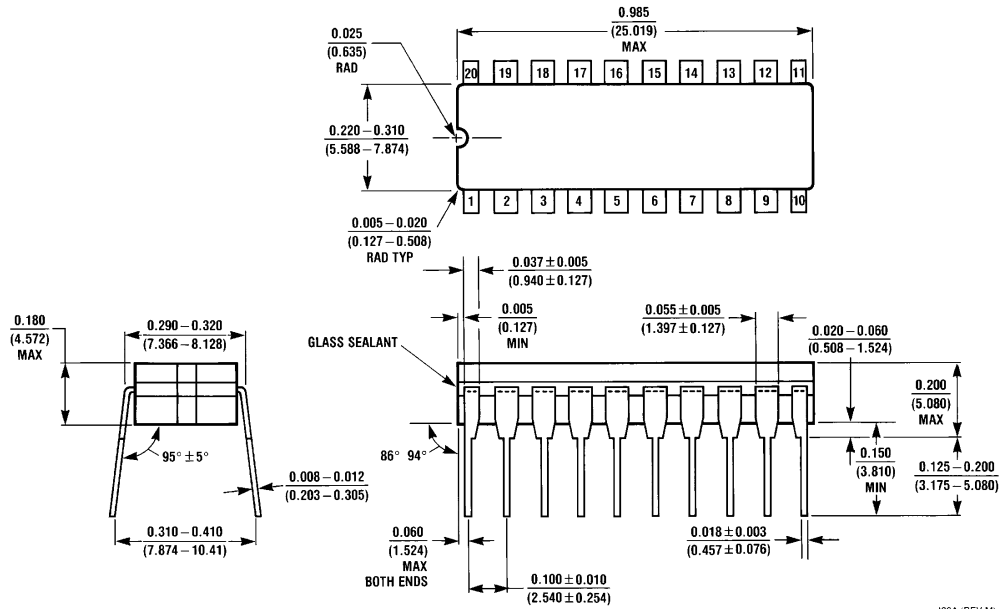
Physical Dimensions inches (millimeters)



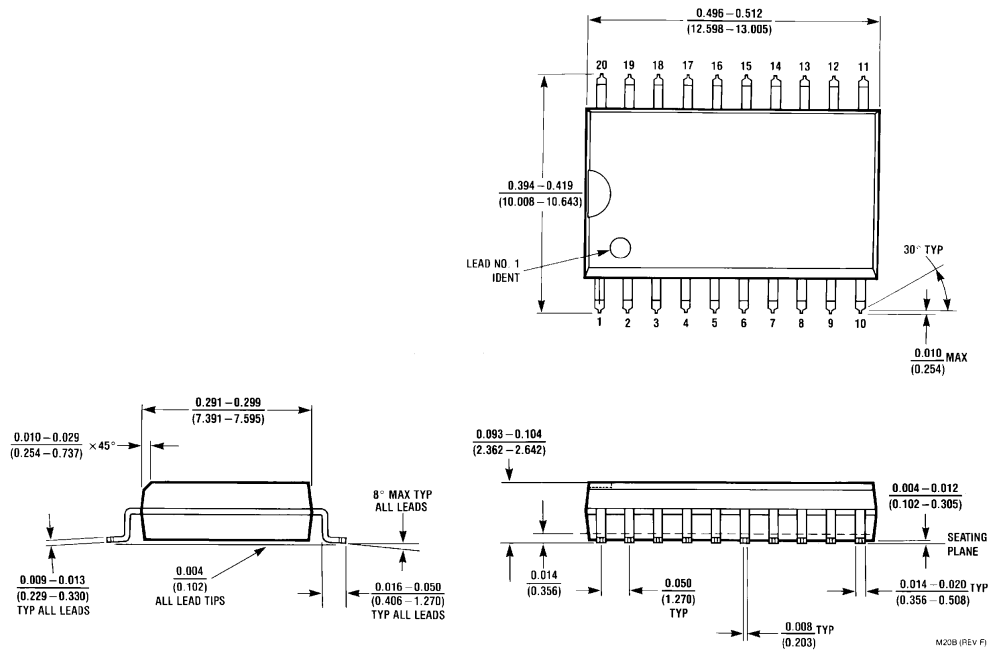
E20A (REV D)

**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

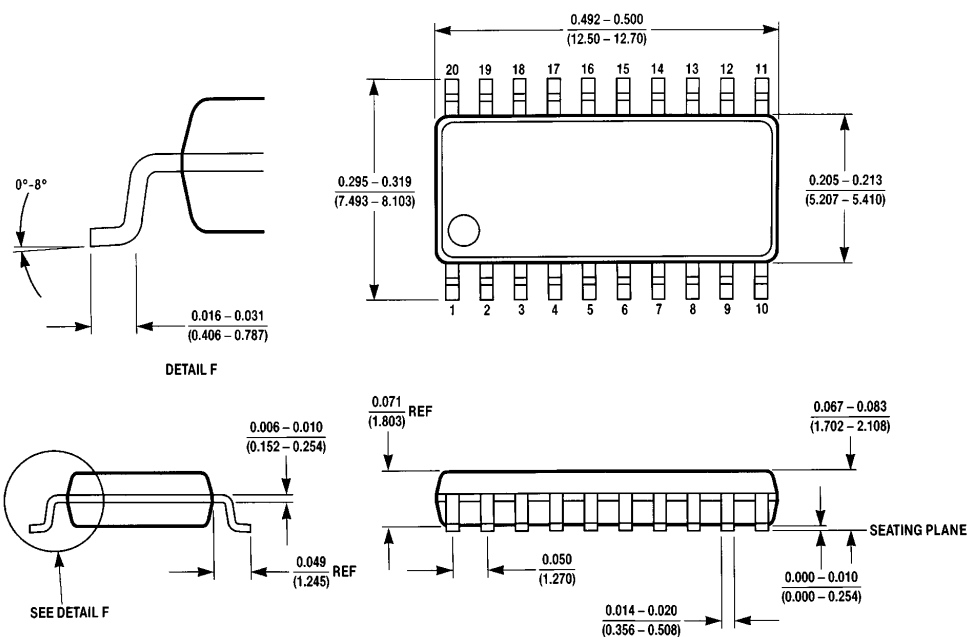
Physical Dimensions inches (millimeters) (Continued)



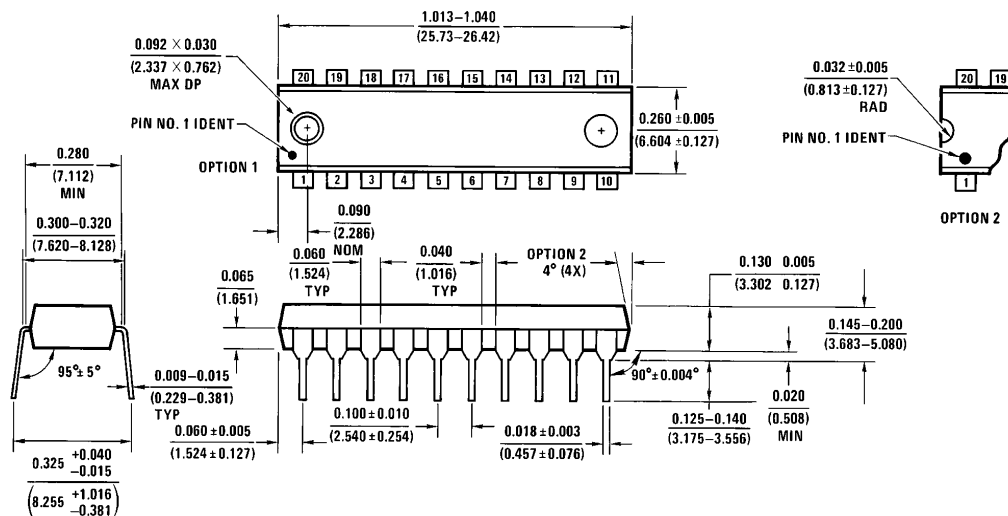
20-Lead Ceramic Dual-In-Lead Package (D)
NS Package Number J20A



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

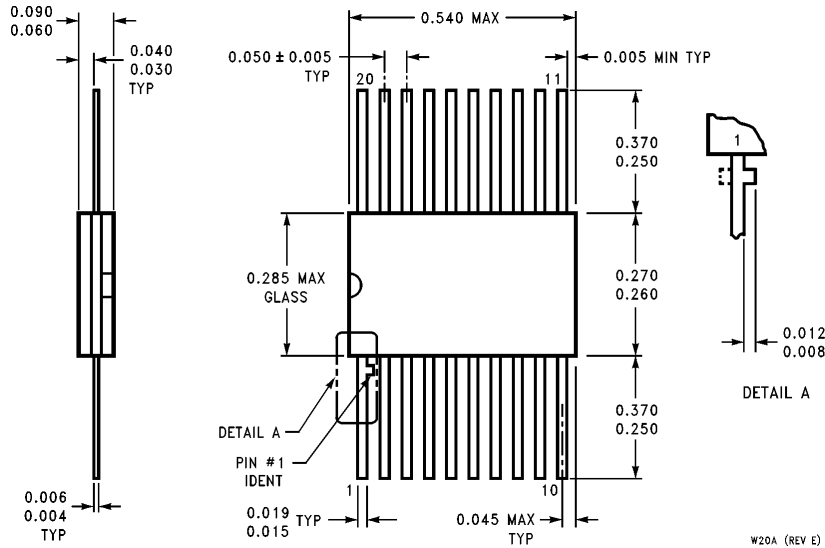
Physical Dimensions inches (millimeters) (Continued)

**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D**



20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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