National Semiconductor

April 2005

LP3981
Micropower, 300mA Ultra Low-Dropout CMOS Voltage Regulator

General Description

The LP3981's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies. This high power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 300 mA, from a 2.5V to 6V input, consuming less than 1µA in disable mode.

The LP3981 is available in MSOP-8 package. For LP3981 in LLP-6 package, contact NSC sales offices. Performance is specified for −40˚C to +125˚C temperature range. The device available in the following output voltages; 2.5V, 2.7V, 2.8V, 2.83V, 3.0V, 3.03V and 3.3V as standard. Other output options can be made available, please contact your local NSC sales office.

Key Specifications

- 2.5 to 6.0V input range
- 300mA guaranteed output
- 60dB PSRR at 1kHz
- ≤1µA quiescent current when shut down
- Fast Turn-On time: 120 µs (typ.) with C_{BYPASS} = 0.01uF
- 132mV typ dropout with 300mA load
- 35µVrms output noise over 10Hz to 100kHz
- −40 to +125˚C junction temperature range for operation
- 2.5V, 2.7V, 2.8V, 2.83V, 3.0V, 3.03V, and 3.3V outputs standard

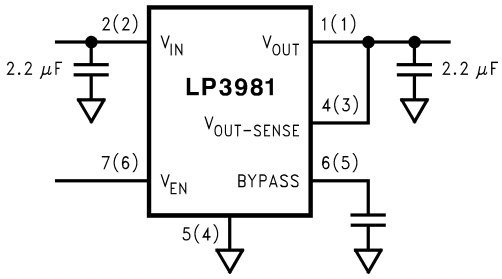
Features

- Small, space saving MSOP-8
- Low Thermal Resistance in LLP-6 package gives excellent power capability
- Logic controlled enable
- Stable with ceramic and high quality tantalum capacitors
- Fast turn-on
- Thermal shutdown and short-circuit current limit

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- Tiny 3.3V ± 5% to 2.5V, 300mA converter

Typical Application Circuit



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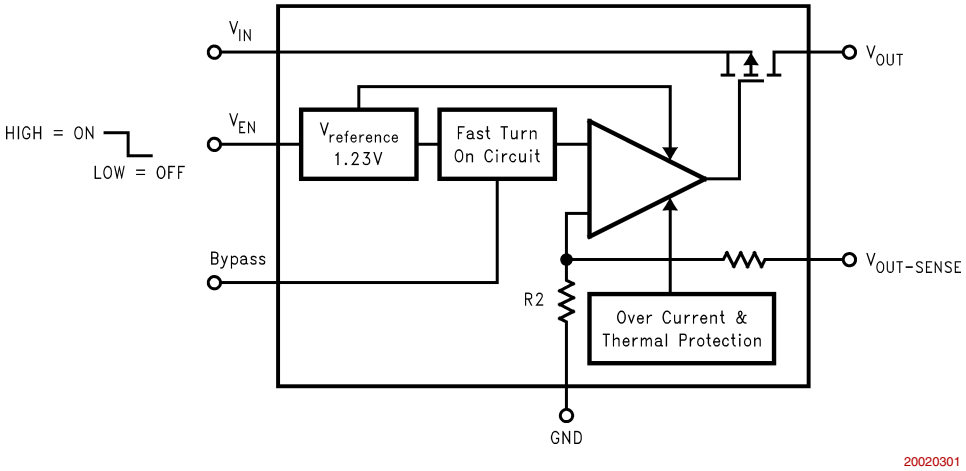
Note: Pin Numbers in parenthesis indicate LLP-6 package.

Block Diagram



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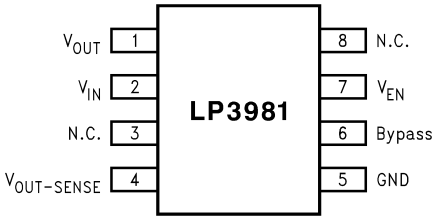
Pin Descriptions

Name	MSOP-8	LLP-6	Function
V_{EN}	7	6	Enable Input Logic, Enable High.
GND	5	4	Common Ground. Connect to PAD.
V_{OUT}	1	1	Output Voltage of the LDO.
V_{IN}	2	2	Input Voltage of the LDO.
Bypass	6	5	Optional bypass capacitor for noise reduction.
$V_{OUT-SENSE}$	4	3	Output. Voltage Sense Pin. Should be connected to V_{OUT} for proper operation.
N.C	3, 8		
GND		PAD	Common Ground. Connect to pin 4.

Connection Diagrams

MSOP-8 Package



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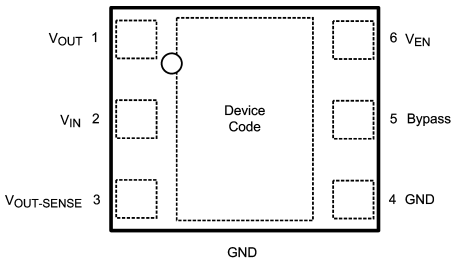
Top View
See NS Package Number MUA008AE

LLP-6 Package



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Top View
See NS Package Number LDC06D

Ordering Information

For LLP-6 Package

Output Voltage (V)	Grade	LP3981 Supplied as 1000 Units, Tape and Reel	LP3981 Supplied as 4500 Units, Tape and Reel	Package Marking
2.5	STD	LP3981ILD-2.5	LP3981ILDX-2.5	LO1UB
2.7	STD	LP3981ILD-2.7	LP3981ILDX-2.7	LO1VB
2.8	STD	LP3981ILD-2.8	LP3981ILDX-2.8	LO1ZB
2.83	STD	LP3981ILD-2.83	LP3981ILDX-2.83	L01SB
3.0	STD	LP3981ILD-3.0	LP3981ILDX-3.0	L017B
3.03	STD	LP3981ILD-3.03	LP3981ILDX-3.03	LO1YB
3.3	STD	LP3981ILD -3.3	LP3981ILDX-3.3	LO1XB

For MSOP-8 Package

Output Voltage (V)	Grade	LP3981 Supplied as 1000 Units, Tape and Reel	LP3981 Supplied as 3500 Units, Tape and Reel	Package Marking
2.5	STD	LP3981IMM-2.5	LP3981IMMX-2.5	LFKB
2.7	STD	LP3981IMM-2.7	LP3981IMMX-2.7	LFLB
2.8	STD	LP3981IMM-2.8	LP3981IMMX-2.8	LFTB
2.83	STD	LP3981IMM-2.83	LP3981IMMX-2.83	LDUB
3.0	STD	LP3981IMM-3.0	LP3981IMMX-3.0	LF3B
3.03	STD	LP3981IMM-3.03	LP3981IMMX-3.03	LFPB
3.3	STD	LP3981IMM-3.3	LP3981IMMX-3.3	LFNB

*Please contact factory regarding the availability of voltage options not listed here.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{EN}	−0.3 to 6.5V
V_{OUT}, $V_{OUT\text{-}SENSE}$	−0.3 to V_{IN} + 0.3, Max 6.5V
Junction Temperature	150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temp.	
Pad Temp.	
Power Dissipation (Note 3)	
θ_{JA} (MSOP-8)	210˚C/W
θ_{JA} (LLP-6)	50˚C/W
Maximum Power Dissipation at 25˚C	
MSOP-8	595mW
LLP-6	2.5W
ESD Rating(Note 4)	
Human Body Model	2kV
Machine Model	200V

Operating Ratings (Notes 1, 2)

V_{IN}	2.7 to 6V
V_{EN}	0 to V_{IN}
Junction Temperature	−40˚C to +125˚C
Maximum Power Dissipation (Note 5)	
MSOP-8	476mW
LLP-6	2.0W

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.2V, V_{IN} = V_{OUT} + 0.5V, C_{IN} = 2.2 µF, C_{BP} = 0.033 µF, I_{OUT} = 1mA, C_{OUT} = 2.2 µF. Typical values and imits appearing in standard typeface are for T_J = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 6, 7)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance			−2 **−3**	2 **3**	% of $V_{OUT(nom)}$
	Line Regulation Error	V_{IN} = V_{OUT} + 0.5V to 6.0V, T_A < +85˚C	0.005	−0.1	0.1	%/V
		V_{IN} = V_{OUT} + 0.5V to 6.0V, T_J ≤125˚C		**−0.2**	**0.2**	%/V
	Load Regulation Error (Note 8)	I_{OUT} = 1 mA to 300 mA	0.0003		**0.005**	%/mA
PSRR	Power Supply Rejection Ratio (Note 10)	V_{IN} = $V_{OUT(nom)}$ + 1V, f = 1 kHz, I_{OUT} = 50 mA (*Figure 2*)	50			dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, f = 10 kHz, I_{OUT} = 50 mA (*Figure 2*)	55			
I_Q	Quiescent Current	V_{EN} = 1.2V, I_{OUT} = 1 mA	70		**120**	µA
		V_{EN} = 1.2V, I_{OUT} = 1 to 300 mA, V_{OUT} = 2.5V(Note 12)	170		**210**	
		V_{EN} = 0.4V	0.003		**1.5**	
	Dropout Voltage (Note 9)	I_{OUT} = 1 mA	0.5		**5**	mV
		I_{OUT} = 200 mA	88		**133**	
		I_{OUT} = 300 mA	132		**200**	
I_{SC}	Short Circuit Current Limit	Output Grounded (Steady State)	600			mA
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{BP} = 0.033µF	35			µVrms
TSD	Thermal Shutdown Temperature		160			˚C
	Thermal Shutdown Hysteresis		20			˚C
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ V_{OUT} (nom) - 5%	455	300		
I_{EN}	Maximum Input Current at V_{EN}	V_{EN} = 0 and V_{IN}	0.001			µA
V_{IL}	Logic Low Input threshold	V_{IN} = 2.7 to 6.0V			**0.4**	V

Electrical Characteristics (Continued)

Unless otherwise specified: V_{EN} = 1.2V, V_{IN} = V_{OUT} + 0.5V, C_{IN} = 2.2 µF, C_{BP} = 0.033 µF, I_{OUT} = 1mA, C_{OUT} = 2.2 µF. Typical values and imits appearing in standard typeface are for T_J = 25˚C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +125˚C. (Notes 6, 7)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IH}	Logic High Input threshold	V_{IN} = 2.7 to 6.0V		**1.4**		V
T_{ON}	Turn-On Time (Note 10) (Note 11)	C_{BYPASS} = 0.033 µF	240		**350**	µs

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The figures given for Absolute Maximum Power disipation for the device are calculated using the following equations:

$$P_D = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

E.g. for the LLP package θ_{JA}=50˚C/W, $T_{J(MAX)}$=150˚C and using T_A=25˚C the maximum power dissipation is found to be 2.5W. The derating factor ($-1/\theta_{JA}$) = −20mW/˚C, thus below 25˚C the power dissipation figure can be increased by 20W per degree, and similarity decreased by this factor for temperatures above 25˚C

Note 4: The human body model is 100pF discharged through 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 5: As for the Maximum Power dissipation, the maximum power in operation is dependant on the ambient temperature. This can be calculated in teh same way using T_J=125˚C, giving 2W as the maximum power dissipation for the LLP package in operation. The same derating factor applies.

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25˚C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.

Note 8: An increase in the load current results in a slight decrease in the output voltage and vice versa.

Note 9: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.

Note 10: Guaranteed by design.

Note 11: Turn-on time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

Note 12: For V_{OUT} > 2.5C, Increase $I_{Q(MAX)}$ by 2.5µA for every 0.1V increase in $V_{OUT(NOM)}$.

i.e. $I_{Q(MAX)}$ = 210 + (($V_{OUT(NOM)}$ - 2.5) * 25)µA

Output Capacitor, Recommended Specification

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitor	Capacitance		2.2	22	µF
		ESR		5	500	mΩ

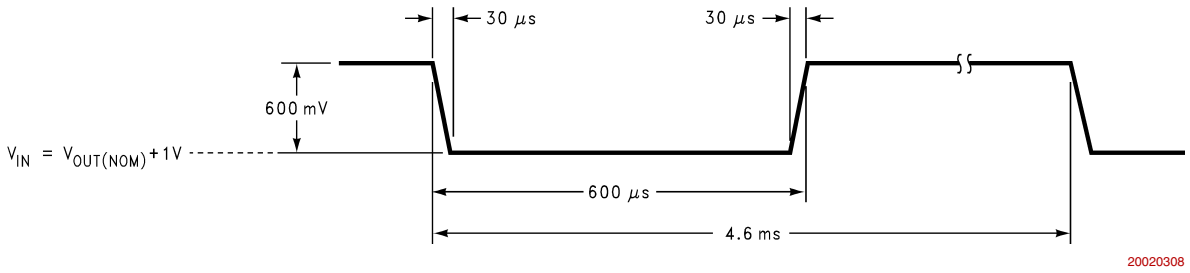


FIGURE 1. Line Transient Response Input Perturbation

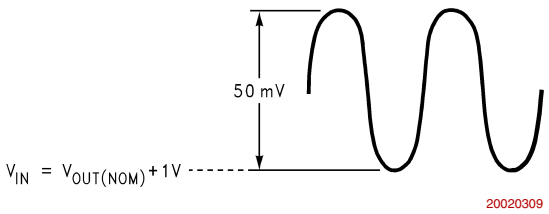
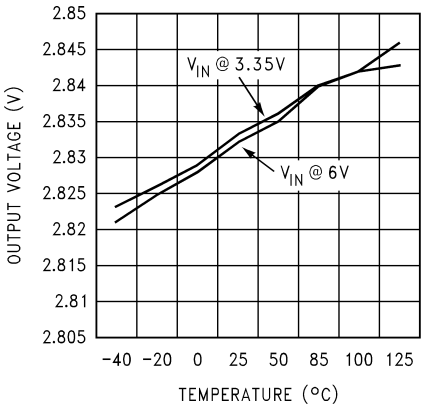


FIGURE 2. PSRR Input Perturbation

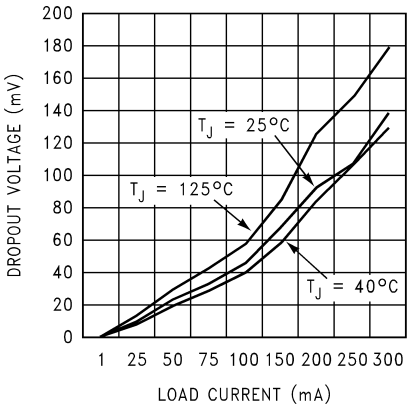
Typical Performance Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 2.2 µF Ceramic, C_{BP} = 0.033 µF, V_{IN} = V_{OUT} + 0.5V, T_A = 25˚C, Enable pin is tied to V_{IN}.

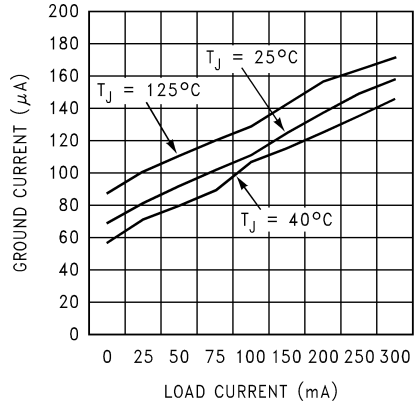
Output Voltage vs. Temperature (V_{OUT} = 2.83V)



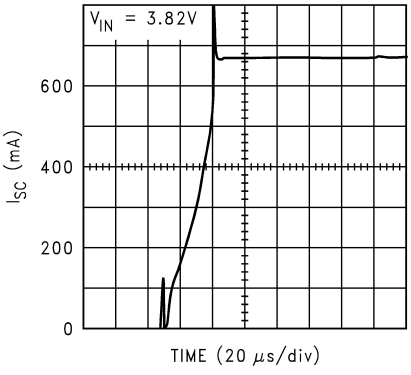
Dropout Voltage vs. Temperature (V_{OUT} = 2.85V)



Ground Current vs. Load Current (V_{OUT} = 2.85V)



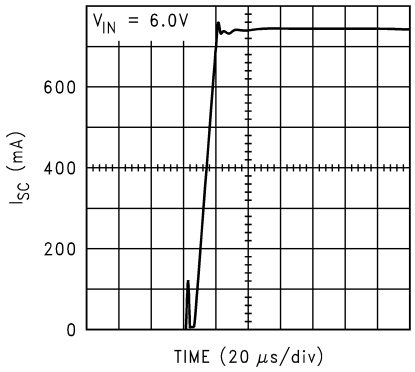
Output Short Circuit Current



Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ Ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}. (Continued)

Output Short Circuit Current



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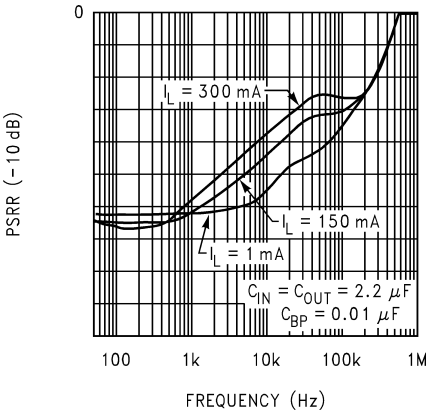
Ripple Rejection ($V_{IN} = V_{OUT} + 1V$)



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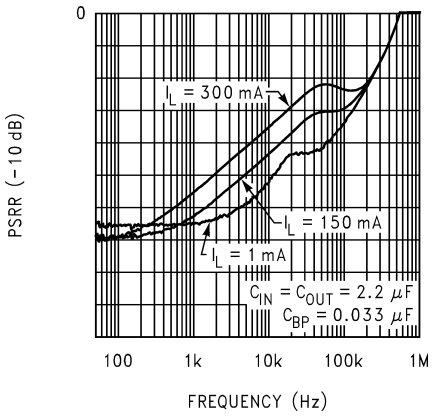
Ripple Rejection ($V_{IN} = V_{OUT} + 1V$)



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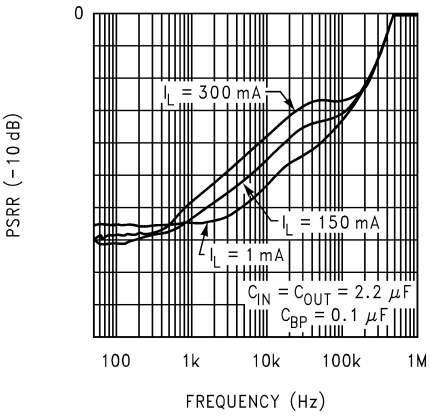
Ripple Rejection ($V_{IN} = V_{OUT} + 1V$)



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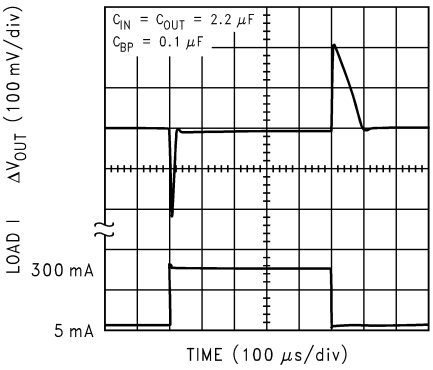
Load Transient Response ($V_{IN} = 3.5V$)



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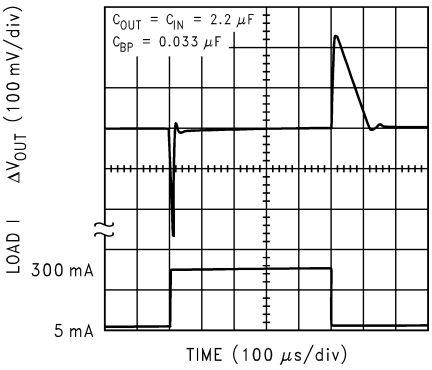
Load Transient Response ($V_{IN} = 3.5V$)



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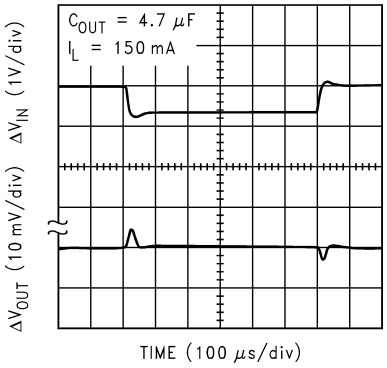
Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ Ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{IN}. (Continued)

Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



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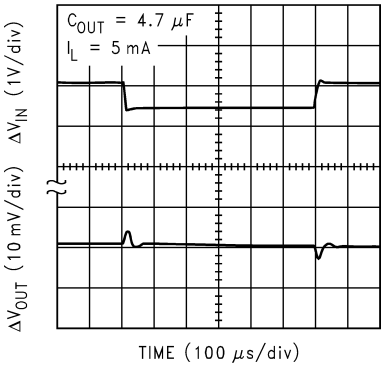
Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



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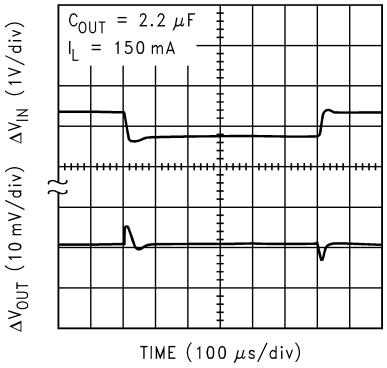
Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



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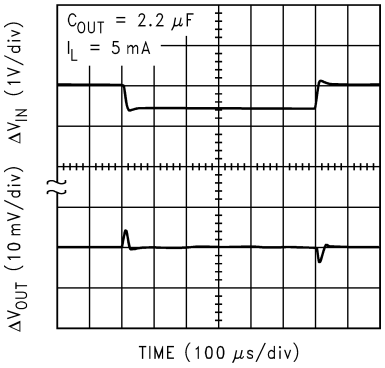
Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



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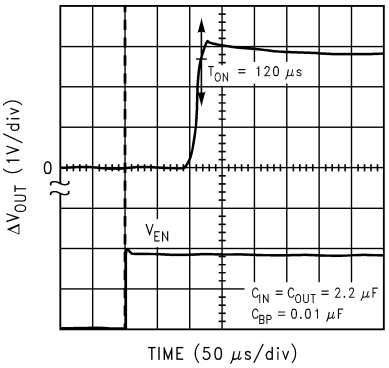
Enable Response (T_{ON})



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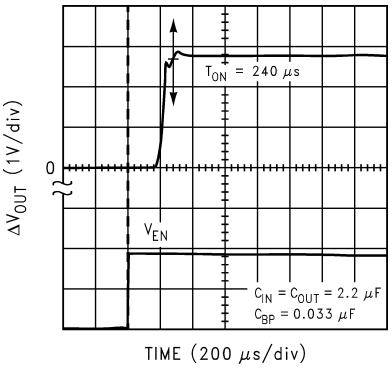
Enable Response (T_{ON})



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Application Hints

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependant on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in notes 3 and 5 in the electrical specifications sections, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

With a $\theta_{JA} = 50^{\circ}C/W$, the device in theLLP package returns a value of 2.0W with a maximum junction temperature of

Application Hints (Continued)

125˚C and an ambient temperature of 25˚C. The device in a MSOP package returns a figure of 0.476W, (θ_{JA} = 210˚C/W).

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal considerations, the voltage drop across the device, and the continuous current capability of the device. The device can deliver 300mA but care must be taken when choosing the continuous current output for the device under the operating load conditions.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3981 requires external capacitors for regulator stability. The LP3981 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 2.2µF is required between the LP3981 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 2.2µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3981 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 2.2 to 22 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3981 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3981 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

NOISE BYPASS CAPACITOR

Connecting a 0.033µF capacitor between the C_{BP} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the bad gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. Hight-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO's, addition of a noise reduction capacitor does not effect the transient response of the device.

CAPACITOR CHARACTERISTICS

The LP3981 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3981.

The ceramic capacitor's capacitance can vary with temperature. Most large value ceramic capacitors (≅ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25˚C to 85˚C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to –40˚C, so some guard band must be allowed.

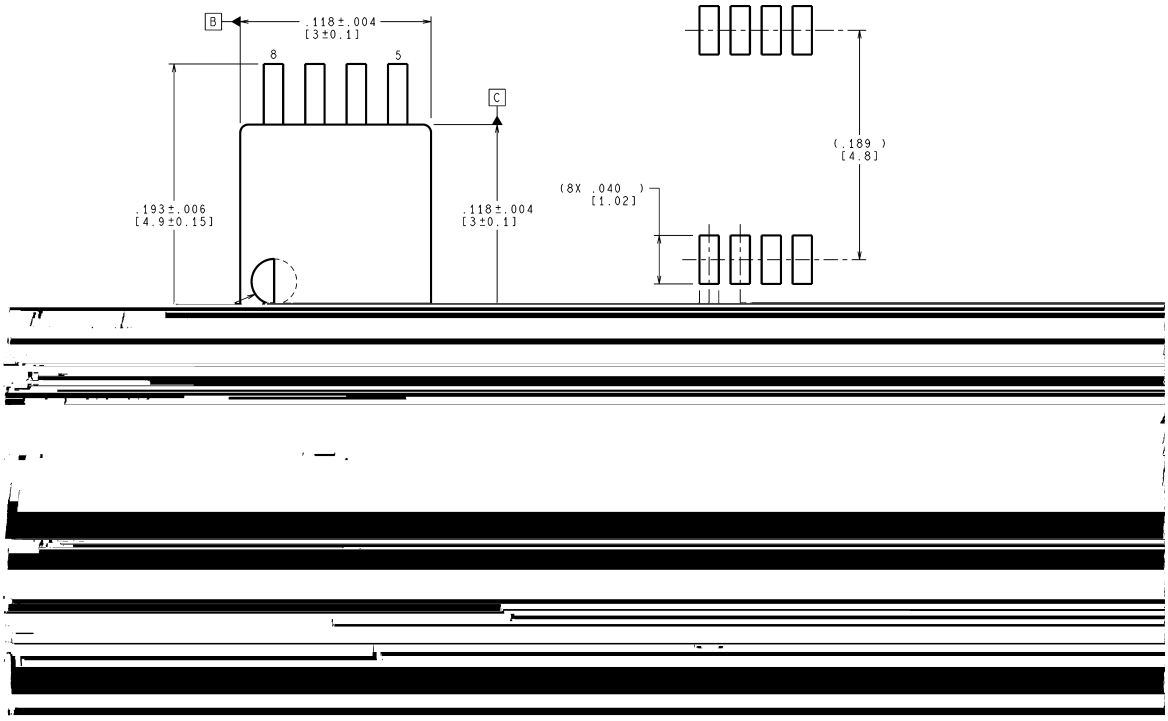
ON/OFF INPUT OPERATION

The LP3981 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

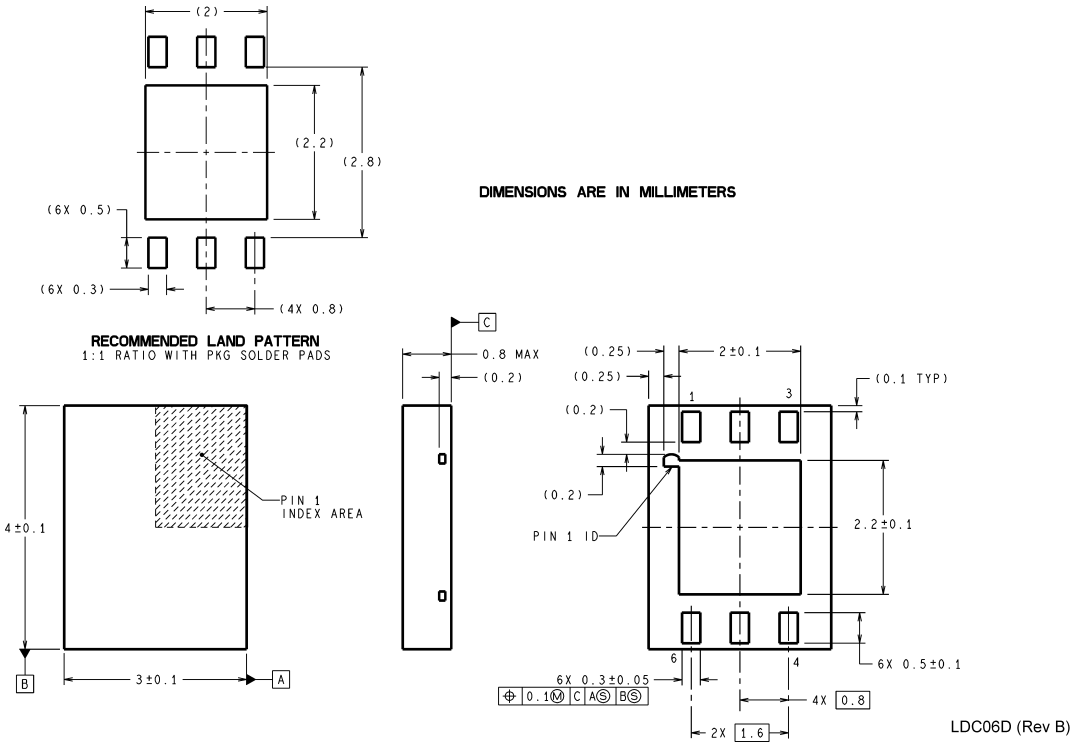
FAST ON-TIME

The LP3981 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number MUA008AE



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Notes

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