

# LP38690/LP38692

## 1A Low Dropout CMOS Linear Regulators

### Stable with Ceramic Output Capacitors

#### General Description

The LP38690/2 low dropout CMOS linear regulators provide tight output tolerance (2.5% typical), extremely low dropout voltage (450mV @ 1A load current,  $V_{OUT} = 5V$ ), and excellent AC performance utilizing ultra low ESR ceramic output capacitors.

The low thermal resistance of the LLP, SOT-223 and T0-252 packages allow the full operating current to be used even in high ambient temperature environments.

The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100  $\mu A$  regardless of load current, input voltage, or operating temperature.

**Dropout Voltage:** 450 mV (typ) @ 1A (typ. 5V out).

**Ground Pin Current:** 55  $\mu A$  (typ) at full load.

**Precision Output Voltage:** 2.5% (25°C) accuracy.

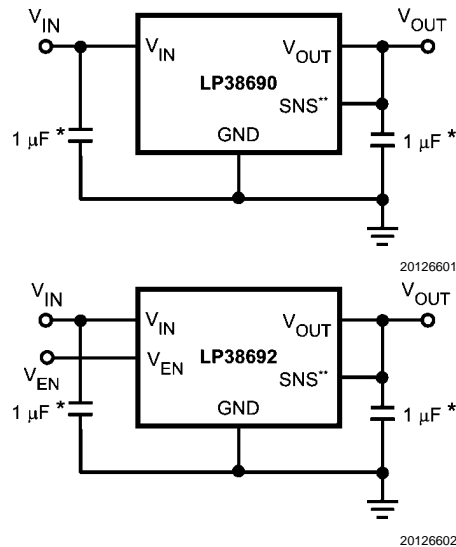
#### Features

- 2.5% output accuracy (25°C)
- Low dropout voltage: 450mV @ 1A (typ, 5V out)
- Wide input voltage range (2.7V to 10V)
- Precision (trimmed) bandgap reference
- Guaranteed specs for -40°C to +125°C
- 1 $\mu A$  off-state quiescent current
- Thermal overload protection
- Foldback current limiting
- T0-252, SOT-223 and 6-Lead LLP packages
- Enable pin (LP38692)

#### Applications

- Hard Disk Drives
- Notebook Computers
- Battery Powered Devices
- Portable Instrumentation

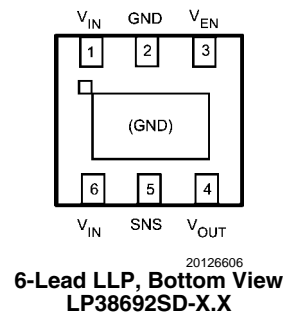
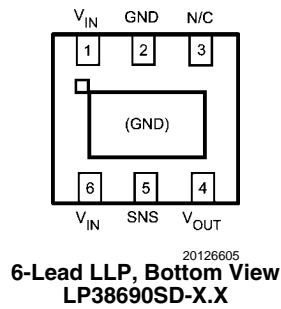
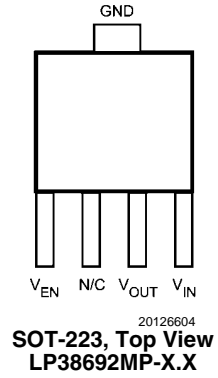
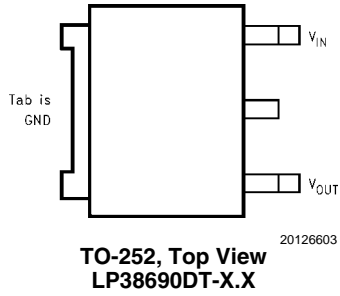
#### Typical Application Circuits



**Note:** \* Minimum value required for stability.

\*\*LLP package devices only.

## Connection Diagrams



## Pin Description

| PIN       | DESCRIPTION  |
|-----------|--|
| $V_{IN}$  | This is the input supply voltage to the regulator. For LLP devices, both $V_{IN}$ pins must be tied together for full current operation (500mA maximum per pin).   |
| GND       | Circuit ground for the regulator. This is connected to the die through the lead frame, and also functions as the heat sink when the large ground pad is soldered down to a copper plane.   |
| SNS       | Output sense pin allows remote sensing at the load which will eliminate the error in output voltage due to voltage drops caused by the resistance in the traces between the regulator and the load. This pin must be tied to $V_{OUT}$ . |
| $V_{EN}$  | The enable pin allows the part to be turned ON and OFF by pulling this pin high or low.  |
| $V_{OUT}$ | Regulated output voltage.  |

## Ordering Information

| Order Number   | Package Marking | Package Type | Package Drawing | Supplied As              |
|----------------|-----------------|--------------|-----------------|--------------------------|
| LP38690SD-1.8  | L113B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38690SD-2.5  | L114B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38690SD-3.3  | L115B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38690SD-5.0  | L116B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38690DT-1.8  | LP38690DT-1.8   | TO-252       | TD03B           | 75 Units per Rail        |
| LP38690DT-2.5  | LP38690DT-2.5   | TO-252       | TD03B           | 75 Units per Rail        |
| LP38690DT-3.3  | LP38690DT-3.3   | TO-252       | TD03B           | 75 Units per Rail        |
| LP38690DT-5.0  | LP38690DT-5.0   | TO-252       | TD03B           | 75 Units per Rail        |
| LP38692SD-1.8  | L123B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38692SD-2.5  | L124B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38692SD-3.3  | L125B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38692SD-5.0  | L126B           | 6-Lead LLP   | SDE06A          | 1000 Units Tape and Reel |
| LP38692MP-1.8  | LJPB            | SOT-223      | MP05A           | 1000 Units Tape and Reel |
| LP38692MP-2.5  | LJRB            | SOT-223      | MP05A           | 1000 Units Tape and Reel |
| LP38692MP-3.3  | LJSB            | SOT-223      | MP05A           | 1000 Units Tape and Reel |
| LP38692MP-5.0  | LJTB            | SOT-223      | MP05A           | 1000 Units Tape and Reel |
| LP38690SDX-1.8 | L113B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38690SDX-2.5 | L114B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38690SDX-3.3 | L115B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38690SDX-5.0 | L116B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38690DTX-1.8 | LP38690DT-1.8   | TO-252       | TD03B           | 2500 Units Tape and Reel |
| LP38690DTX-2.5 | LP38690DT-2.5   | TO-252       | TD03B           | 2500 Units Tape and Reel |
| LP38690DTX-3.3 | LP38690DT-3.3   | TO-252       | TD03B           | 2500 Units Tape and Reel |
| LP38690DTX-5.0 | LP38690DT-5.0   | TO-252       | TD03B           | 2500 Units Tape and Reel |
| LP38692SDX-1.8 | L123B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38692SDX-2.5 | L124B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38692SDX-3.3 | L125B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38692SDX-5.0 | L126B           | 6-Lead LLP   | SDE06A          | 4500 Units Tape and Reel |
| LP38692MPX-1.8 | LJPB            | SOT-223      | MP05A           | 2000 Units Tape and Reel |
| LP38692MPX-2.5 | LJRB            | SOT-223      | MP05A           | 2000 Units Tape and Reel |
| LP38692MPX-3.3 | LJSB            | SOT-223      | MP05A           | 2000 Units Tape and Reel |
| LP38692MPX-5.0 | LJTB            | SOT-223      | MP05A           | 2000 Units Tape and Reel |

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

|                                   |                    |
|-----------------------------------|--------------------|
| Storage Temperature Range         | -65°C to +150°C    |
| Lead Temp. (Soldering, 5 seconds) | 260°C              |
| ESD Rating (Note 3)               | 2 kV               |
| Power Dissipation (Note 2)        | Internally Limited |

|                                       |                    |
|---------------------------------------|--------------------|
| V(max) All pins (with respect to GND) | -0.3V to 12V       |
| I <sub>OUT</sub>                      | Internally Limited |
| Junction Temperature                  | -40°C to +150°C    |

**Operating Ratings**

|                                      |                 |
|--------------------------------------|-----------------|
| V <sub>IN</sub> Supply Voltage       | 2.7V to 10V     |
| Operating Junction Temperature Range | -40°C to +125°C |

**Electrical Characteristics** Limits in standard typeface are for T<sub>J</sub> = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V<sub>IN</sub> = V<sub>OUT</sub> + 1V, C<sub>IN</sub> = C<sub>OUT</sub> = 10 μF, I<sub>LOAD</sub> = 10mA. Min/Max limits are guaranteed through testing, statistical correlation, or design.

| Symbol                             | Parameter                                   | Conditions  | MIN         | TYP (Note 4) | MAX                 | Units             |
|------------------------------------|---|---|-------------|--------------|---------------------|-------------------|
| V <sub>O</sub>                     | Output Voltage Tolerance                    |   | -2.5        |              | 2.5                 | %V <sub>OUT</sub> |
|                                    |   | 100 μA < I <sub>L</sub> < 1A<br>V <sub>O</sub> + 1V V <sub>IN</sub> 10V | <b>-5.0</b> |              | <b>5.0</b>          |                   |
| V <sub>O</sub> / V <sub>IN</sub>   | Output Voltage Line Regulation (Note 6)     | V <sub>O</sub> + 0.5V V <sub>IN</sub> 10V<br>I <sub>L</sub> = 25mA      |             | 0.03         | <b>0.1</b>          | %/V               |
| V <sub>O</sub> / I <sub>L</sub>    | Output Voltage Load Regulation (Note 7)     | 1 mA < I <sub>L</sub> < 1A<br>V <sub>IN</sub> = V <sub>O</sub> + 1V     |             | 1.8          | <b>5</b>            | %/A               |
| V <sub>IN</sub> - V <sub>OUT</sub> | Dropout Voltage (Note 8)                    | (V <sub>O</sub> = 1.8V)<br>I <sub>L</sub> = 1A                          |             | 950          | <b>1600</b>         | mV                |
|                                    |   | (V <sub>O</sub> = 2.5V)<br>I <sub>L</sub> = 0.1A<br>I <sub>L</sub> = 1A |             | 80<br>800    | <b>145<br/>1300</b> |                   |
|                                    |   | (V <sub>O</sub> = 3.3V)<br>I <sub>L</sub> = 0.1A<br>I <sub>L</sub> = 1A |             | 65<br>650    | <b>110<br/>1000</b> |                   |
|                                    |   | (V <sub>O</sub> = 5V)<br>I <sub>L</sub> = 0.1A<br>I <sub>L</sub> = 1A   |             | 45<br>450    | <b>100<br/>800</b>  |                   |
| I <sub>Q</sub>                     | Quiescent Current                           | V <sub>IN</sub> 10V, I <sub>L</sub> = 100 μA - 1A                       |             | 55           | <b>100</b>          | μA                |
|                                    |   | V <sub>EN</sub> 0.4V, (LP38692 Only)                                    |             | 0.001        | <b>1</b>            |                   |
| I <sub>L</sub> (MIN)               | Minimum Load Current                        | V <sub>IN</sub> - V <sub>O</sub> 4V                                     |             |              | <b>100</b>          |                   |
| I <sub>FB</sub>                    | Foldback Current Limit                      | V <sub>IN</sub> - V <sub>O</sub> > 5V                                   |             | 450          |                     | mA                |
|                                    |   | V <sub>IN</sub> - V <sub>O</sub> < 4V                                   |             | 1500         |                     |                   |
| PSRR                               | Ripple Rejection                            | V <sub>IN</sub> = V <sub>O</sub> + 2V(DC), with 1V(p-p) / 120Hz Ripple  |             | 55           |                     | dB                |
| T <sub>SD</sub>                    | Thermal Shutdown Activation (Junction Temp) |   |             | 160          |                     | °C                |
| T <sub>SD</sub> (HYST)             | Thermal Shutdown Hysteresis (Junction Temp) |   |             | 10           |                     |                   |

| Symbol       | Parameter                     | Conditions                              | MIN        | TYP (Note 4) | MAX        | Units             |
|--------------|-------------------------------|---|------------|--------------|------------|-------------------|
| $e_n$        | Output Noise                  | BW = 10Hz to 10kHz<br>$V_O = 3.3V$      |            | 0.7          |            | $\mu V/\sqrt{Hz}$ |
| $V_O$ (LEAK) | Output Leakage Current        | $V_O = V_O(NOM) + 1V @ 10V_{IN}$        |            | 0.5          | 12         | $\mu A$           |
| $V_{EN}$     | Enable Voltage (LP38692 Only) | Output = OFF                            |            |              | <b>0.4</b> | V                 |
|              |                               | Output = ON, $V_{IN} = 4V$              | <b>1.8</b> |              |            |                   |
|              |                               | Output = ON, $V_{IN} = 6V$              | <b>3.0</b> |              |            |                   |
|              |                               | Output = ON, $V_{IN} = 10V$             | <b>4.0</b> |              |            |                   |
| $I_{EN}$     | Enable Pin Leakage            | $V_{EN} = 0V$ or $10V$ , $V_{IN} = 10V$ | -1         | 0.001        | 1          | $\mu A$           |

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

**Note 2:** At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance ( $\theta_{JA}$ ) for the TO-252 is approximately 90°C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the TO-252, the  $\theta_{JA}$  drops to approximately 50°C/W. The SOT-223 package has a  $\theta_{JA}$  of approximately 125°C/W when soldered down to a minimum sized pattern (less than 0.1 square inch) and approximately 70°C/W when soldered to a copper area of one square inch. The  $\theta_{JA}$  values for the LLP package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to application note AN-1187). If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

**Note 3:** ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.

**Note 4:** Typical numbers represent the most likely parametric norm for 25°C operation.

**Note 5:** If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

**Note 6:** Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

**Note 7:** Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.

**Note 8:** Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

Block Diagrams

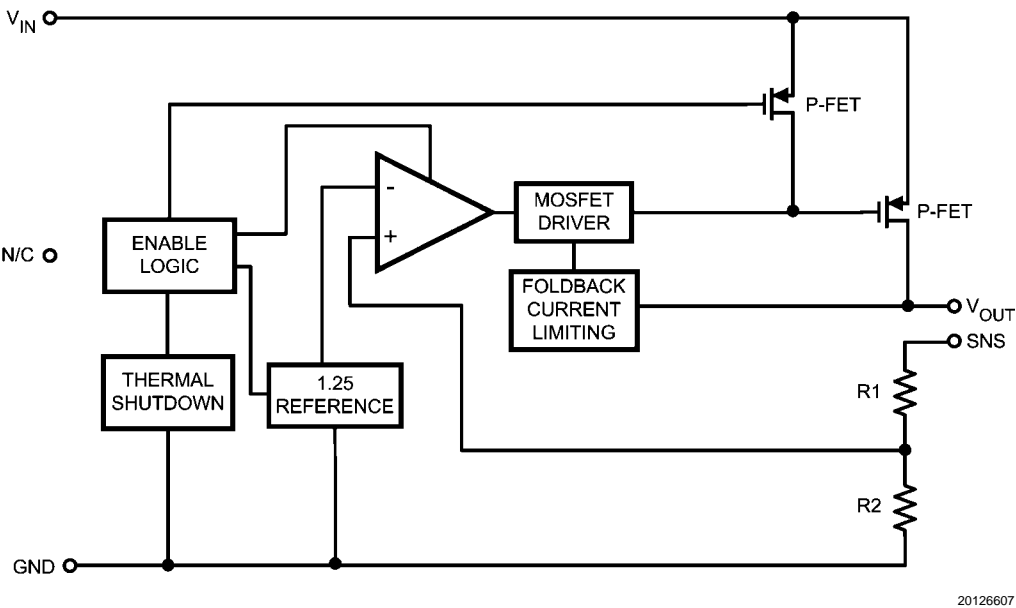


FIGURE 1. LP38690 Functional Diagram (LLP)

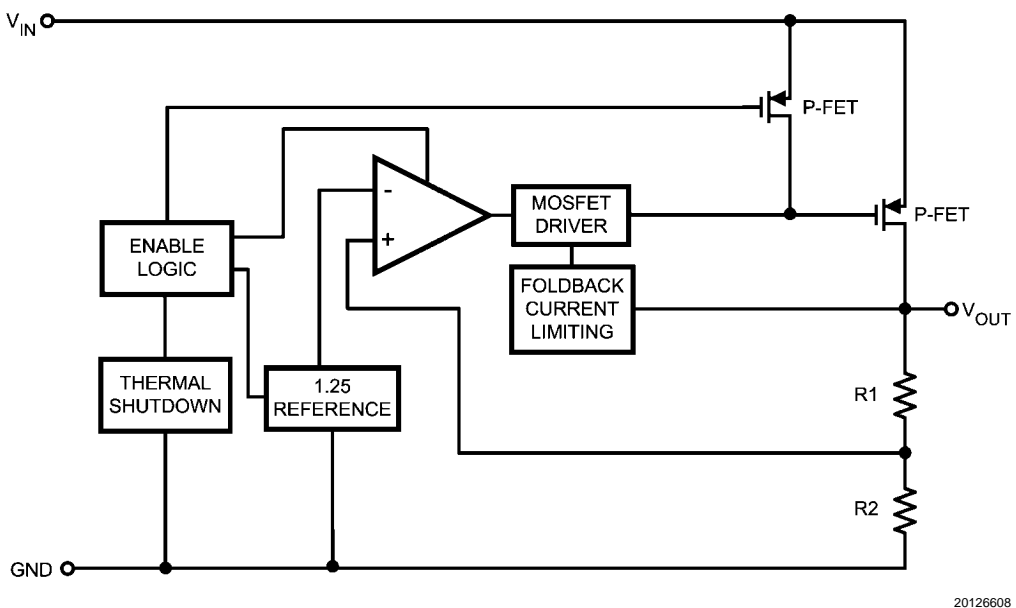


FIGURE 2. LP38690 Functional Diagram (TO-252)

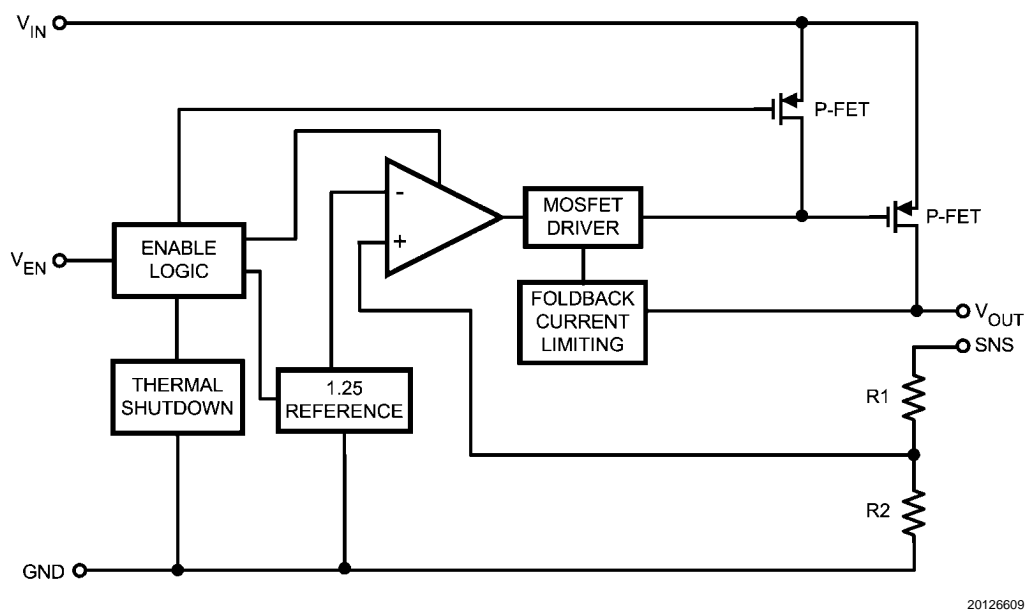


FIGURE 3. LP38692 Functional Diagram (LLP)

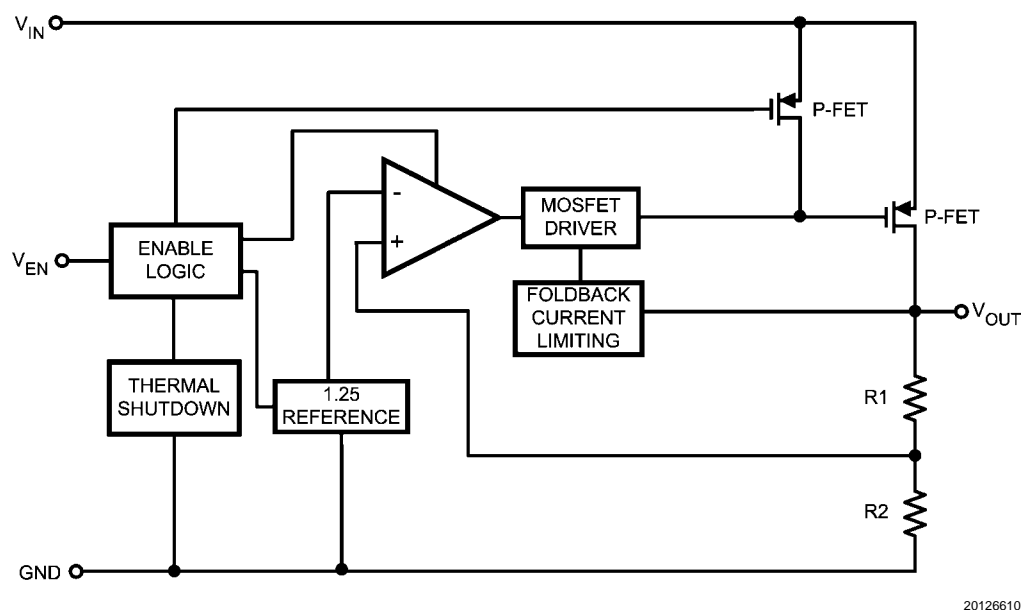
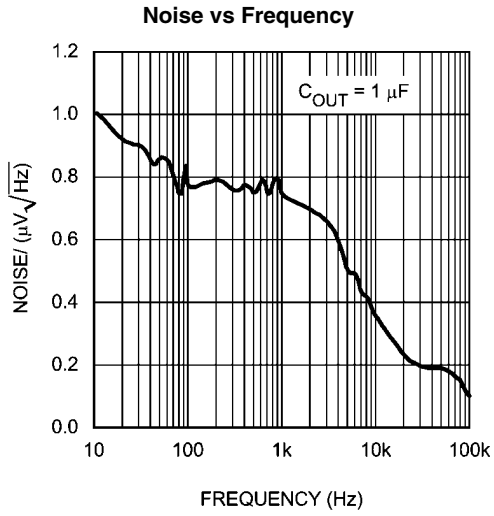


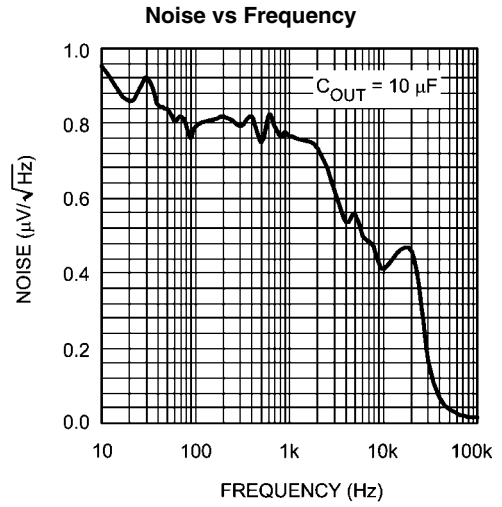
FIGURE 4. LP38692 Functional Diagram (SOT-223)

## Typical Performance Characteristics

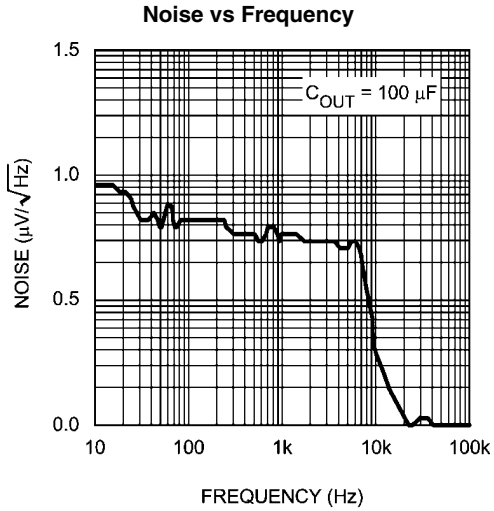
Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $C_{IN} = C_{OUT} = 10\ \mu\text{F}$ , Enable pin is tied to  $V_{IN}$  (LP38692 only),  $V_{OUT} = 1.8\text{V}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $I_L = 10\text{mA}$ .



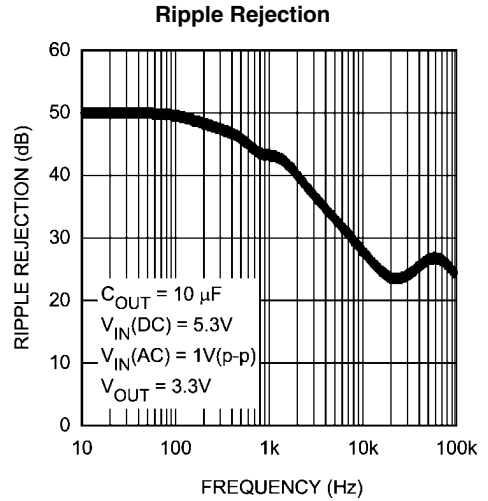
20126635



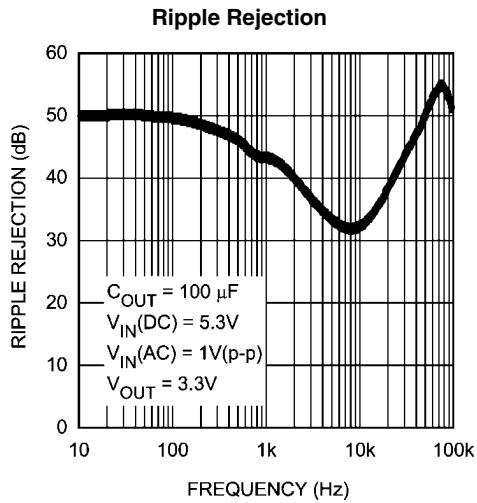
20126636



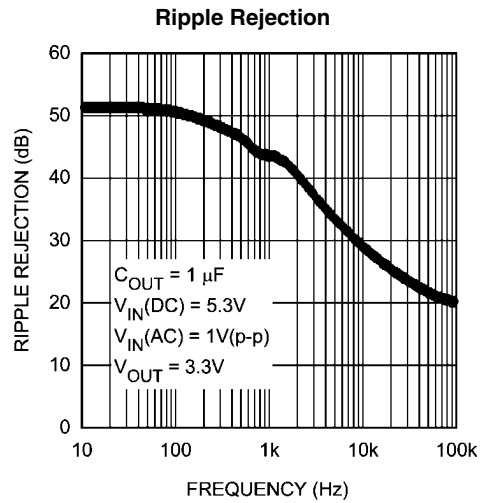
20126637



20126618



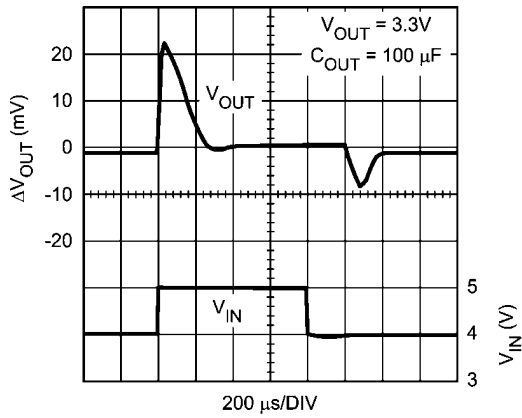
20126620



20126622

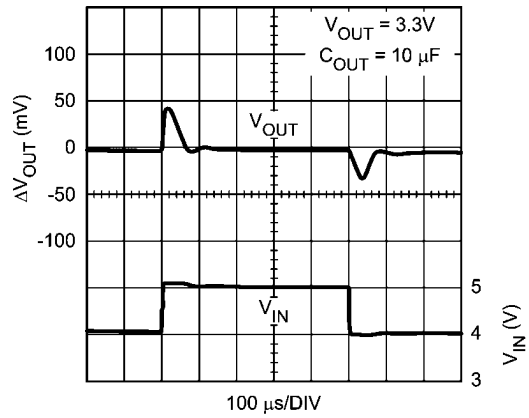


Line Transient Response



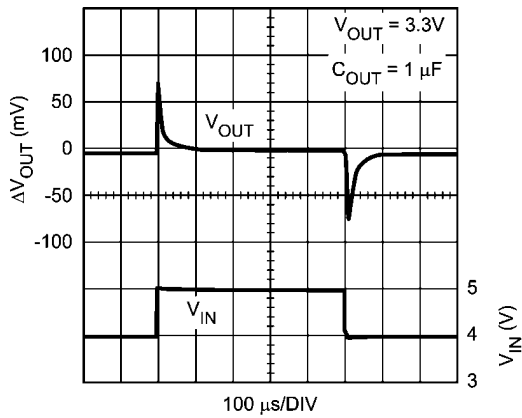
20126624

Line Transient Response



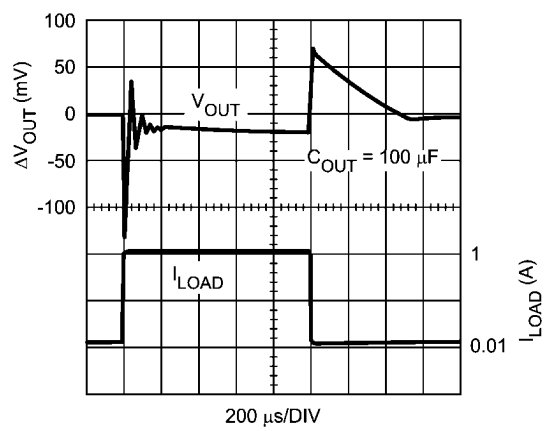
20126626

Line Transient Response



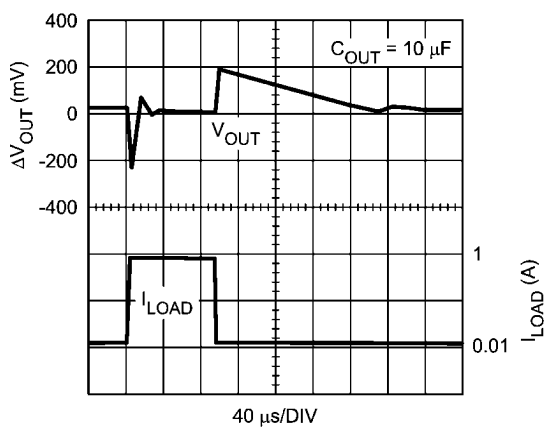
20126628

Load Transient Response



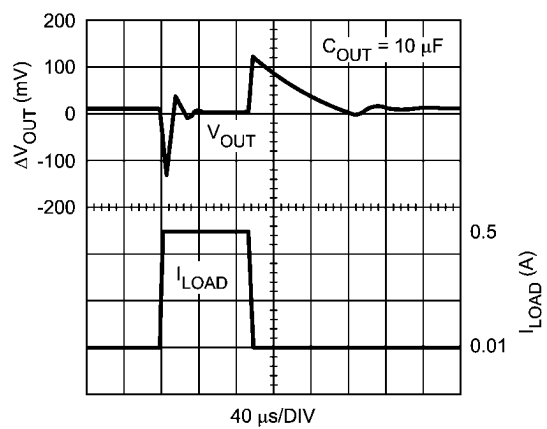
20126640

Load Transient Response

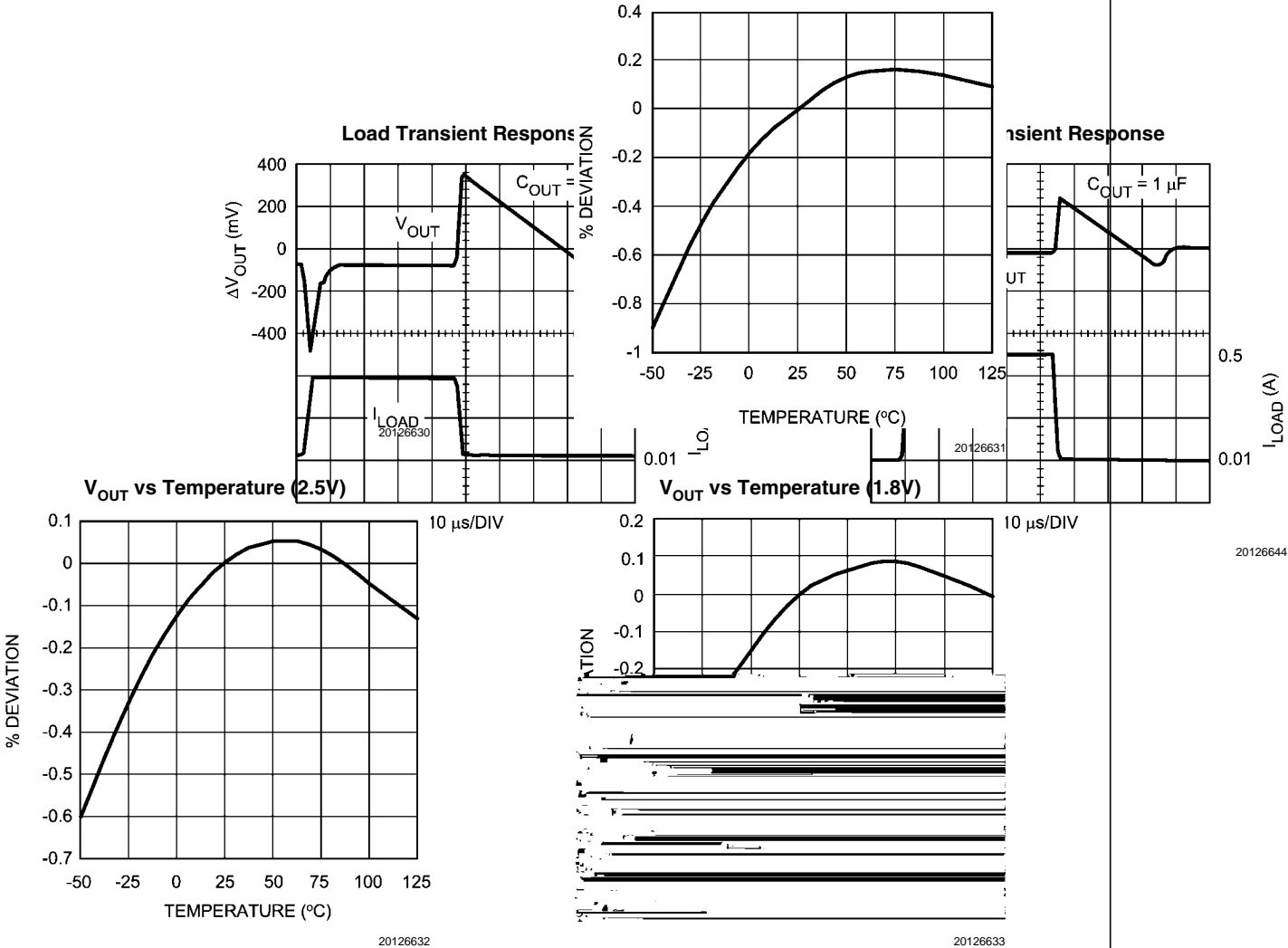


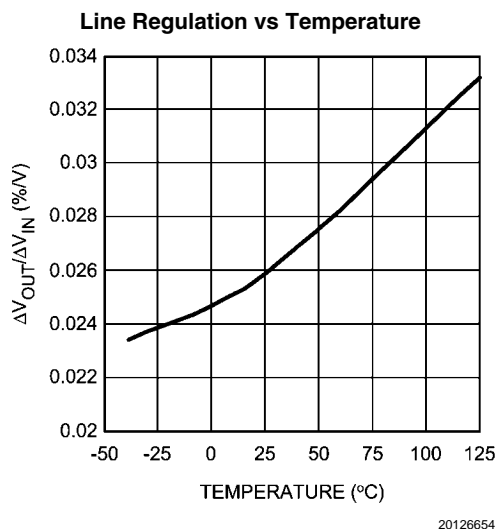
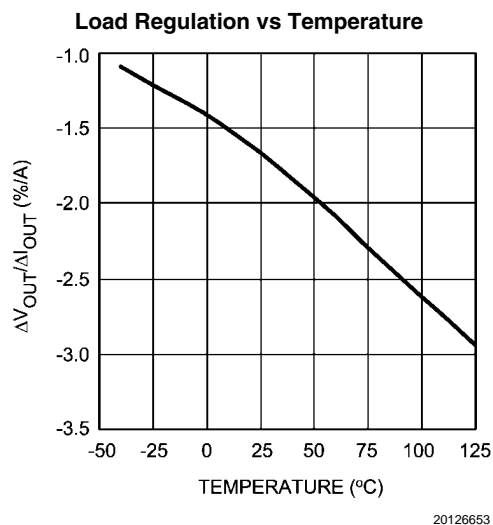
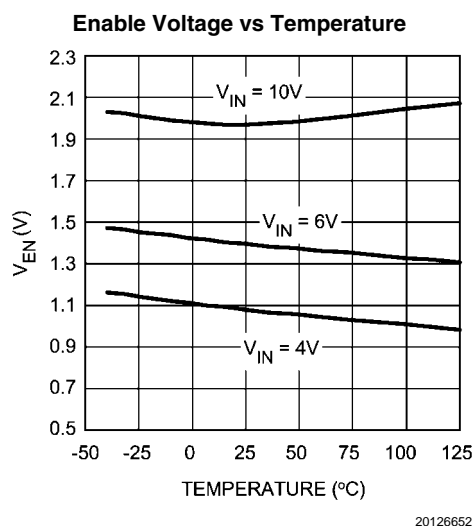
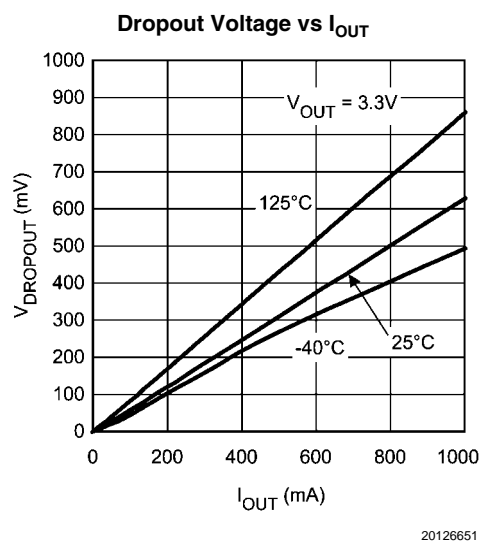
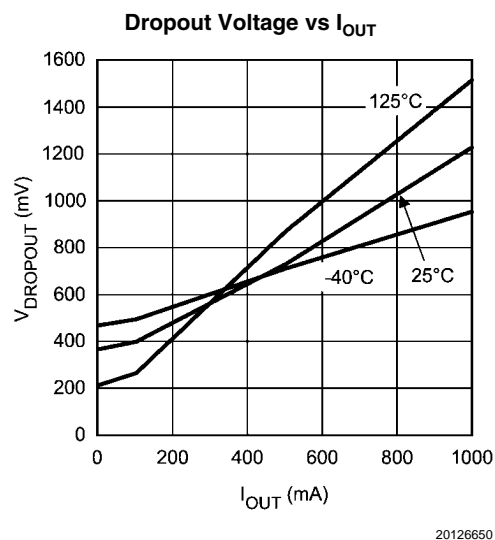
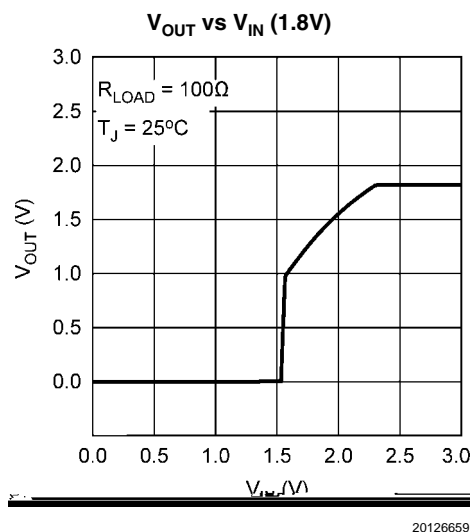
20126641

Load Transient Response



20126642





## Application Hints

### EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

**INPUT CAPACITOR:** An input capacitor of at least  $1\mu\text{F}$  is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

**OUTPUT CAPACITOR:** An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is  $1\mu\text{F}$ . Ceramic capacitors are recommended (the LP38690/2 was designed for use with ultra low ESR capacitors). The LP38690/2 is stable with any output capacitor ESR between zero and 100 Ohms.

**ENABLE PIN (LP38692 only):** The LP38692 has an enable pin which turns the regulator output on and off. Pulling the enable pin down to a logic low will turn the part off. The voltage the pin has to be pulled up to in order to assure the part is on depends on input voltage (refer to Electrical Characteristics section). This pin should be tied to  $V_{\text{IN}}$  if the enable function is not used.

**Foldback Current Limiting:** Foldback current limiting is built into the LP38690/2 which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ . Typically, when this differential voltage exceeds 5V, the load current will limit at about 450 mA. When the  $V_{\text{IN}} - V_{\text{OUT}}$  differential is reduced below 4V, load current is limited to about 1500 mA.

### SELECTING A CAPACITOR

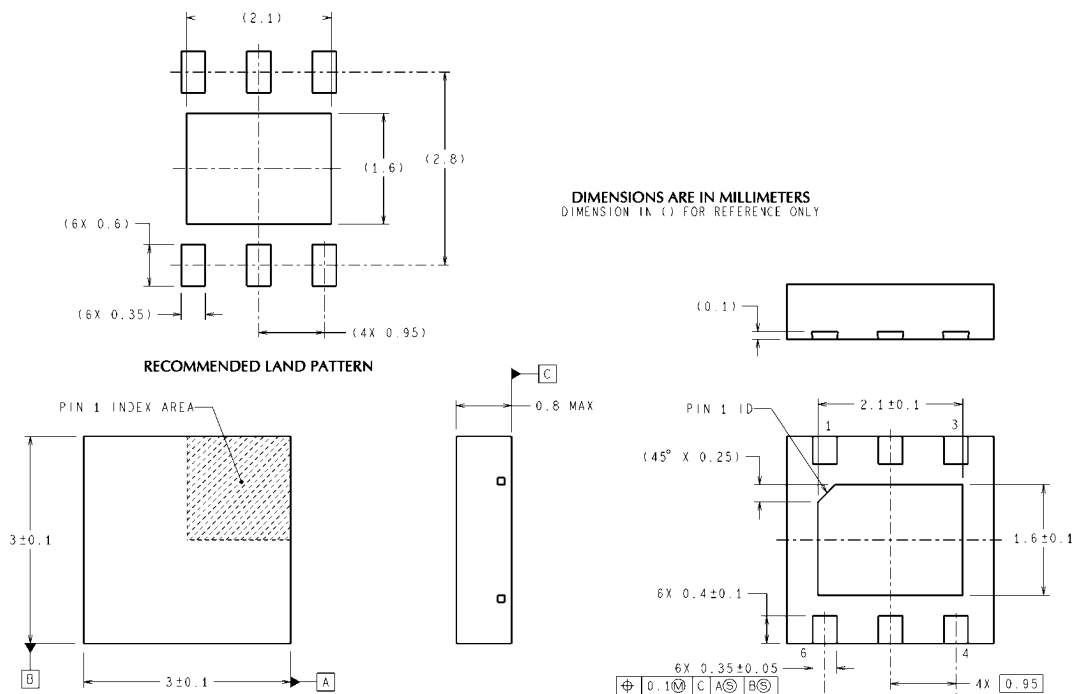
It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

### Capacitor Characteristics

**CERAMIC:** For values of capacitance in the 10 to  $100\mu\text{F}$  range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 m

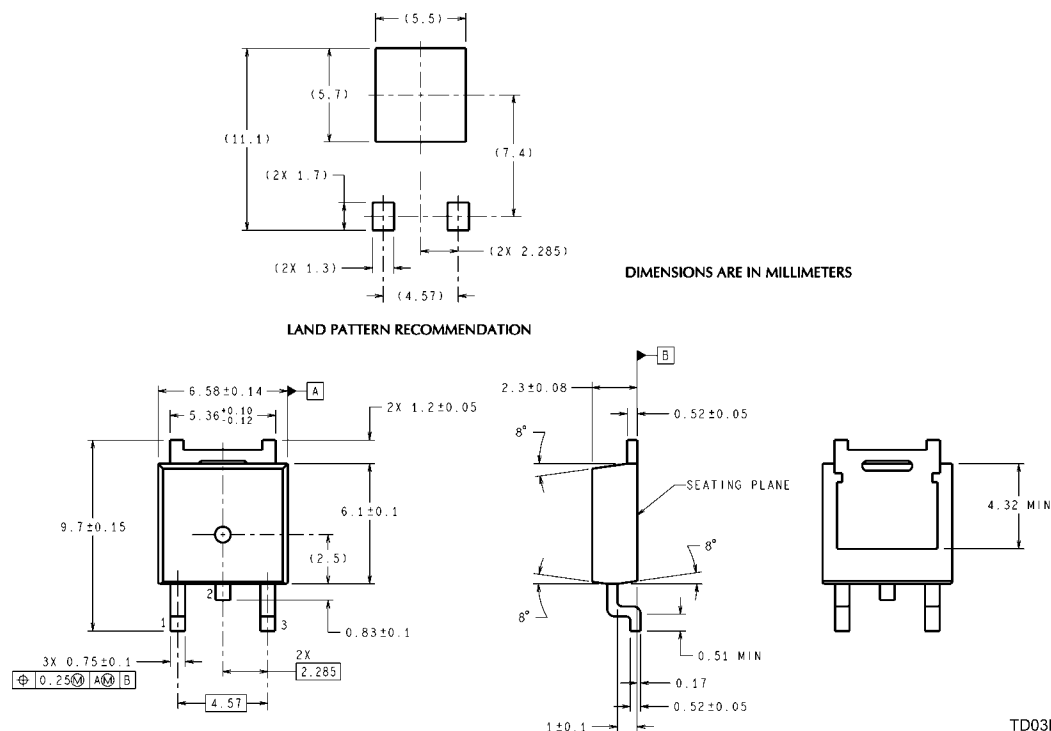
a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies. Attention should be paid to the units of measurement. Spot noise is measured in units  $\mu\text{V}/\sqrt{\text{Hz}}$  or  $\text{nV}/\sqrt{\text{Hz}}$  and total output noise is measured in  $\mu\text{V}(\text{rms})$

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

**Physical Dimensions** inches (millimeters) unless otherwise noted

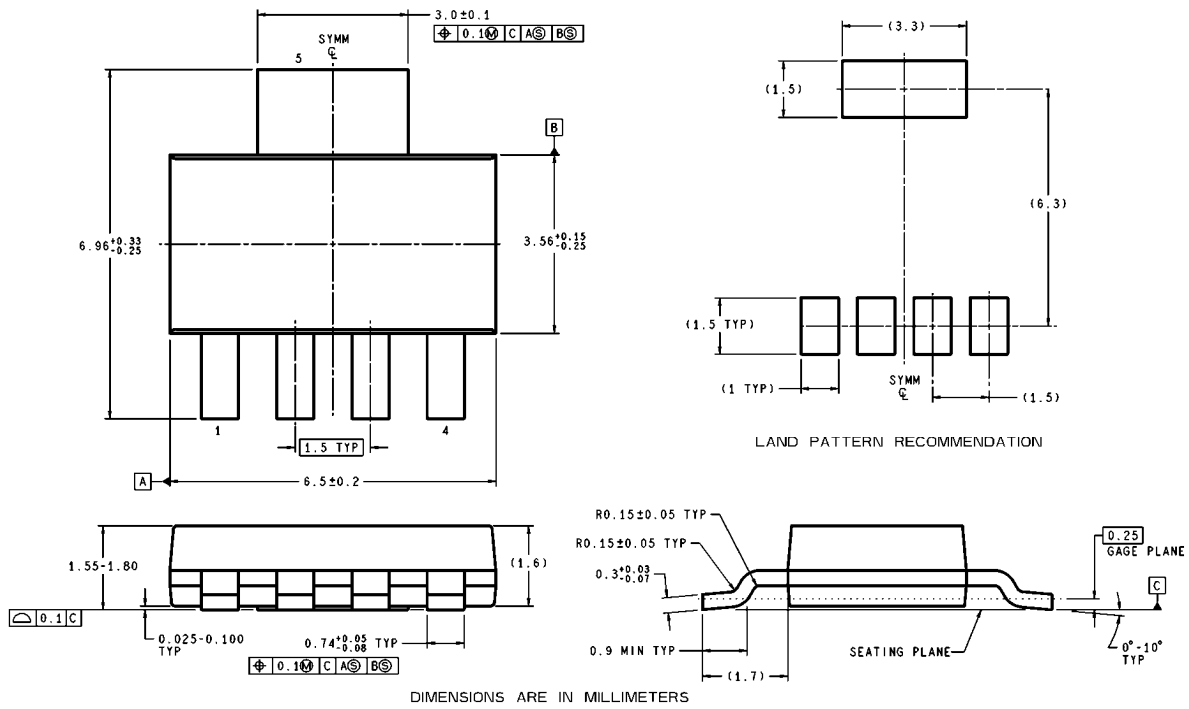
**6-lead, LLP Package**  
**NS Package Number SDE06A**

SDE06A (Rev A)



**TO-252 Package**  
**NS Package Number TD03B**

TD03B (Rev C)



MP05A (Rev A)

**SOT-223 Package**  
**NS Package Number MP05A**

# Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

| Products   |   | Design Support  |  |
|------------|---|---|--|
| Amplifiers | <a href="http://www.national.com/amplifiers">www.national.com/amplifiers</a>  | WEBENCH   | <a href="http://www.national.com/webench">www.national.com/webench</a>   |
| Audio      | <b>National Semiconductor Americas Technical Support Center</b><br>Email: <a href="mailto:support@nsc.com">support@nsc.com</a><br>Tel: 1-800-272-9959 | <b>National Semiconductor Europe Technical Support Center</b><br>Email: <a href="mailto:europe.support@nsc.com">europe.support@nsc.com</a><br>German Tel: +49 (0) 180 5010 771<br>English Tel: +44 (0) 870 850 4288 | <b>National Semiconductor Asia Pacific Technical Support Center</b><br>Email: <a href="mailto:ap.support@nsc.com">ap.support@nsc.com</a> |
|            |   |   | <b>National Semiconductor Japan Technical Support Center</b><br>Email: <a href="mailto:jpn.feedback@nsc.com">jpn.feedback@nsc.com</a>    |

[www.national.com](http://www.national.com)