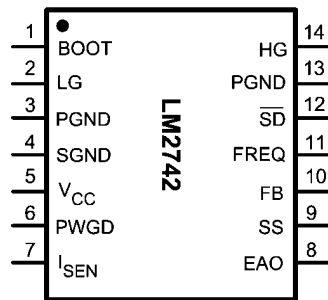


Connection Diagram



14-Lead Plastic TSSOP
 $\theta_{JA} = 155^{\circ}\text{C/W}$

20087511

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2742MTC	TSSOP-14	MTC14	94 Units, Rail
LM2742MTCX	TSSOP-14	MTC14	2500 Units on Tape and Reel

Pin Descriptions

BOOT (Pin 1) - Supply rail for the N-channel MOSFET gate drive. The voltage should be at least one gate threshold above the regulator input voltage to properly turn on the high-side N-FET.

LG (Pin 2) - Gate drive for the low-side N-channel MOSFET. This signal is interlocked with HG to avoid shoot-through problems.

PGND (Pins 3, 13) - Ground for FET drive circuitry. It should be connected to system ground.

SGND (Pin 4) - Ground for signal level circuitry. It should be connected to system ground.

V_{CC} (Pin 5) - Supply rail for the controller.

PWGD (Pin 6) - Power Good. This is an open drain output. The pin is pulled low when the chip is in UVP, OVP, or UVLO mode. During normal operation, this pin is connected to V_{CC} or other voltage source through a pull-up resistor.

ISEN (Pin 7) - Current limit threshold setting. This sources a fixed 50μA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side FET.

EAO (Pin 8) - Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp

signal to determine the duty cycle. This pin is necessary for compensating the control loop.

SS (Pin 9) - Soft start pin. A capacitor connected between this pin and ground sets the speed at which the output voltage ramps up. Larger capacitor value results in slower output voltage ramp but also lower inrush current.

FB (Pin 10) - This is the inverting input of the error amplifier, which is used for sensing the output voltage and compensating the control loop.

FREQ (Pin 11) - The switching frequency is set by connecting a resistor between this pin and ground.

SD (Pin 12) - IC Logic Shutdown. When this pin is pulled low the chip turns off both the high side and low side switches. While this pin is low, the IC will not start up. An internal 20μA pull-up connects this pin to V_{CC}. For a device which turns on the low side switch during shutdown, see the pin compatible LM2737.

HG (Pin 14) - Gate drive for the high-side N-channel MOSFET. This signal is interlocked with LG to avoid shoot-through problems.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	7V
BOOTV	21V
LG and HG to GND (Note 3)	-2V to 21V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C
Soldering Information	

Lead Temperature (soldering, 10sec)	260°C
Infrared or Convection (20sec)	235°C
ESD Rating	2 kV

Operating Ratings

Supply Voltage (V_{CC})	4.5V to 5.5V
Junction Temperature Range	-40°C to +125°C
Thermal Resistance (θ_{JA})	155°C/W

Electrical Characteristics

$V_{CC} = 5V$ unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J = +25^\circ C$. Limits appearing in boldface type apply over full Operating Temperature Range. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB_ADJ}	FB Pin Voltage	$V_{CC} = 4.5V, 0^\circ C \text{ to } +125^\circ C$	0.591	0.6	0.609	V
		$V_{CC} = 5V, 0^\circ C \text{ to } +125^\circ C$	0.591	0.6	0.609	
		$V_{CC} = 5.5V, 0^\circ C \text{ to } +125^\circ C$	0.591	0.6	0.609	
		$V_{CC} = 4.5V, -40^\circ C \text{ to } +125^\circ C$	0.589	0.6	0.609	
		$V_{CC} = 5V, -40^\circ C \text{ to } +125^\circ C$	0.589	0.6	0.609	
		$V_{CC} = 5.5V, -40^\circ C \text{ to } +125^\circ C$	0.589	0.6	0.609	
V_{ON}	UVLO Thresholds	Rising		4.2		V
		Falling		3.6		
I_{Q-V5}	Operating V_{CC} Current	SD = 5V, FB = 0.55V Fsw = 600kHz	1	1.5	2	mA
		SD = 5V, FB = 0.65V Fsw = 600kHz	0.8	1.7	2.2	
	Shutdown V_{CC} Current	SD = 0V	0.15	0.4	0.7	mA
t_{PWGD1}	PWGD Pin Response Time	FB Voltage Going Up		6		μs
t_{PWGD2}	PWGD Pin Response Time	FB Voltage Going Down		6		μs
I_{SD}	SD Pin Internal Pull-up Current			20		μA
I_{SS-ON}	SS Pin Source Current	SS Voltage = 2.5V 0°C to +125°C	8	11	15	μA
		-40°C to +125°C	5	11	15	
I_{SS-OC}	SS Pin Sink Current During Over Current	SS Voltage = 2.5V		95		

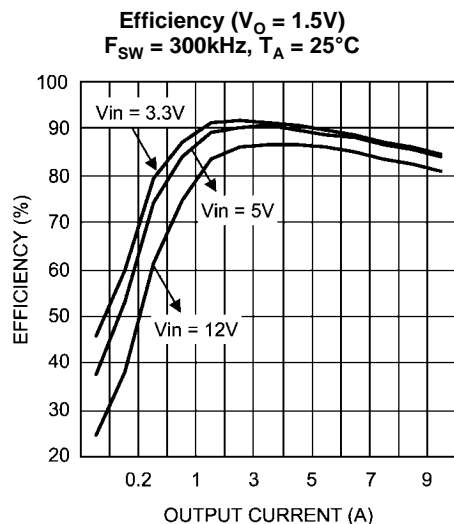
Symbol	Parameter	Conditions	Min	Typ	Max	Units
GATE DRIVE						
I_{Q-BOOT}	BOOT Pin Quiescent Current	BOOT = 12V, EN = 0 0°C to +125°C -40°C to +125°C		95 95	160 215	μA
R_{DS1}	Top FET Driver Pull-Up ON resistance	BOOT-SW = 5V@350mA		3		Ω
R_{DS2}	Top FET Driver Pull-Down ON resistance	BOOT-SW = 5V@350mA		2		Ω
R_{DS3}	Bottom FET Driver Pull-Up ON resistance	BOOT-SW = 5V@350mA		3		Ω
R_{DS4}	Bottom FET Driver Pull-Down ON resistance	BOOT-SW = 5V@350mA		2		Ω
OSCILLATOR						
f_{OSC}	PWM Frequency	$R_{FADJ} = 590k\Omega$		50		kHz
		$R_{FADJ} = 88.7k\Omega$		300		
		$R_{FADJ} = 42.2k\Omega$, 0°C to +125°C	500	600	700	
		$R_{FADJ} = 42.2k\Omega$, -40°C to +125°C	490	600	700	
		$R_{FADJ} = 17.4k\Omega$		1400		
		$R_{FADJ} = 11.3k\Omega$		2000		
D	Max Duty Cycle	$f_{PWM} = 300kHz$ $f_{PWM} = 600kHz$		90 88		%
t_{on-min}	Minimum on-time			40		ns
LOGIC INPUTS AND OUTPUTS						
V_{SD-IH}	SD Pin Logic High Trip Point			2.6	3.5	V
V_{SD-IL}	SD Pin Logic Low Trip Point	0°C to +125°C -40°C to +125°C	1.3 1.25	1.6 1.6		V
$V_{PWGD-TH-LO}$	PWGD Pin Trip Points	FB Voltage Going Down 0°C to +125°C -40°C to +125°C	0.413 0.410	0.430 0.430	0.446 0.446	V
$V_{PWGD-TH-HI}$	PWGD Pin Trip Points	FB Voltage Going Up 0°C to +125°C -40°C to +125°C	0.691 0.688	0.710 0.710	0.734 0.734	V
$V_{PWGD-HYS}$	PWGD Hysteresis	FB Voltage Going Down FB Voltage Going Up		35 110		mV

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. **Operating ratings** indicate conditions for which the device operates correctly. **Operating Ratings** do not imply guaranteed performance limits.

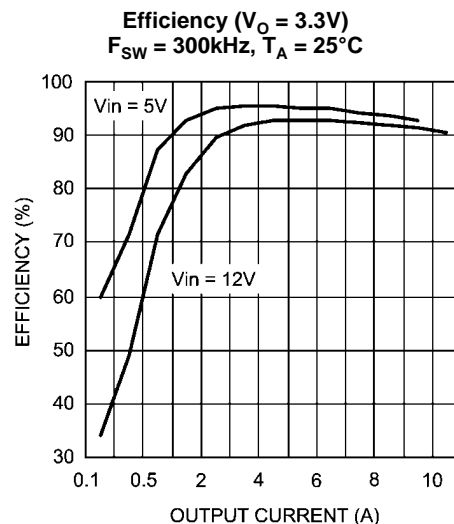
Note 2: The human body model is a 100pF capacitor discharged through a 1.5k resistor into each pin.

Note 3: The LG and HG pin can have -2V to -0.5V applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a LG and HG pin voltage range of -0.5V to 21V.

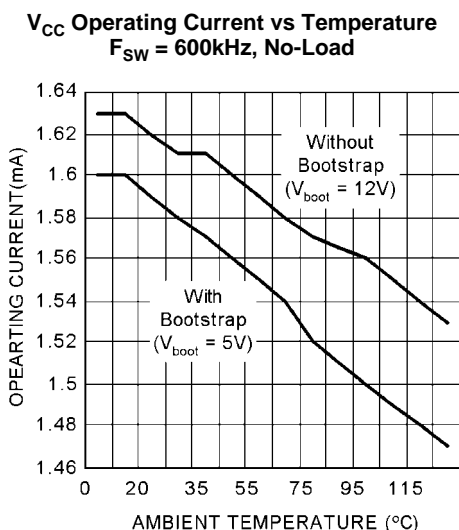
Typical Performance Characteristics



20087512

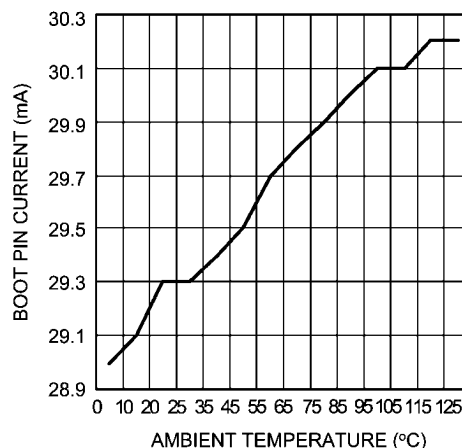


20087513



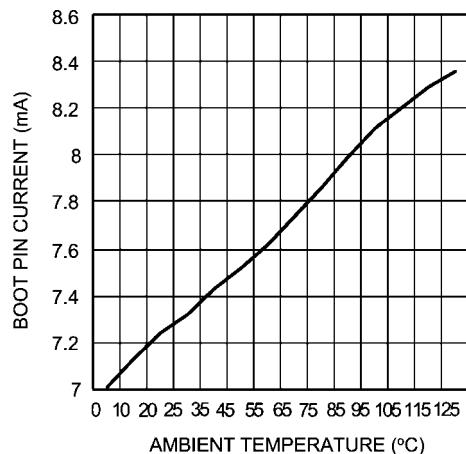
20087514

Bootpin Current vs Temperature for $BOOTV = 12V$
 $F_{SW} = 600kHz$, Si4826DY FET, No-Load



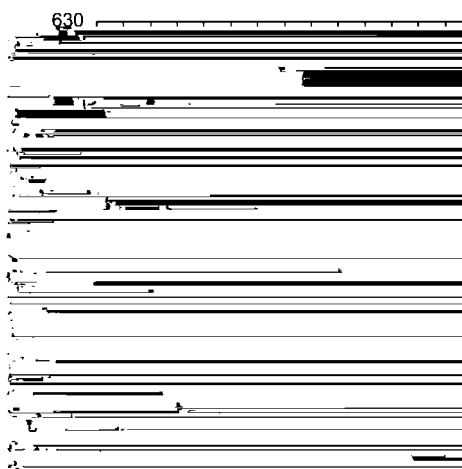
20087515

Bootpin Current vs Temperature with 5V Bootstrap
 $F_{SW} = 600kHz$, Si4826DY FET, No-Load



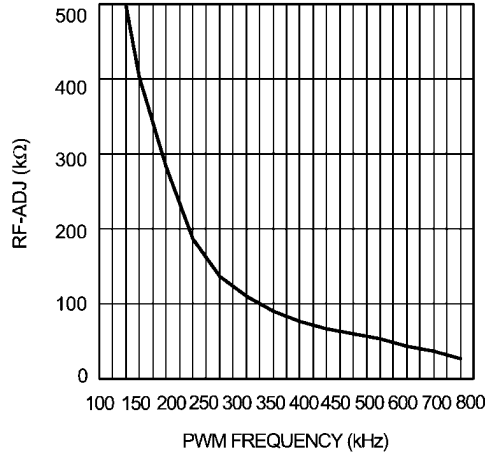
20087516

PWM Frequency vs Temperature
 for $R_{FADJ} = 43.2k\Omega$



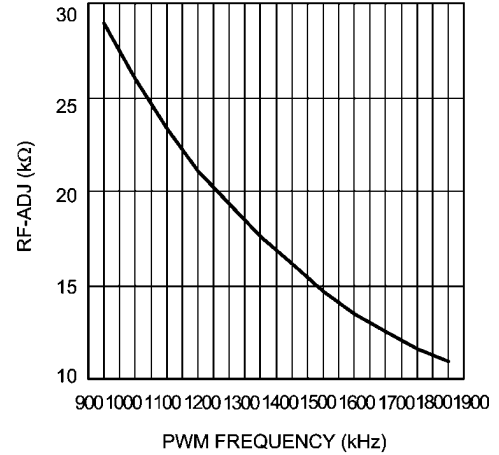
20087517

R_{FADJ} vs PWM Frequency
(in 100 to 800kHz range), $T_A = 25^\circ\text{C}$



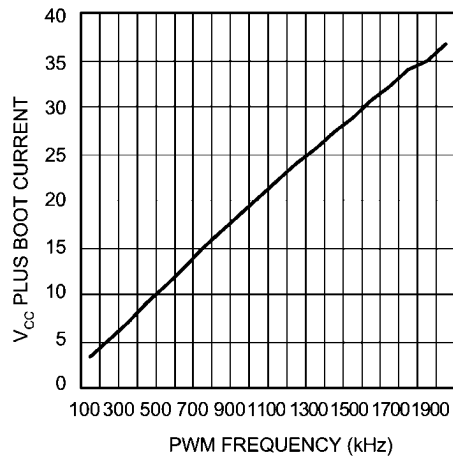
20087518

R_{FADJ} vs PWM Frequency
(in 900 to 2000kHz range), $T_A = 25^\circ\text{C}$



20087519

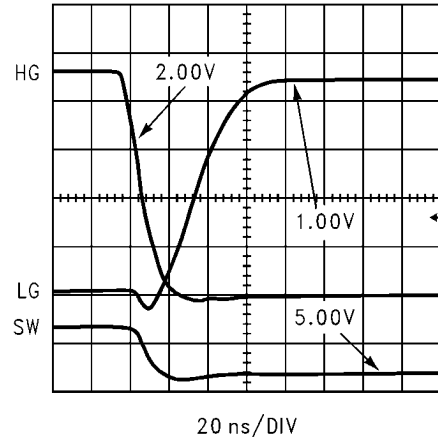
V_{CC} Operating Current Plus Boot Current vs PWM Frequency
(Si4826DY FET, $T_A = 25^\circ\text{C}$)



20087520

Switch Waveforms (HG Falling)

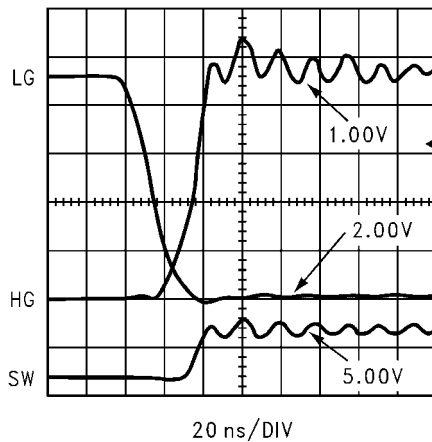
$V_{IN} = 5\text{V}$, $V_O = 1.8\text{V}$
 $I_O = 3\text{A}$, $C_{SS} = 10\text{nF}$
 $F_{SW} = 600\text{kHz}$



20087523

Switch Waveforms (HG Rising)

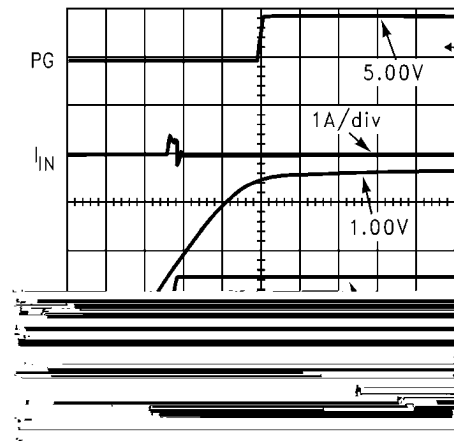
$V_{IN} = 5\text{V}$, $V_O = 1.8\text{V}$
 $I_O = 3\text{A}$, $F_{SW} = 600\text{kHz}$



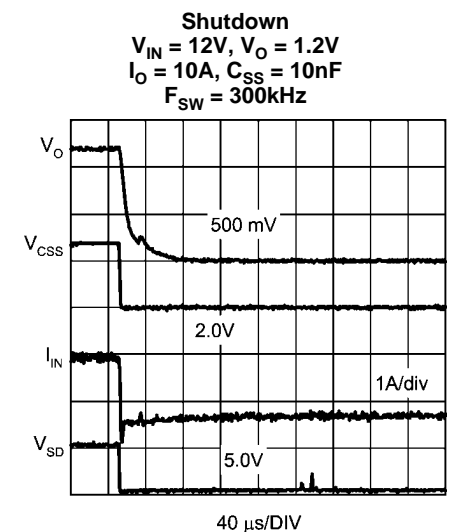
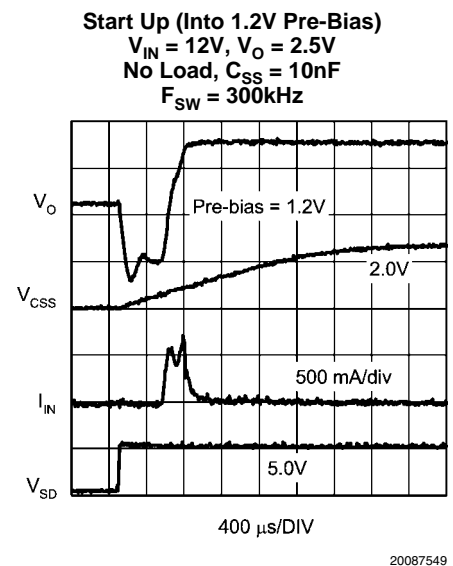
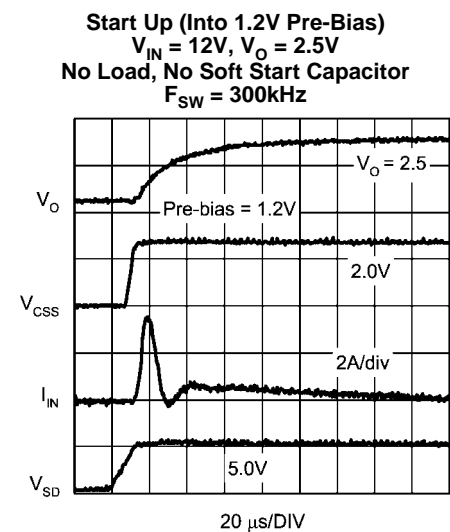
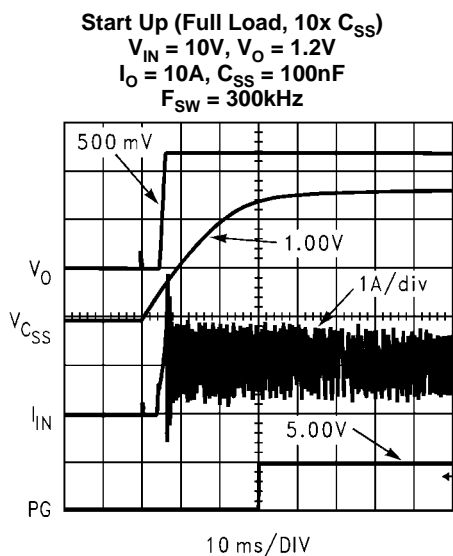
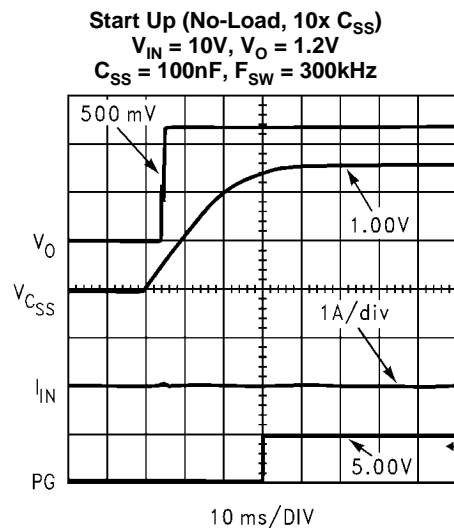
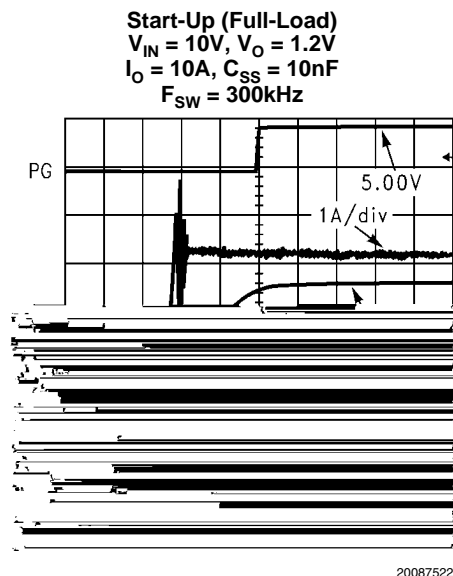
20087524

Start-Up (No-Load)

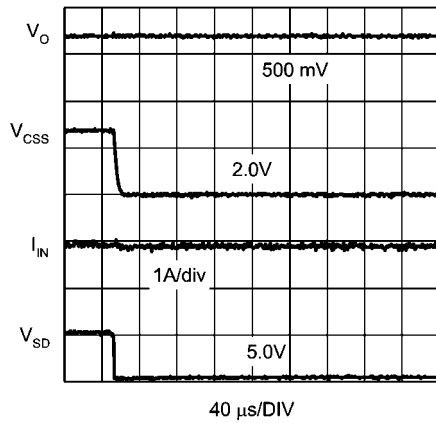
$V_{IN} = 10\text{V}$, $V_O = 1.2\text{V}$
 $C_{SS} = 10\text{nF}$, $F_{SW} = 300\text{kHz}$



20087521

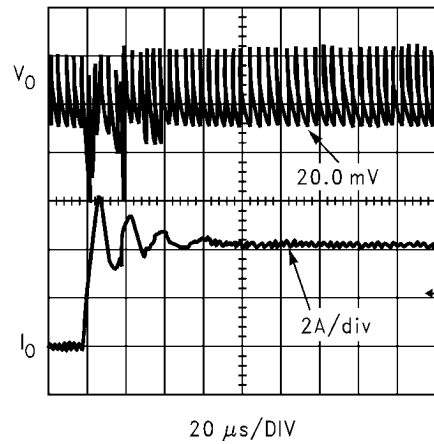


Shutdown (No Load)
 $V_{IN} = 12V$, $V_O = 1.2V$
 $I_O = 10A$, $C_{SS} = 10nF$
 $F_{SW} = 300kHz$



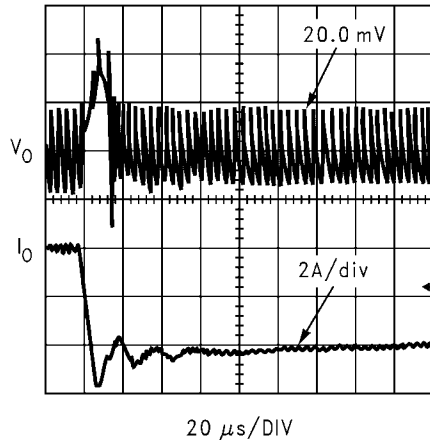
20087533

Load Transient Response ($I_O = 0$ to 4A)
 $V_{IN} = 12V$, $V_O = 1.2V$
 $F_{SW} = 300kHz$



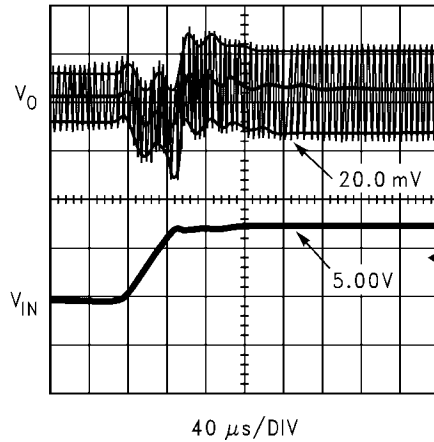
20087528

Load Transient Response ($I_O = 4$ to 0A)
 $V_{IN} = 12V$, $V_O = 1.2V$
 $F_{SW} = 300kHz$



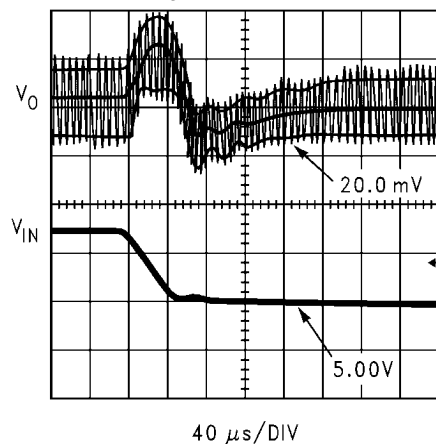
20087529

Line Transient Response ($V_{IN} = 5V$ to 12V)
 $V_O = 1.2V$, $I_O = 5A$
 $F_{SW} = 300kHz$



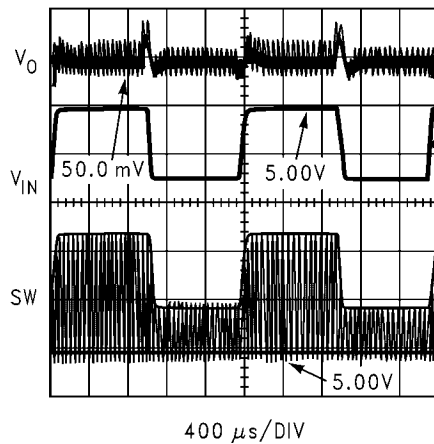
20087530

Line Transient Response ($V_{IN} = 12V$ to 5V)
 $V_O = 1.2V$, $I_O = 5A$
 $F_{SW} = 300kHz$



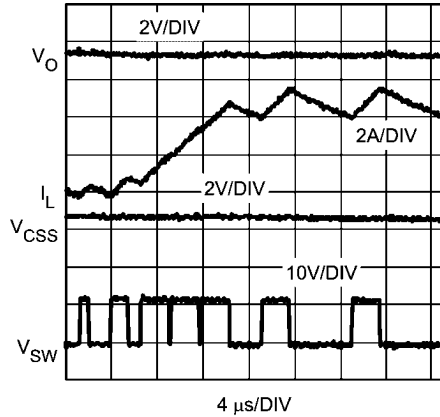
20087531

Line Transient Response
 $V_O = 1.2V$, $I_O = 5A$
 $F_{SW} = 300kHz$



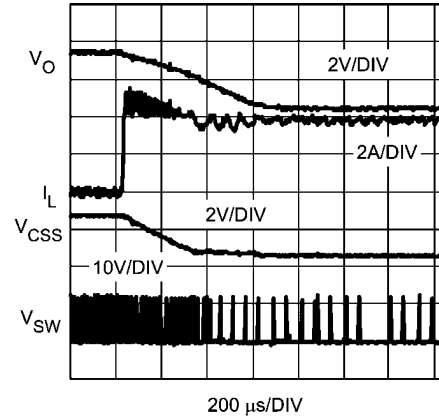
20087532

Peak Current During Current Limit
 $V_{IN} = 12V$, $V_O = 3.3V$, $I_{LIM} = 4A$, $F_{SW} = 300kHz$, $L = 15\mu H$



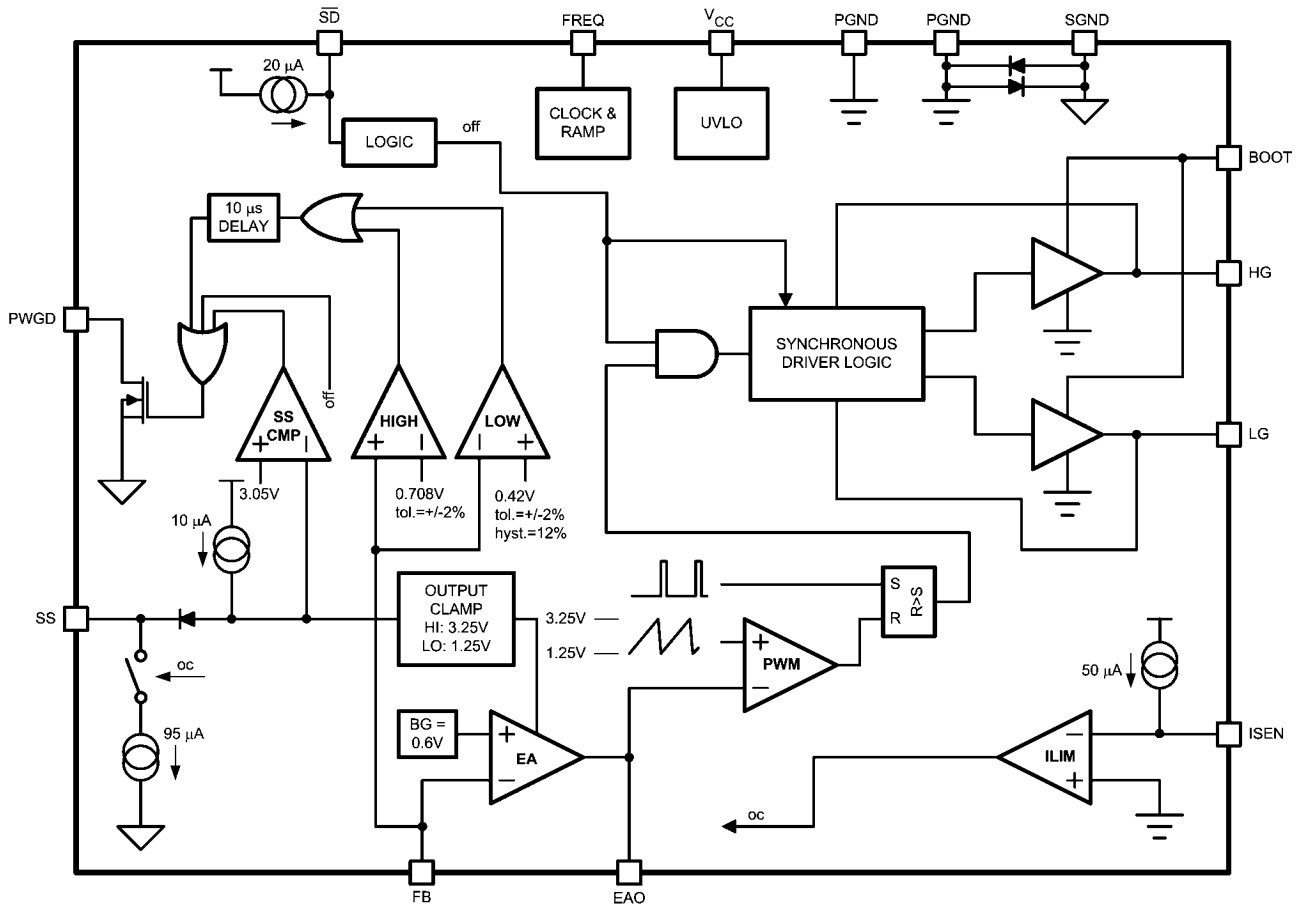
20087552

Peak Current During Current Limit
 $V_{IN} = 12V$, $V_O = 3.3V$, $I_{LIM} = 4A$, $F_{SW} = 300kHz$, $L = 15\mu H$



20087553

Block Diagram



20087501

Application Information

THEORY OF OPERATION

The LM2742 is a voltage-mode, high-speed synchronous buck regulator with a PWM control scheme. It is designed for use in set-top boxes, thin clients, DSL/Cable modems, and other applications that require high efficiency buck converters. It has power good (PWRGD), and output shutdown (\overline{SD}). Current limit is achieved by sensing the voltage V_{DS} across the low side FET. During current limit the high side gate is turned off and the low side gate turned on. The soft start capacitor is discharged by a 95 μ A source (reducing the maximum duty cycle) until the current is under control.

START UP

When V_{CC} exceeds 4.2V and the shutdown pin \overline{SD} sees a logic high the soft start capacitor begins charging through an internal fixed 10 μ A source. During this time the output of the error amplifier is allowed to rise with the voltage of the soft start capacitor. This capacitor, C_{SS} , determines soft start time, and can be determined approximately by:

$$C_{SS} = \frac{t_{ss}}{2.5 \times 10^5}$$

An application for a microprocessor might need a delay of 3ms, in which case C_{SS} would be 12nF. For a different device, a 100ms delay might be more appropriate, in which case C_{SS} would be 400nF. (390 10%) During soft start the PWRGD flag is forced low and is released when the voltage reaches a set value. At this point this chip enters normal operation mode and the Power Good flag is released.

Since the output is floating when the LM2742 is turned off, it is possible that the output capacitor may be precharged to some positive value. During start-up, the LM2742 operates fully synchronous and will discharge the output capacitor to some extent depending on the output voltage, soft start capacitance, and the size of the output capacitor.

NORMAL OPERATION

While in normal operation mode, the LM2742 regulates the output voltage by controlling the duty cycle of the high side and low side FETs. The equation governing output voltage is:

$$V_O = 0.6 \times (R_{FB1} + R_{FB2}) / R_{FB1}$$

The PWM frequency is adjustable between 50kHz and 2MHz and is set by an external resistor, R_{FADJ} , between the FREQ pin and ground. The resistance needed for a desired frequency is approximately:

$$R_{FADJ} = \left(\frac{20500}{\text{freq}[\text{kHz}]} \right)^{1.0526} \text{ k}\Omega$$

MOSFET GATE DRIVERS

The LM2742 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Power for the drivers is supplied through the BOOT pin. For the high side gate (HG) to fully turn on the top FET, the BOOT voltage must be at least one $V_{GS(th)}$ greater than V_{in} . ($BOOT \geq 2 \times V_{in}$) This voltage can be supplied by a separate, higher voltage source, or supplied from a local charge pump structure. In a system such as a desktop computer, both 5V and 12V are usually available. Hence if V_{in} was 5V, the 12V supply could be used for BOOT. 12V is more than $2 \times V_{in}$, so the HG would operate

correctly. For a BOOT of 12V, the initial gate charging current is 2A, and the initial gate discharging current is typically 6A.

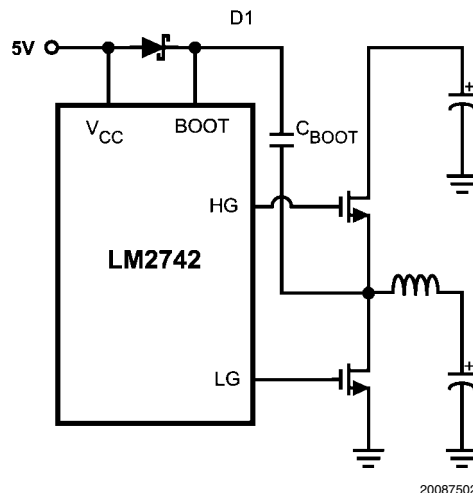


FIGURE 1. BOOT Supplied by Charge Pump

In a system without a separate, higher voltage, a charge pump (bootstrap) can be built using a diode and small capacitor, Figure 1. The capacitor serves to maintain enough voltage between the top FET gate and source to control the device even when the top FET is on and its source has risen up to the input voltage level.

The LM2742 gate drivers use a BiCMOS design. Unlike some other bipolar control ICs, the gate drivers have rail-to-rail swing, ensuring no spurious turn-on due to capacitive coupling.

POWER GOOD SIGNAL

The power good signal is the or-gated flag representing over-voltage and under-voltage protection. If the output voltage is 18% over its nominal value, $V_{FB} = 0.7V$, or falls 30% below that value, $V_{FB} = 0.41V$, the power good flag goes low. It will return to a logic high whenever the feedback pin voltage is between 70% and 118% of 0.6V. The power good pin is an open drain output that can be pulled up to logic voltages of 5V or less with a 10k Ω resistor.

UVLO

The 4.2V turn-on threshold on V_{CC} has a built in hysteresis of 0.6V. Therefore, if V_{CC} drops below 3.6V, the chip enters UVLO mode. UVLO consists of turning off the top FET, turning off the bottom FET, and remaining in that condition until V_{CC} rises above 4.2V. As with shutdown, the soft start capacitor is discharged through a FET, ensuring that the next start-up will be smooth.

CURRENT LIMIT

Current limit is realized by sensing the voltage across the low side FET while it is on. The $R_{DS(on)}$ of the FET is a known value, hence the current through the FET can be determined as:

$$V_{DS} = I \times R_{DS(on)}$$

The current through the low side FET while it is on is also the falling portion of the triangle wave inductor current. The current limit threshold is determined by an external resistor, R_{CS} , connected between the switch node and the I_{SEN} pin. A constant current of 50 μ A is forced through R_{CS} , causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has

been reached. R_{CS} can be found by using the following equation:

$$R_{CS} = R_{DS(ON)(LOW)} * I_{LIM} / 50\mu A$$

For example, a conservative 15A current limit in a 10A design with a minimum $R_{DS(ON)}$ of $10m\Omega$ would require a $3.3k\Omega$ resistor. Because current sensing is done across the low side FET, no minimum high side on-time is necessary. In the current limit mode the LM2727/37 will turn the high side off and the keep low side on for as long as necessary. The LM2727/37 enters current limit mode if the inductor current exceeds the current limit threshold at the point where the high side FET turns off and the low side FET turns on. (The point of peak inductor current. See .) Note that in normal operation mode the high side FET always turns on at the beginning of a clock cycle. In current limit mode, by contrast, the high side FET on pulse is skipped. This causes inductor current to fall. Unlike a normal operation switching cycle, however, in a current limit mode switching cycle the high side FET will turn on as soon as inductor current has fallen to the current limit threshold. The LM2727/37 will continue to skip high side FET pulses until the inductor current peak is below the current limit threshold, at which point the system resumes normal operation.

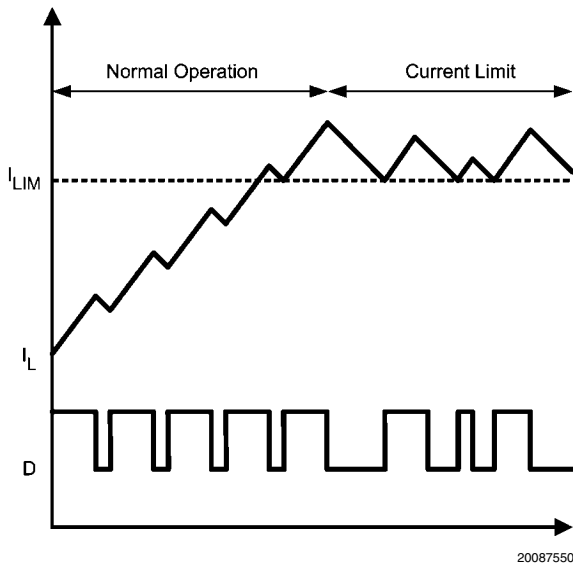


FIGURE 2. Current Limit Threshold

Unlike a high side FET current sensing scheme, which limits the peaks of inductor current, low side current sensing is only allowed to limit the current during the converter off-time, when inductor current is falling. Therefore in a typical current limit plot the valleys are normally well defined, but the peaks are variable, according to the duty cycle. The PWM error amplifier and comparator control the off pulse of the high side FET, even during current limit mode, meaning that peak inductor current can exceed the current limit threshold. Assuming that the output inductor does not saturate, the maximum peak inductor current during current limit mode can be calculated with the following equation:

$$I_{PK-CL} = I_{LIM} + (T_{OSC} - 200 \text{ ns}) \frac{V_{IN} - V_O}{L}$$

Where T_{OSC} is the inverse of switching frequency f_{OSC} . The 200ns term represents the minimum off-time of the duty cycle,

which ensures enough time for correct operation of the current sensing circuitry. See the plots entitled Peak Current During Current Limit in the *Typical Performance Characteristics* section.

In order to minimize the time period in which peak inductor current exceeds the current limit threshold, the IC also discharges the soft start capacitor through a fixed $95\mu A$ source. The output of the LM2727/37 internal error amplifier is limited by the voltage on the soft start capacitor. Hence, discharging the soft start capacitor reduces the maximum duty cycle D of the controller. During severe current limit this reduction in duty cycle will reduce the output voltage if the current limit conditions last for an extended time. Output inductor current will be reduced in turn to a flat level equal to the current limit threshold. The third benefit of the soft start capacitor discharge is a smooth, controlled ramp of output voltage when the current limit condition is cleared. During the first few nanoseconds after the low side gate turns on, the low side FET body diode conducts. This causes an additional $0.7V$ drop in V_{DS} . The range of V_{DS} is normally much lower. For example, if $R_{DS(ON)}$ were $10m\Omega$ and the current through the FET was $10A$, V_{DS} would be $0.1V$. The current limit would see $0.7V$ as a $70A$ current and enter current limit immediately. Hence current limit is masked during the time it takes for the high side switch to turn off and the low side switch to turn on.

SHUT DOWN

If the shutdown pin \overline{SD} is pulled low, the LM2742 discharges the soft start capacitor through a MOSFET switch. The high side and low side switches are turned off. The LM2742 remains in this state until \overline{SD} is released.

DESIGN CONSIDERATIONS

The following is a design procedure for all the components needed to create the circuit shown in *Figure 4* in the Example Circuits section, a $5V$ in to $1.2V$ out converter, capable of delivering $10A$ with an efficiency of 85% . The switching frequency is $300kHz$. The same procedures can be followed to create many other designs with varying input voltages, output voltages, and output currents.

Input Capacitor

The input capacitors in a Buck switching converter are subjected to high stress due to the input current waveform, which is a square wave. Hence input caps are selected for their ripple current capability and their ability to withstand the heat generated as that ripple current runs through their ESR. Input rms ripple current is approximately:

$$I_{rms_rip} = I_o * \sqrt{D(1 - D)}$$

The power dissipated by each input capacitor is:

$$P_D = \frac{I_{rms_rip}^2 * ESR}{n^2}$$

Here, n is the number of capacitors, and indicates that power loss in each cap decreases rapidly as the number of input caps increase. The worst-case ripple for a Buck converter occurs during full load, when the duty cycle $D = 50\%$.

In the $5V$ to $1.2V$ case, $D = 1.2/5 = 0.24$. With a $10A$ maximum load the ripple current is $4.3A$. The Sanyo 10MV5600AX aluminum electrolytic capacitor has a ripple current rating of $2.35A$, up to $105^\circ C$. Two such capacitors make a conservative design that allows for unequal current sharing between

individual caps. Each capacitor has a maximum ESR of 18mΩ at 100 kHz. Power loss in each device is then 0.05W, and total loss is 0.1W. Other possibilities for input and output capacitors include MLCC, tantalum, OSCON, SP, and POSCAPS.

Input Inductor

The input inductor serves two basic purposes. First, in high power applications, the input inductor helps insulate the input power supply from switching noise. This is especially important if other switching converters draw current from the same supply. Noise at high frequency, such as that developed by the LM2742 at 1MHz operation, could pass through the input stage of a slower converter, contaminating and possibly interfering with its operation.

An input inductor also helps shield the LM2742 from high frequency noise generated by other switching converters. The second purpose of the input inductor is to limit the input current slew rate. During a change from no-load to full-load, the input inductor sees the highest voltage change across it, equal to the full load current times the input capacitor ESR. This value divided by the maximum allowable input current slew rate gives the minimum input inductance:

$$L_{in} = \frac{\Delta V}{\left(\frac{di}{dt}\right)_{max}}$$

In the case of a desktop computer system, the input current slew rate is the system power supply or "silver box" output current slew rate, which is typically about 0.1A/μs. Total input capacitor ESR is 9mΩ, hence ΔV is 10*0.009 = 90 mV, and the minimum inductance required is 0.9μH. The input inductor should be rated to handle the DC input current, which is approximated by:

$$I_{N-DC} = \frac{I_o * D}{\eta}$$

In this case I_{N-DC} is about 2.8A. One possible choice is the TDK SLF12575T-1R2N8R2, a 1.2μH device that can handle 8.2Arms, and has a DCR of 7mΩ.

Output Inductor

The output inductor forms the first half of the power stage in a Buck converter. It is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple. (ΔI_o) The inductance is chosen by selecting between tradeoffs in output ripple, efficiency, and response time. The smaller the output inductor, the more quickly the converter can respond to transients in the load current. If the inductor value is increased, the ripple through the output capacitor is reduced and thus the output ripple is reduced. As shown in the efficiency calculations, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. An increase in frequency can mean increasing loss in the FETs due to the charging and discharging of the gates. Generally the switching frequency is chosen so that conduction loss outweighs switching loss. The equation for output inductor selection is:

$$L = \frac{V_{in} - V_o}{\Delta I_o * F_{SW}} * D$$

A good range for ΔI_o is 25 to 50% of the output current. In the past, 30% was considered a maximum value for output currents higher than about 2Amps, but as output capacitor technology improves the ripple current can be allowed to increase. Plugging in the values for output current ripple, input voltage, output voltage, switching frequency, and assuming a 40% peak-to-peak output current ripple yields an inductance of 1.5μH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is $(I_o + 0.5*\Delta I_o)$. This is 12A for a 10A design. The Coilcraft D05022-152HC is 1.5μH, is rated to 15Arms, and has a DCR of 4mΩ.

Output Capacitor

The output capacitor forms the second half of the power stage of a Buck switching converter. It is used to control the output voltage ripple (ΔV_o) and to supply load current during fast load transients.

In this example the output current is 10A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. (Other possibilities include ceramic, tantalum, and solid electrolyte capacitors, however the ceramic type often do not have the large capacitance needed to supply current for load transients, and tantalums tend to be more expensive than aluminum electrolytic.) Aluminum capacitors tend to have very high capacitance and fairly low ESR, meaning that the ESR zero, which affects system stability, will be much lower than the switching frequency. The large capacitance means that at switching frequency, the ESR is dominant, hence the type and number of output capacitors is selected on the basis of ESR. One simple formula to find the maximum ESR based on the desired output voltage ripple, ΔV_o and the designed output current ripple, ΔI_o , is:

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_o}$$

In this example, in order to maintain a 2% peak-to-peak output voltage ripple and a 40% peak-to-peak inductor current ripple, the required maximum ESR is 6mΩ. Three Sanyo 10MV5600AX capacitors in parallel will give an equivalent ESR of 6mΩ. The total bulk capacitance of 16.8mF is enough to supply even severe load transients. Using the same capacitors for both input and output also keeps the bill of materials simple.

Mosfets

MOSFETS are a critical part of any switching controller and have a direct impact on the system efficiency. In this case the target efficiency is 85% and this is the variable that will determine which devices are acceptable. Loss from the capacitors, inductors, and the LM2742 itself are detailed in the Efficiency section, and come to about 0.54W. To meet the target efficiency, this leaves 1.45W for the FET conduction loss, gate charging loss, and switching loss. Switching loss is particularly difficult to estimate because it depends on many factors. When the load current is more than about 1 or 2 amps, conduction losses outweigh the switching and gate charging losses. This allows FET selection based on the $R_{DS(on)}$ of the FET. Adding the FET switching and gate-charging losses to the equation leaves 1.2W for conduction losses. The equation for conduction loss is:

$$P_{Cnd} = D(I_o^2 * R_{DS(on)} * k) + (1-D)(I_o^2 * R_{DS(on)} * k)$$

The factor k is a constant which is added to account for the increasing $R_{DS(on)}$ of a FET due to heating. Here, $k = 1.3$. The Si4442DY has a typical $R_{DS(on)}$ of 4.1mΩ. When plugged into

the equation for P_{CND} the result is a loss of 0.533W. If this design were for a 5V to 2.5V circuit, an equal number of FETs on the high and low sides would be the best solution. With the duty cycle $D = 0.24$, it becomes apparent that the low side FET carries the load current 76% of the time. Adding a second FET in parallel to the bottom FET could improve the efficiency by lowering the effective $R_{DS(on)}$. The lower the duty cycle, the more effective a second or even third FET can be. For a minimal increase in gate charging loss (0.054W) the decrease in conduction loss is 0.15W. What was an 85% design improves to 86% for the added cost of one SO-8 MOSFET.

Control Loop Components

The circuit is this design example and the others shown in the Example Circuits section have been compensated to improve their DC gain and bandwidth. The result of this compensation is better line and load transient responses. For the LM2742, the top feedback divider resistor, R_{fb2} , is also a part of the compensation. For the 10A, 5V to 1.2V design, the values are: $C_{c1} = 4.7\text{pF}$ 10%, $C_{c2} = 1\text{nF}$ 10%, $R_c = 229\text{k}\Omega$ 1%. These values give a phase margin of 63° and a bandwidth of 29.3kHz.

Support Capacitors and Resistors

The C_{inx} capacitors are high frequency bypass devices, designed to filter harmonics of the switching frequency and input noise. Two $1\mu\text{F}$ ceramic capacitors with a sufficient voltage rating (10V for the Circuit of *Figure 4*) will work well in almost any case.

R_{IN} and C_{IN} are standard filter components designed to ensure smooth DC voltage for the chip supply. Depending on noise, R_{IN} should be 10 to 100Ω , and C_{IN} should be between 0.1 and $2.2\mu\text{F}$. C_{BOOT} is the bootstrap capacitor, and should be $0.1\mu\text{F}$. (In the case of a separate, higher supply to the BOOT pin, this $0.1\mu\text{F}$ cap can be used to bypass the supply.) Using a Schottky device for the bootstrap diode allows the minimum drop for both high and low side drivers. The On Semiconductor BAT54 or MBR0520 work well.

R_p is a standard pull-up resistor for the open-drain power good signal, and should be $10\text{k}\Omega$. If this feature is not necessary, it can be omitted.

R_{CS} is the resistor used to set the current limit. Since the design calls for a peak current magnitude ($I_o + 0.5 * \Delta I_o$) of 12A, a safe setting would be 15A. (This is well below the saturation current of the output inductor, which is 25A.) Following the equation from the Current Limit section, use a $3.3\text{k}\Omega$ resistor.

R_{FADJ} is used to set the switching frequency of the chip. Following the equation in the Theory of Operation section, the closest 1% tolerance resistor to obtain $f_{SW} = 300\text{kHz}$ is $88.7\text{k}\Omega$.

C_{SS} depends on the users requirements. Based on the equation for C_{SS} in the Theory of Operation section, for a 3ms delay, a 12nF capacitor will suffice.

EFFICIENCY CALCULATIONS

A reasonable estimation of the efficiency of a switching controller can be obtained by adding together the loss in each current carrying element and using the equation:

$$\eta = \frac{P_o}{P_o + P_{\text{total-loss}}}$$

The following shows an efficiency calculation to complement the Circuit of *Figure 4*. Output power for this circuit is $1.2\text{V} \times 10\text{A} = 12\text{W}$.

Chip Operating Loss

$$P_{IQ} = I_{Q-V_{CC}} * V_{CC}$$

$$2\text{mA} \times 5\text{V} = 0.01\text{W}$$

FET Gate Charging Loss

$$P_{GC} = n * V_{CC} * Q_{GS} * f_{OSC}$$

The value n is the total number of FETs used. The Si4442DY has a typical total gate charge, Q_{GS} , of 36nC and an r_{ds-on} of $4.1\text{m}\Omega$. For a single FET on top and bottom: $2 * 5 * 36\text{E-}9 * 300,000 = 0.108\text{W}$

FET Switching Loss

$$P_{SW} = 0.5 * V_{in} * I_o * (t_r + t_f) * f_{OSC}$$

The Si4442DY has a typical rise time t_r and fall time t_f of 11 and 47ns, respectively. $0.5 * 5 * 10 * 58\text{E-}9 * 300,000 = 0.435\text{W}$

FET Conduction Loss

$$P_{Cn} = 0.533\text{W}$$

Input Capacitor Loss

$$P_{Cin} = \frac{I_{\text{rms-rip}}^2 * \text{ESR}}{n}$$

$$I_{\text{rms-rip}} = I_o * \sqrt{D(1-D)}$$

$$4.282 * 0.018 / 2 = 0.164\text{W}$$

Input Inductor Loss

$$P_{Lin} = I_{in}^2 * \text{DCR}_{\text{input-L}}$$

$$I_{IN} = \frac{I_o * D}{\eta_{\text{est'd}}}$$

$$2.822 * 0.007 = 0.055\text{W}$$

Output Inductor Loss

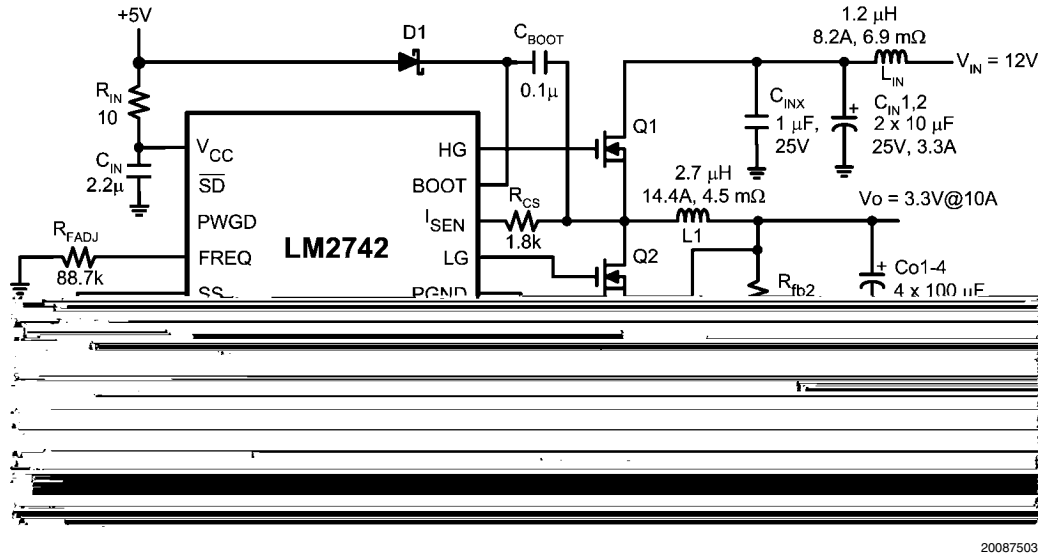
$$P_{Lout} = I_o^2 * \text{DCR}_{\text{output-L}}$$

$$10^2 * 0.004 = 0.4\text{W}$$

System Efficiency

$$\frac{12}{12 + 1.7} = 87.5\%$$

Example Circuits

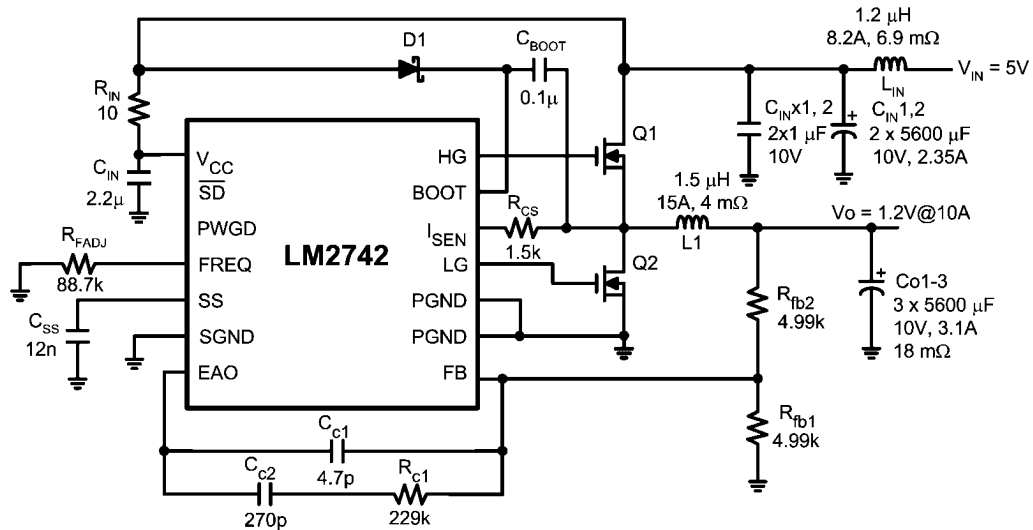


20087503

FIGURE 3. 5V-16V to 3.3V, 10A, 300kHz

This circuit and the one featured on the front page have been designed to deliver high current and high efficiency in a small package, both in area and in height. The tallest component in

this circuit is the inductor L1, which is 6mm tall. The compensation has been designed to tolerate input voltages from 5 to 16V.

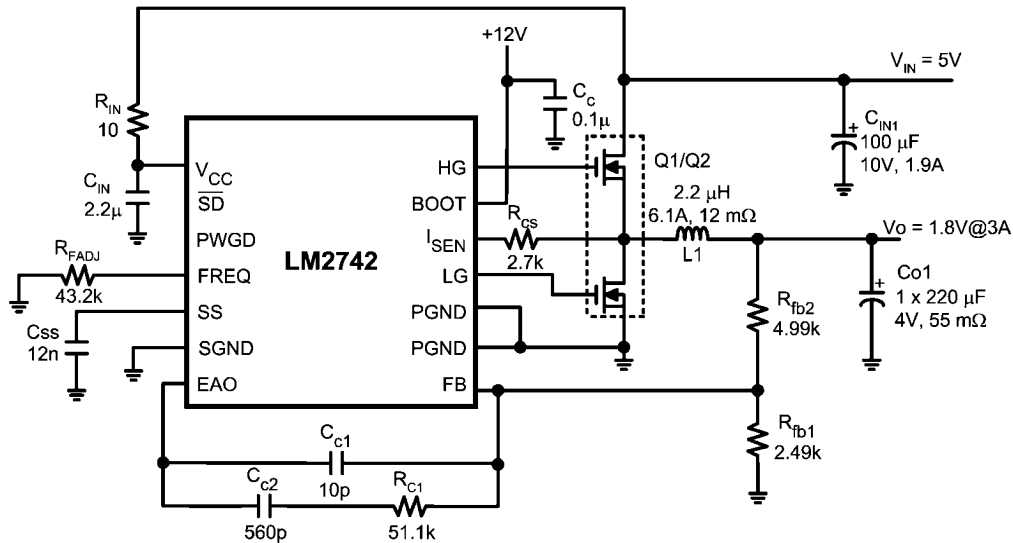


20087504

FIGURE 4. 5V to 1.2V, 10A, 300kHz

This circuit design, detailed in the Design Considerations section, uses inexpensive aluminum capacitors and off-the-shelf inductors. It can deliver 10A at better than 85% efficiency.

Large bulk capacitance on input and output ensure stable operation.

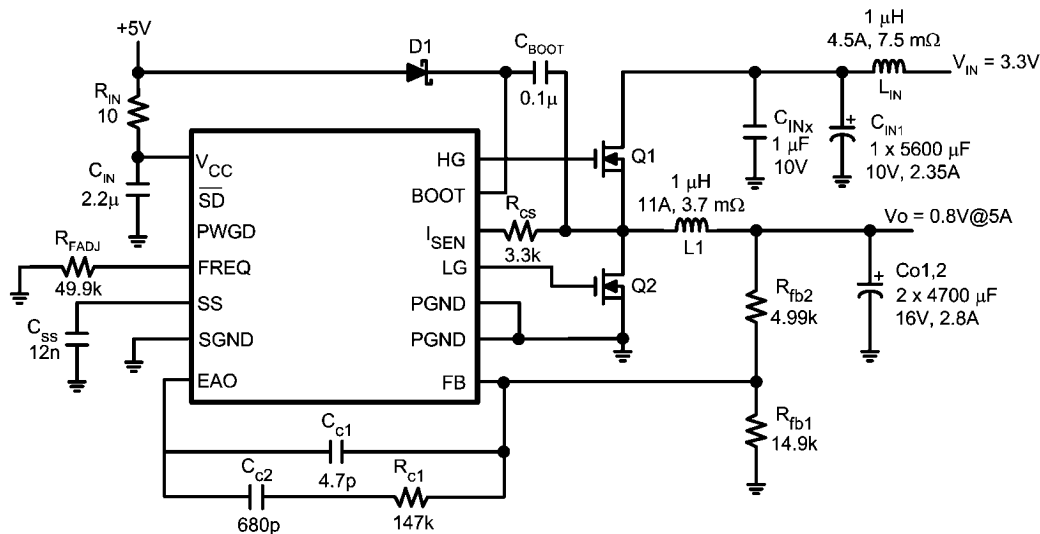


20087505

FIGURE 5. 5V to 1.8V, 3A, 600kHz

The example circuit of *Figure 5* has been designed for minimum component count and overall solution size. A switching frequency of 600kHz allows the use of small input/output capacitors and a small inductor. The availability of separate 5V and 12V supplies (such as those available from desk-top computer supplies) and the low current further reduce com-

ponent count. Using the 12V supply to power the MOSFET drivers eliminates the bootstrap diode, D1. At low currents, smaller FETs or dual FETs are often the most efficient solutions. Here, the Si4826DY, an asymmetric dual FET in an SO-8 package, yields 92% efficiency at a load of 2A.

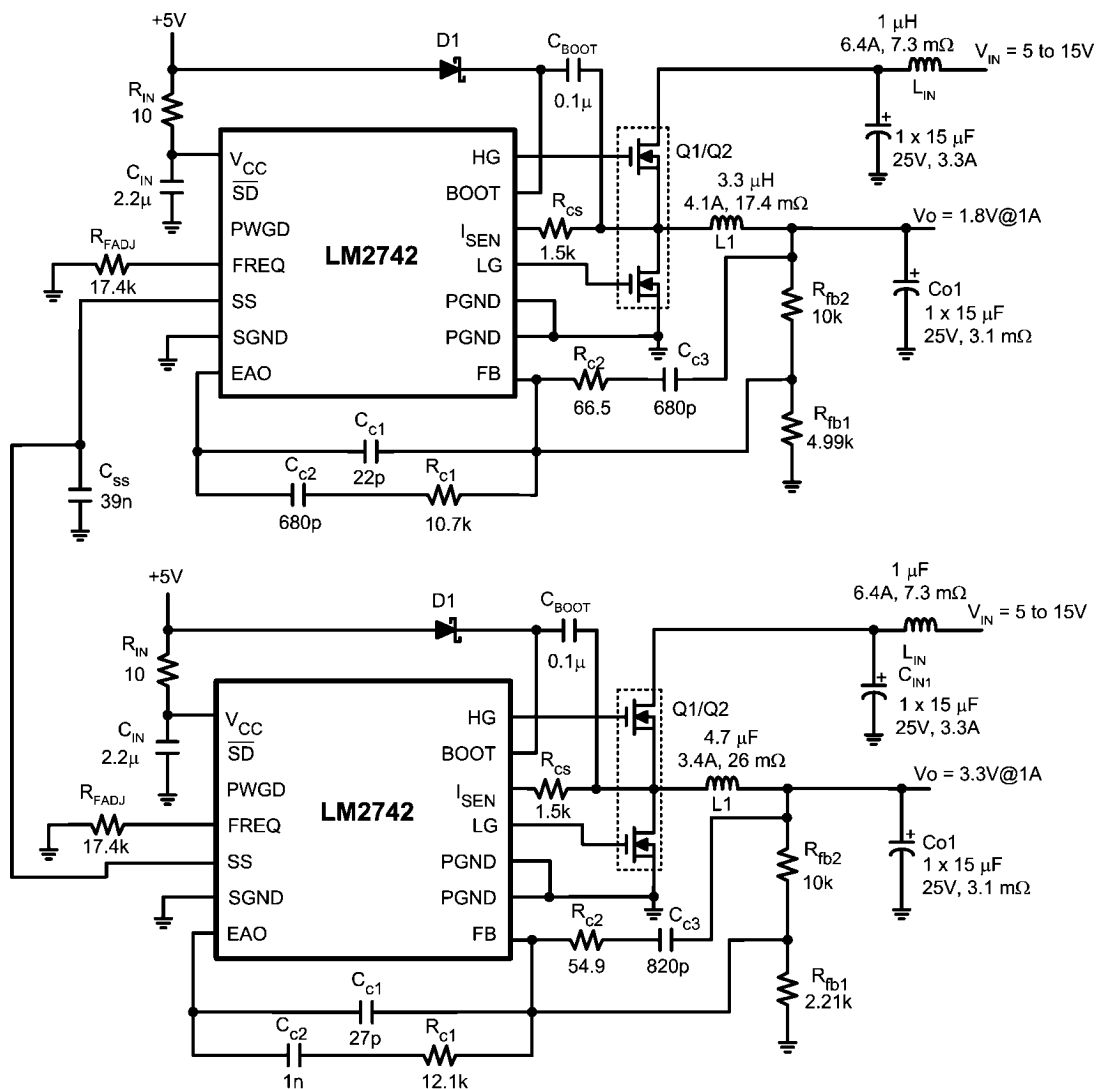


20087506

FIGURE 6. 3.3V to 0.8V, 5A, 500kHz

The circuit of *Figure 6* demonstrates the LM2742 delivering a low output voltage at high efficiency (87%). A separate 5V

supply is required to run the chip, however the input voltage can be as low as 2.2

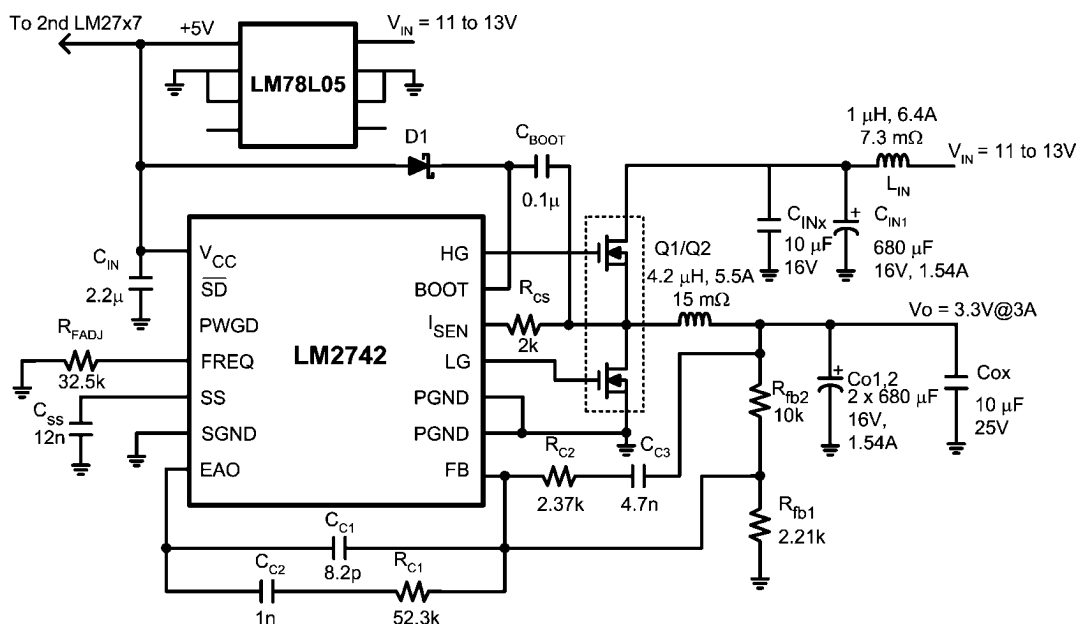


20087507

FIGURE 7. 1.8V and 3.3V, 1A, 1.4MHz, Simultaneous

The circuits in Figure 7 are intended for ADSL applications, where the high switching frequency keeps noise out of the data transmission range. In this design, the 1.8 and 3.3V outputs come up simultaneously by using the same softstart capacitor. Because two current sources now charge the same capacitor, the capacitance must be doubled to achieve the

same softstart time. (Here, 40nF is used to achieve a 5ms softstart time.) A common softstart capacitor means that, should one circuit enter current limit, the other circuit will also enter current limit. The additional compensation components R_{c2} and C_{c3} are needed for the low ESR, all ceramic output capacitors, and the wide (3x) range of V_{IN} .

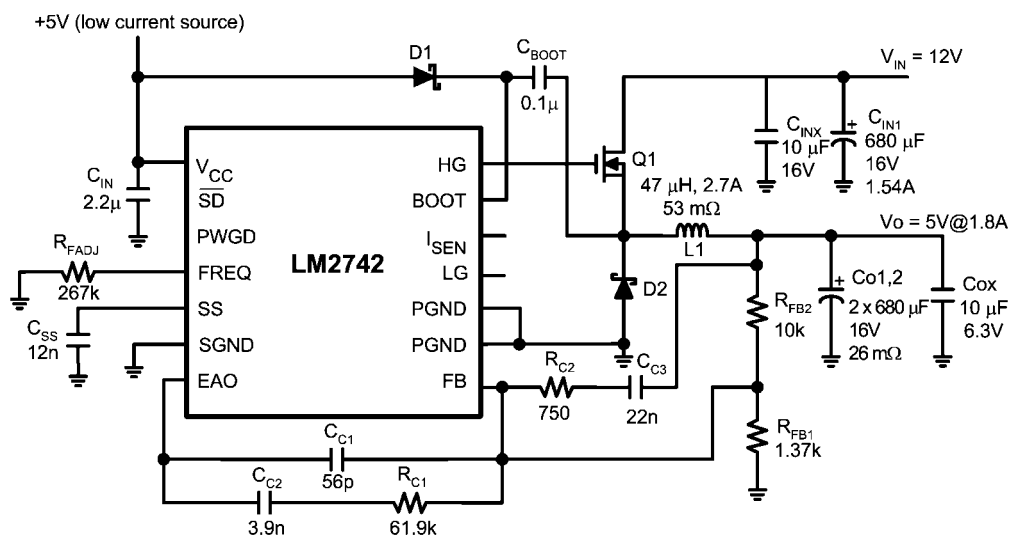


20087508

FIGURE 8. 12V Unregulated to 3.3V, 3A, 750kHz

This circuit shows the LM2742 paired with a cost effective solution to provide the 5V chip power supply, using no extra components other than the LM78L05 regulator itself. The input voltage comes from a 'brick' power supply which does not

regulate the 12V line tightly. Additional, inexpensive 10uF ceramic capacitors (C_{inx} and C_{ox}) help isolate devices with sensitive databands, such as DSL and cable modems, from switching noise and harmonics.



20087509

FIGURE 9. 12V to 5V, 1.8A, 100kHz

In situations where low cost is very important, the LM2742 can also be used as an asynchronous controller, as shown in the above circuit. Although a schottky diode in place of the bottom FET will not be as efficient, it will cost much less than the FET. The 5V at low current needed to run the LM2742 could

come from a zener diode or inexpensive regulator, such as the one shown in Figure 8. Because the LM2742 senses current in the low side MOSFET, the current limit feature will not function in an asynchronous design. The ISEN pin should be left open in this case.

TABLE 1. Bill of Materials for Typical Application Circuit

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2742	Synchronous Controller	TSSOP-14	TSSOP-14	1	NSC
Q1, Q2	Si4884DY	N-MOSFET	SO-8	30V, 13mΩ, 15nC	1	Vishay
L1	RLF7030T-1R5N6R1	Inductor	7.1x7.1x3.2mm	1.5μH, 6.1A 9.6mΩ	1	TDK
Cin1, Cin2	C2012X5R1J106M	MLCC	0805	10μF 6.3V	2	TDK
Cinx	C3216X7R1E105K	Capacitor	1206	1μF, 25V	1	TDK
Co1, Co2	6MV2200WG	AL-E	10mm D 20mm H	2200μF 6.3V125mΩ	2	Sanyo
Cboot	VJ1206X104XXA	Capacitor	1206	0.1μF, 25V	1	Vishay
Cin	C3216X7R1E225K	Capacitor	1206	2.2μF, 25V	1	TDK
Css	VJ1206X123KXX	Capacitor	1206	12nF, 25V	1	Vishay
Cc1	VJ1206A2R2KXX	Capacitor	1206	2.2pF 10%	1	Vishay
Cc2	VJ1206A181KXX	Capacitor	1206	180pF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10Ω 5%	1	Vishay
Rfadj	CRCW12066342F	Resistor	1206	63.4kΩ 1%	1	Vishay
Rc1	CRCW12063923F	Resistor	1206	392kΩ 1%	1	Vishay
Rfb1	CRCW12061002F	Resistor	1206	10kΩ 1%	1	Vishay
Rfb2	CRCW12061002F	Resistor	1206	10kΩ 1%	1	Vishay
Rcs	CRCW1206222J	Resistor	1206	2.2kΩ 5%	1	Vishay

TABLE 2. Bill of Materials for Circuit of Figure 3
(Identical to BOM for 1.5V except as noted below)

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
L1	RLF12560T-2R7N110	Inductor	12.5x12.8x6mm	2.7μH, 14.4A 4.5mΩ	1	TDK
Co1, Co2, Co3, Co4	10TPB100M	POSCAP	7.3x4.3x2.8mm	100μF 10V 1.9Arms	4	Sanyo
Cc1	VJ1206A6R8KXX	Capacitor	1206	6.8pF 10%	1	Vishay
Cc2	VJ1206A271KXX	Capacitor	1206	270pF 10%	1	Vishay
Cc3	VJ1206A471KXX	Capacitor	1206	470pF 10%	1	Vishay
Rc2	CRCW12068451F	Resistor	1206	8.45kΩ 1%	1	Vishay
Rfb1	CRCW12061102F	Resistor	1206	11kΩ 1%	1	Vishay

TABLE 3. Bill of Materials for Circuit of Figure 4

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2742	Synchronous Controller	TSSOP-14		1	NSC
Q1	Si4442DY	N-MOSFET	SO-8	30V, 4.1mΩ, @ 4.5V, 36nC	1	Vishay
Q2	Si4442DY	N-MOSFET	SO-8	30V, 4.1mΩ, @ 4.5V, 36nC	1	Vishay
D1	BAT-54	Schottky Diode	SOT-23	30V	1	Vishay
Lin	SLF12575T-1R2N8R2	Inductor	12.5x12.5x7.5mm	12μH, 8.2A, 6.9mΩ	1	Coilcraft
L1	D05022-152HC	Inductor	22.35x16.26x8mm	1.5μH, 15A, 4mΩ	1	Coilcraft
Cin1, Cin2	10MV5600AX	Aluminum Electrolytic	16mm D 25mm H	5600μF10V 2.35Arms	2	Sanyo
Cinx	C3216X7R1E105K	Capacitor	1206	1μF, 25V	1	TDK
Co1, Co2, Co3	10MV5600AX	Aluminum Electrolytic	16mm D 25mm H	5600μF10V 2.35Arms	2	Sanyo
Cboot	VJ1206X104XXA	Capacitor	1206	0.1μF, 25V	1	Vishay
Cin	C3216X7R1E225K	Capacitor	1206	2.2μF, 25V	1	TDK
Css	VJ1206X123KXX	Capacitor	1206	12nF, 25V	1	Vishay

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
Cc1	VJ1206A4R7KXX	Capacitor	1206	4.7pF 10%	1	Vishay
Cc2	VJ1206A102KXX	Capacitor	1206	1nF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10 Ω 5%	1	Vishay
Rfadj	CRCW12068872F	Resistor	1206	88.7k Ω 1%	1	Vishay
Rc1	CRCW12062293F	Resistor	1206	229k Ω 1%	1	Vishay
Rfb1	CRCW12064991F	Resistor	1206	4.99k Ω 1%	1	Vishay
Rfb2	CRCW12064991F	Resistor	1206	4.99k Ω 1%	1	Vishay
Rcs	CRCW1206152J	Resistor	1206	1.5k Ω 5%	1	Vishay

TABLE 4. Bill of Materials for Circuit of Figure 5

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2742	Synchronous Controller	TSSOP-14		1	NSC
Q1/Q2	Si4826DY	Asymetric Dual N-MOSFET	SO-8	30V, 24m Ω / 8nC Top 16.5m Ω / 15nC	1	Vishay
L1	DO3316P-222	Inductor	12.95x9.4x 5.21mm	2.2 μ H, 6.1A, 12m Ω	1	Coilcraft
Cin1	10TPB100ML	POSCAP	7.3x4.3x3.1mm	100 μ F 10V 1.9Arms	1	Sanyo
Co1	4TPB220ML	POSCAP	7.3x4.3x3.1mm	220 μ F 4V 1.9Arms	1	Sanyo
Cc	C3216X7R1E105K	Capacitor	1206	1 μ F, 25V	1	TDK
Cin	C3216X7R1E225K	Capacitor	1206	2.2 μ F, 25V	1	TDK
Css	VJ1206X123KXX	Capacitor	1206	12nF, 25V	1	Vishay
Cc1	VJ1206A100KXX	Capacitor	1206	10pF 10%	1	Vishay
Cc2	VJ1206A561KXX	Capacitor	1206	560pF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10 Ω 5%	1	Vishay
Rfadj	CRCW12064222F	Resistor	1206	42.2k Ω 1%	1	Vishay
Rc1	CRCW12065112F	Resistor	1206	51.1k Ω 1%	1	Vishay
Rfb1	CRCW12062491F	Resistor	1206	2.49k Ω 1%	1	Vishay
Rfb2	CRCW12064991F	Resistor	1206	4.99k Ω 1%	1	Vishay
Rcs	CRCW1206272J	Resistor	1206	2.7k Ω 5%	1	Vishay

TABLE 5. Bill of Materials for Circuit of Figure 6

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2742	Synchronous Controller	TSSOP-14		1	NSC
Q1	Si4884DY	N-MOSFET	SO-8	30V, 13.5m Ω , @ 4.5V 15.3nC	1	Vishay
Q2	Si4884DY	N-MOSFET	SO-8	30V, 13.5m Ω , @ 4.5V 15.3nC	1	Vishay
D1	BAT-54	Schottky Diode	SOT-23	30V	1	Vishay
Lin	P1166.102T	Inductor	7.29x7.29 3.51mm	1 μ H, 11A 3.7m Ω	1	Pulse
L1	P1168.102T	Inductor	12x12x4.5 mm	1 μ H, 11A, 3.7m Ω	1	Pulse
Cin1	10MV5600AX	Aluminum Electrolytic	16mm D 25mm H	5600 μ F 10V 2.35Arms	1	Sanyo
Cinx	C3216X7R1E105K	Capacitor	1206	1 μ F, 25V	1	TDK
Co1, Co2, Co3	16MV4700WX	Aluminum Electrolytic	12.5mm D 30mm H	4700 μ F 16V 2.8Arms	2	Sanyo
Cboot	VJ1206X104XXA	Capacitor	1206	0.1 μ F, 25V	1	Vishay
Cin	C3216X7R1E225K	Capacitor	1206	2.2 μ F, 25V	1	TDK
Css	VJ1206X123KXX	Capacitor	1206	12nF, 25V	1	Vishay

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
Cc1	VJ1206A4R7KXX	Capacitor	1206	4.7pF 10%	1	Vishay
Cc2	VJ1206A681KXX	Capacitor	1206	680pF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10 Ω 5%	1	Vishay
Rfadj	CRCW12064992F	Resistor	1206	49.9k Ω 1%	1	Vishay
Rc1	CRCW12061473F	Resistor	1206	147k Ω 1%	1	Vishay
Rfb1	CRCW12061492F	Resistor	1206	14.9k Ω 1%	1	Vishay
Rfb2	CRCW12064991F	Resistor	1206	4.99k Ω 1%	1	Vishay
Rcs	CRCW1206332J	Resistor	1206	3.3k Ω 5%	1	Vishay

TABLE 6. Bill of Materials for Circuit of Figure 7

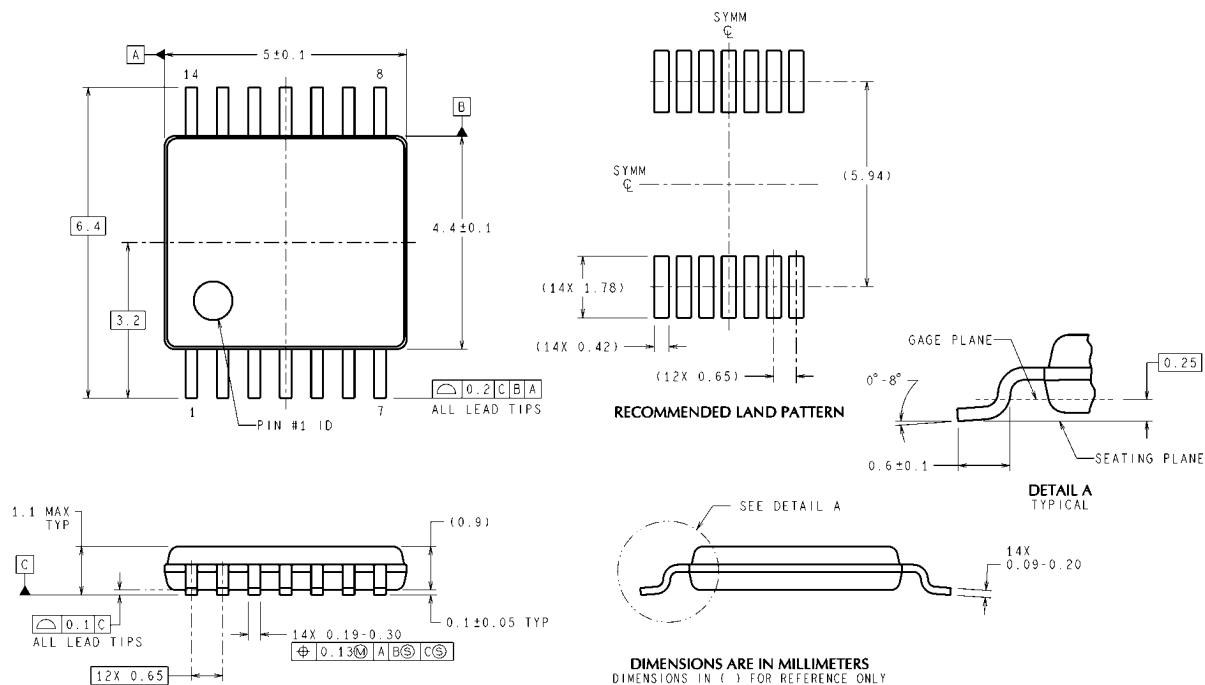
ID	Part Number	Type	Size	Parameters	Qty.	Vendor
U1	LM2742	Synchronous Controller	TSSOP-14		1	NSC
Q1/Q2	Si4826DY	Assymetric Dual N-MOSFET	SO-8	30V, 24m Ω / 8nC Top 16.5m Ω / 15nC	1	Vishay
D1	BAT-54	Schottky Diode	SOT-23	30V	1	Vishay
Lin	RLF7030T-1R0N64	Inductor	6.8x7.1x3.2mm	1 μ H, 6.4A, 7.3m Ω	1	TDK
L1	RLF7030T-3R3M4R1	Inductor	6.8x7.1x3.2mm	3.3 μ H, 4.1A, 17.4m Ω	1	TDK
Cin1	C4532X5R1E156M	MLCC	1812	15 μ F 25V 3.3Arms	1	Sanyo
Co1	C4532X5R1E156M	MLCC	1812	15 μ F 25V 3.3Arms	1	Sanyo
Cboot	VJ1206X104XXA	Capacitor	1206	0.1 μ F, 25V	1	TDK
Cin	C3216X7R1E225K	Capacitor	1206	2.2 μ F, 25V	1	TDK
Css	VJ1206X393KXX	Capacitor	1206	39nF, 25V	1	Vishay
Cc1	VJ1206A220KXX	Capacitor	1206	22pF 10%	1	Vishay
Cc2	VJ1206A681KXX	Capacitor	1206	680pF 10%	1	Vishay
Cc3	VJ1206A681KXX	Capacitor	1206	680pF 10%	1	Vishay
Rin	CRCW1206100J	Resistor	1206	10 Ω 5%	1	Vishay
Rfadj	CRCW12061742F	Resistor	1206	17.4k Ω 1%	1	Vishay
Rc1	CRCW12061072F	Resistor	1206	10.7k Ω 1%	1	Vishay
Rc2	CRCW120666R5F	Resistor	1206	66.5 Ω 1%	1	Vishay
Rfb1	CRCW12064991F	Resistor	1206	4.99k Ω 1%	1	Vishay
Rfb2	CRCW12061002F	Resistor	1206	10k Ω 1%	1	Vishay
Rcs	CRCW1206152J	Resistor	1206	1.5k Ω 5%	1	Vishay

TABLE 7. Bill of Materials for 3.3V Circuit of Figure 7
(Identical to BOM for 1.8V except as noted below)

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
L1	RLF7030T-4R7M3R4	Inductor	6.8x7.1x 3.2mm	4.7 μ H, 3.4A, 26m Ω	1	TDK
Cc1	VJ1206A270KXX	Capacitor	1206	27pF 10%	1	Vishay
Cc2	VJ1206X102KXX	Capacitor	1206	1nF 10%	1	Vishay
Cc3	VJ1206A821KXX	Capacitor	1206	820pF 10%	1	Vishay
Rc1	CRCW12061212F	Resistor	1206	12.1k Ω 1%	1	Vishay
Rc2	CRCW12054R9F	Resistor	1206	54.9 Ω 1%	1	Vishay
Rfb1	CRCW12062211F	Resistor	1206	2.21k Ω 1%	1	Vishay
Rfb2	CRCW12061002F	Resistor	1206	10k Ω 1%	1	Vishay

TABLE 8. Bill of Materials for Circuit of *Figure 8*

ID	Part Number	Type	Size	Parameters	Qty.	Vendor
Rfb2	CRCW12061002F	Resistor	1206	10k Ω 1%	1	Vishay
Rcs	CRCW1206122F	Resistor	1206	1.2k Ω 5%	1	Vishay

Physical Dimensions inches (millimeters) unless otherwise noted

TSSOP-14 Pin Package
NS Package Number MTC14

MTC14 (Rev D)

Notes

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