May 2001

National Semiconductor

DS90LV048A
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV048A is a quad CMOS flow-through differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV048A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV048A has a flow-through pinout for easy PCB layout.

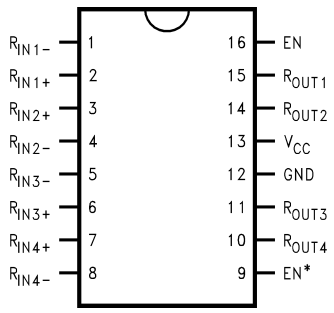
The EN and EN* inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four receivers. The DS90LV048A and companion LVDS line driver (eg. DS90LV047A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 150 ps channel-to-channel skew (typical)
- 100 ps differential skew (typical)
- 2.7 ns maximum propagation delay
- 3.3V power supply design
- High impedance LVDS inputs on power down
- Low Power design (40mW 3.3V static)
- Interoperable with existing 5V LVDS drivers
- Accepts small swing (350 mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- 0V to −100mV threshold region
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (-40˚C to +85˚C)
- Available in SOIC and TSSOP package

Connection Diagram

Dual-in-Line



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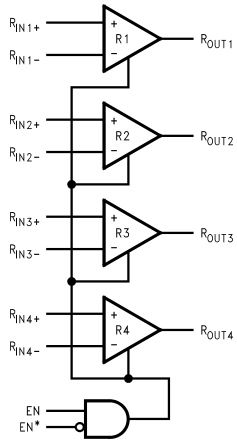
Order Number DS90LV048ATM, DS90LV048ATMTC
See NS Package Number M16A, MTC16

Functional Diagram



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Truth Table

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
H	L or Open	$V_{ID} \geq 0V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H
All other combinations of ENABLE inputs		X	Z

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (R_{IN+}, R_{IN-})	−0.3V to 3.9V
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation +25˚C	
M Package	1025 mW
MTC Package	866 mW
Derate M Package	8.2 mW/˚C above +25˚C
Derate MTC Package	6.9 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating (Note 10)	
(HBM, 1.5 kΩ, 100 pF)	≥ 10 kV
(EIAJ, 0 Ω, 200 pF)	≥ 1200 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	V
Operating Free Air Temperature (T_A)	−40	25	+85	˚C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V, 0.05V, 2.95V (Note 13)		R_{IN+}, R_{IN-}		−35	0	mV
V_{TL}	Differential Input Low Threshold				−100	−35		mV
VCMR	Common-Mode Voltage Range	VID = 200mV pk to pk (Note 5)			0.1		2.3	V
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6V or 0V		−10	±5	+10	µA
		V_{IN} = 0V			−10	±1	+10	µA
		V_{IN} = +3.6V	V_{CC} = 0V		-20	±1	+20	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.3		V
		I_{OH} = −0.4 mA, Input terminated			2.7	3.3		V
		I_{OH} = −0.4 mA, Input shorted			2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.05	0.25	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V (Note 11)			−15	−47	−100	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	µA
V_{IH}	Input High Voltage			EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_I	Input Current	V_{IN} = 0V or V_{CC}, Other Input = V_{CC} or GND			−10	±5	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current Receivers Enabled	EN = V_{CC}, Inputs Open		V_{CC}		9	15	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, Inputs Open				1	5	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 3, 4, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF	1.2	2.0	2.7	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.2	1.9	2.7	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 6)	(*Figure 1* and *Figure 2*)	0	0.1	0.4	ns
t_{SKD2}	Differential Channel-to-Channel Skew; same device (Note 7)		0	0.15	0.5	ns
t_{SKD3}	Differential Part to Part Skew (Note 8)				1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 9)				1.5	ns
t_{TLH}	Rise Time			0.5	1.0	ns
t_{THL}	Fall Time			0.35	1.0	ns

Switching Characteristics (Continued)
Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 3, 4, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHZ}	Disable Time High to Z	R_L = 2 kΩ		8	14	ns
t_{PLZ}	Disable Time Low to Z	C_L = 15 pF		8	14	ns
t_{PZH}	Enable Time Z to High	(*Figure 3* and *Figure 4*)		9	14	ns
t_{PZL}	Enable Time Z to Low			9	14	ns
f_{MAX}	Maximum Operating Frequency (Note 14)	All Channels Switching	200	250		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +3.3V, T_A = +25˚C.

Note 4: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.

Note 5: The VCMR range is reduced for larger VID. Example: if VID = 400mV, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0V to 2.4V, but is supported only with inputs shorted and no external common-mode voltage applied. A VID up to V_{CC}− 0V may be applied to the R_{IN+}/ R_{IN-} inputs with the Common-Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when VID is increased from 200mV to 400mV. Skew specifications apply for 200mV ≤ VID ≤ 800mV over the common-mode range .

Note 6: t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel

Note 7: t_{SKD2}, Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

Note 8: t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5˚C of each other within the operating temperature range.

Note 9: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max−Min| differential propagation delay.

Note 10: ESD Rating:HBM (1.5 kΩ, 100 pF) ≥ 10kV

EIAJ (0Ω, 200 pF) ≥ 1200V

Note 11: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 12: C_L includes probe and jig capacitance.

Note 13: V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range −0.2V to V_{CC}− VID/2. However, to be compliant with AC specifications, the common voltage range is 0.1V to 2.3V

Note 14: f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output criteria: 60/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), Load = 15 pF (stray plus probes).

Parameter Measurement Information

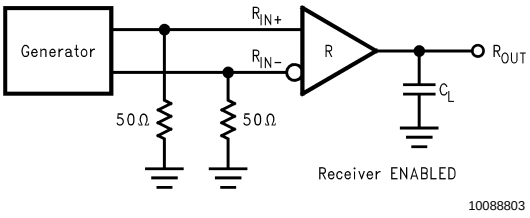


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

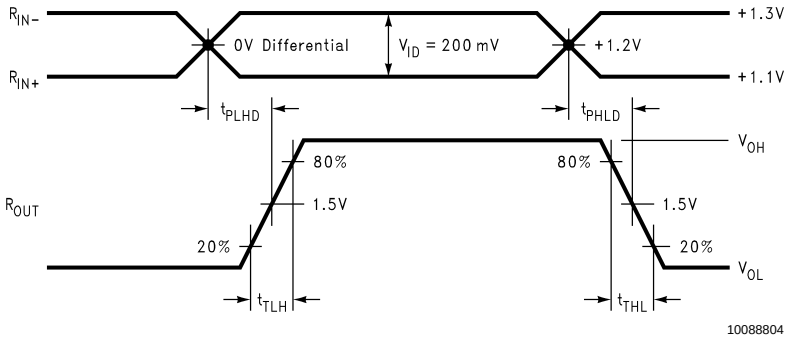
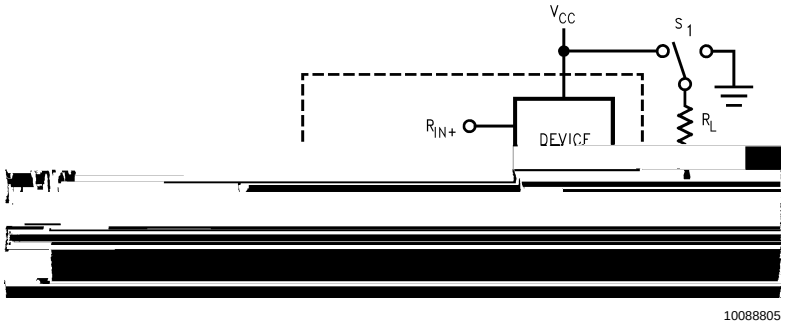


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL} and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

FIGURE 3. Receiver TRI-STATE Delay Test Circuit

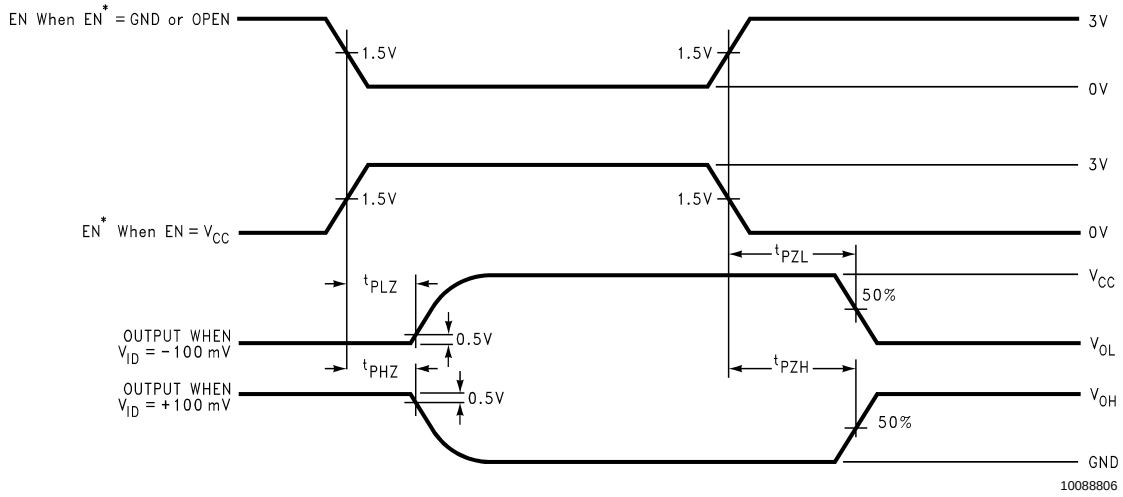


FIGURE 4. Receiver TRI-STATE Delay Waveforms

Typical Application

Balanced System

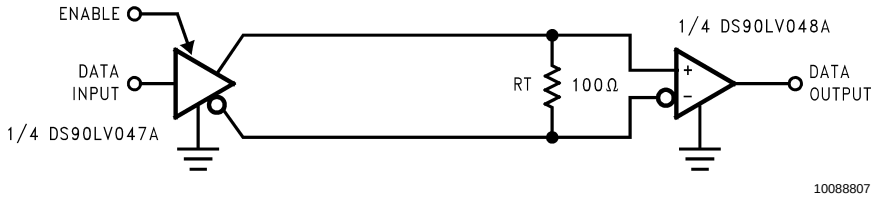


FIGURE 5. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-002), AN-808, AN-977, AN-971, AN-916, AN-805, AN-903. The latest applications material is available on the web at: www.national.com/lvds.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 5.* This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω (selected to match the media), and is located as close to the receiver input pins as possible. The

Applications Information (Continued)

termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV048A differential line receiver is capable of detecting signals as low as 100mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{CC}, but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

The DS90LV048A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1µF and 0.001µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC Board considerations:

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s)

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces:

Use controlled impedance traces which match the differen-

Applications Information (Continued)

gin (+25mV − (−35mV)). With the enhanced threshold region of −100mV to 0V, this small external fail-safe biasing of +25mV (with respect to 0V) gives a DNM of a comfortable 60mV. With the standard threshold region of ±100mV, the external fail-safe biasing would need to be +25mV with respect to +100mV or +125mV, giving a DNM of 160mV which is stronger fail-safe biasing than is necessary for the DS90LV048A. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

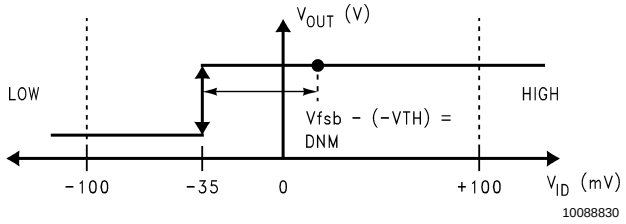


FIGURE 6. VTC of the DS90LV048A LVDS Receiver

Fail-Safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV048A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

Additional information on fail-safe biasing of LVDS devices may be found in AN-1194.

Pin Descriptions

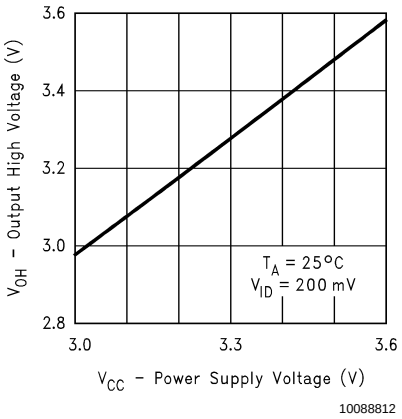
Pin No.	Name	Description
2, 3, 6, 7	R_{IN+}	Non-inverting receiver input pin
1, 4, 5, 8	R_{IN-}	Inverting receiver input pin
10, 11, 14, 15	R_{OUT}	Receiver output pin
16	EN	Receiver enable pin: When EN is low, the receiver is disabled. When EN is high and EN* is low or open, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
9	EN*	Receiver enable pin: When EN* is high, the receiver is disabled. When EN* is low or open and EN is high, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
13	V_{CC}	Power supply pin, +3.3V ± 0.3V
12	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M16A	DS90LV048ATM
−40˚C to +85˚C	TSSOP/MTC16	DS90LV048ATMTC

Typical Performance Curves

Output High Voltage vs Power Supply Voltage



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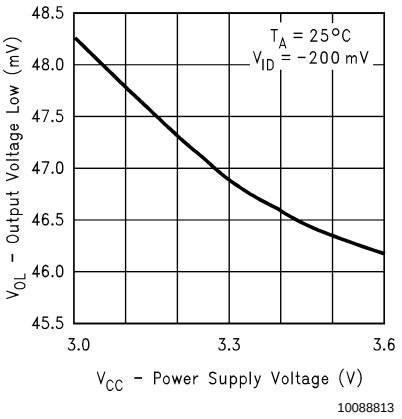
Output Low Voltage vs Power Supply Voltage



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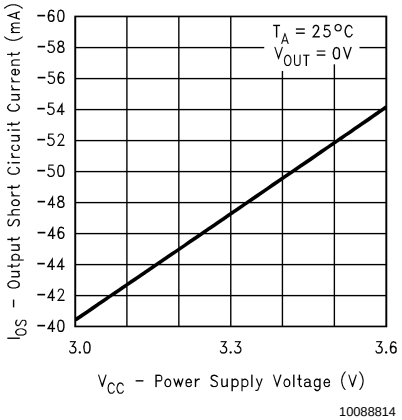
Output Short Circuit Current vs Power Supply Voltage



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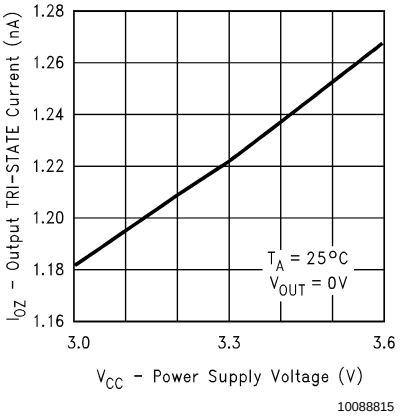
Output TRI-STATE Current vs Power Supply Voltage



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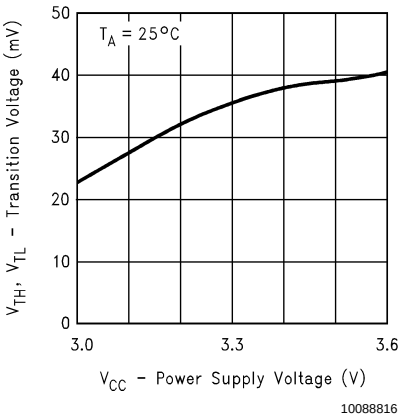
Differential Transition Voltage vs Power Supply Voltage



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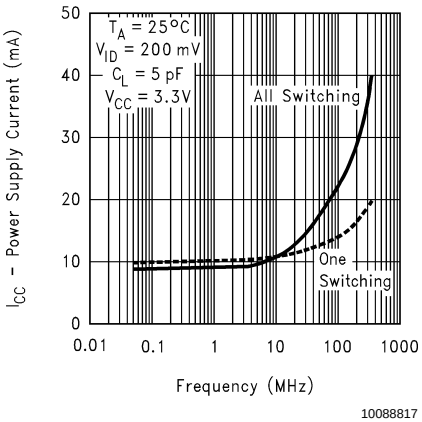
Power Supply Current vs Frequency



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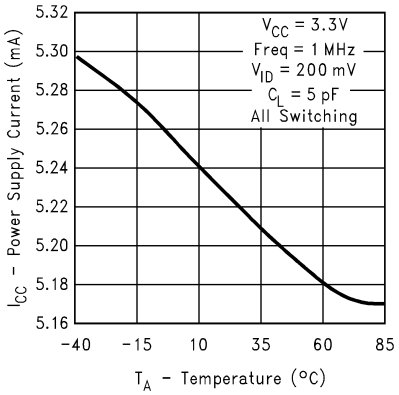
Typical Performance Curves (Continued)

Power Supply Current vs Ambient Temperature



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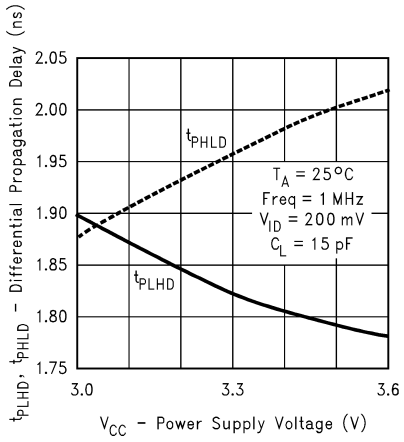
Differential Propagation Delay vs Power Supply Voltage



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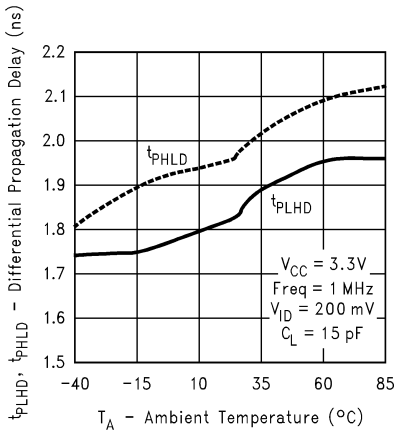
Differential Propagation Delay vs Ambient Temperature



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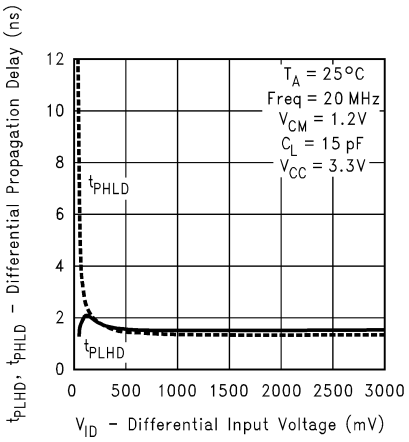
Differential Propagation Delay vs Differential Input Voltage



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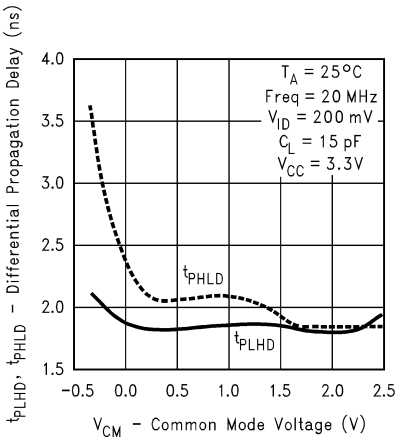
Differential Propagation Delay vs Common-Mode Voltage



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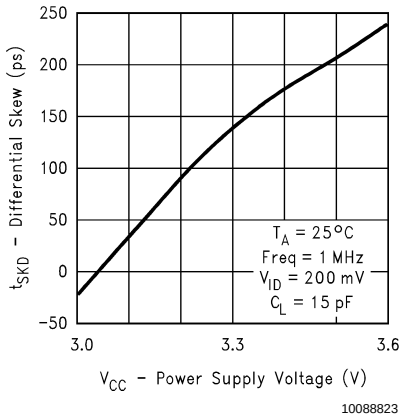
Differential Skew vs Power Supply Voltage



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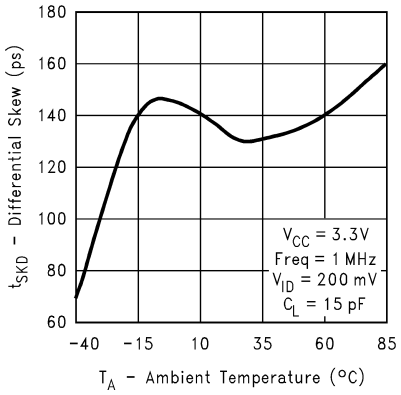
Typical Performance Curves (Continued)

Differential Skew vs Ambient Temperature



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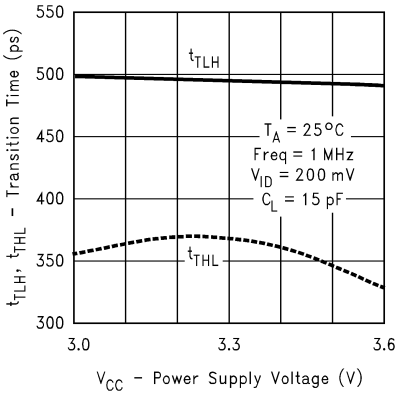
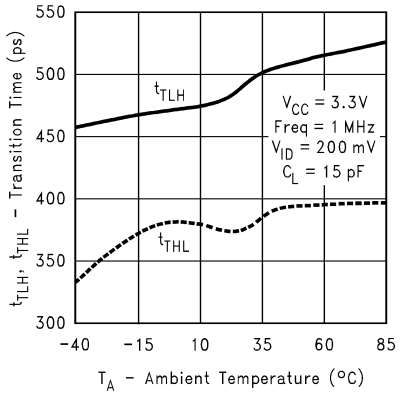
Transition Time vs Power Supply Voltage



10088825

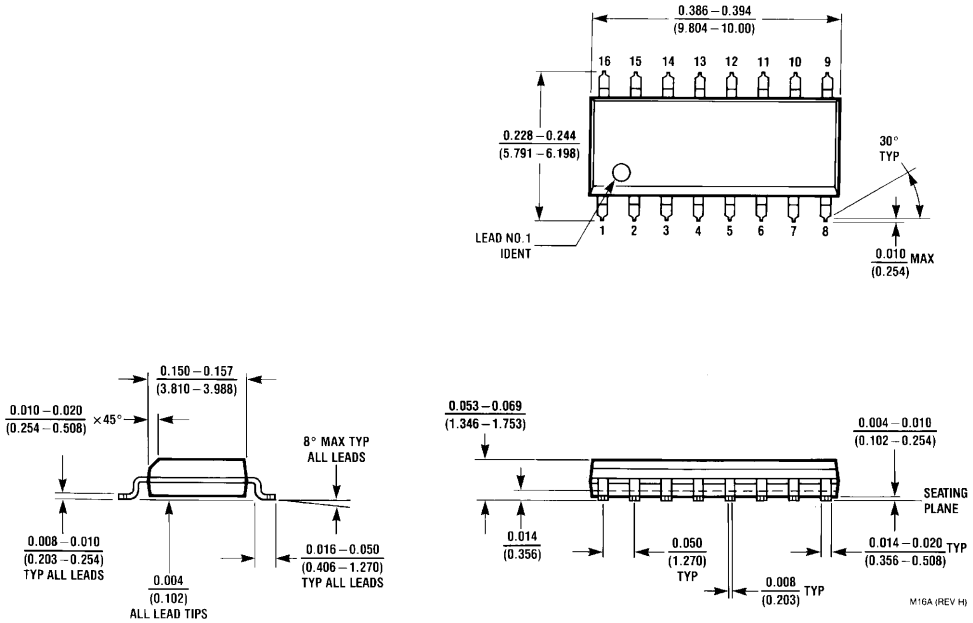
Transition Time vs Ambient Temperature



10088826

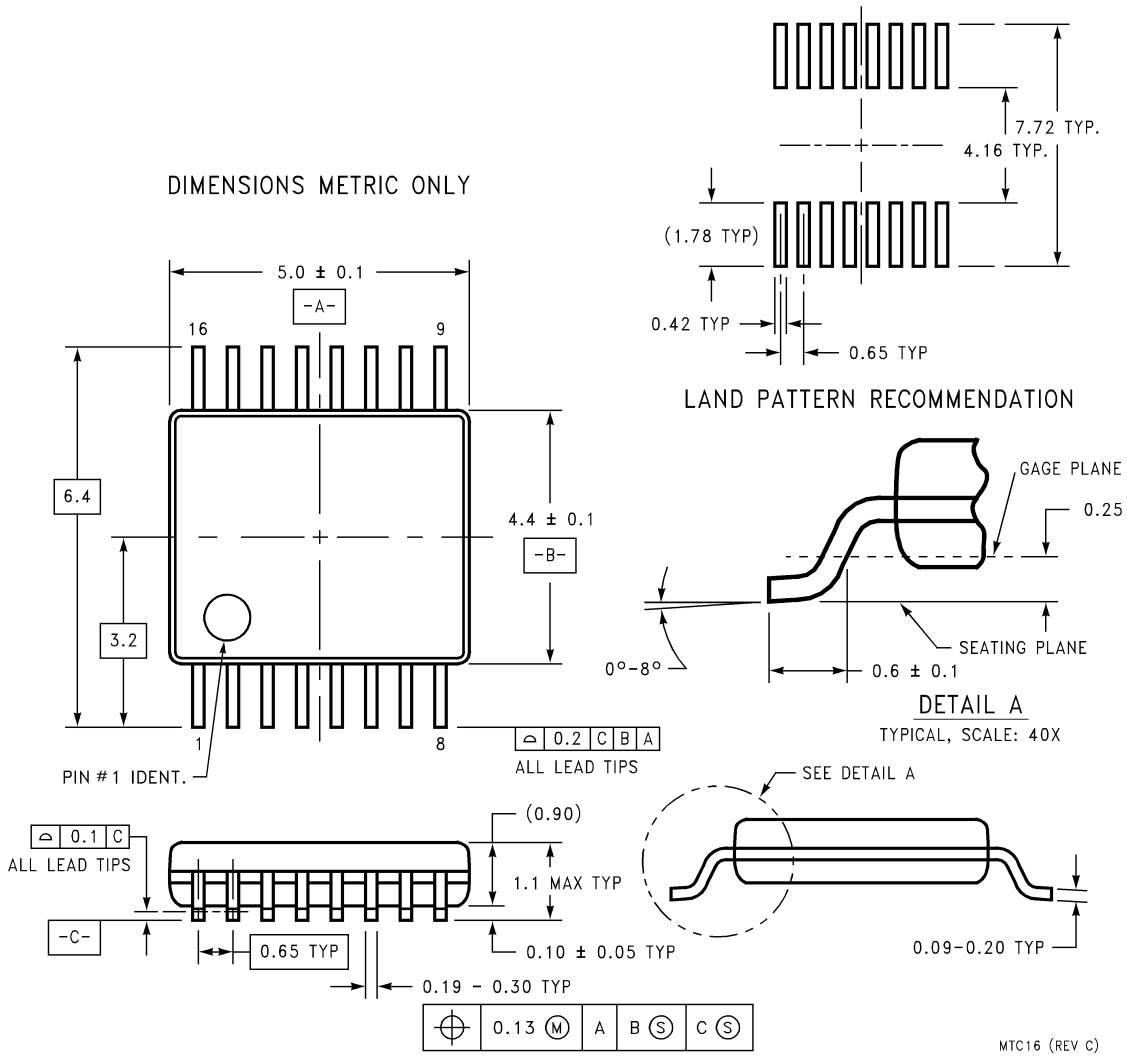
Physical Dimensions inches (millimeters)

unless otherwise noted



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV048ATM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.100" Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV048ATMTC
NS Package Number MTC16

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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