National Semiconductor

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DS90LV032A
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032A is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input Fail-safe. The receiver output will be HIGH for all fail-safe conditions.

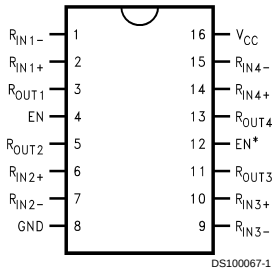
The DS90LV032A and companion LVDS line driver (eg. DS90LV031A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns channel-to-channel skew (typical)
- 0.1 ns differential skew (typical)
- 3.3 ns maximum propagation delay
- 3.3V power supply design
- Power down high impedance on LVDS inputs
- Low Power design (40mW 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) VID
- Supports open, short and terminated input fail-safe
- Compatible with ANSI/TIA/EIA-644
- Industrial temp. operating range (-40˚C to +85˚C)
- Available in SOIC and TSSOP Packaging

Connection Diagram

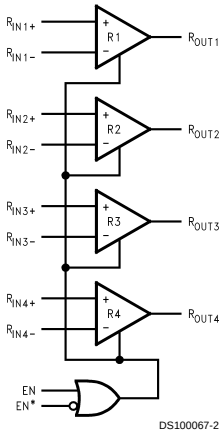
Dual-in-Line



DS100067-1

Order Number DS90LV032ATM
or DS90LV032ATMTC
See NS Package Number M16A or MTC16

Functional Diagram



DS100067-2

ENABLES		INPUTS	OUTPUT
EN	**EN***	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (R_{IN+}, R_{IN-})	−0.3V to +3.9V
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation +25˚C	
M Package	1025 mW
MTC Package	866 mW
Derate M Package	8.2 mW/˚C above +25˚C
Derate MTC Package	6.9 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
(Soldering 4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating (Note 10)	
(HBM 1.5 kΩ, 100 pF)	≥ 4.5 kV
(EIAJ 0 Ω, 200 pF)	≥ 250 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	V
Operating Free Air Temperature (T_A)	−40	25	+85	˚C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V (Note 13)		R_{IN+}, R_{IN-}		+20	+100	mV
V_{TL}	Differential Input Low Threshold				−100	−20		mV
VCMR	Common-Mode Voltage Range	VID = 200 mV peak to peak (Note 5)			0.1		2.3	V
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6V or 0V		−10	±1	+10	µA
		V_{IN} = 0V			−10	±1	+10	µA
		V_{IN} = +3.6V	V_{CC} = 0V		-20		+20	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.0		V
		I_{OH} = −0.4 mA, Input terminated			2.7	3.0		V
		I_{OH} = −0.4 mA, Input shorted			2.7	3.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.1	0.25	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V (Note 11)			−15	−48	−120	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	µA
V_{IH}	Input High Voltage			EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_I	Input Current	V_{IN} = 0V or V_{CC}, Other Input = V_{CC} or GND			−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current Receivers Enabled	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		10	15	mA
		EN, EN* = 2.4V or 0.5V, Inputs Open				10	15	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, EN* = V_{CC}, Inputs Open				3	5	mA

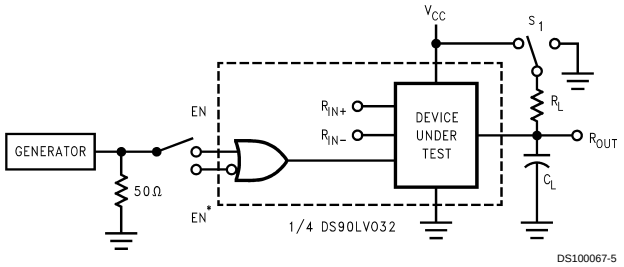
Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 3, 4, 7, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 10 pF	1.8		3.3	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.8		3.3	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 6)	(*Figure 1* and *Figure 2*)	0	0.1	0.35	ns
t_{SKD2}	Differential Channel-to-Channel Skew-same device (Note 7)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (Note 8)				1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 9)				1.5	ns
t_{TLH}	Rise Time			0.35	1.2	ns
t_{THL}	Fall Time			0.35	1.2	ns

Switching Characteristics (Continued)

Parameter Measurement Information (Continued)



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

FIGURE 3. Receiver TRI-STATE Delay Test Circuit

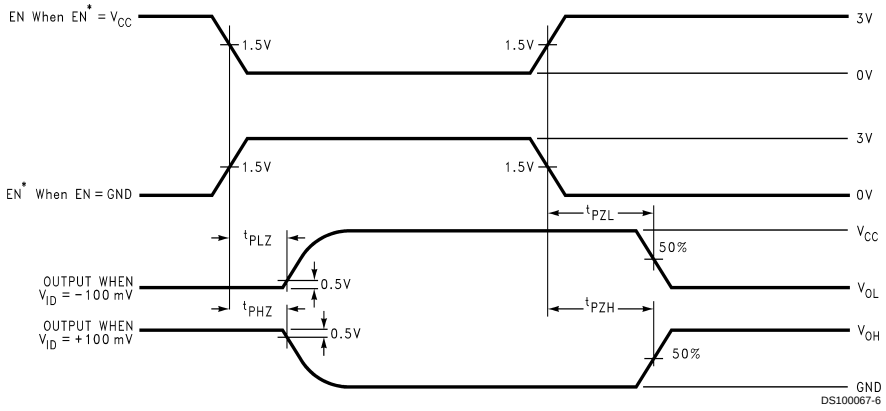


FIGURE 4. Receiver TRI-STATE Delay Waveforms

Typical Application

Balanced System

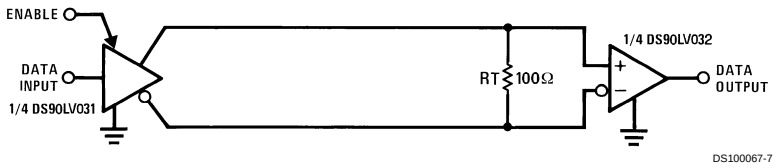


FIGURE 5. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-001), AN808, AN1035, AN977, AN971, AN916, AN805, AN903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 5.* This configuration provides a clean signaling environment for the fast edge rates of the drivers . The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

Applications Information (Continued)

The DS90LV032A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins have a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations:

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and

Applications Information (Continued)

3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

The footprint of the DS90LV032A is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

Pin Descriptions

Pin No.	Name	Description
2, 6, 10, 14	R_{IN+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{IN-}	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M16A	DS90LV032ATM
−40˚C to +85˚C	TSSOP/MTC16	DS90LV032ATMTC

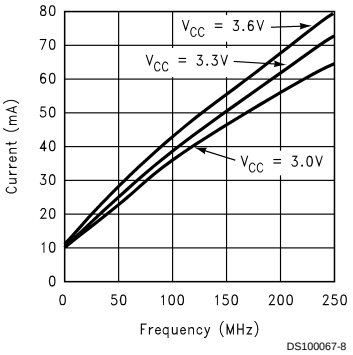


FIGURE 6. ICC vs Frequency, four channels switching

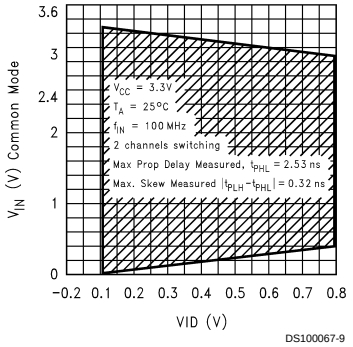


FIGURE 7. Typical Common-Mode Range variation with respect to amplitude of differential input

Applications Information (Continued)

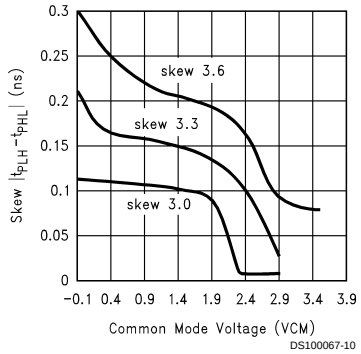


FIGURE 8. Typical Pulse Skew variation versus common-mode voltage

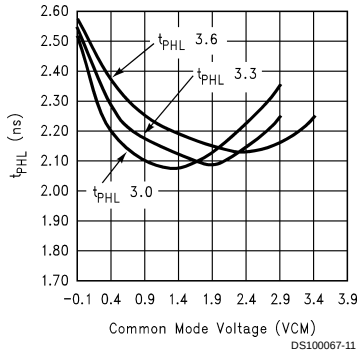


FIGURE 9. Variation in High to Low Propagation Delay versus VCM

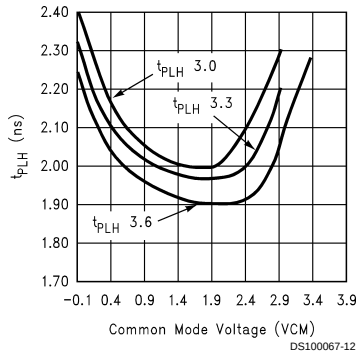
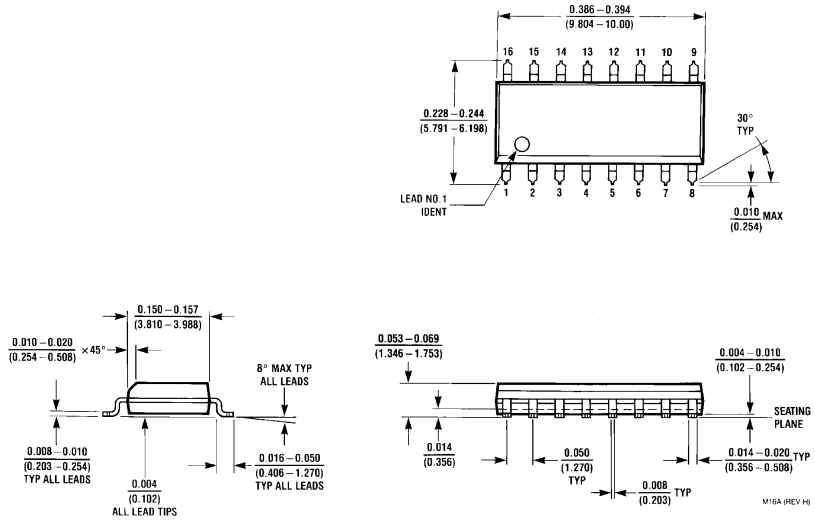


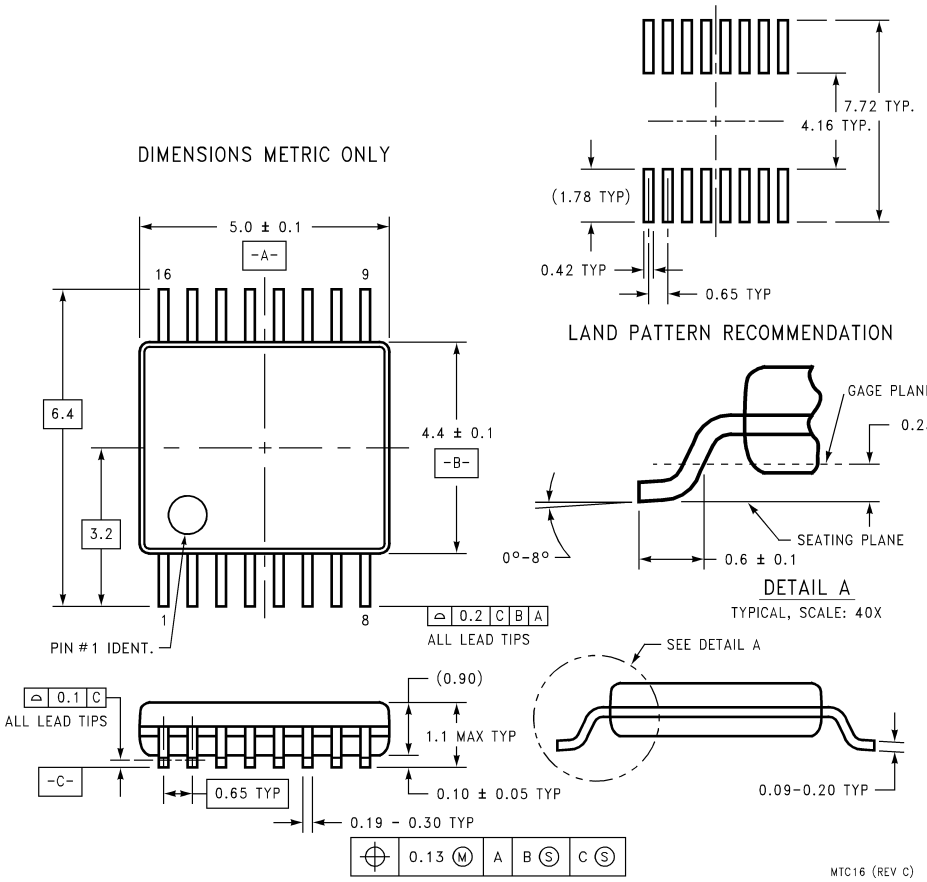
FIGURE 10. Variation in Low to High Propagation Delay versus VCM

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV032ATM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.100" Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV032ATMTC
NS Package Number MTC16

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