

DS25BR440

3.125 Gbps Quad LVDS Buffer with Transmit Pre-Emphasis and Receive Equalization

General Description

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR440 features two levels of transmit pre-emphasis (PE) and two levels of receive equalization (EQ). Both of these features compensate for interconnect losses and ultimately maximize noise margin. A loss-of-signal ($\overline{\text{LOS}}$) circuit monitors each input channel and a unique $\overline{\text{LOS}}$ pin is asserted when no signal is detected at that input

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

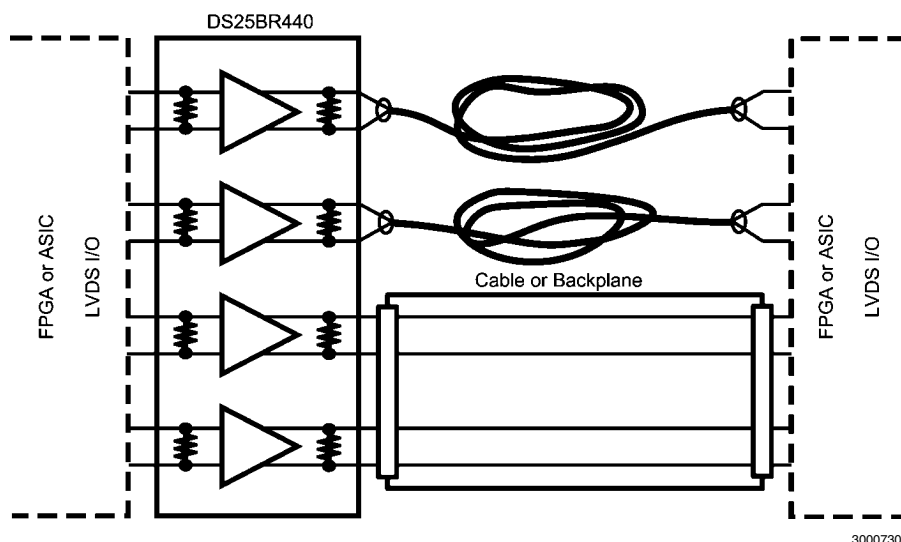
Features

- DC - 3.125 Gbps low jitter, low skew, low power operation
- Pin selectable transmit pre-emphasis and receive equalization eliminate data dependant jitter
- Wide input common mode voltage range allows DC-coupled interface to LVDS, CML and LVPECL drivers
- $\overline{\text{LOS}}$ circuitry detects open inputs fault
- Integrated 100Ω input and output terminations
- 8 kV ESD on LVDS I/O pins protects adjoining components
- Small 6 mm x 6 mm LLP-40 space saving package

Applications

- Clock and data buffering and repeating
- Copper cable driving and equalization
- FR-4 equalization
- OC-48 / STM-16

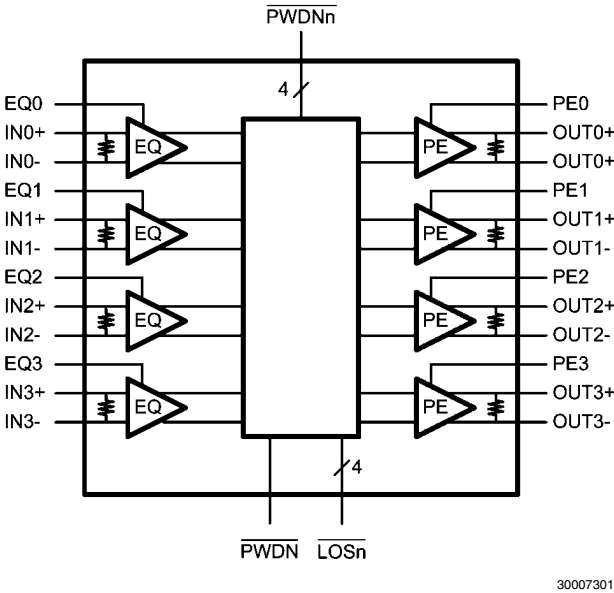
Typical Application



Ordering Code

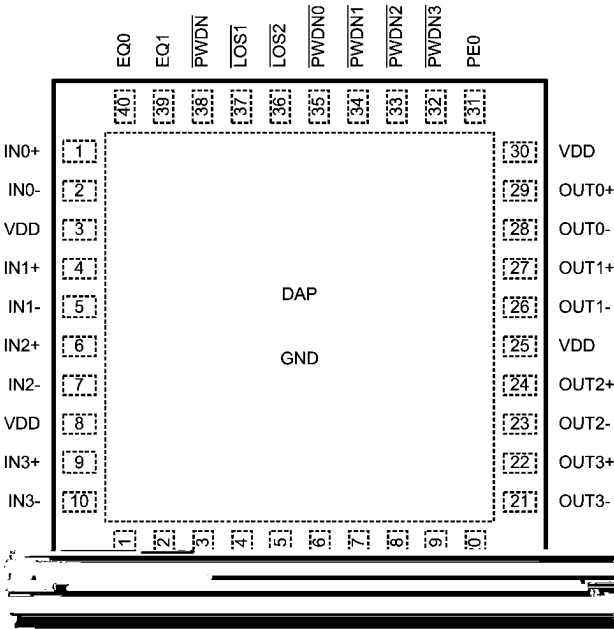
NSID	Function	Available Equalization Levels	Available Pre-Emphasis Levels
DS25BR440TSQ	Quad Buffer / Repeater	Off / On	Off / On

Block Diagram



30007301

Connection Diagram



30007302

DS25BR440 Pin Diagram

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1- , IN2+, IN2- , IN3+, IN3-	1, 2, 4, 5, 6, 7, 9, 10	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0- , OUT1+, OUT1- , OUT2+, OUT2- , OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
EQ0, EQ1, EQ2, EQ3	40, 39, 11, 12	I, LVCMOS	Receive equalization level select pins.
PE0, PE1, PE2, PE3	31, 20, 19, 18	I, LVCMOS	Transmit pre-emphasis level select pins.
PWDN0, PWDN1, PWDN2, PWDN3	35, 34, 33, 32	I, LVCMOS	Channel output power down pins. When the $\overline{\text{PWDNn}}$ is set to L, the channel output OUTn is in the power down mode. The $\overline{\text{LOS}}$ circuitry on the corresponding input remains enabled.
$\overline{\text{LOS0}}$, $\overline{\text{LOS1}}$, $\overline{\text{LOS2}}$, $\overline{\text{LOS3}}$	14, 37, 36, 13	O, LVCMOS	Loss Of Signal output pins, $\overline{\text{LOSn}}$ report when an open input fault condition is detected at the input, INn. These are open drain outputs. External pull up resistors are required.
NC	17	NC	NO CONNECT pins. May be left floating.
$\overline{\text{PWDN}}$	38	I, LVCMOS	Device power down pin. When the $\overline{\text{PWDN}}$ is set to L, the device is in the power down mode. The $\overline{\text{LOS}}$ circuitry is disabled as well.
VDD	3, 8, 15, 25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and a pad (DAP - die attach pad).

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to ($V_{CC} + 0.3V$)
LVCMOS Output Voltage	−0.3V to ($V_{CC} + 0.3V$)
LVDS Input Voltage	−0.3V to +4V
LVDS Differential Input Voltage	0.0V to +1V
LVDS Output Voltage	−0.3V to ($V_{CC} + 0.3V$)
LVDS Differential Output Voltage	0.0V to +1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SQA Package	2.44W
Derate SQA Package	19.49 mW/°C above +25°C

Package Thermal Resistance

θ_{JA}	+26.9°C/W
θ_{JC}	+3.8°C/W

ESD Susceptibility

HBM (Note 1)	≥8 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 3.6V$ $V_{CC} = 3.6V$		0	±10	μA
I_{IL}	Low Level Input Current	$V_{IN} = GND$ $V_{CC} = 3.6V$		0	±10	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}$, $V_{CC} = 0V$		−0.9	−1.5	V
V_{OL}	Low Level Output Voltage	$I_{OL} = 4 \text{ mA}$		0.26	0.4	V
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage	$V_{CM} = +0.05V$ or $V_{CC} - 0.05V$	0		1	V
V_{TH}	Differential Input High Threshold			0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	$V_{ID} = 100 \text{ mV}$	0.05		$V_{CC} - 0.05$	V
I_{IN}	Input Current	$V_{IN} = +3.6V$ or $0V$ $V_{CC} = 3.6V$ or $0V$		±1	±10	μA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current (Note 8)	OUT to GND		-35	-55	mA
		OUT to V_{CC}		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	PE = OFF, EQ = OFF $\overline{PWDN} = H$		162	190	mA
I_{CCZ}	Power Down Supply Current	$\overline{PWDN} = L$		55	63	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .

Note 7: Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics (Notes 9, 10)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
LVDS OUTPUT AC SPECIFICATIONS							
t _{PLHD}	Differential Propagation Delay Low to High (Note 11)	R _L = 100Ω		390	600	ps	
t _{PHLD}	Differential Propagation Delay High to Low (Note 11)			400	600	ps	
t _{SKD1}	Pulse Skew t _{PLHD} – t _{PHLD} (Notes 11, 12)			10	50	ps	
t _{SKD2}	Channel to Channel Skew (Notes 11, 13)			18	65	ps	
t _{SKD3}	Part to Part Skew (Notes 11, 14)			50	170	ps	
t _{LHT}	Rise Time (Note 11)	R _L = 100Ω		80	160	ps	
t _{HLT}	Fall Time (Note 11)			80	160	ps	
t _{ON}	Any PWDN to Output Active Time			8	20	μs	
t _{OFF}	Any PWDN to Output Inactive Time			5	12	ns	
JITTER PERFORMANCE WITH EQ = Off, PE = Off (Note 11) (Figure 5)							
t _{RJ1}	Random Jitter (RMS Value)	V _{ID} = 350 mV	2.5 Gbps		0.5	1	ps
t _{RJ2}	No Test Channels (Note 15)	V _{CM} = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t _{DJ1}	Deterministic Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		6	22	ps
t _{DJ2}	No Test Channels (Note 16)	V _{CM} = 1.2V K28.5 (NRZ)	3.125 Gbps		10	29	ps
t _{TJ1}	Total Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		0.04	0.09	UI _{P-P}
t _{TJ2}	No Test Channels (Note 17)	V _{CM} = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.06	0.14	UI _{P-P}
JITTER PERFORMANCE WITH EQ = Off, PE = On (Note 11) (Figures 6, 9)							
t _{RJ1B}	Random Jitter (RMS Value)	V _{ID} = 350 mV	2.5 Gbps		0.5	1	ps
t _{RJ2B}	Test Channel B (Note 15)	V _{CM} = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t _{DJ1B}	Deterministic Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		7	15	ps
t _{DJ2B}	Test Channel B (Note 16)	V _{CM} = 1.2V K28.5 (NRZ)	3.125 Gbps		4	23	ps
t _{TJ1B}	Total Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		0.05	0.10	UI _{P-P}
t _{TJ2B}	Test Channel B (Note 17)	V _{CM} = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.06	0.14	UI _{P-P}
JITTER PERFORMANCE WITH EQ = On, PE = Off (Note 11) (Figures 7, 9)							
t _{RJ1D}	Random Jitter (RMS Value)	V _{ID} = 350 mV	2.5 Gbps		0.5	1	ps
t _{RJ2D}	Test Channel D (Note 15)	V _{CM} = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t _{DJ1D}	Deterministic Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		14	30	ps
t _{DJ2D}	Test Channel D (Note 16)	V _{CM} = 1.2V K28.5 (NRZ)	3.125 Gbps		15	30	ps
t _{TJ1D}	Total Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		0.08	0.15	UI _{P-P}
t _{TJ2D}	Test Channel D (Note 17)	V _{CM} = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.10	0.17	UI _{P-P}

Symbol	Parameter	Conditions		Min	Typ	Max	Units
JITTER PERFORMANCE WITH EQ = On, PE = On (Note 11) (Figures 8, 9)							
t _{RJ1BD}	Random Jitter (RMS Value)	V _{ID} = 350 mV	2.5 Gbps		0.5	1	ps
t _{RJ2BD}	Input Test Channel D Output Test Channel B (Note 15)	V _{CM} = 1.2V Clock (RZ)	3.125 Gbps		0.5	1	ps
t _{DJ1BD}	Deterministic Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		11	23	ps
t _{DJ2BD}	Input Test Channel D Output Test Channel B (Note 16)	V _{CM} = 1.2V K28.5 (NRZ)	3.125 Gbps		5	24	ps
t _{TJ1BD}	Total Jitter (Peak to Peak)	V _{ID} = 350 mV	2.5 Gbps		0.08	0.14	UI _{P-P}
t _{TJ2BD}	Input Test Channel D Output Test Channel B (Note 17)	V _{CM} = 1.2V PRBS-23 (NRZ)	3.125 Gbps		0.10	0.20	UI _{P-P}

Note 9: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 10: Typical values represent most likely parametric norms for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 13: t_{SKD2} , Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).

Note 14: t_{SKD3} , Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 15: Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 16: Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 17: Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

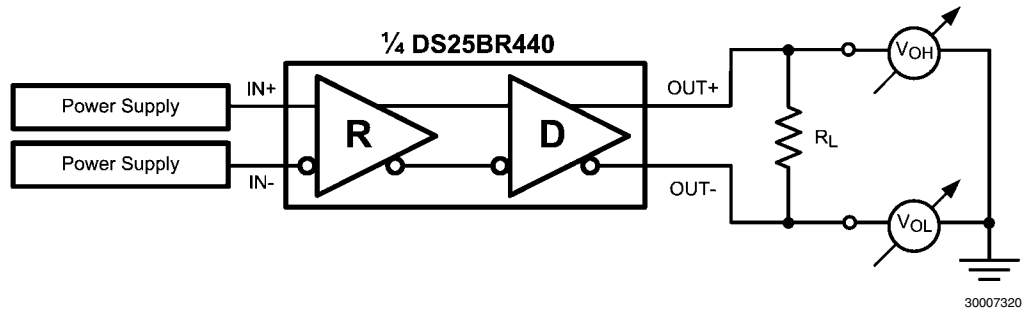


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

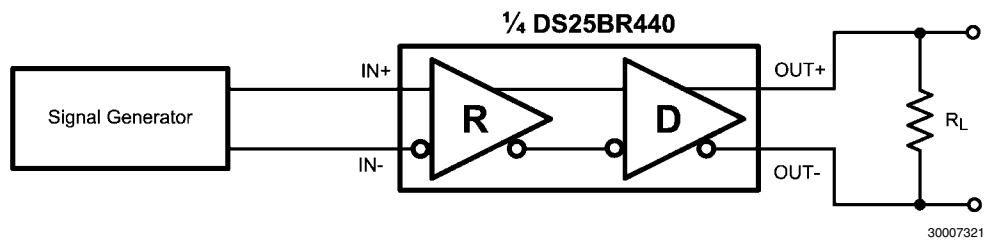


FIGURE 2. Differential Driver AC Test Circuit

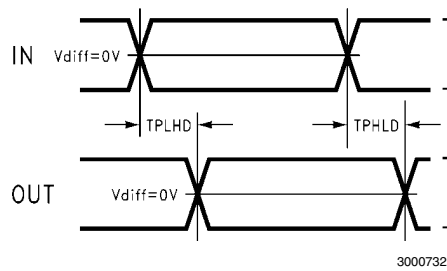


FIGURE 3. Propagation Delay Timing Diagram

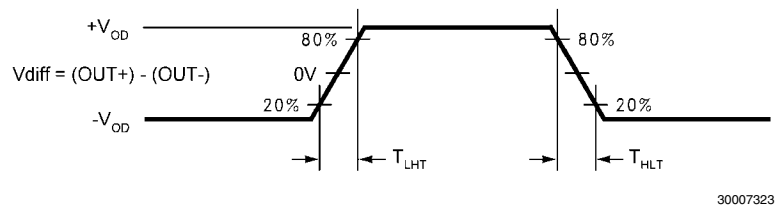
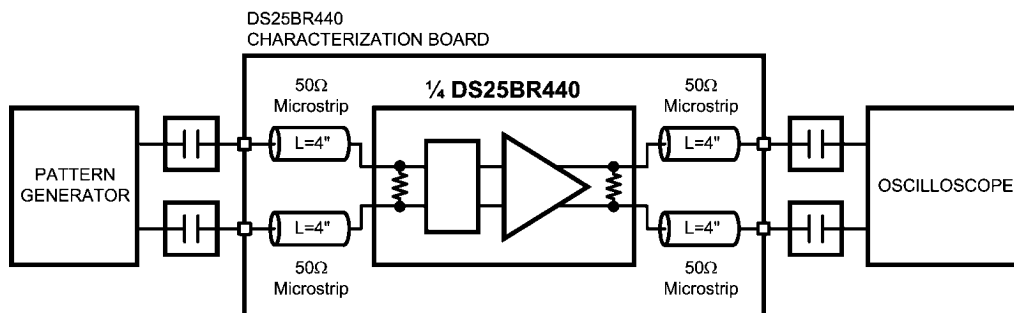


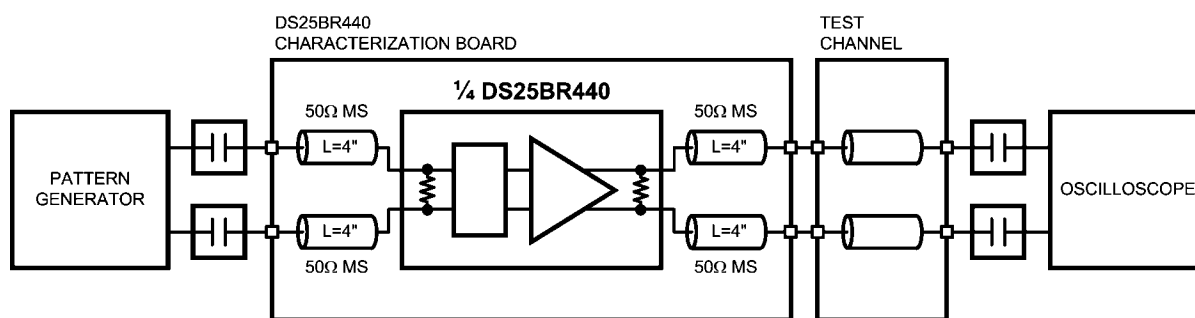
FIGURE 4. LVDS Output Transition Times

Pre-Emphasis and Equalization Test Circuits



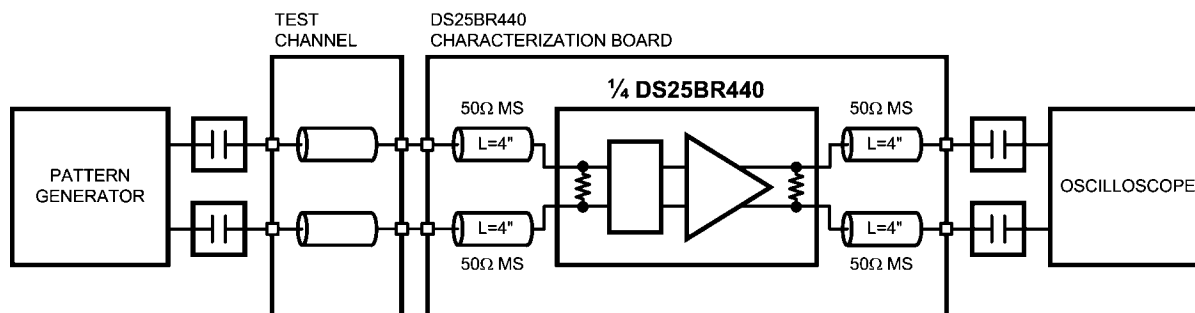
30007329

FIGURE 5. Jitter Performance Test Circuit



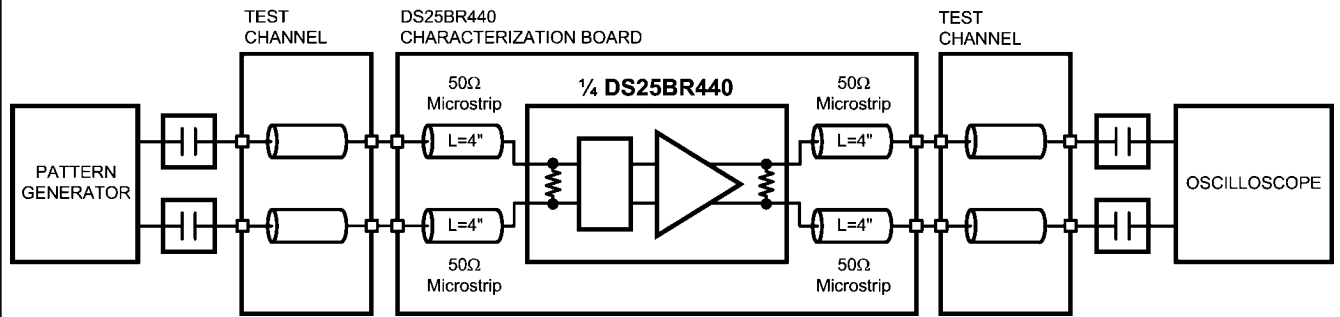
30007327

FIGURE 6. Pre-emphasis Performance Test Circuit



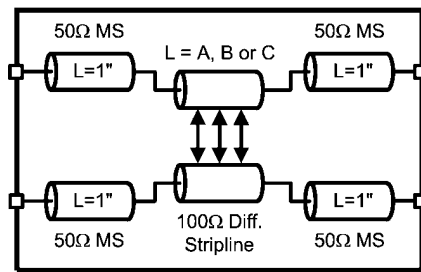
30007326

FIGURE 7. Equalization Performance Test Circuit



30007330

FIGURE 8. Pre-emphasis and Equalization Performance Test Circuit



30007328

FIGURE 9. Test Channel Block Diagram

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Functional Description

The DS25BR440 is a 3.125 Gbps Quad LVDS buffer optimized for high-speed signal routing and repeating over lossy FR-4 printed circuit board backplanes and balanced cables.

The DS25BR440 has a pre-emphasis control pin for each output for switching the transmit pre-emphasis to ON and

OFF setting and an equalization control pin for each input for switching the receive equalization to ON and OFF setting. The following are the transmit pre-emphasis and receive equalization truth tables.

Transmit Pre-emphasis Truth Table

OUTPUT OUT _n , n = {0, 1, 2, 3}	
CONTROL Pin (PE _n) State	Pre-emphasis Level
0	OFF
1	ON

Transmit Pre-emphasis Level Selection for an Output OUT_n

Receive Equalization Truth Table

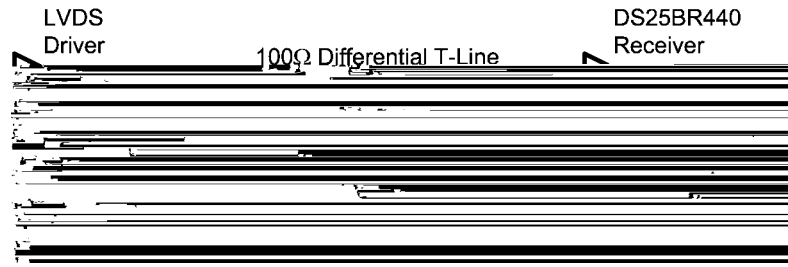
INPUT IN _n , n = {0, 1, 2, 3}	
CONTROL Pin (EQ _n) State	Equalization Level
0	OFF
1	ON

Receive Equalization Level Selection for an Input IN_n

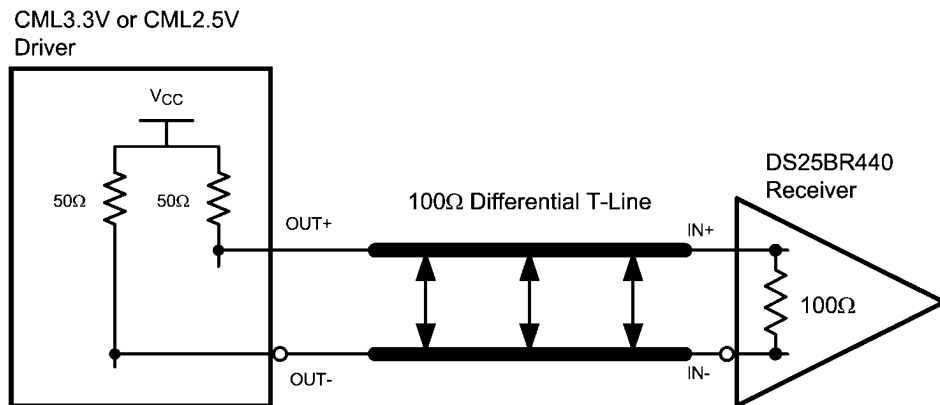
Input Interfacing

The DS25BR440 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR440 can be DC-coupled with all common differential

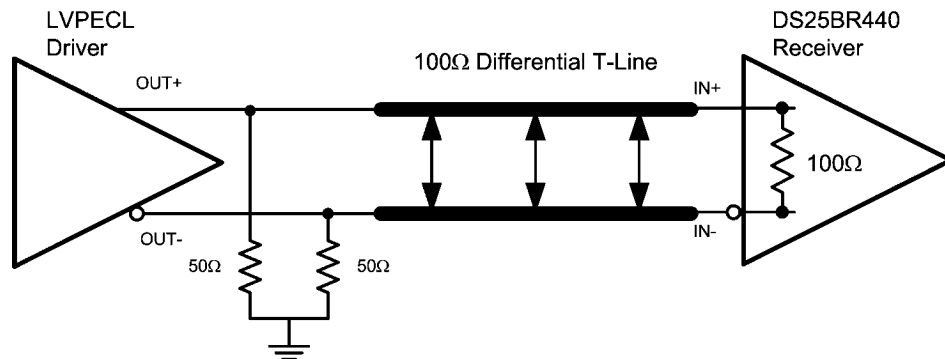
drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR440 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to an DS25BR440 Input



Typical CML Driver DC-Coupled Interface to an DS25BR440 Input

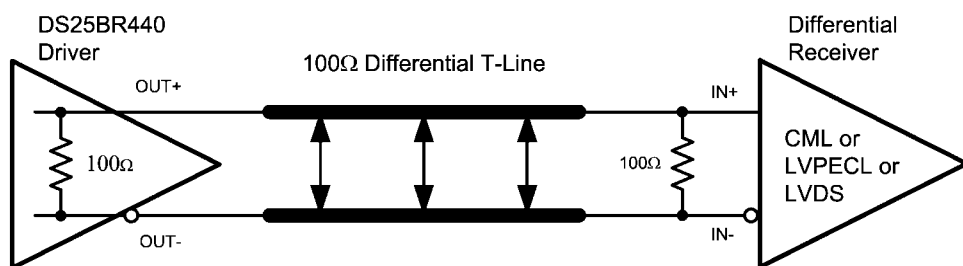


Typical LVPECL Driver DC-Coupled Interface to an DS25BR440 Input

Output Interfacing

The DS25BR440 outputs signals compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and

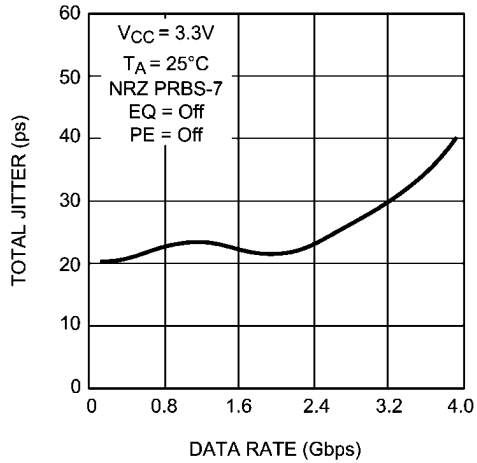
assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



Typical DS25BR440 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

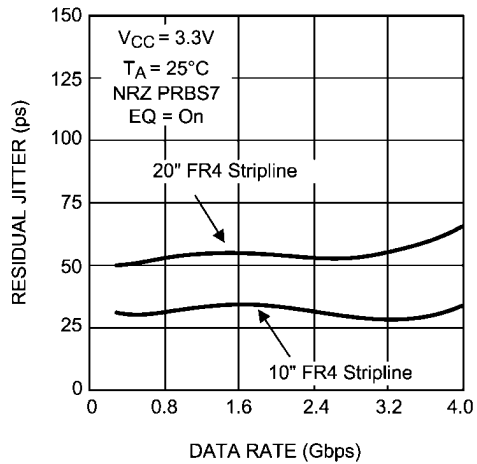
30007334

Typical Performance



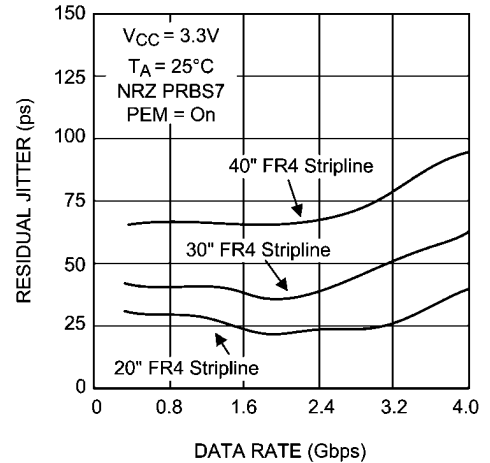
Total Jitter as a Function of Data Rate

30007350



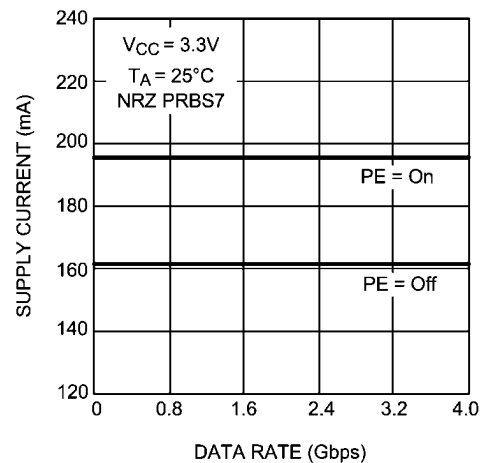
Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level

30007351



Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level

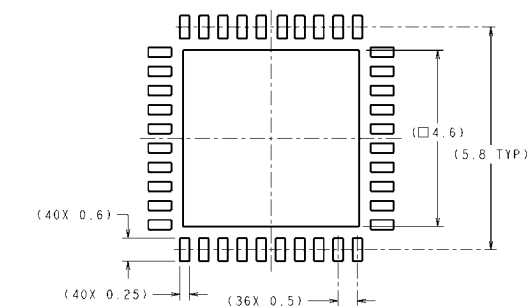
30007355



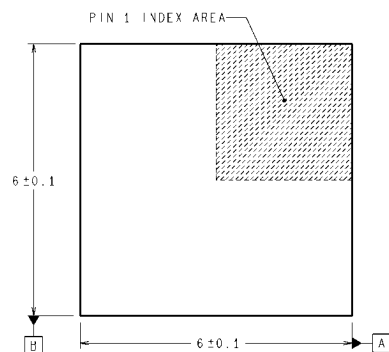
Supply Current as a Function of Data Rate and PE Level

30007357

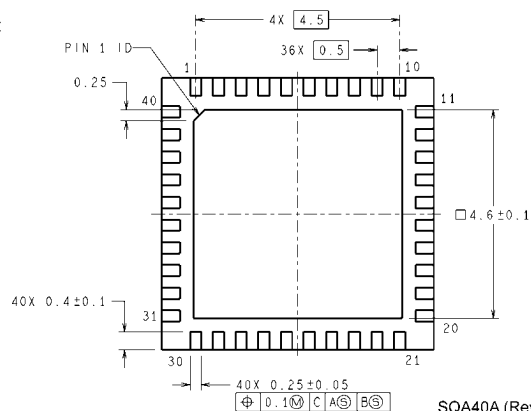
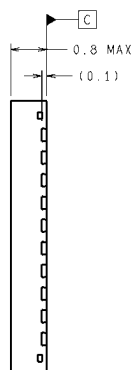
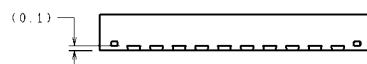
Physical Dimensions inches (millimeters) unless otherwise noted



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SQA40A (Rev B)

Order Number DS25BR440TSQ
NS Package Number SQA40A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adac	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



**National Semiconductor
Americas Technical
Support Center**
Email:
new.feedback@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe
Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia
Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan
Technical Support Center**
Email: jpn.feedback@nsc.com