Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

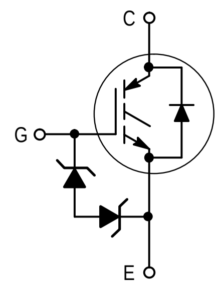
N–Channel Enhancement–Mode Silicon Gate

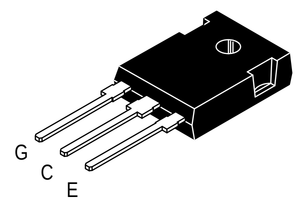
MGW14N60ED

IGBT IN TO–247
14 A @ 90°C
18 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
ON–VOLTAGE

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Its new 600V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co–packaged IGBTs save space, reduce assembly time and cost. This new E–series introduces an energy efficient, ESD protected, and short circuit rugged device.

- Industry Standard TO–247 Package
- High Speed: E_{off} = 60 μJ/A typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400V
- Low On–Voltage — 2.0V typical at 10A, 125°C
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate–Emitter Zener Diodes





CASE 340K–01
STYLE 4
TO–247 AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	18 14 28	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	112 0.89	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.1 1.9 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		$V_{(BR)CES}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		$V_{(BR)ECS}$	15	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	10	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	50	μAdc
ON CHARACTERISTICS(1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 5.0 Adc)		$V_{CE(on)}$	—	1.6	1.9	Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)			—	1.5	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	2.0	2.4	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	5.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1020	—	pF
Output Capacitance		C_{oes}	—	104	—	
Transfer Capacitance		C_{res}	—	17	—	
SWITCHING CHARACTERISTICS(1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω) Energy losses include “tail”	$t_{d(on)}$	—	38	—	ns
Rise Time		t_r	—	40	—	
Turn–Off Delay Time		$t_{d(off)}$	—	120	—	
Fall Time		t_f	—	204	—	
Turn–Off Switching Loss		E_{off}	—	0.35	0.45	mJ
Turn–On Switching Loss		E_{on}	—	0.27	0.35	
Total Switching Loss		E_{ts}	—	0.62	0.80	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	32	—	ns
Rise Time		t_r	—	30	—	
Turn–Off Delay Time		$t_{d(off)}$	—	208	—	
Fall Time		t_f	—	212	—	
Turn–Off Switching Loss		E_{off}	—	0.63	—	mJ
Turn–On Switching Loss		E_{on}	—	0.40	—	
Total Switching Loss		E_{ts}	—	1.03	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	57	—	nC
		Q_1	—	12	—	
		Q_2	—	25	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 5.0 Adc)		V_{FEC}	—	1.6	1.9	Vdc
(I_{EC} = 5.0 Adc, T_J = 125°C)			—	1.3	—	
(I_{EC} = 10 Adc)			1.7	2.0	2.3	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 10 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	75	—	ns
		t_a	—	31	—	
		t_b	—	44	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.16	—	μC
Reverse Recovery Time	(I_F = 10 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	139	—	ns
		t_a	—	45	—	
		t_b	—	94	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.40	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	7.5	—	nH

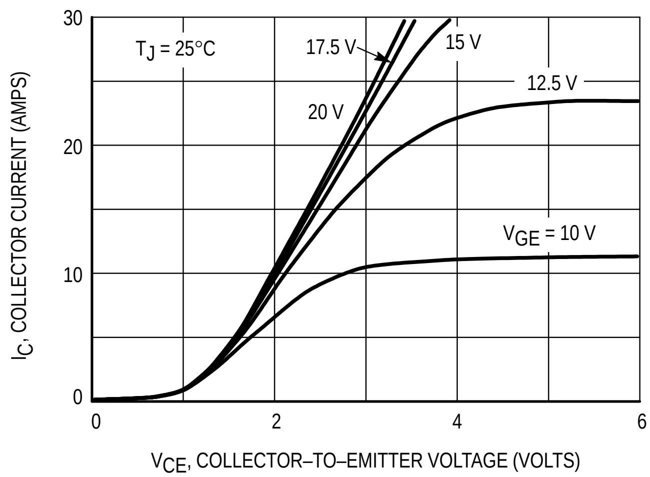


Figure 1. Output Characteristics

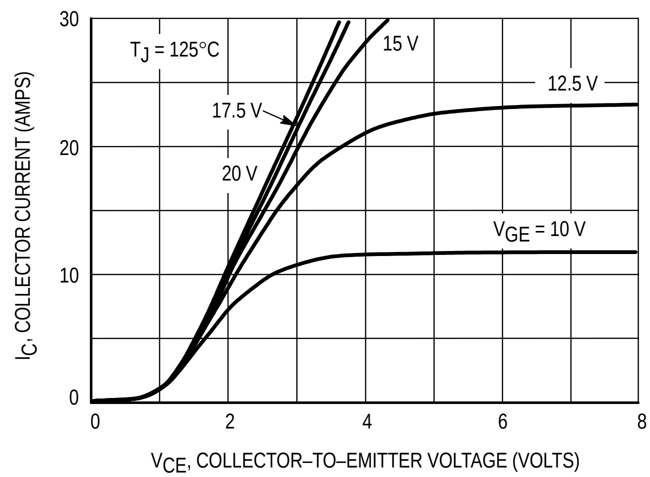


Figure 2. Output Characteristics

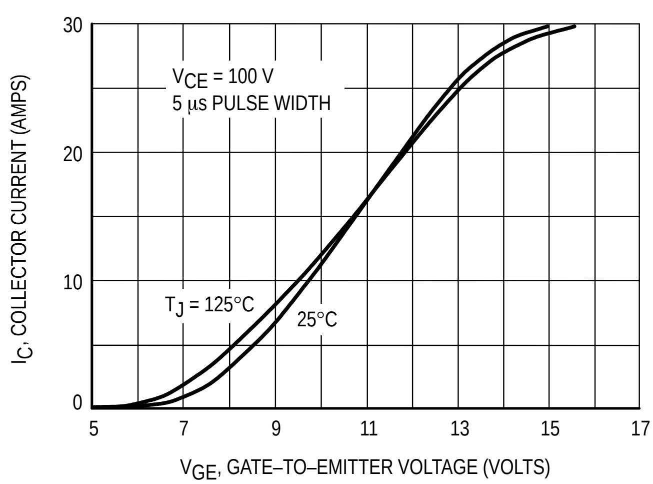


Figure 3. Transfer Characteristics

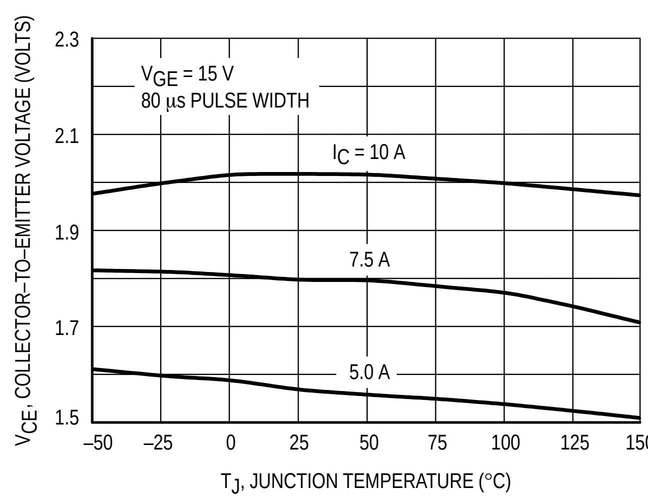


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

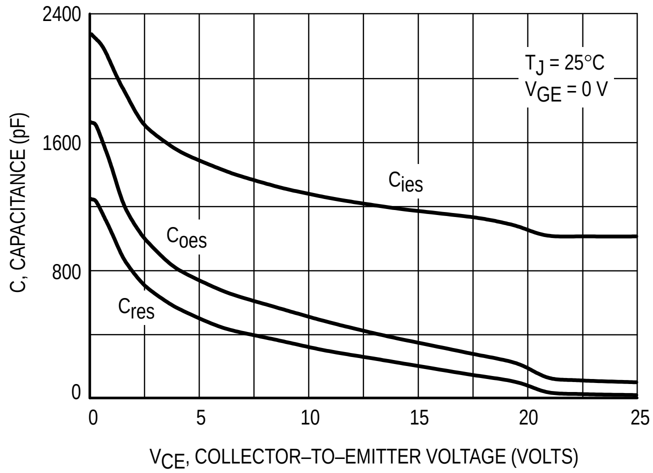


Figure 5. Capacitance Variation

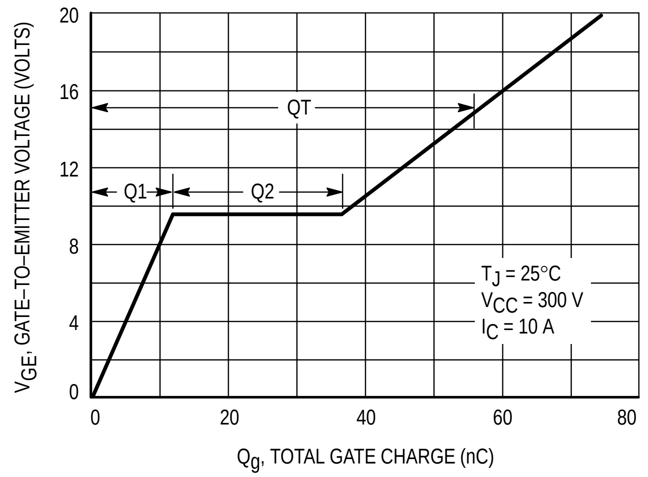


Figure 6. Gate–to–Emitter Voltage versus Total Charge

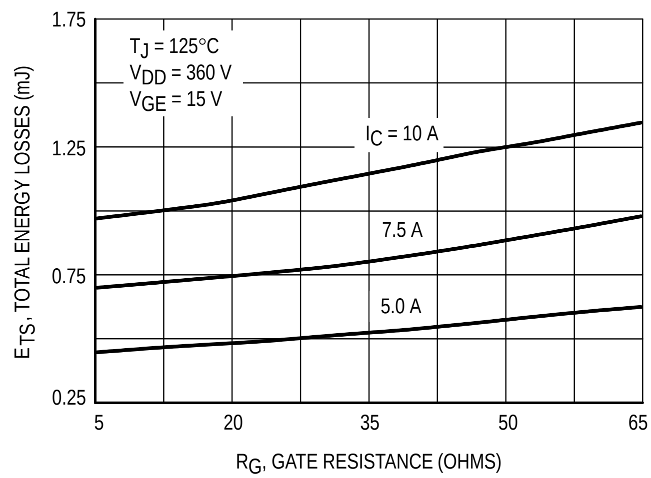


Figure 7. Total Energy Losses versus Gate Resistance

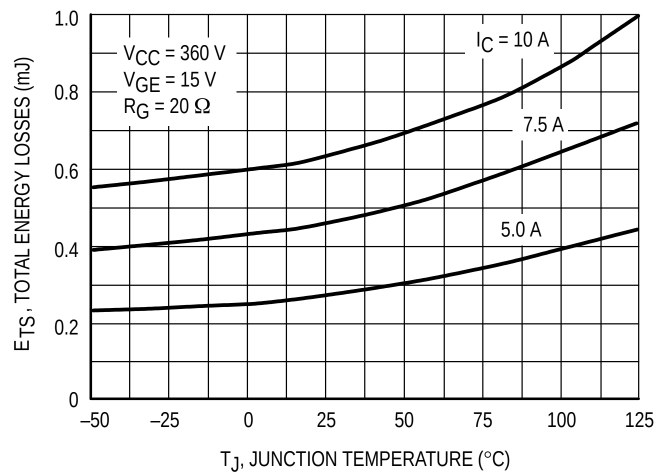


Figure 8. Total Energy Losses versus Junction Temperature

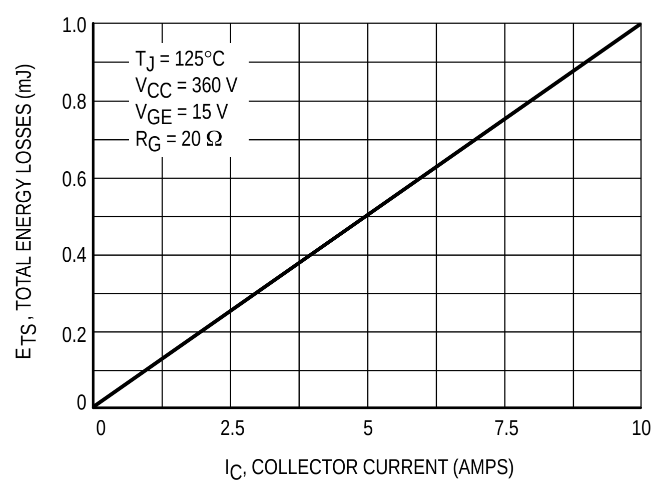


Figure 9. Total Energy Losses versus Collector Current

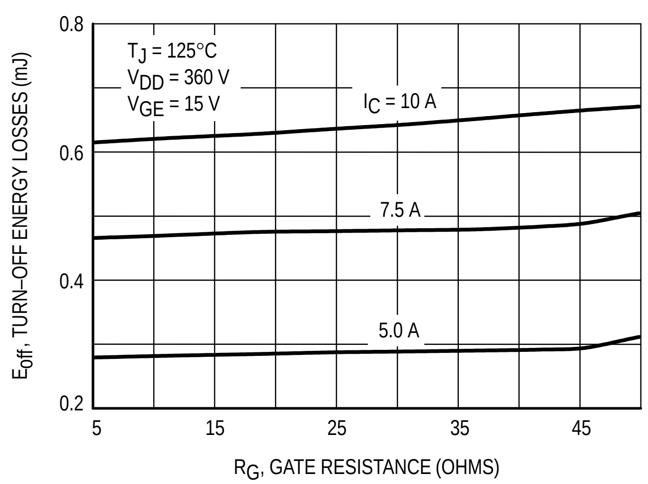


Figure 10. Turn–Off Energy Losses versus Gate Resistance

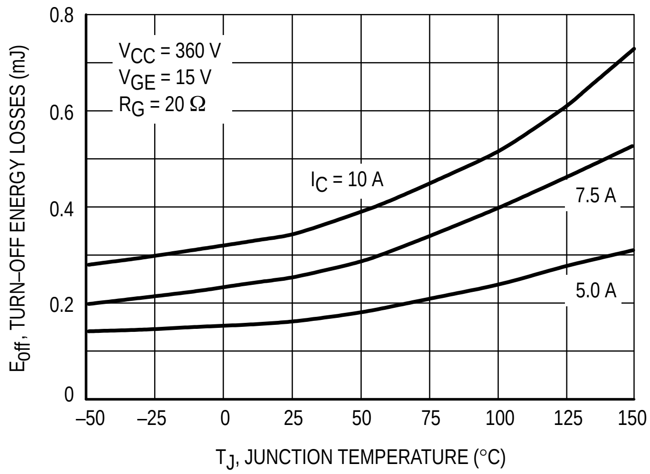


Figure 11. Turn–Off Energy Losses versus Junction Temperature

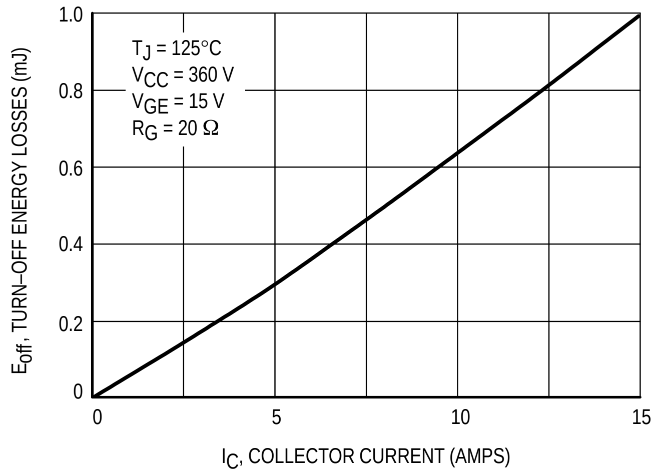


Figure 12. Turn–Off Energy Losses versus Collector Current

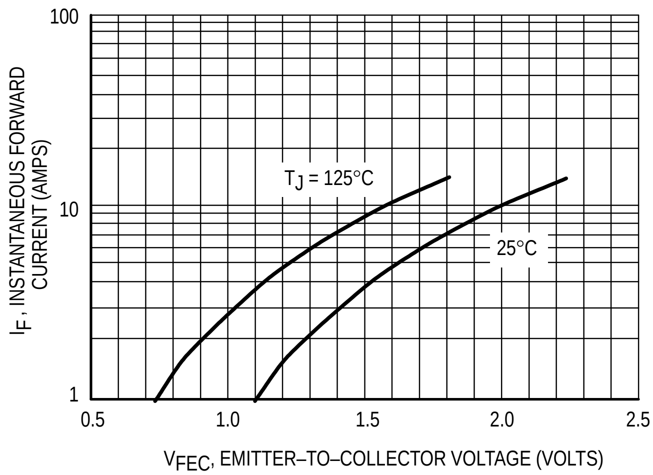


Figure 13. Forward Characteristics versus Current

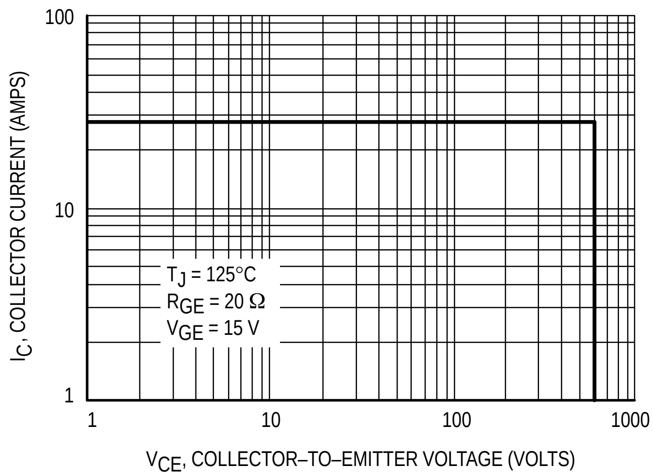
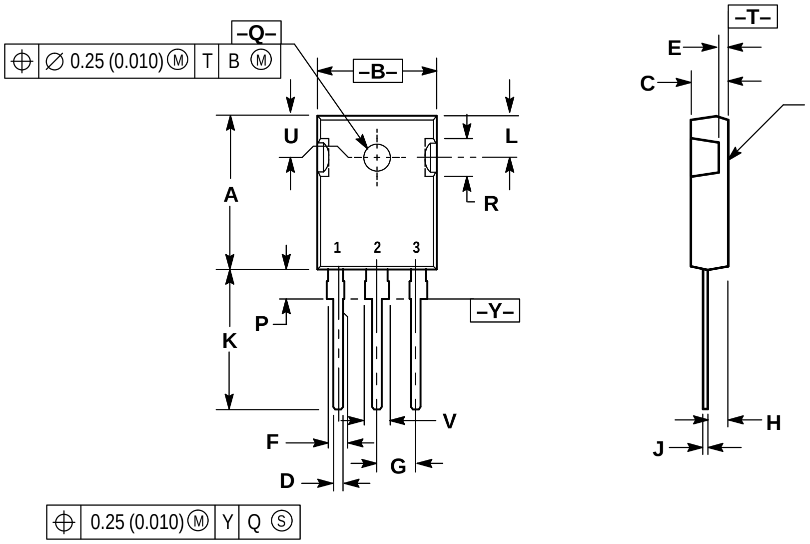


Figure 14. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS



NOTES:
DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340K–01
ISSUE A

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