

CYRUSTEK ES5116 A/D CONVERTER Datasheet

<http://www.manuallib.com/cyrustek/es5116-a-d-converter-datasheet.html>

The ES5116 is low power monolithic CMOS 3 1/2 digit LCD display A/D converter. It contains the internal clock, voltage reference, seven-segment decoders, LCD display drivers and a back plane driver. The improved internal zener reference voltage circuit gives the analog common a small temperature coefficient of typically.

ManualLib.com collects and classifies the global product instruction manuals to help users access anytime and anywhere, helping users make better use of products.

<http://www.manuallib.com>



Features

- Guaranteed zero reading with zero input
- Low input leakage current (1pA typical)
- Internal Reference with low temperature drift (60ppm/°C typically)
- Low noise (15uVp-p typical)
- Direct LCD display driver-no external components required
- Differential input and voltage reference
- Precision null detection with true polarity at zero
- Internal clock circuit
- No additional active circuits required
- Low Battery Indication
- Display-Hold

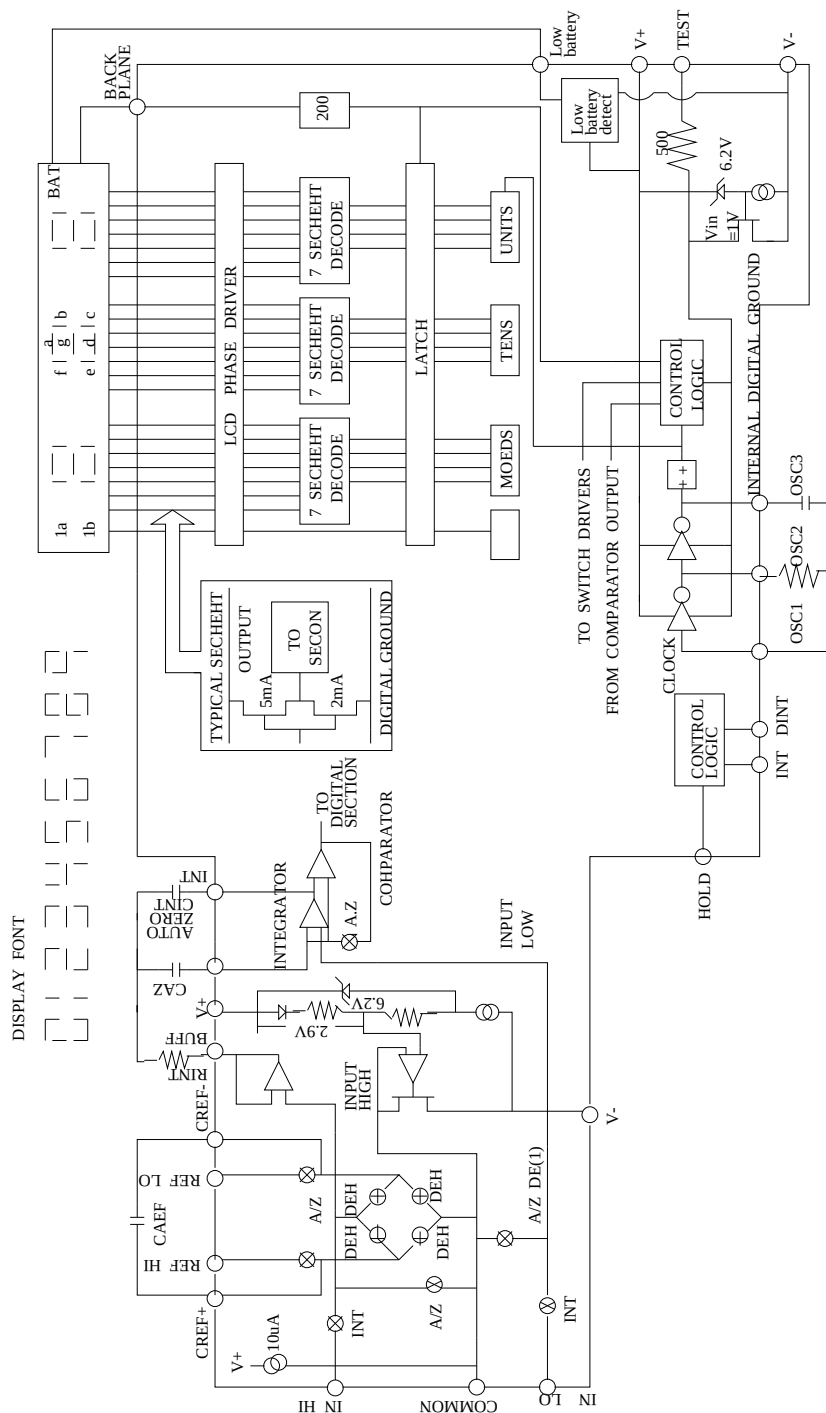
Description

The ES5116 is low power monolithic CMOS 3 1/2 digit LCD display A/D converter. It contains the internal clock, voltage reference, seven-segment decoders, LCD display drivers and a back plane driver. The improved internal zener reference voltage circuit gives the analog common a small temperature coefficient of 60ppm/°C typically. The high accuracy characteristics of the ES5116 perform very low linearity error and roll-over error. The high input impedance ($> 10^{12} \Omega$) and low input leakage current (1pA typical) give the ES5116 a good application in the field of high impedance circuit measurement. The differential input and reference are suitable for measuring bridge transducer or ohms by using ratio-metric method. The dual slope conversion technique makes the ES5116 a good normal and common mode rejection ratio. With a suitable oscillator frequency, the ES5116 has a high rejection of 50Hz, 60Hz and 400Hz line frequency noise. With single power supply, a few passive components and a LCD display, ES5116 can be built as high performance panel meter. Existing Display hold, low battery flag integration and De-integration are four additional features.

Application

1. Digital panel meters
2. Digital multi-meters
3. Thermometers
4. Capacitance meters
5. pH meters
6. Photo-meters

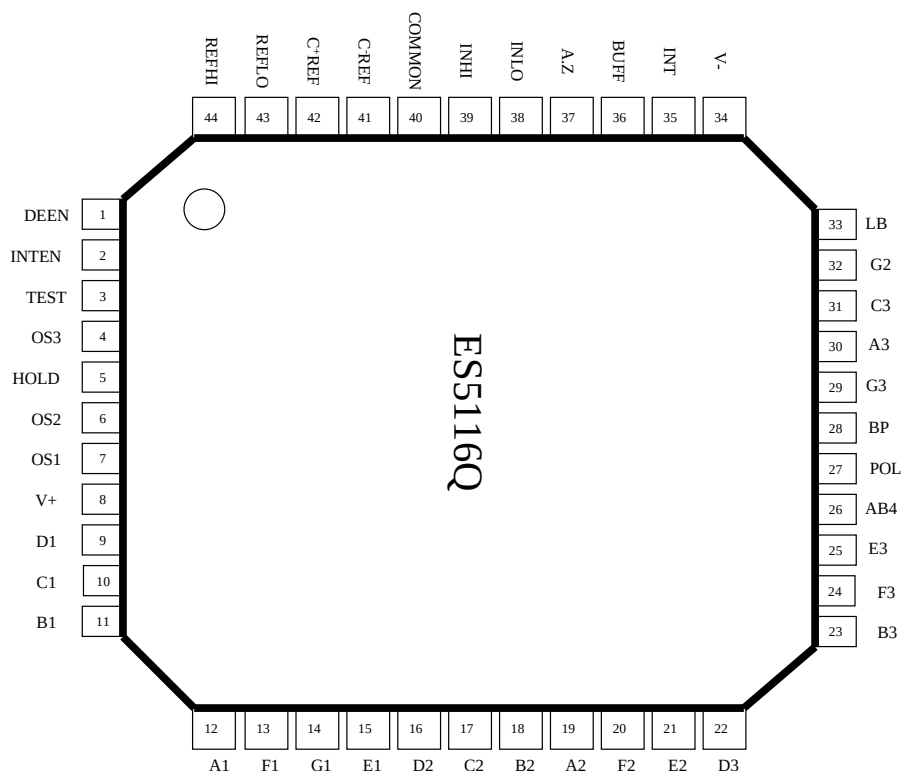
Block Diagram





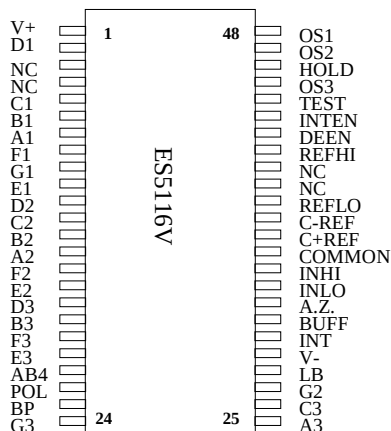
Pin Assignment

1 QFP-44pin package





2 SSOP-48pin package



Pin Description

Pin No.	Symbol	Type	Description
¹ 1	DEEN	O	De-integration status flag.
2	INTEN	O	Integration status flag.
3	TEST	I	Pull high to V+ all LCD segments will be activated.
4	OS3	–	Crystal oscillator connection.
5	HOLD	I	Hold pin, pull high to hold display.
6	OS2	–	Crystal oscillator connection.
7	OS1	–	Crystal oscillator connection.
8	V+	–	Positive supply voltage. Connecting to battery positive terminal.
9	D1	O	LCD segment line.
10	C1	O	LCD segment line.
11	B1	O	LCD segment line.
12	A1	O	LCD segment line.
13	F1	O	LCD segment line.
14	G1	O	LCD segment line.
15	E1	O	LCD segment line.
16	D2	O	LCD segment line.
17	C2	O	LCD segment line.
18	B2	O	LCD segment line.
19	A2	O	LCD segment line.

continued on next page. . .



...continued from previous page			
Pin No.	Symbol	Type	Description
20	F2	O	LCD segment line.
21	E2	O	LCD segment line.
22	D3	O	LCD segment line.
23	B3	O	LCD segment line.
24	F3	O	LCD segment line.
25	E3	O	LCD segment line.
26	AB4	O	LCD segment line.
27	POL	O	LCD segment line.
28	BP	O	LCD segment line.
29	G3	O	LCD segment line.
30	A3	O	LCD segment line.
31	C3	O	LCD segment line.
32	G2	O	LCD segment line.
33	LB	O	Low-battery flag segment driver.
34	V-	–	Negative supply voltage. Connecting to battery negative terminal.
35	INT	O	Integration cycle output.
36	BUFF	O	Integration resistor connection for buffer output.
37	A.Z	–	Auto-zero capacitor connection.
38	INLO	–	Low analog input signal connection.
39	INHI	–	High analog input signal connection.
40	COMMON	–	Set the common-mode voltage for the system.
41	C+REF	–	Positive capacitor connection for on-chip DC-DC converter.
42	C-REF	–	Negative capacitor connection for on-chip DC-DC converter.
43	REF LO	I	Low differential reference input connection.
44	REF HI	I	High differential reference input connection.

Note:

1. Pin No. of QFP-44 pin package.

Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage (V^+ to V^-)	12V
Analog Input Voltage (either input)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	TEST to V^+
Power Dissipation(plastic package)	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to 160°C
Lead Temperature (soldering,10sec)	270°C

Electrical Characteristics



Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Zero Input Reading	—	$V_{IN} = 0.0V$ Full-Scale=200.0mV	-000.0	± 000.0	+000.0	Digital Reading
Ratio-metric Reading	—	$V_{IN}=V_{REF}$, $V_{REF}=100mV$	999	999/1000	1000	Digital Reading
Linearity (Max.deviation from best straight line fit)	—	full-Scale=200mV or Full-Scale=2.000V	-1	± 0.2	1	Counts
roll-over Error	—	$-V_{IN}=+V_{IN} \sim 200.0mV$	-1	± 0.2	+1	Counts
Common Mode Rejection Ratio	—	$V_{CM}=\pm 1V, V_{IN}=0V$ Full-Scale=200.0mV	—	50	—	$\mu V/V$
Low battery flag	—	V^+ to V^-	6.7	7.0	7.3	V
Noise	—	$V_{IN} = 0V$, Full-Scale = 200.0mV	—	15	—	μV_{p-p}
Input Leakage Current	—	$V_{IN} = 0V$	—	1	10	pA
Zero Reading Drift	—	$V_{IN} = 0V$, $0^\circ C \leq T_A \leq +70^\circ C$	—	0.2	1	$\mu V/^\circ C$
Analog COMMON Voltage (with respect to V^+)	—	25K Ω Between Common and Positive Supply	2.8	3.0	3.2	V
Analog COMMON Temperature Coefficient	—	25K Ω Between Common and V^+ , $0^\circ C \leq T_A \leq +70^\circ C$	—	60	75	ppm/ $^\circ C$
Segment Drive Voltage	—	V^+ to V^- =9V	4	5	6	V
Back plane Drive Voltage	—	V^+ to V^-	4	5	6	V
Supply Current (Does not include COMMON current)	—	$V_{IN}=0V$	—	0.6	0.75	mA

Functional Description

1 Analog Common

The COMMON pin is used to set the common-mode voltage for the system which the input signals are floating. In most of the applications, INLO, REFLO and COMMON pins are usually connected. It can remove common-mode voltage concerns. In other applications, INLO does not connect with COMMON. The ES5116 generates a common mode voltage, which has the high CMRR (86dB typical.) Nevertheless, it should be care to prevent the output of the integrator from saturation.

The COMMON pin is also used as a voltage reference. It outputs a voltage which is around 2.9 volts below the positive supply. The COMMON voltage has a low output impedance of 15 Ω typically.

The analog COMMON is connected internally to an NMOS which can sink 30mA. This NMOS will hold the COMMON voltage at 2.9 volts when an external load attempts to pull the COMMON voltage toward the positive supply. The source current of COMMON is only 10 μA , so it is easy to pull COMMON voltage to a more negative voltage.

When the total supply voltage is large enough to cause the zener to regulate(>7V,) the COMMON voltage will have a low temperature coefficient less than 60ppm/ $^\circ C$ typically. This voltage can be used to generate the reference voltage.

2 Reference Voltage

For an 1000 counts reading, the input signal must be equal to the reference voltage. As a result, it requires the input signal be twice the reference voltage for a 2000 counts full-scale reading. Thus, for the 200.0 mV and 2.000V full-scale, the reference voltage should equal 100.0mV and 1.000V, In some applications the full-scale input voltage may be different to 200 mV or 2.000 V. For example, in the 600 mV full-scale applications, the reference voltage should be set to 300 mV.



The differential reference should be used during the measurement of resistor by the ratio-metric method and when a digital reading of zero is desired for $V_{in} \neq 0$, a compensating offset voltage can be applied between COMMON and INLO, and the voltage of being measured is connected between COMMON and INHI.

3 System Timing

The oscillator frequency is divided by four prior to clocking the internal decade counters. The signal integration takes a fixed 1000 counts time period which is equal to 4000 clock pulses. The back plane drive signal is derived by dividing oscillator frequency by 800. To make a maximum noise rejection of line frequency (60Hz or 50Hz,) the signal integration period should be a multiple of the line frequency period. For 60Hz-noise rejection, oscillator frequencies of 120KHz, 80KHz, 60KHz, 48KHz, 40KHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 100KHz, 50KHz, 40KHz, etc. would be suitable.

For all ranges of frequency R_{osc} should be 100K Ω , C_{osc} is selected from the approximate equation $f \sim 0.45/RC$. For 48KHz clock (3reading/second), $C_{osc} = 100pF$.

4 Integrating Resistor

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 μA . Both of them can supply 20 μA drive currents with negligible linearity errors. The integrating resistor is chosen to remain linear drive region in the output stage. It should not be so large that the leakage current of printed circuit board will induce errors. The recommended integrating resistor value for the 200 mV and 2 V full-scale are 47K Ω and 470 K Ω respectively.

5 Integrating Capacitor

The integrating capacitor should be selected to maximize integrator output voltage swing without causing output saturation. For 3 readings/second (48KHz clock,) a 0.22 μF value of C_{INT} is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal $\pm 2V$ integrator swing.

The integrating capacitor must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

6 Auto-Zero Capacitor

The auto-zero capacitor size has some influence on system noise. A 0.47 μF capacitor is recommended for 200mV full scale. A 0.047 μF capacitor is adequate for 2V full scale applications. A mylar type dielectric capacitor is adequate.

7 Reference Voltage Capacitor

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF} . A 0.1 μF value capacitor is acceptable when INLO is connected with COMMON. A mylar type dielectric capacitor is adequate.

8 TEST

The TEST pin is tied to the internally generated digital ground through a 500 Ω resistor. Its potential is 5V less than $V+$. The TEST pin load should be no more than 1 mA.

If TEST is pulled high to $V+$, all segments plus the minus sign will be activated. It may destroy the LCD display as keeping in this mode for several minutes.

9 Segment Drivers

For 3 readings/second (48KHz clock) the BP frequency is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven in the same frequency/amplitude. They are in phase with BP when the segment should be OFF, but out of phase when ON. The polarity indication is "ON" for negative voltage inputs.



10 Integration Status(INTEN)

The INTEN is an output signal of the converter, it keeps on "high" during the signal integration phase.

11 De-Integration Status(DEEN)

The DEEN is an output signal of the converter, it keeps on "high" during the reference de-integration phase.

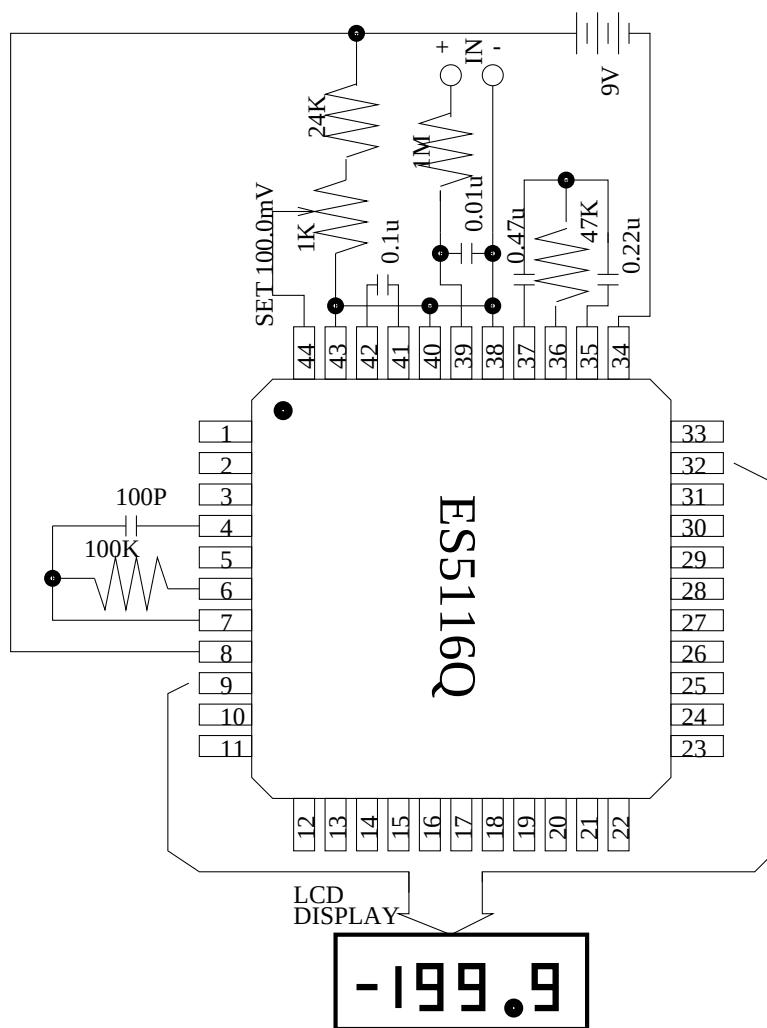
12 Hold

When the hold pin is connected to V+ the conversion result will not be update. The conversion is still free running during hold mode.

13 Low Battery Flag(LB)

When the supply voltage (V+ to V-) is less then 6.9 Volt, The LCD segment of Low Battery Flag is turned on.

Test Circuit

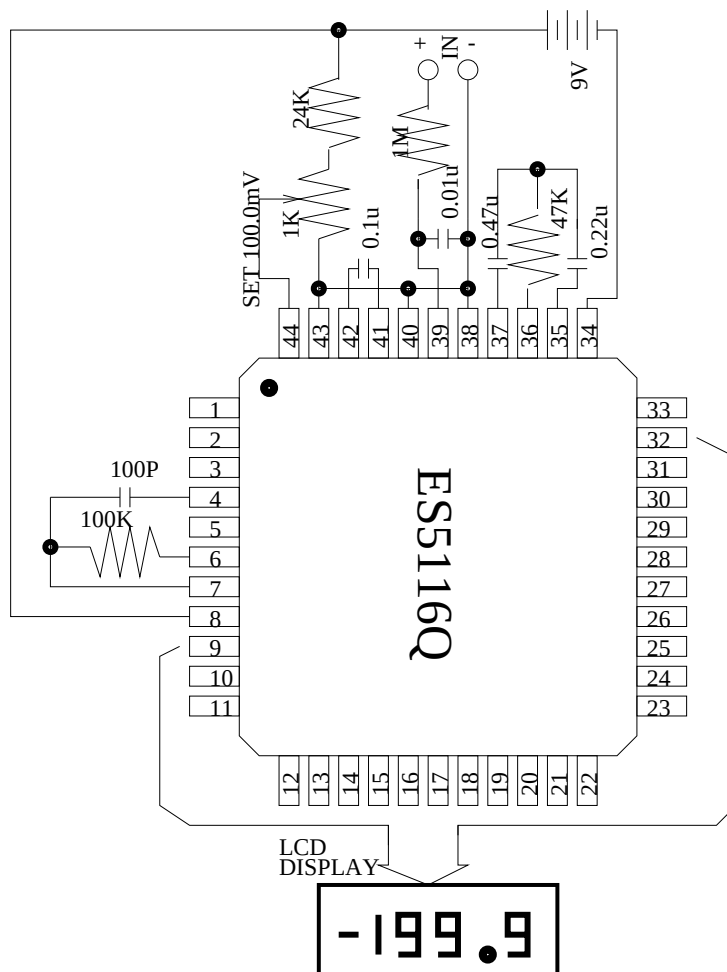


Clock Frequency 48KHz (3 readings/sec)



Application Circuit

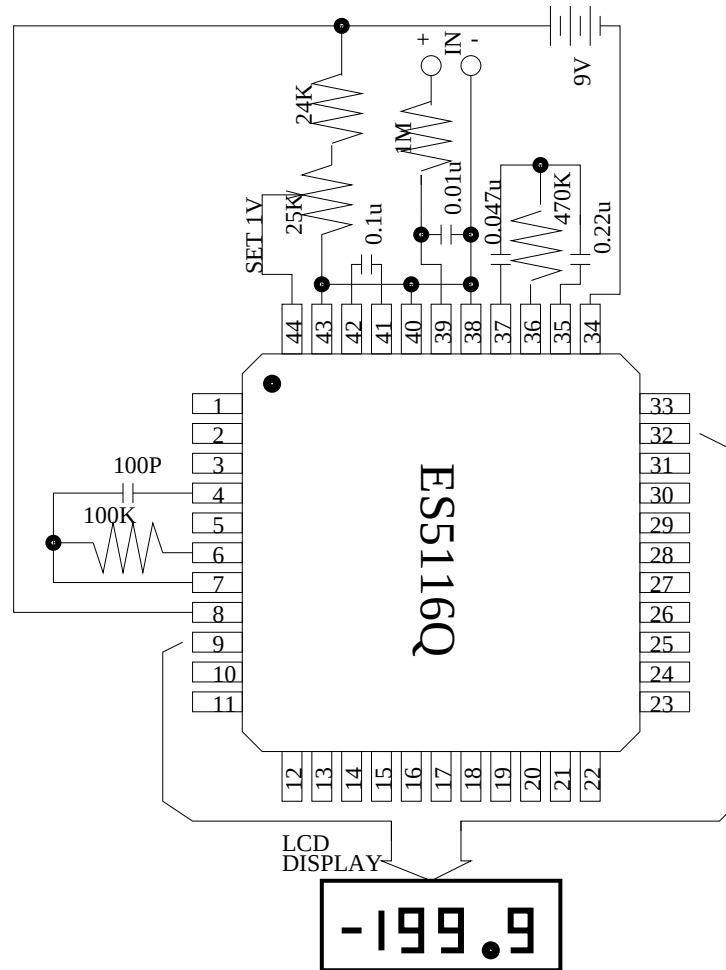
1. This circuit uses analog COMMON voltage as reference voltage. Values here are for 200.0mV full scale, 3 readings/sec.



Clock Frequency 48KHz (3 readings/sec)



2. The values of this circuit are for 2.000V full scale, 3 readings/sec.



Clock Frequency 48KHz (3 readings/sec)