## Analog Power AM20P02-99D MOSFET Datasheet

http://www.manuallib.com/analog-power/am20p02-99d-mosfet-datasheet.html

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low rDS(on) and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and cordless telephones.

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Analog Power AM20P02-99D

### P-Channel 20-V (D-S) MOSFET

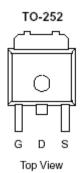
These miniature surface mount MOSFETs utilize High Cell Density process. Low r<sub>DS(on)</sub> assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

•	Low $r_{DS(on)}$ Provides Higher Efficiency and
	Extends Battery Life

- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (±25) for battery pack applications

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)}(m\Omega)$	<b>I</b> <sub>D</sub> (A)		
-20	$118 @ V_{GS} = -4.5V$	17		
	$178 @ V_{GS} = -2.5V$	14		





ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage			-20	V	
Gate-Source Voltage	$V_{GS}$	±12	V		
Continuous Drain Current <sup>a</sup> T <sub>A</sub> =25°C			17	Α	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	±40	A		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-30	A		
Power Dissipation <sup>a</sup>	$T_A=25^{\circ}C$	$P_{\mathrm{D}}$	50	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{ heta JA}$	50	°C/W	
Maximum Junction-to-Case	$R_{ heta JC}$	3.0	°C/W	

1

#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

(C)

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SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)							
Danamatan	Gl1	-	Limits			T 1-4-24	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \text{ uA}$	-0.7				
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1		
Zero Gate Voltage Drain Current	1DSS	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-41			A	
Drain-Source On-Resistance <sup>A</sup>		$V_{GS} = -4.5 \text{ V}, I_D = -17 \text{ A}$			118	mΩ	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$V_{GS} = -2.5 \text{ V}, I_D = -14 \text{ A}$			178	1115.2	
Forward Tranconductance <sup>A</sup>	$g_{\mathrm{fs}}$	$V_{DS} = -10 \text{ V}, I_D = -17 \text{ A}$		31		S	
Diode Forward Voltage	$V_{\mathrm{SD}}$	$I_S = -41 \text{ A}, V_{GS} = 0 \text{ V}$		-0.7		V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_{\mathrm{g}}$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$		12.2		nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -21 \text{ A}$		1.1			
Gate-Drain Charge	$Q_{gd}$	1 <sub>D</sub> 21 A		1.5		1	
Switching							
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = -10 \text{ V}, R_L = 15 \Omega, ID = -41$		15		nS	
Rise Time	t <sub>r</sub>	BB . E .		12			
Turn-Off Delay Time	$t_{d(off)}$	A, $VGEN = -4.5 \text{ V}$ , $RG = 6\Omega$		62		113	
Fall-Time	$t_{\mathrm{f}}$	022		46			

#### Notes

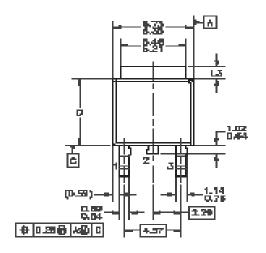
a. Pulse test:  $PW \le 300us duty cycle \le 2\%$ .

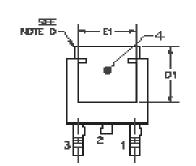
b. Guaranteed by design, not subject to production testing.

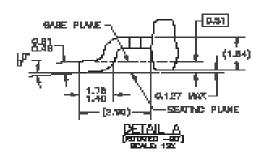
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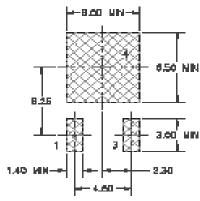
**Analog Power** AM20P02-99D

# Package Information

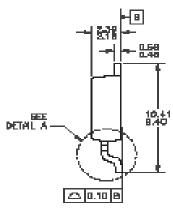








LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- UNLESS CHEEPASE SPECIFIED
  ALL DIVERSIONS ARE IN INLLUMETERS.
  THIS PROCESS CONFORMS TO JEDEC, TO-262,
  168UE C, VARIATION AS IN 68, DATED NOW 1989.
  DIVERSIONING AND TOLERANGING PER
- ASNE T19-0H-1894.
  HEXT SINK TOP ELGE COULD BE IN CHANFERED CORNERS OR ELBE PROTEUSION.
  DINESIENS LED, E1-201 TABLE:

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