EiceDRIVER™

1EDN751x/1EDN851x



Features

Fast, Precise, Strong and Compatible

- 5 ns slew rate to support high speed Superjunction MOSFET (like CoolMos™ C7) or GaN devices
- 19 ns propagation delay precision for fast MOSFET and GaN switching
- 8 A sink and 4 A source driver capability enables fast switching for very high efficiency applications and powers low ohmic MOSFET
- Industry standard packages and pinout ease system-design upgrades

The New Reference in Ruggedness

- 4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET protection under abnormal conditions
- -10 V input voltage capability delivers robustness and crucial safety margin when device is driven from pulse-transformers
- 5 A reverse current robustness eliminates the need for output protection circuitry

Applications

- Server SMPS (Switch Mode Power Supplies)
- TeleCom SMPS
- DC-to-DC Converter
- Bricks
- Power Tools
- Industrial SMPS
- Motor Control

Example Topologies

- Synchronous Rectification
- Power Factor Correction PFC (DCM, CCM)
- LLC, ZVS in combination with pulse transformer for isolation

Description

The 1EDN7x/1EDN8x is an advanced single-channel driver. It is suited to drive logic and normal level MOSFETs and supports OptiMOS™, CoolMOS™, Standard Level MOSFETs, Superjunction MOSFETs, as well as IGBTs and GaN Power devices.

The control and enable inputs are LV-TTL compatible (CMOS 3.3 V) with an input voltage range from -5 V to +20 V. -10 V input pin robustness protects the driver against latch-up or electrical overstress which can be induced by parasitic ground inductances. This greatly enhances system stability.

4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET and GaN protection under abnormal conditions. Under such circumstances, this UVLO mechanism provides crucial independence from whether and when other supervisors circuitries detect abnormal conditions.

The output is able to sink 8 A and source 4 A currents utilizing a true rail-to-rail stage. This ensures very low on-resistance of 0.85 Ω up to the positive and 0.35 Ω down to the negative rail respectively. Industry-leading reverse current robustness eliminates the need for Schottky diodes at the outputs and reduces the bill-of-material.

The pinout of the 1EDN family is compatible with the industry standard. Three package variants, SOT23 6-pin, 5-pin and WSON 6-pin, allow optimization of PCB board space usage and thermal characteristics.

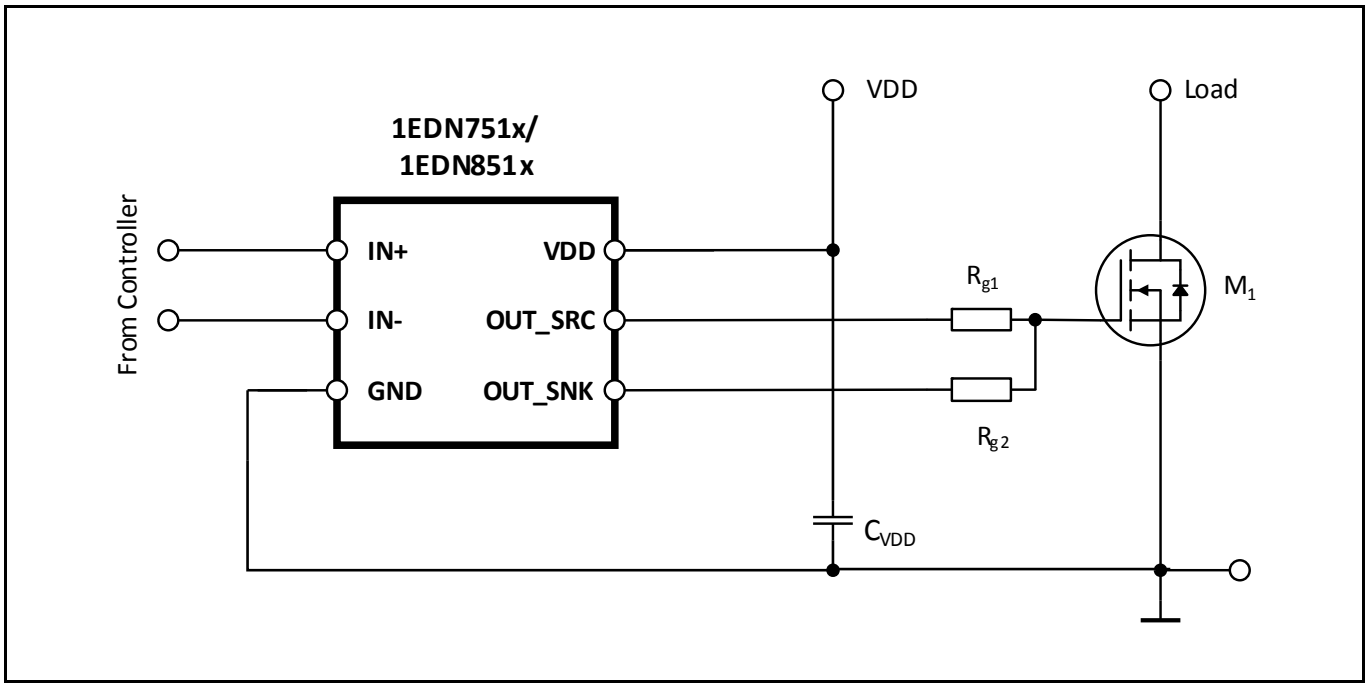

Figure 1 Typical application

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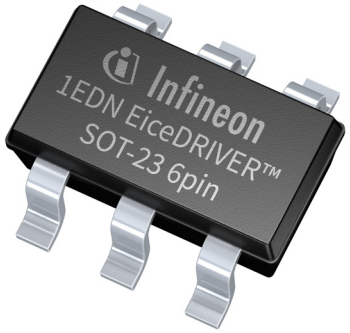
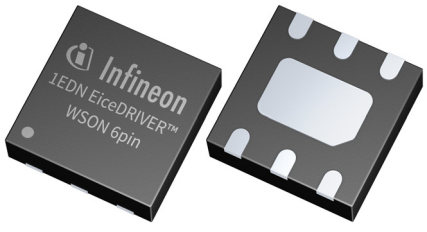
1 Product Versions

The 1EDN751x/1EDN851x is available in 2 different Undervoltage Lockout and 3 package versions.

Table 1 Product Versions

Package	Type. UVLO	Part Number	IC Topside Marking Code
PG-SOT23-6-2			
	**4.2 V**	1EDN7511B	71
	8 V	1EDN8511B	81
PG-SOT23-5-1			
	**4.2 V**	1EDN7512B	72
PG-WSON-6-1			
	**4.2 V**	1EDN7512G	1N7512 AG_XXX HYYWW

1.1 Undervoltage Lockout Versions

The 2 Undervoltage Lockout versions are indicated by the variable x in the product version 1EDNz:

- z=7: lower voltage for logic level MOSFETs (typ. 4.2 V)
- z=8: higher voltage for standard and superjunction MOSFETs (typ. 8.0 V)

Please refer to the functional description section for more details in **Chapter 4.5**

1.2 Package Versions

Following versions regarding UVLO and output configuration are available.

- a standard SOT-23; 6 pin (1EDN7511B and 1EDN8511B)
- a standard SOT-23; 5 pin (1EDN7512B)
- a leadless WSON-6; 6 pin (1EDN7512G)

2 Pin Configuration and Description

The pin configuration for the PG-SOT23-6-2 package is shown in **Figure 2**. Pin description is given below in **Table 2**. For functional details, please read **Chapter 4**.

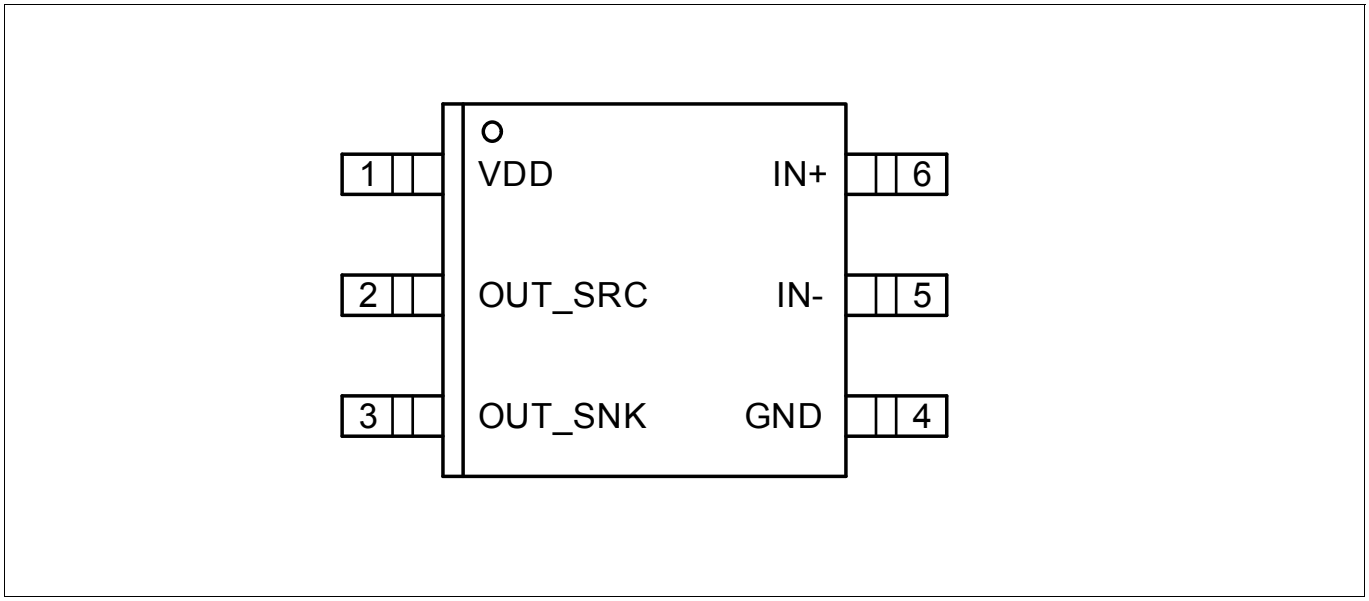


Figure 2 Pin Configuration PG-SOT23-6-2 (top side view)

Table 2 Pin Configuration

Symbol	Description
IN+	Non-inverting Input Logic Input; if IN+ is low or left open causes OUT low
IN-	Inverting Input Logic Input; if IN- is high or left open, causes OUT low
GND	Ground
VDD	Positive Supply Voltage Operating range 4.5 V to 20 V
OUT_SNK	Driver Output Sink Low-impedance output with sink capability
OUT_SRC	Driver Output Source Low-impedance output with source capability

Note: The pin configuration in the PG-SOT23-6-2 features separated source and sink outputs.

Pin Configuration and Description

The pin configuration for the PG-SOT23-5-1 package is shown in **Figure 3**. Pin description is given below in **Table 3**. For functional details, please read **Chapter 4**.

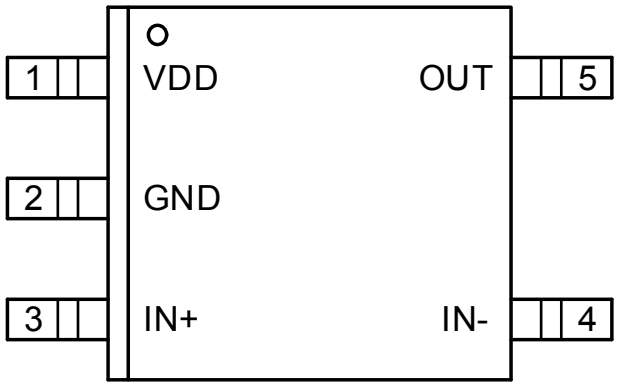


Figure 3 Pin Configuration PG-SOT23-5-1 (top side view)

Table 3 Pin Configuration

Symbol	Description
IN+	Non-inverting Input Logic Input; if IN+ is low or left open causes OUT low
IN-	Inverting Input Logic Input; if IN- is high or left open, causes OUT low
GND	Ground
VDD	Positive Supply Voltage Operating range 4.5 V to 20 V
OUT	Driver Output Low-impedance output and sink capability

Note: Package PG-SOT23-5-1 features a shorted source sink output.

The pin configuration for the PG-WSON-6-1 package is shown in **Figure 4**. Pin description is given below in **Table 4**. For functional details, please read **Chapter 4**.

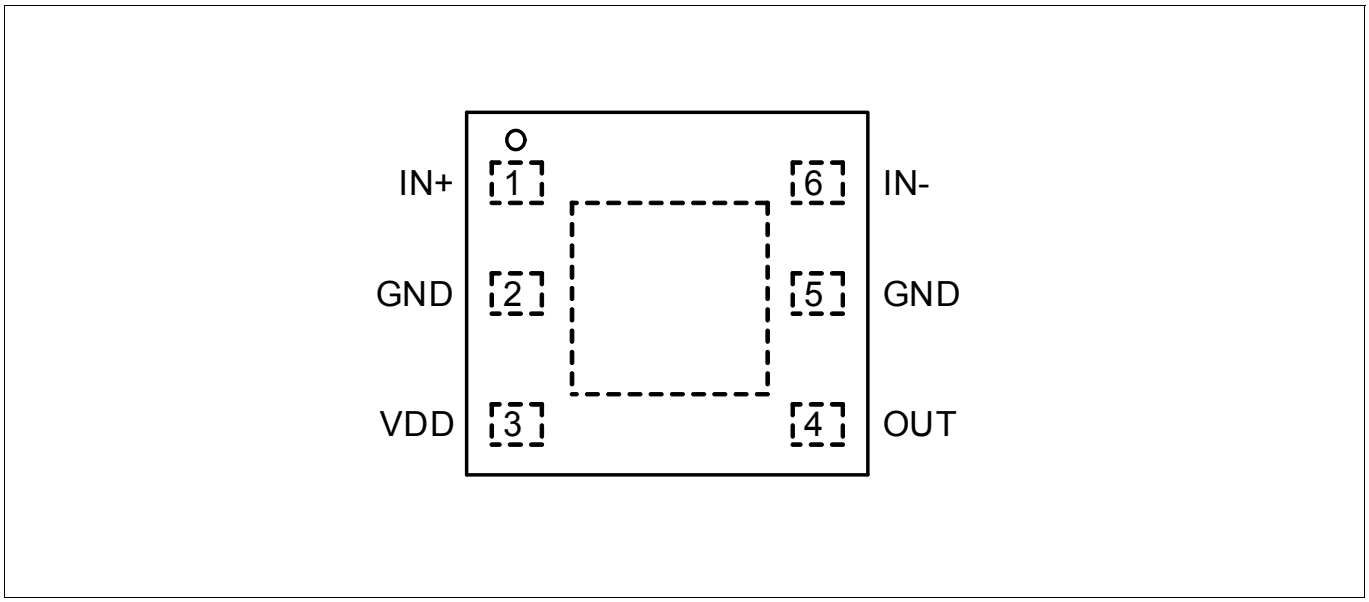


Figure 4 Pin Configuration PG-WSON-6-1 (top side view)

Table 4 Pin Configuration

Symbol	Description
IN+	Non-inverting Input Logic Input; if IN+ is low or left open causes OUT low
IN-	Inverting Input Logic Input; if IN- is high or left open, causes OUT low
GND	Ground
VDD	Positive Supply Voltage Operating range 4.5 V to 20 V
OUT	Driver Output Low-impedance output with source and sink capability

Note:

1. *Package PG-WSON-6-1 has a combined source sink output.*
2. *Exposed pad of PG-WSON-6-1 package has to be connected to GND pin.*

3 Block Diagram

A simplified functional block diagram for the PG-SOT23-6-2 is given in **Figure 5**. This version has separated source and sink outputs.

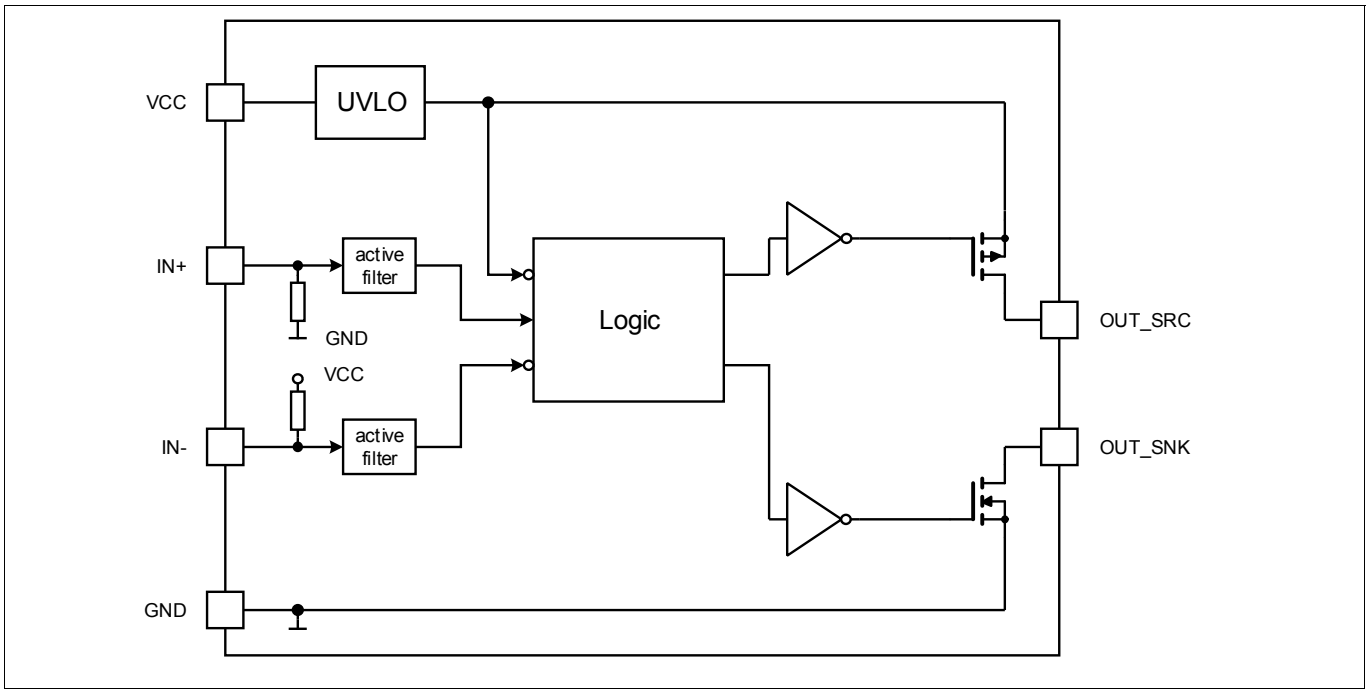


Figure 5 Block Diagram 1EDN7511B and 1EDN8511B

A simplified functional block diagram for PG-WSON-6-1 is depicted in **Figure 6**. This version has one common output.

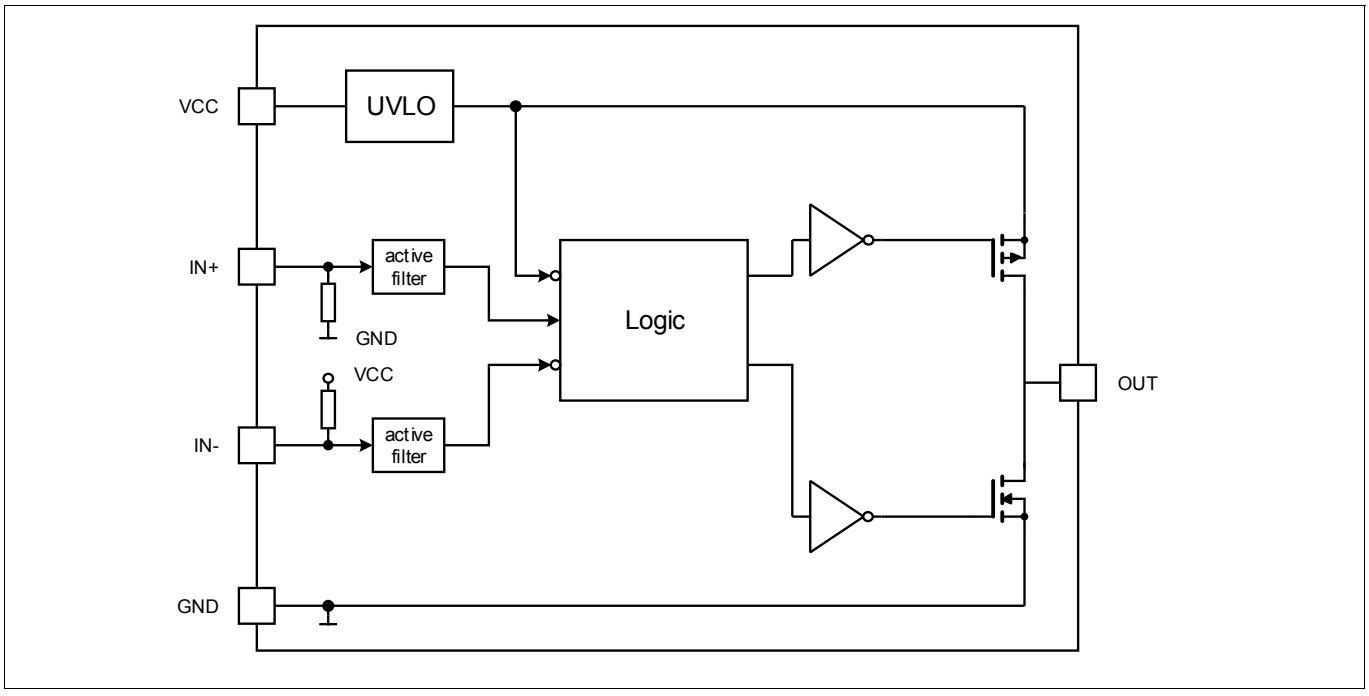


Figure 6 Block Diagram 1EDN7512B 1EDN7512G

4 Functional Description

4.1 Introduction

The 1EDN751x/1EDN851x is a fast single-channel driver for low-side switches. Rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications.

The focus on robustness at the input and output side gives this device an additional safety margin in critical abnormal situations. An extended negative voltage range protects input pins against ground shifts. No current flows over the ESD structure in the IC during a negative input level. Output is robust against reverse current. The interaction with the power MOSFET, even reverse reflected power will be handled by the strong internal output stage.

Inputs are compatible with LV-TTL signal levels. The threshold voltages with a typical hysteresis of 1.1 V are kept constant over the supply voltage range.

Since the 1EDN751x/1EDN851x aims particularly at fast-switching applications, signal delays and rise/fall times have been minimized to support low switching losses in the MOSFET.

4.2 Supply Voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of 1EDN751x/1EDN851x when driving very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2 V or of 8 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

4.3 Driver Inputs

The non-inverting input is internally pulled down to a logic low voltage. The inverting input is internally pulled up to a logic high voltage. This prevents a switch-on event during power-up and a not-driven input condition.

All inputs are compatible with LV-TTL levels and provide a hysteresis of typically 1.1 V. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross-current over signal wires during GND shifts between signal source (controller) and driver input.

4.4 Driver Outputs

The rail-to-rail output stage realized with complementary MOS transistors is able to provide a typical 4 A of sourcing and 8 A sinking current. This asymmetrical push-pull stage enables a perfect “brake before make” (turn off ist faster than turn on) condition, which is needed in half-bridge power MOSFET stages.

This driver output stage has a shoot-through protection and current limiting behavior.

The output impedance is very low with a typical value below 0.85 Ω for the sourcing p-channel MOS and 0.35 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower’s voltage drop.

The gate drive output is held low actively in case of floating inputs or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, the output is held under defined conditions.

4.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The UVLO level is set to a typical value of 4.2 V / 8 V (with hysteresis). UVLO of 4.2 V is normally used for logic level based MOSFETs. For higher level, like standard and high voltage superjunction MOSFETS, an UVLO voltage of typically 8 V is available.

5 Characteristics

The absolute maximum ratings are listed in **Table 5**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{VDD}	-0.3		22	V	
Voltage at pins IN+, IN-	V_{IN}	-10		22	V	
Voltage at pins OUT, OUT_SRC, OUT_SNK	V_{OUT}	-0.3		V_{VDD}+0.3	V	Note[1]
		-2		V_{VDD}+0.3	V	Repetitive pulse < 200ns[2]
Reverse current peak at pins OUT, OUT_SRC/OUT_SNK	I_{SNK_rev} I_{SRC_rev}			-5 5	A_{pk}	< 500 ns
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_S	-55		150	°C	
ESD capability	V_{ESD}			1.5	kV	Charged Device Mode (CDM) [3]
ESD capability	V_{ESD}			2.5	kV	Human Body Model (HBM) [4]

1) Voltage spikes resulting from reverse current peaks are allowed.
2) Values are verified by characterization on bench.
3) According to JESD22-C101
4) According to JESD22-A114

5.2 Thermal Characteristics

Table 6 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PG-SOT23-6-2, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}		170		K/W	
Thermal resistance junction-case (top) [2]	R_{thJC25}		81		K/W	
Thermal resistance junction-board [3]	R_{thJB25}		52		K/W	
Characterization parameter junction-case (top)[4]	Ψ_{thJC25}		14		K/W	

Table 6 Thermal Characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Characterization parameter junction-board [5]	Ψ_{thJB25}		51		K/W	
PG-SOT23-5-1, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}		180		K/W	
Thermal resistance junction-case (top) [2]	R_{thJC25}		76		K/W	
Thermal resistance junction-board [3]	R_{thJB25}		60		K/W	
Thermal resistance junction-bottom (heat sink)[6]	R_{thJB25}		16		K/W	
Characterization parameter junction-case (top) [4]	Ψ_{thJB25}		14		K/W	
Characterization parameter junction-board [5]	Ψ_{thJB25}		52		K/W	
PG-WSON-6-1, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}		63		K/W	
Thermal resistance junction-case (top) [2]	R_{thJP25}		83		K/W	
Thermal resistance junction-board [3]	R_{thJB25}		16		K/W	
Thermal resistance junction-bottom (heat sink) [6]	R_{thJB25}		16		K/W	
Characterization parameter junction-top [4]	Ψ_{thJC25}		9		K/W	
Characterization parameter junction-board [5]	Ψ_{thJB25}		15		K/W	

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

6) The junction-to-bottom thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.3 Operating Range

Table 7 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	4.5		20	V	Min defined by UVLO
Logic input voltage	V_{IN}	-5		20	V	
Junction temperature	T_J	-40		150	°C	1)

1) Continuous operation above 125 °C may reduce life time.

5.4 Electrical Characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_J=25°C.

Table 8 Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	I_{VDDqu1}		0.4		mA	OUT = high, V_{VDD}= 12 V
VDD quiescent current	I_{VDDqu2}		0.37		mA	OUT = low, V_{VDD}= 12 V

Table 9 Undervoltage Lockout for Logic Level MOSFET

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	3.9	4.2	4.5	V	
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	3.6	3.9	4.2	V	
UVLO threshold hysteresis	$UVLO_{hys}$		0.3		V	

Table 10 Undervoltage Lockout for Standard and Superjunction MOSFET Version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	7.4	8.0	8.6	V	
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	6.5	7.0	7.5	V	
UVLO threshold hysteresis	$UVLO_{hys}$	—	1.0	—	V	

Table 11 Logic Inputs IN+, IN-

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	
Input voltage threshold for transition HL	V_{INL}	0.8	1.0	1.2	V	
Input pull up resistor[1)]	$R_{IN\,H}$		400		kΩ	
Input pull down resistor[2)]	$R_{IN\,L}$		100		kΩ	

1) Inputs with initial high logic level
2) Inputs with initial low logic level

Table 12 Static Output Caracteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High Level (Sourcing) Output Resistance	R_{on_SRC}	0.42	0.85	1.46	Ω	I_{SRC} = 50 mA
High Level (Sourcing) Output Current	I_{SRC_peak}		4.0	1)	A	
Low Level (Sinking) Output Resistance	R_{on_SNK}	0.18	0.35	0.64	Ω	I_{SNK} = 50 mA
Low Level (Sinking) Output Current	I_{SNK_Peak}		-8.0	2)	A	

1) Active limited by design at approx. 5.2 A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed
2) Active limited by design at approx. -10.4 A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

Table 13 Dynamic Characteristics (see Figure 7, Figure 8, Figure 9)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input to output propagation delay	T_{PDON}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Input to output propagation delay	T_{PDOFF}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Rise Time	T_{RISE}	—	6.5	11[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Fall Time	T_{FAll}	—	4.5	9[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Minimum input pulse width that changes output state	T_{PW}	—	6	10	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V

1) Parameter verified by design, not 100% tested in production.

6 Timing Diagrams

Figure 7 shows the definition of rise, fall and delay times for the inputs. This is also valid for the inverted control.

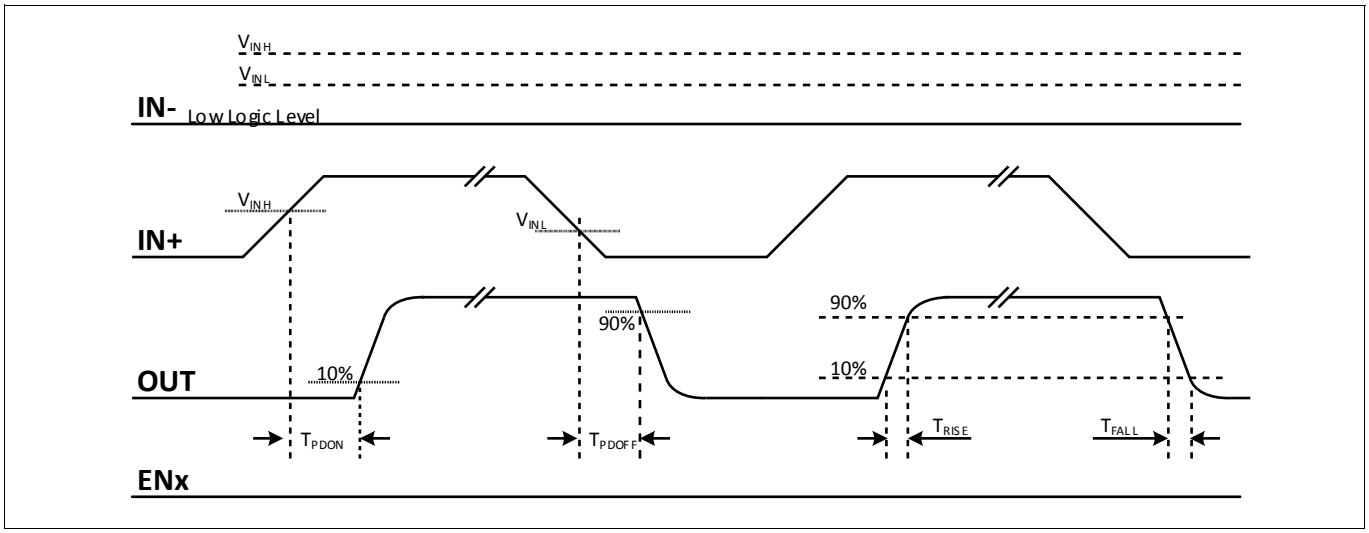


Figure 7 Propagation Delay, Rise and Fall Time, Non-inverted

Figure 8 illustrates the undervoltage lockout function.

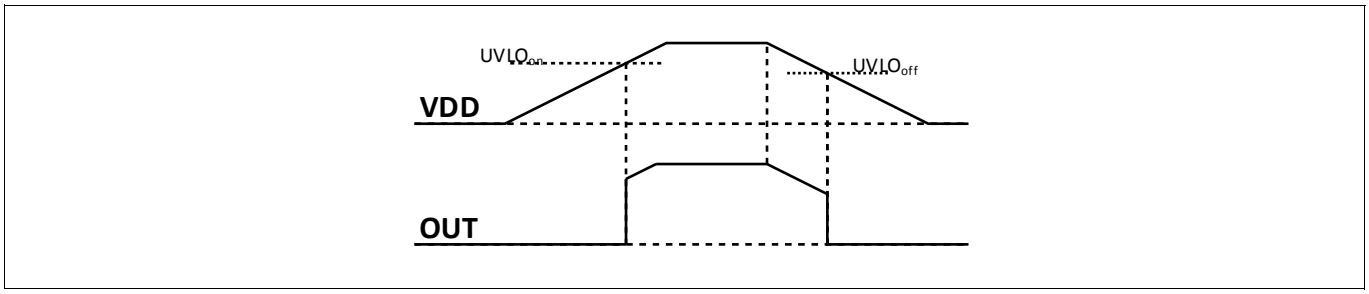


Figure 8 UVLO Behaviour, Input INx Drives OUT Normally High.

Figure 9 illustrates the minimum input pulse width that changes output state.

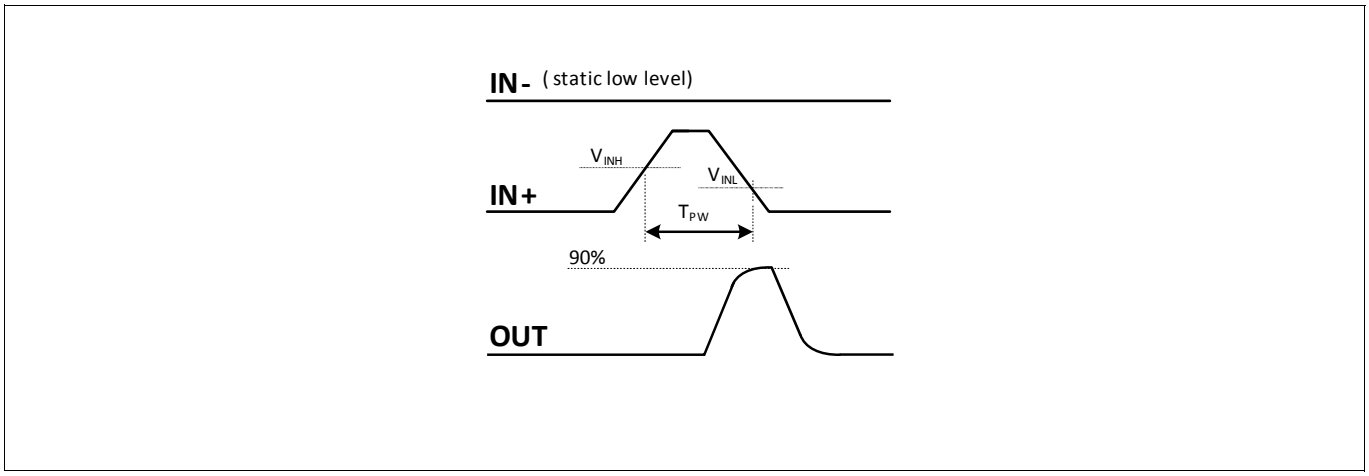


Figure 9 TPW, minimum input pulse width that changes output state.

7 Typical Characteristics

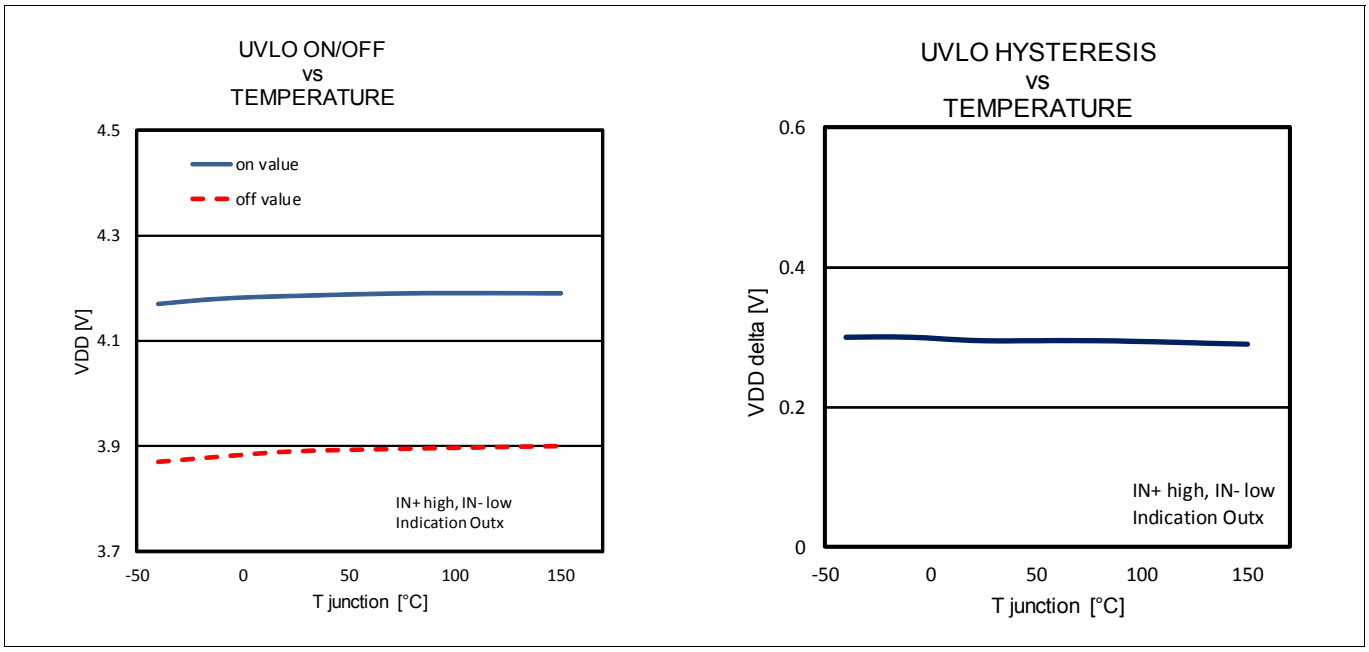


Figure 10 Undervoltage Lockout 1EDN7x (4.2 V)

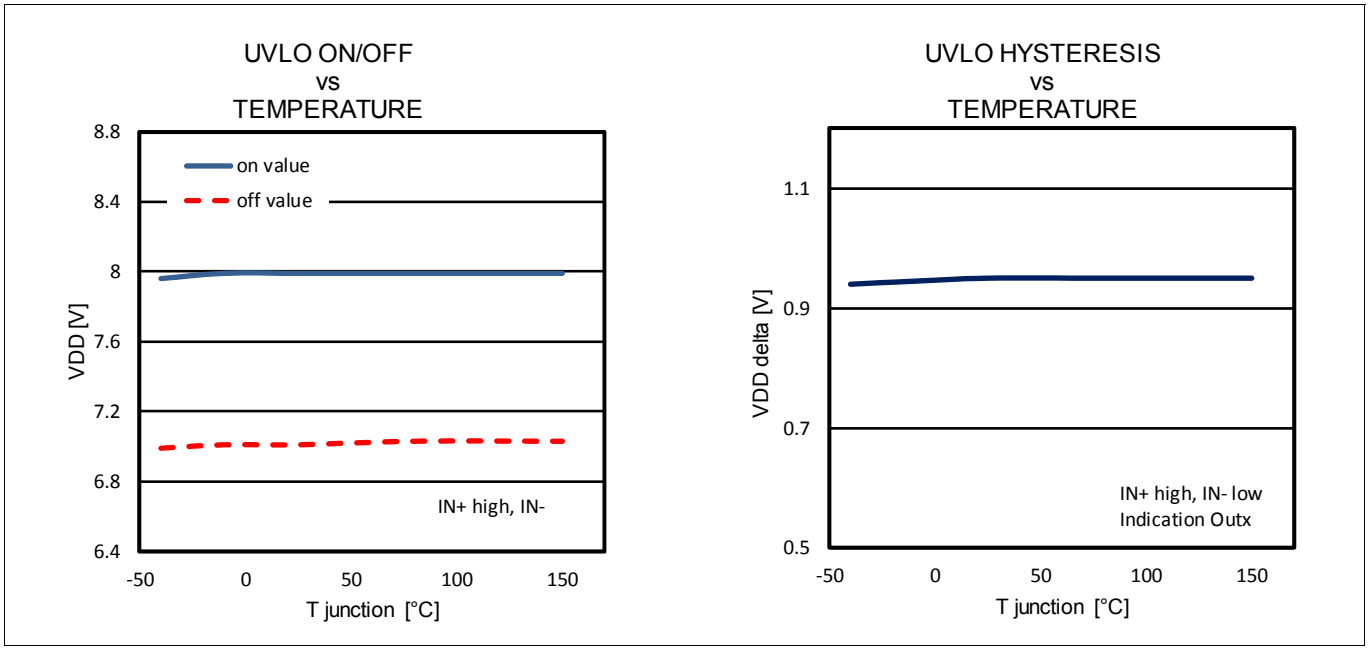


Figure 11 Undervoltage Lockout 1EDN8x (8 V)

Typical Characteristics

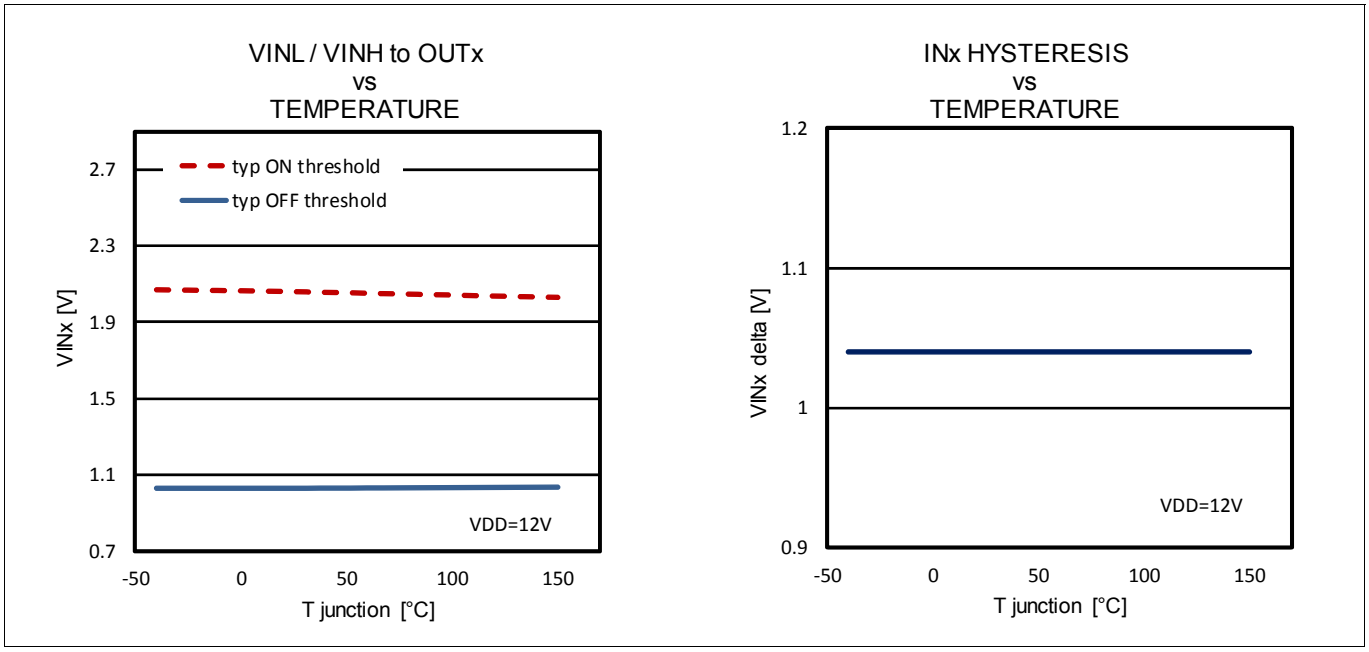


Figure 12 Input (INx) Characteristic

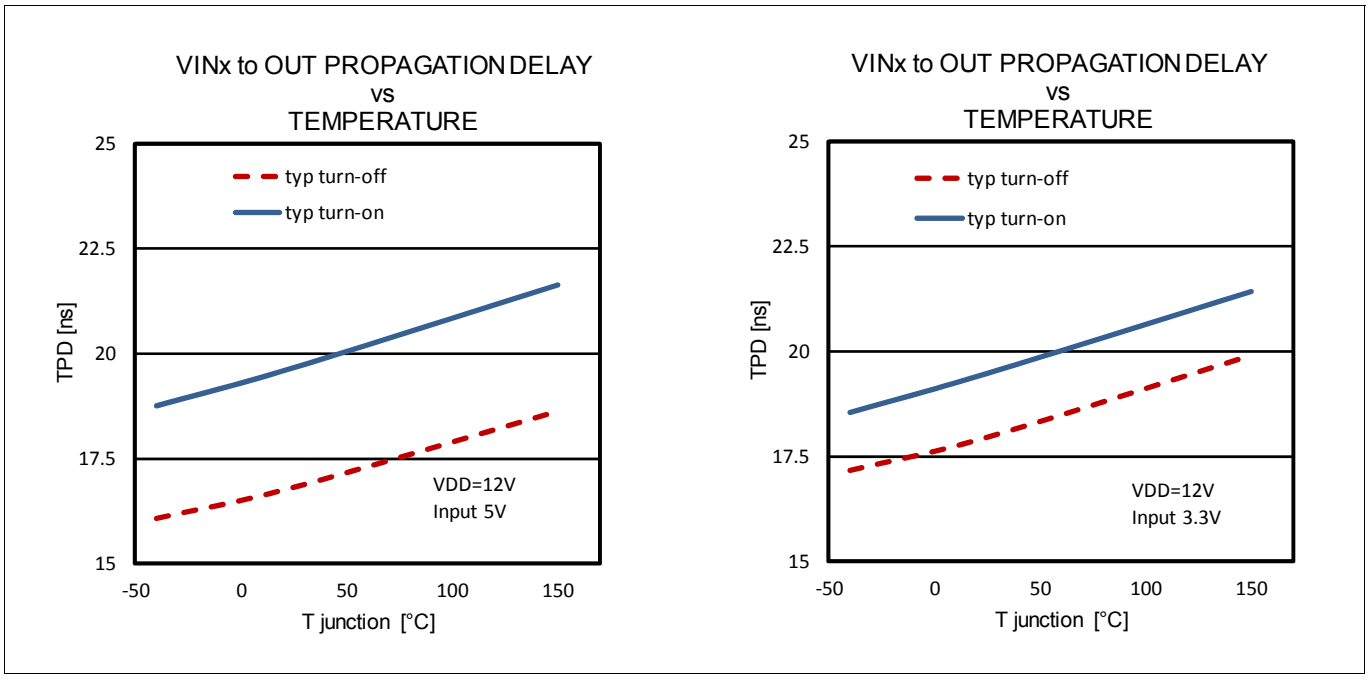


Figure 13 Propagation Delay (INx) on Different Input Logic Levels (See Figure 7)

Typical Characteristics

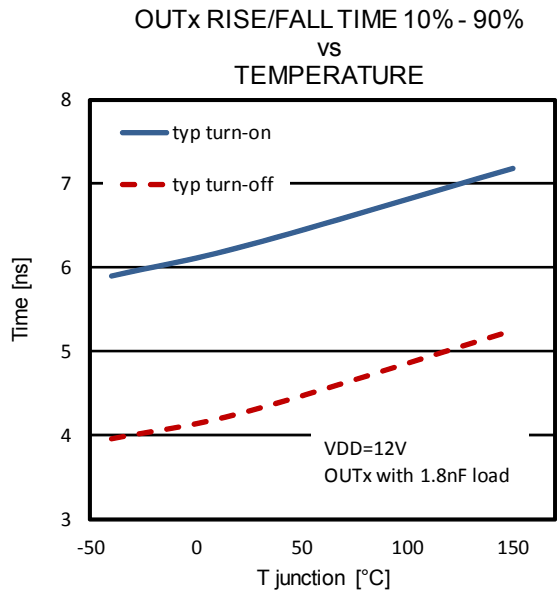


Figure 14 Rise / Fall Times with Load on Output

Typical Characteristics

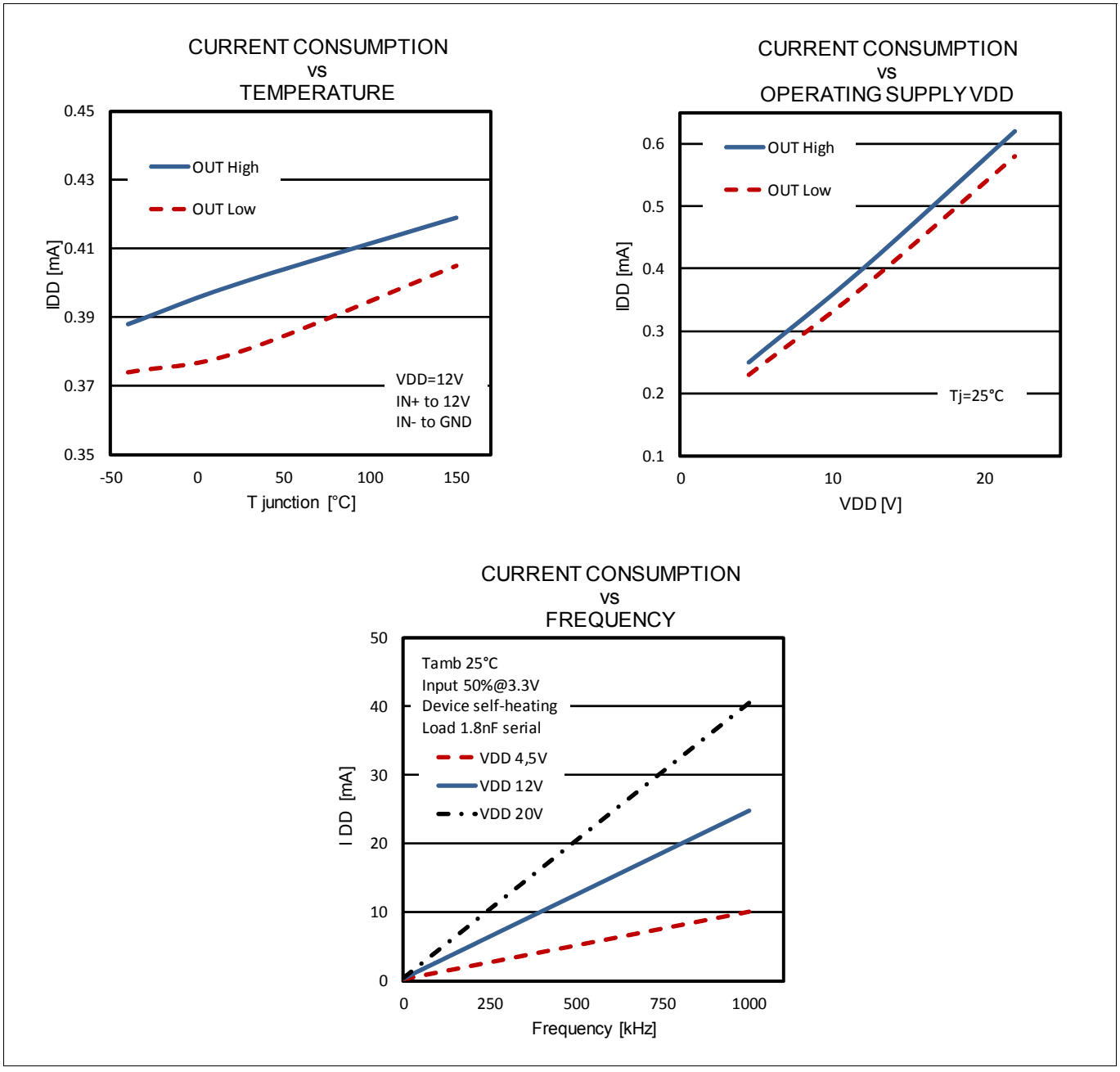


Figure 15 Power Consumption Related to Temperature, Voltage Supply and Frequency

Typical Characteristics

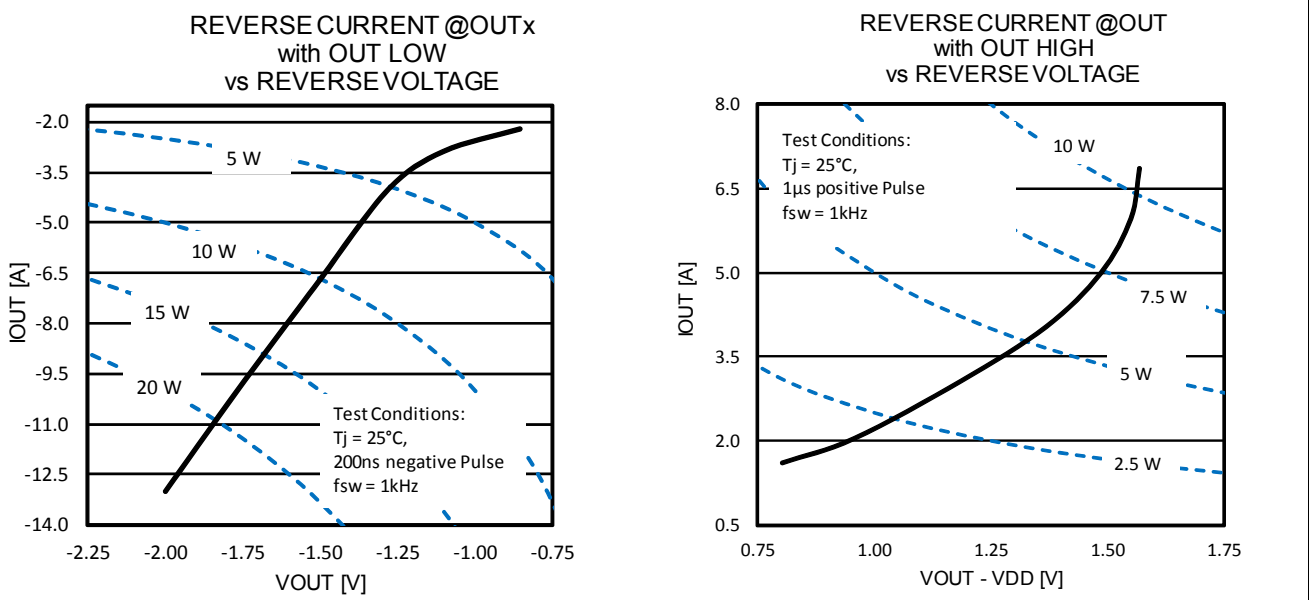
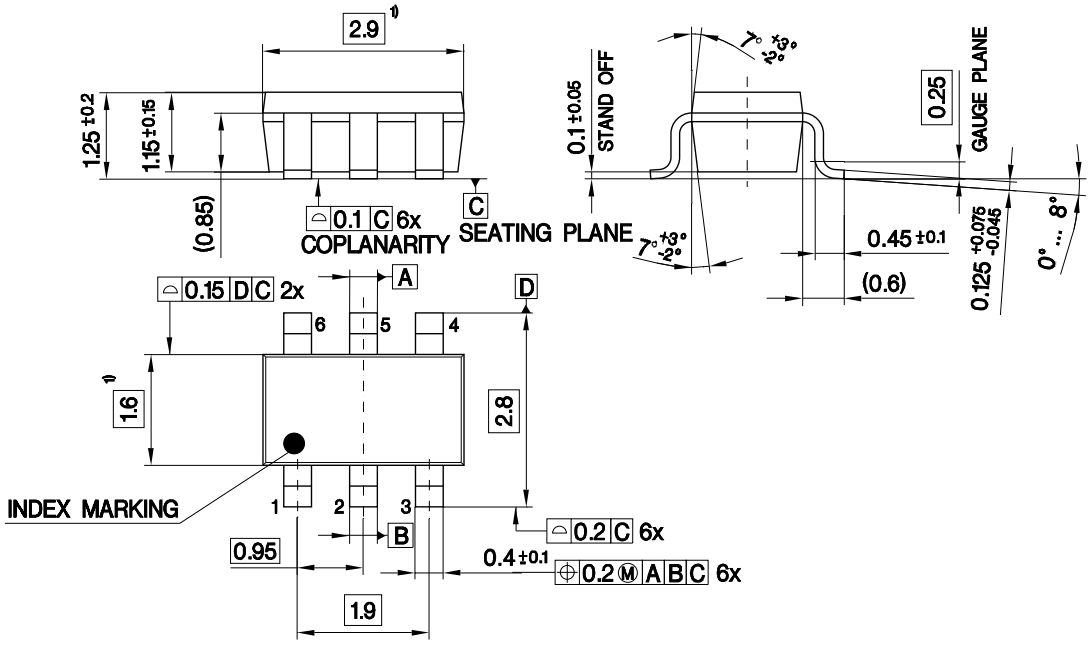


Figure 16 Output OUTx with reverse current and resulting power dissipation

8 Outline Dimensions



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

Figure 17 PG-SOT23-6-2 Outline Dimensions

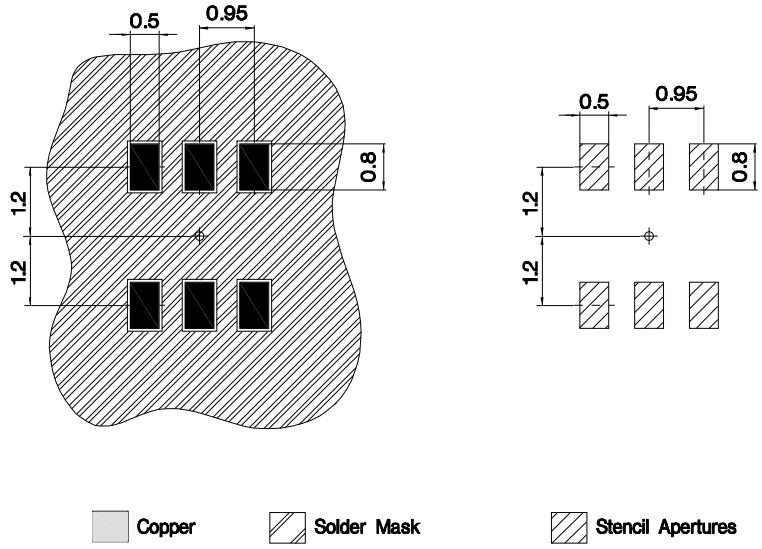


Figure 18 PG-SOT23-6-2 Footprint Dimensions

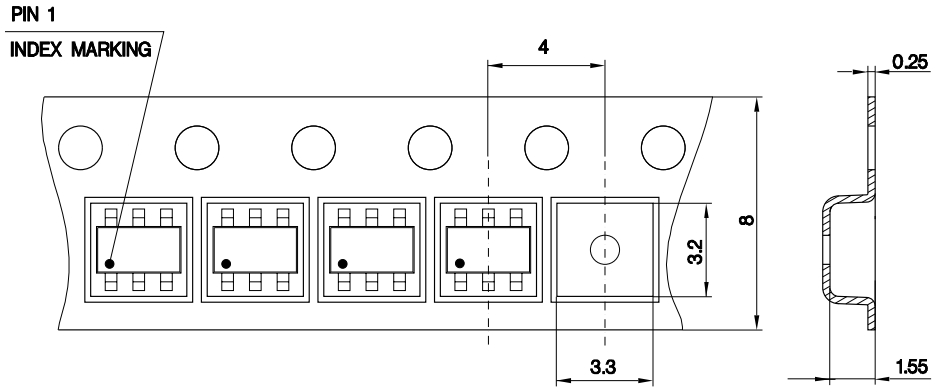


Figure 19 PG-SOT23-6-2 Packaging Dimensions

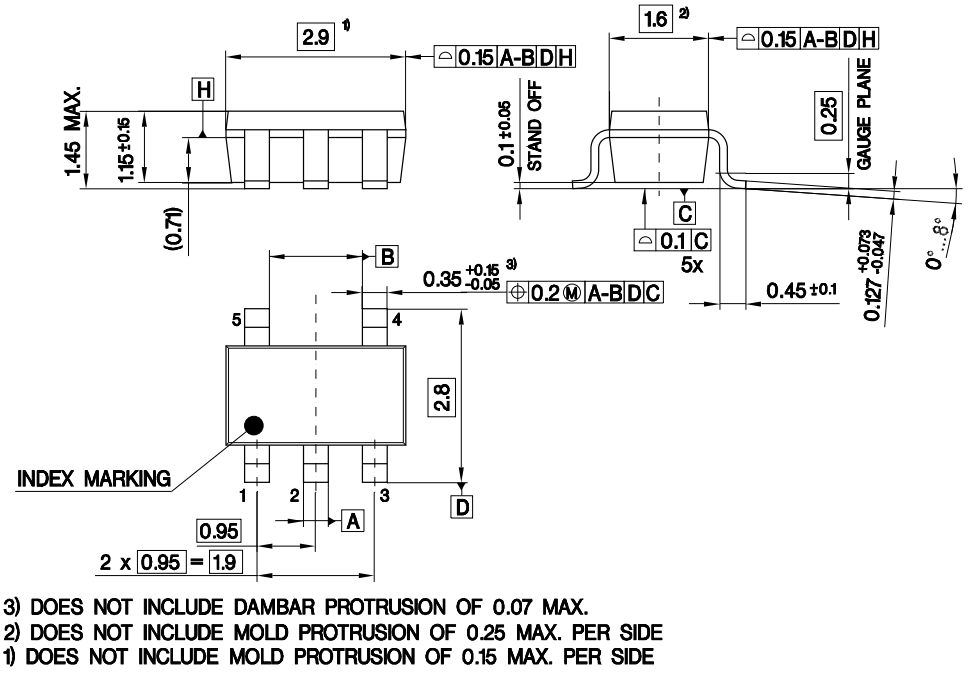


Figure 20 PG-SOT23-5-1 Outline Dimensions

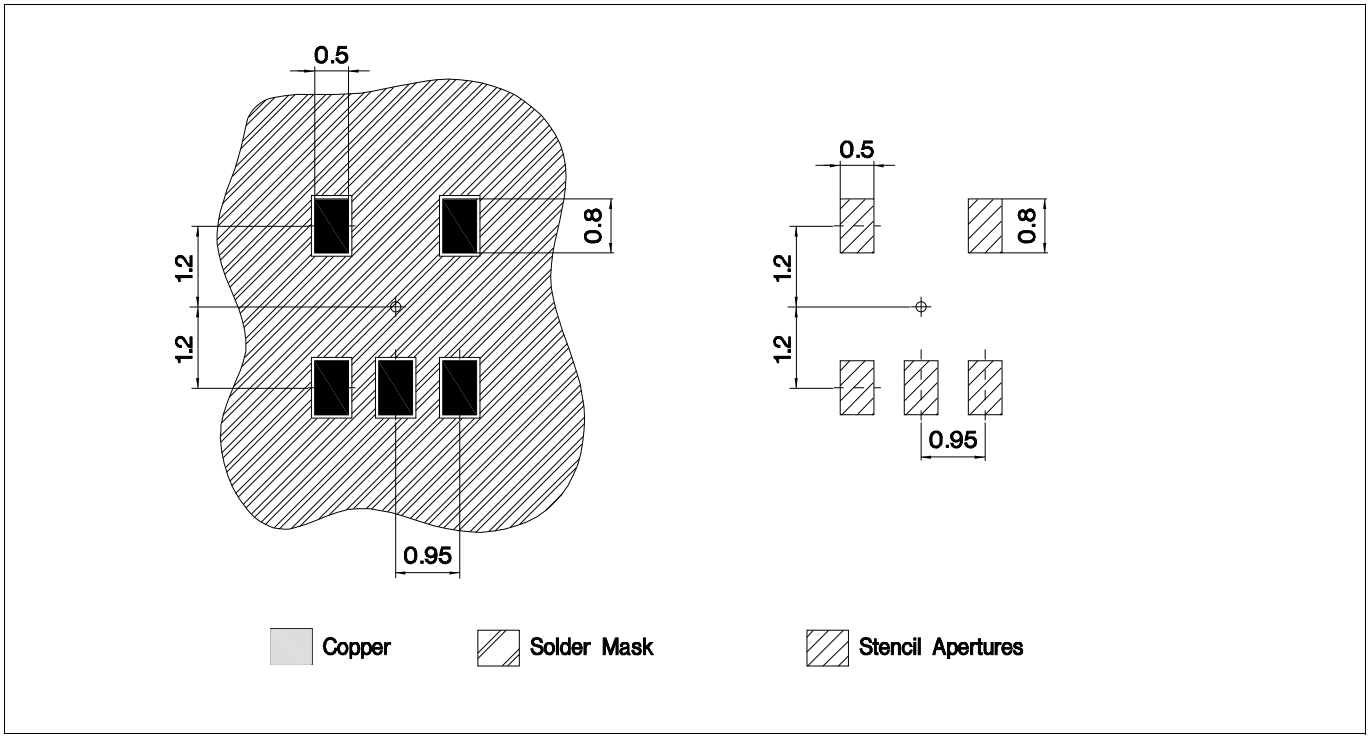


Figure 21 PG-SOT23-5-1 Footprint Dimensions

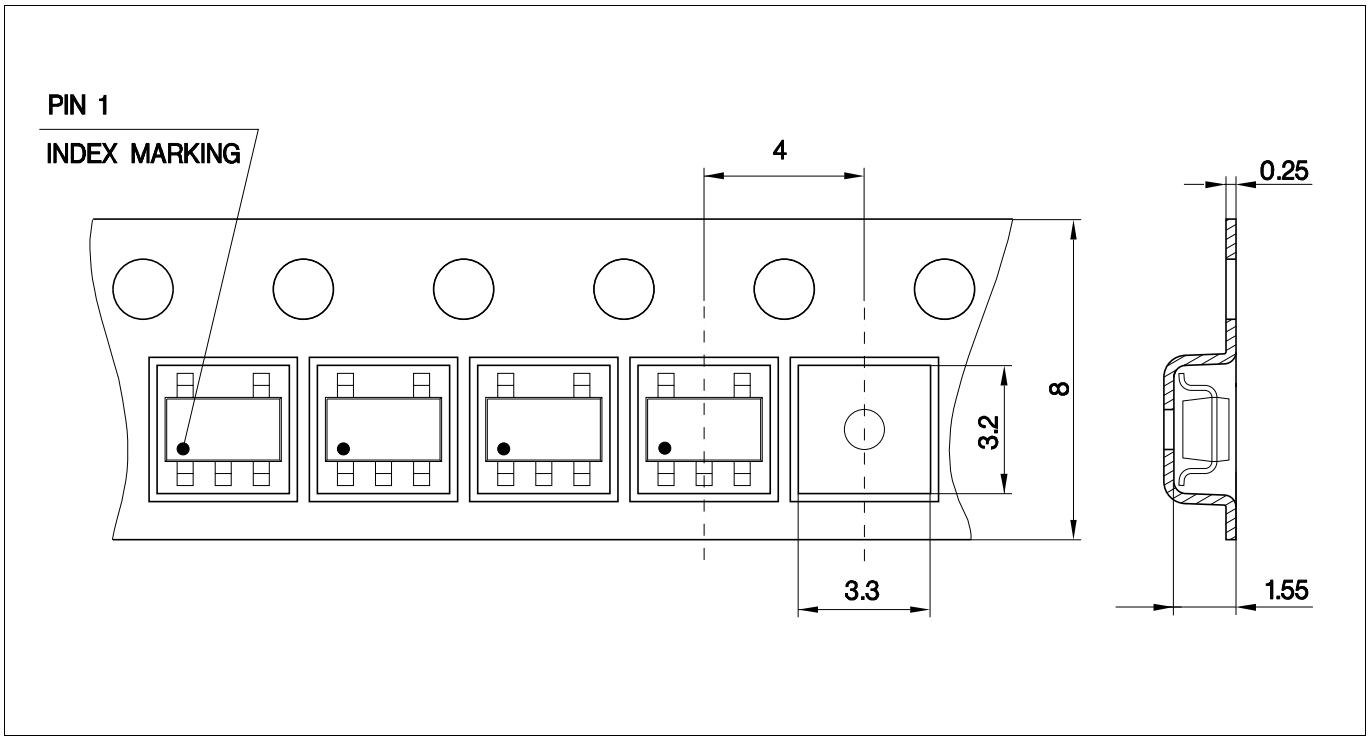


Figure 22 PG-SOT23-5-1 Packaging Dimensions

Outline Dimensions

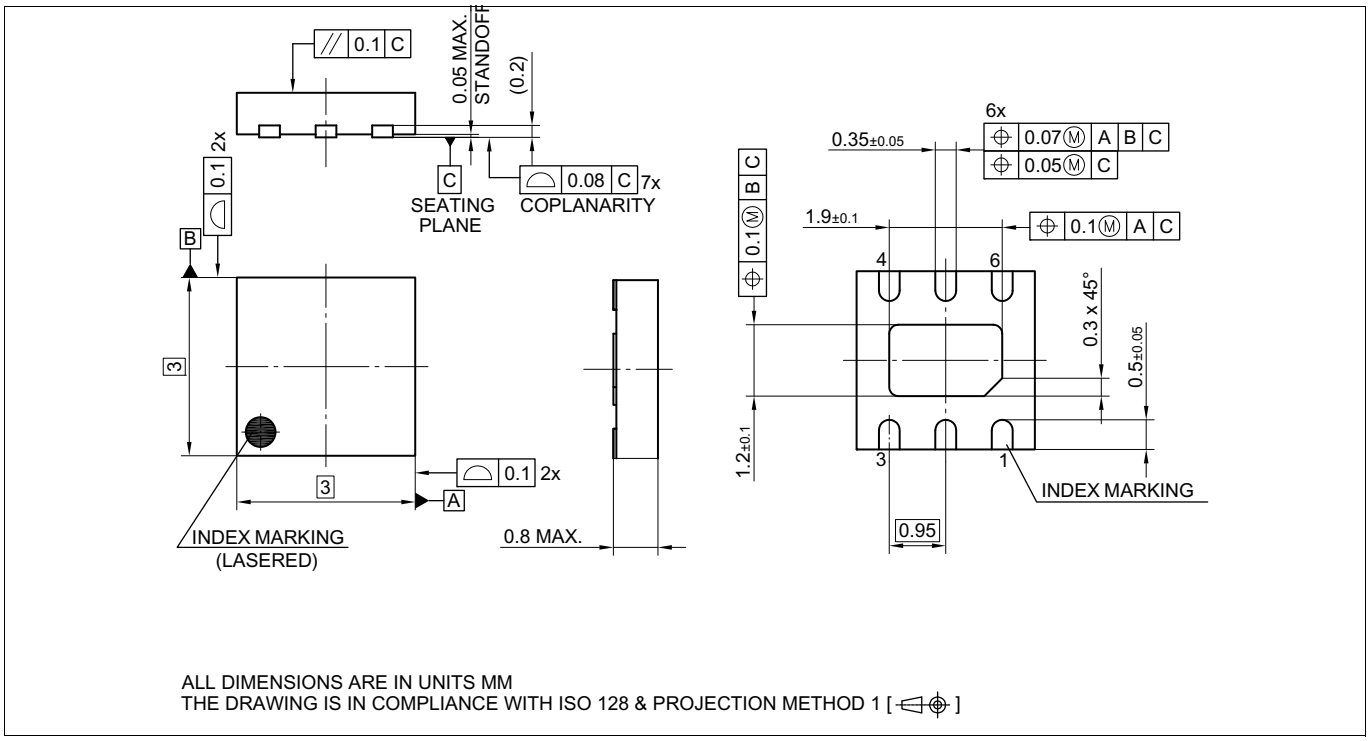


Figure 23 PG-WSON-6-1 Outline Dimensions

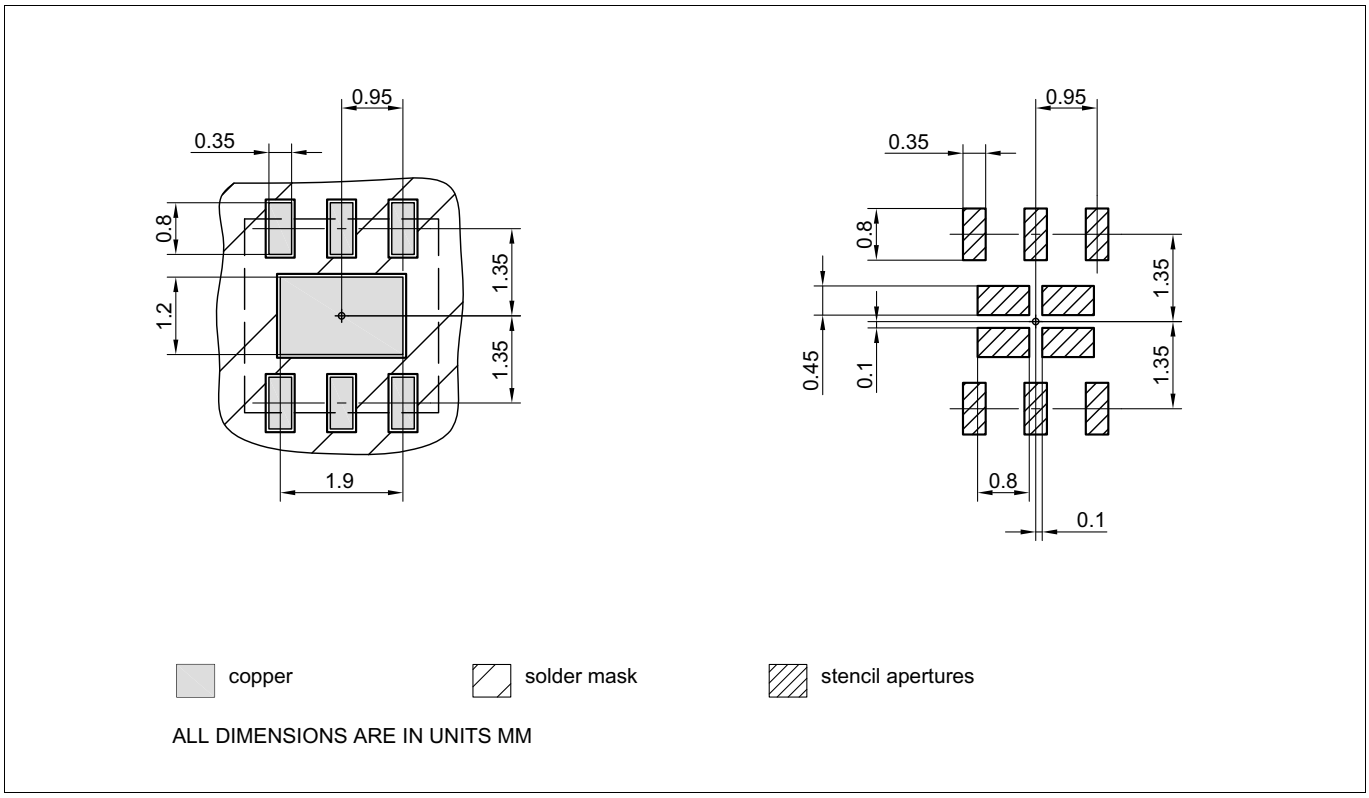


Figure 24 PG-WSON-6-1 Footprint Dimensions

Outline Dimensions

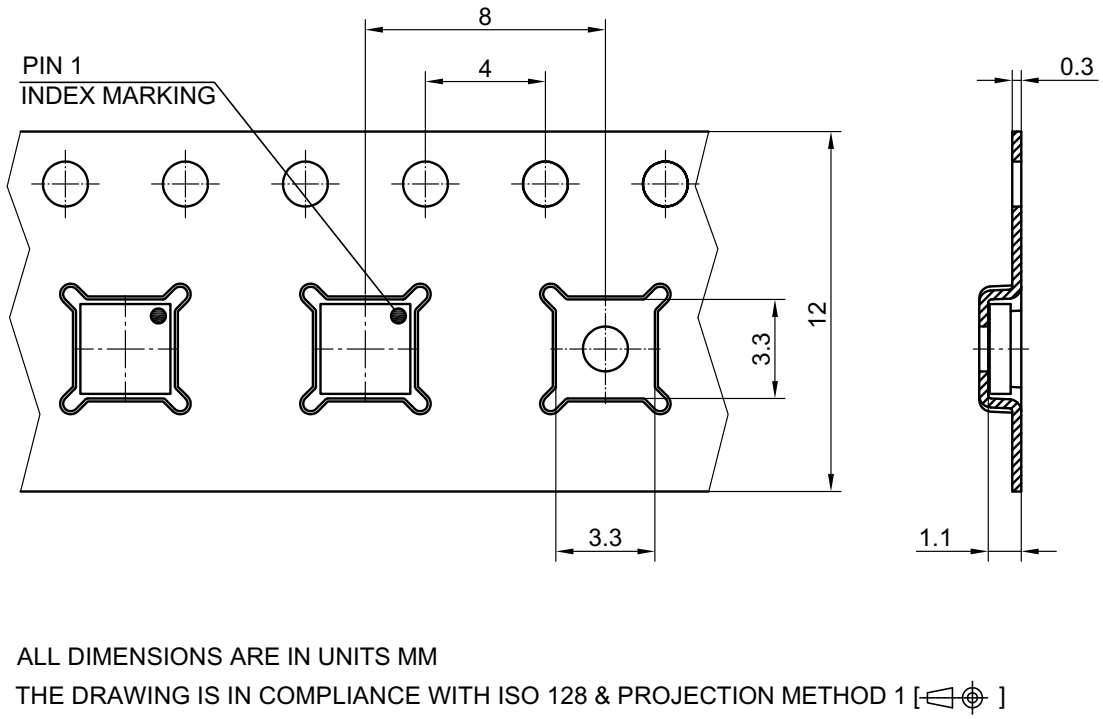


Figure 25 PG-WSON-6-1 Packaging Dimensions

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/cms/en/product/technology/packages/**.*
2. *Pin description and orientation is located in **Chapter 2**.*

9 Revision History

Page/ Item	Subjects (major changes since previous revision)	Responsible
Rev. 2.2, 2018-04-20		**Vincent Zhang**
26	**Updated package diagram**	
Rev. 2.1, 2017-10-02		**Tobias Gerber**
	Updated from version 1.0	
15	Symbols correction Ron_SRC, Ron_SNK, ISRC_peak, ISNK_Peak : **Table 12**	
15	Adding max. and min. values of Ron_SRC, Ron_SNK: **Table 12**	
16	Insert pulse timing diagram: **Figure 9**	
23	Restructured dimensional tolerances in drawing: **Figure 20**	

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