EN - For pricing and availability in your local country please visit one of the below links:

DE - Informationen zu Preisen und Verfügbarkeit in Ihrem Land erhalten Sie über die unten aufgeführten Links:

FR - Pour connaître les tarifs et la disponibilité dans votre pays, cliquez sur l'un des liens suivants:

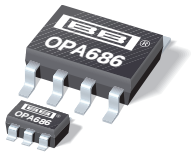
OPA686U

EN
This Datasheet is presented by the manufacturer

DE
Dieses Datenblatt wird vom Hersteller bereitgestellt

FR
Cette fiche technique est présentée par le fabricant

BURR-BROWN®



OPA686

For most current data sheet and other product information, visit www.burr-brown.com

SpeedPLUS™ Wideband, Low Noise, Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- HIGH BANDWIDTH: 250MHz (G = +10)
- LOW INPUT VOLTAGE NOISE: 1.3nV/√Hz
- VERY LOW DISTORTION: –90dBc (5MHz)
- HIGH SLEW RATE: 600V/µs
- HIGH DC ACCURACY
- LOW SUPPLY CURRENT: 12mA
- HIGH GAIN BANDWIDTH PRODUCT: 1600MHz
- STABLE FOR GAINS ≥ 7

APPLICATIONS

- HIGH DYNAMIC RANGE ADC PREAMP
- LOW NOISE, WIDEBAND, TRANSIMPEDANCE AMPLIFIER
- WIDEBAND, HIGH GAIN AMPLIFIER
- LOW NOISE DIFFERENTIAL RECEIVER
- VDSL LINE RECEIVER
- ULTRASOUND CHANNEL AMPLIFIER
- IMPROVED REPLACEMENT FOR THE CLC425

DESCRIPTION

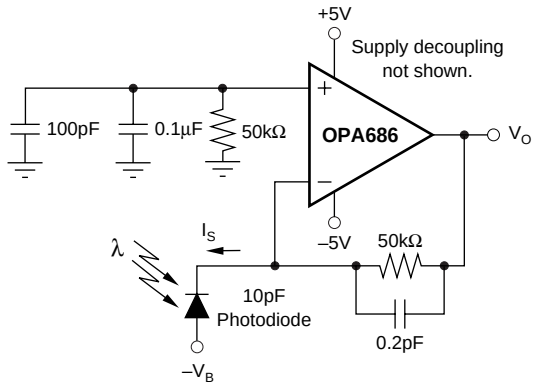
The OPA686 combines very high gain bandwidth and large signal performance with very low input voltage noise while dissipating a low 12mA supply current. The classical differential input stage, along with two stages of forward gain and a high power output stage, combine to make the OPA686 an exceptionally low distortion amplifier with excellent DC accuracy and output drive. The voltage feedback architecture allows all standard op amp applications to be implemented with very high performance.

The combination of low input voltage and current noise, along with a 1.6GHz gain bandwidth product, make the OPA686 an ideal amplifier for wideband transimpedance stages. As a voltage gain stage, the OPA686 is optimized for a flat response at a gain of +10 and is guaranteed stable down to a noise gain of +7.

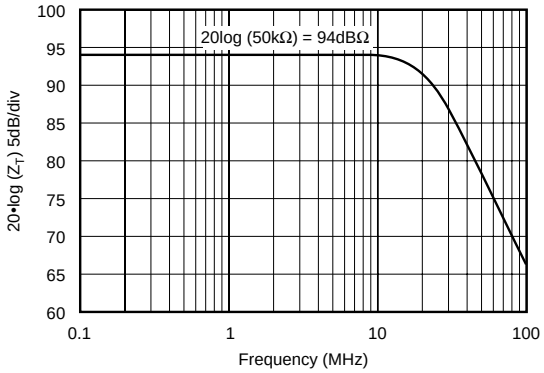
A new external compensation technique can be used to give a very flat frequency response below the minimum stable gain for the OPA686, further improving its already exceptional distortion performance. Using this compensation makes the OPA686 one of the premier 12- to 14-bit analog-to-digital converter input drivers. The supply current for the OPA686 is precisely trimmed to 12.4mA at +25°C. This, along with carefully defined supply current tempcos in the input and output stages, combine to provide exceptional performance over the full specified temperature range.

OPA686 RELATED PRODUCTS

SINGLES	DUALS	INPUT NOISE VOLTAGE (nV/√Hz)	GAIN BANDWIDTH PRODUCT (MHz)
OPA643		2.3	800
	OPA2686	1.3	1600
OPA687		0.95	3600



High Gain, 20MHz Transimpedance Amplifier



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS: $V_S = \pm 5V$

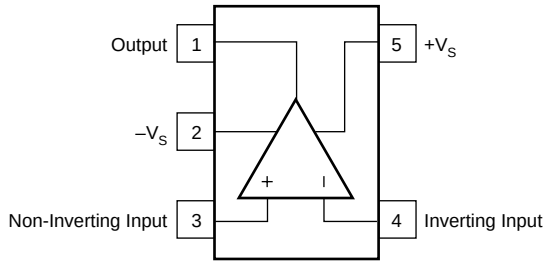
$R_F = 453\Omega$, $R_L = 100\Omega$, and G =+10, unless otherwise noted. Figure 1 for AC performance.

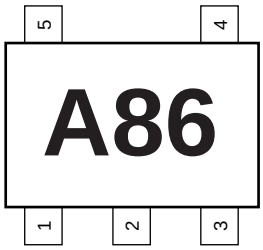
PARAMETER	CONDITIONS	OPA686U, N						
		TYP	GUARANTEED					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (Figure 1)								
Closed-Loop Bandwidth	G = +7, $R_G = 50\Omega$, V_O = 200mVp-p	425				MHz	typ	C
	G = +10, $R_G = 50\Omega$, V_O = 200mVp-p	250	200	170	140	MHz	min	B
	G = +20, $R_G = 50\Omega$, V_O = 200mVp-p	100	80	65	55	MHz	min	B
Gain Bandwidth Product	G ≥ +40	1600	1250	1100	1000	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +10, $R_L = 100\Omega$, V_O = 200mVp-p	40	35	30	25	MHz	min	B
Peaking at a Gain of +7		2				dB	typ	C
Harmonic Distortion	G = +10, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	$R_L = 100\Omega$	–72	–67	–65	–60	dBc	max	B
	$R_L = 500\Omega$	–90	–85	–80	–75	dBc	max	B
3rd Harmonic	$R_L = 100\Omega$	–95	–90	–85	–80	dBc	max	B
	$R_L = 500\Omega$	–110	–105	–100	–95	dBc	max	B
Two-Tone, 3rd-Order Intercept	G = +10, f = 10MHz	43	40	39	37	dBm	min	B
Input Voltage Noise	f > 1MHz	1.3	1.5	1.6	1.7	nV/√Hz	max	B
Input Current Noise	f > 1MHz	1.8	2.3	2.4	2.5	pA/√Hz	max	B
Rise/Fall Time	0.2V Step	1.4	1.75	2	2.5	ns	max	B
Slew Rate	2V Step	600	500	400	310	V/µs	min	B
Settling Time to 0.01%	2V Step	18				ns	typ	C
0.1%	2V Step	16	14	21	25	ns	max	B
1%	2V Step	11	12	14	18	ns	max	B
Differential Gain	G = +10, NTSC, $R_L = 150\Omega$	0.02				%	typ	C
Differential Phase	G = +10, NTSC, $R_L = 150\Omega$	0.02				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	80	**75**	70	70	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.35	**±1.0**	±1.2	±1.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			5	10	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–10	**–17**	–18	–20	µA	max	A
Input Bias Current Drift	V_{CM} = 0V			50	100	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.5	**±1.0**	±1.5	±1.8	µA	max	A
Input Offset Current Drift	V_{CM} = 0V			5	10	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.2	**±3.0**	±2.9	±2.8	V	min	A
Common-Mode Rejection (CMR)	V_{CM} = ±1V, Input Referred	100	**90**	85	75	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0V	6 || 2				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	2.9 || 1				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	≥ 400Ω Load	±3.5	**±3.2**	±3.1	±3.0	V	min	A
	100Ω Load	±3.3	**±3.0**	±2.8	±2.8	V	min	A
Current Output, Sourcing	V_O = 0V	80	**60**	55	50	mA	min	A
Current Output, Sinking	V_O = 0V	–80	**–60**	–55	–40	mA	min	A
Closed-Loop Output Impedance	G = +10, f = 100kHz	0.008				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Max Quiescent Current	V_S = ±5V	12.4	**12.9**	13	13.9	mA	max	A
Min Quiescent Current	V_S = ±5V	12.4	**11.9**	11.9	11	mA	min	A
Power Supply Rejection Ratio								
+PSRR, –PSRR	$\|V_S\|$ = 4.5 to 5.5, Input Referred	78	**70**	70	65	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: U, N Package		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U 8-Pin, SO-8		125				°C/W	typ	C
N 5-Pin, SOT23		150				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ±CMIR limits.

PIN CONFIGURATIONS

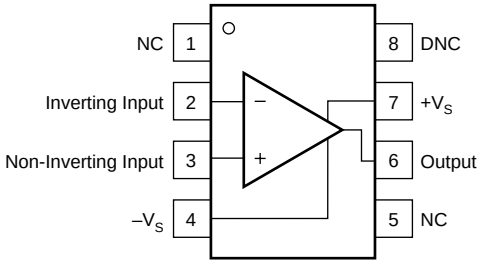
Top View **SOT23-5**





Pin Orientation/Package Marking

Top View **SO-8**



DNC: Do Not Connect
NC: No Connection

ABSOLUTE MAXIMUM RATINGS

Power Supply	±6.5V$_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Voltage Range	±V$_S$
Storage Temperature Range: U, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T$_J$)	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
OPA686U	SO-8 Surface Mount	182	–40°C to +85°C	OPA686U	OPA686U	Rails
"	"	"	"	"	OPA686U/2K5	Tape and Reel
OPA686N	5-Lead SOT23-5	331	–40°C to +85°C	A86	OPA686N/250	Tape and Reel
"	"		"	"	OPA686N/3K	Tape and Reel

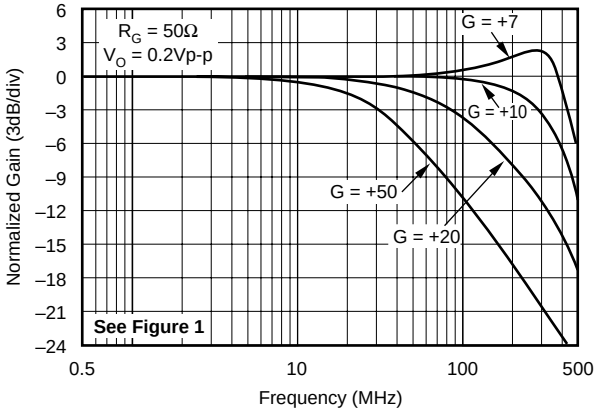
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA686U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

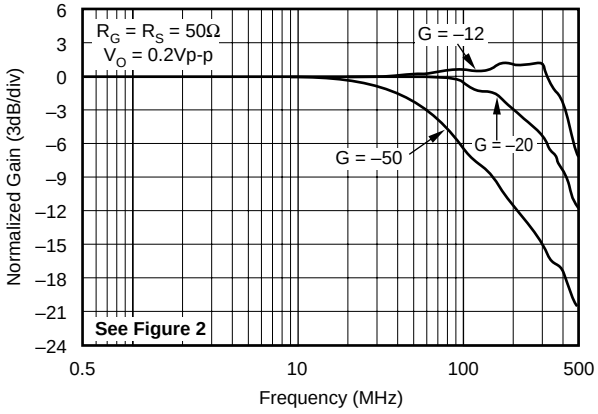
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

At T_A = +25°C, G = +10, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted.

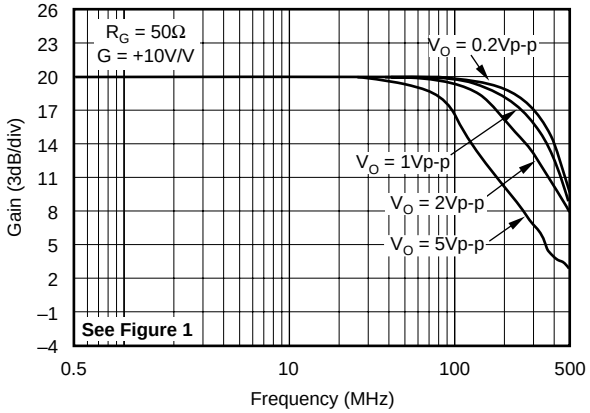
NON-INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



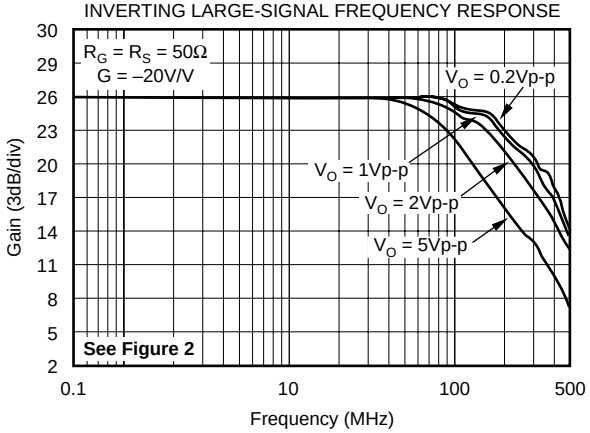
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



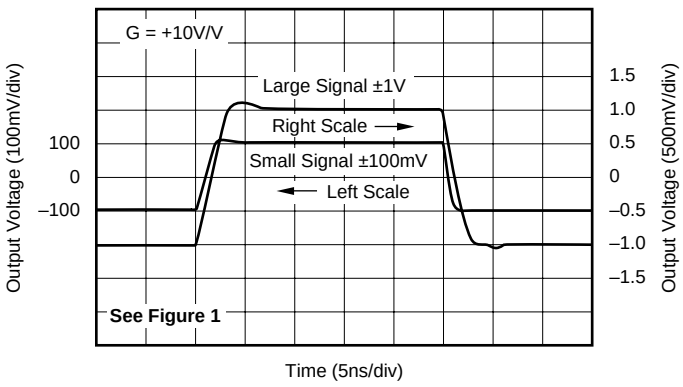
NON-INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



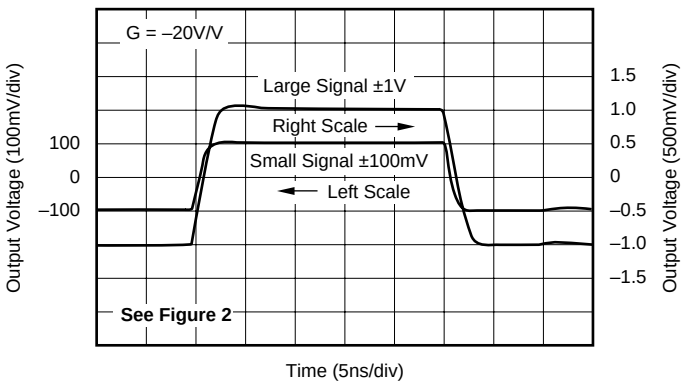
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NON-INVERTING PULSE RESPONSE



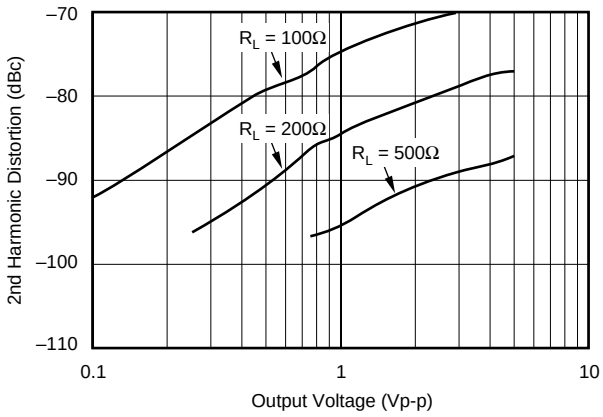
INVERTING PULSE RESPONSE



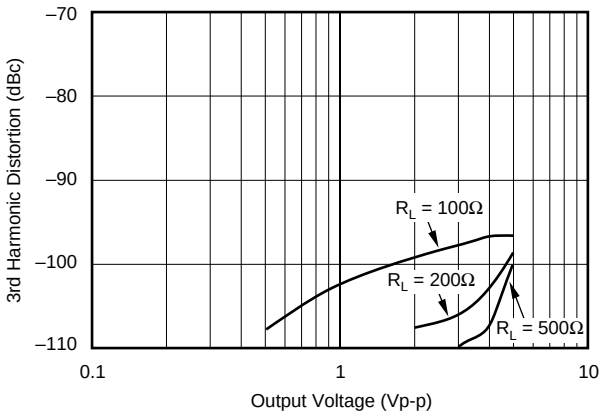
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (CONT)

At T_A = +25°C, G = +10, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1.

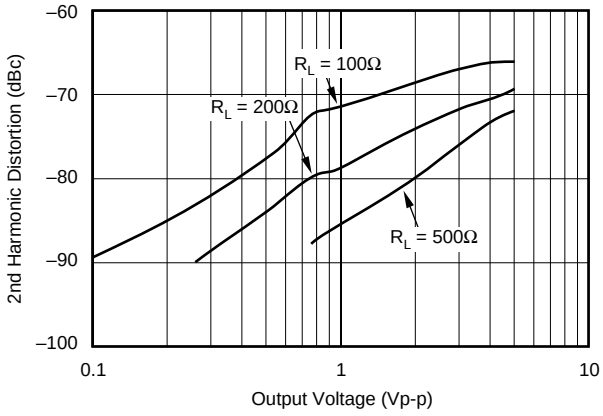
5MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



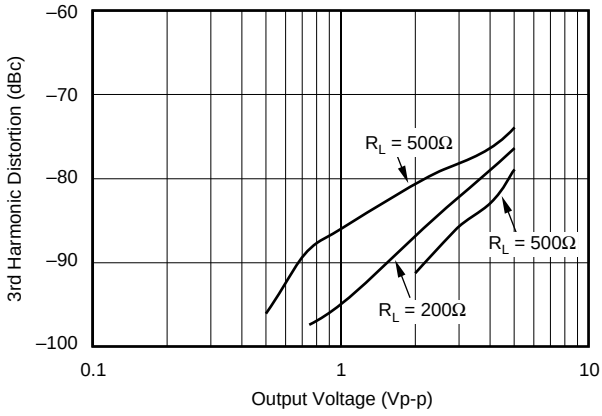
5MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE



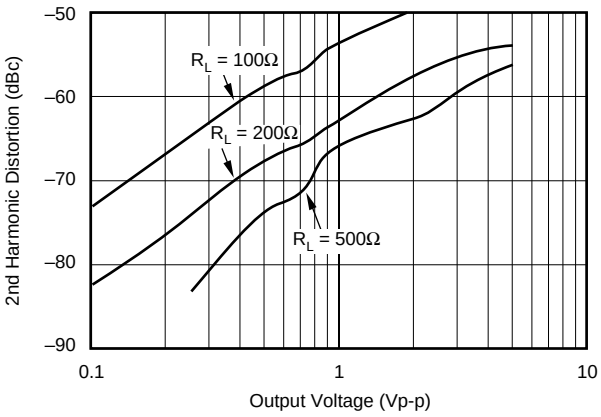
10MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



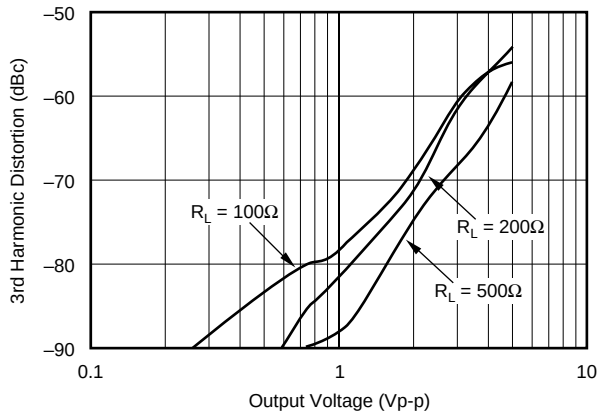
10MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE



20MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



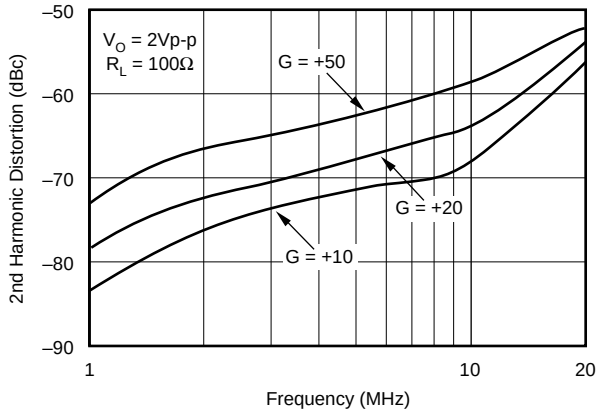
20MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE



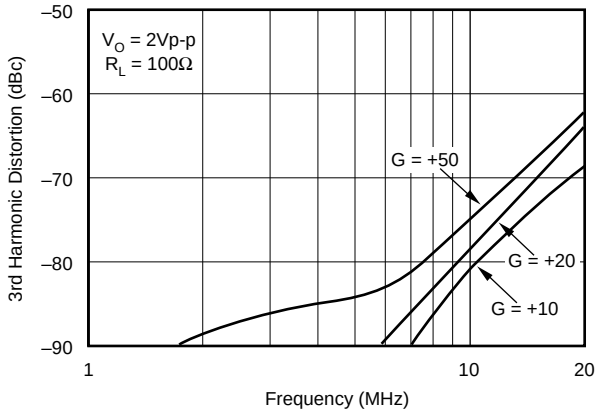
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

At T_A = +25°C, G = +10, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1.

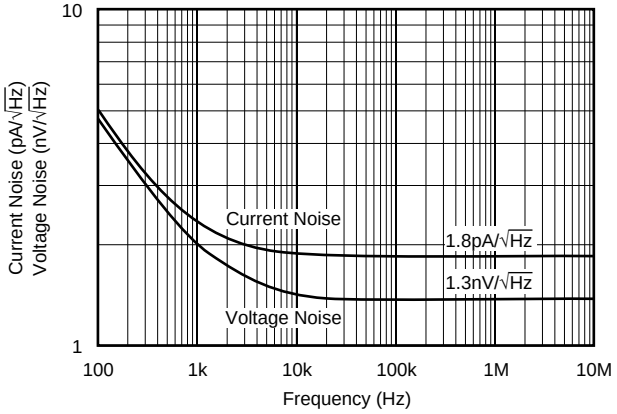
2nd HARMONIC DISTORTION vs FREQUENCY



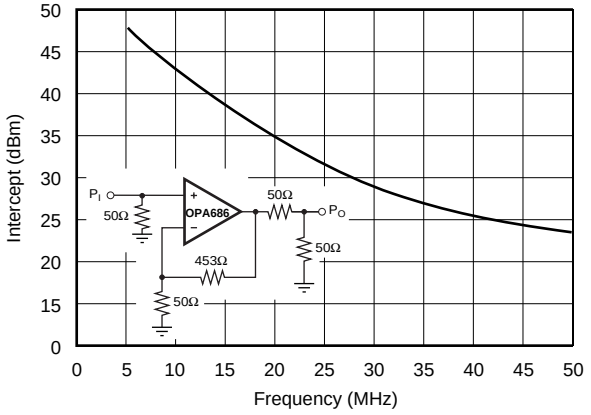
3rd HARMONIC DISTORTION vs FREQUENCY



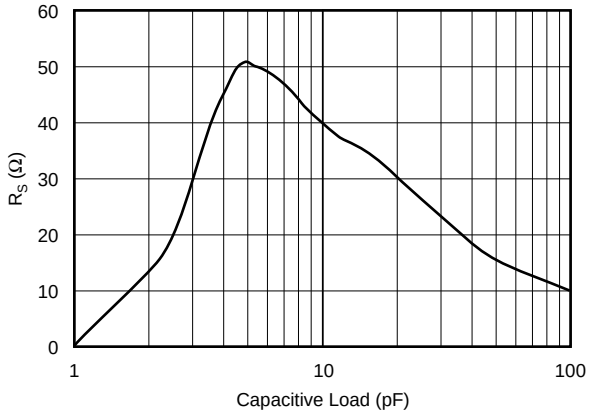
INPUT VOLTAGE and CURRENT NOISE DENSITY



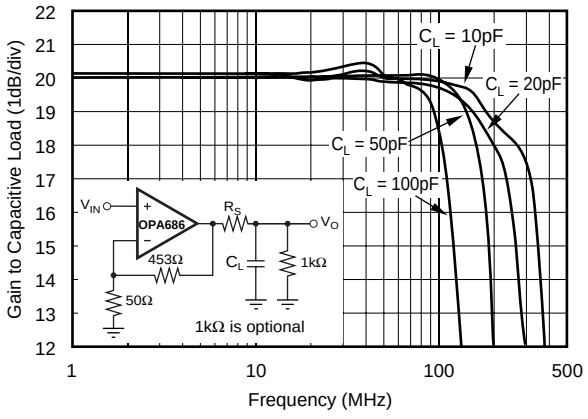
TWO-TONE, 3rd-0RDER INTERMODULATION INTERCEPT vs FREQUENCY



R_S vs CAPACITIVE LOAD



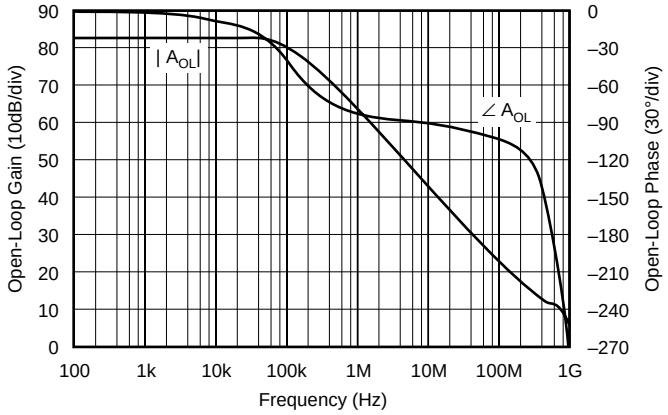
FREQUENCY RESPONSE vs CAPACITIVE LOAD



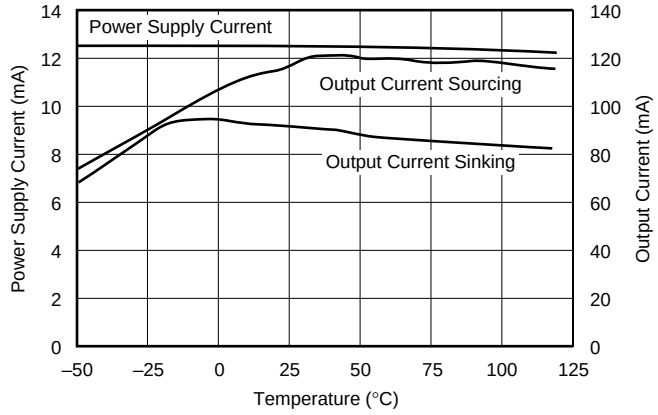
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (CONT)

At T_A = +25°C, G = +10, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1.

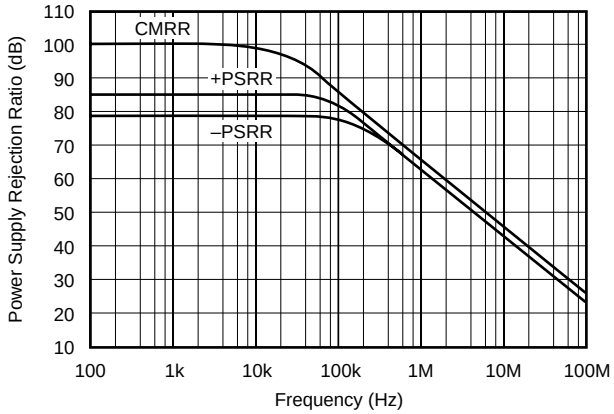
OPEN-LOOP GAIN and PHASE



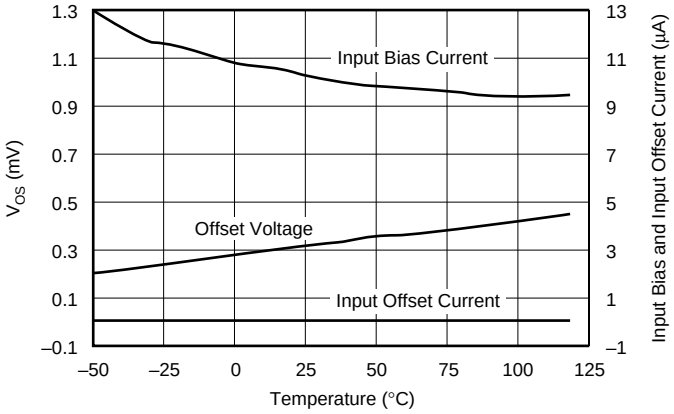
POWER SUPPLY and OUTPUT CURRENT vs TEMPERATURE



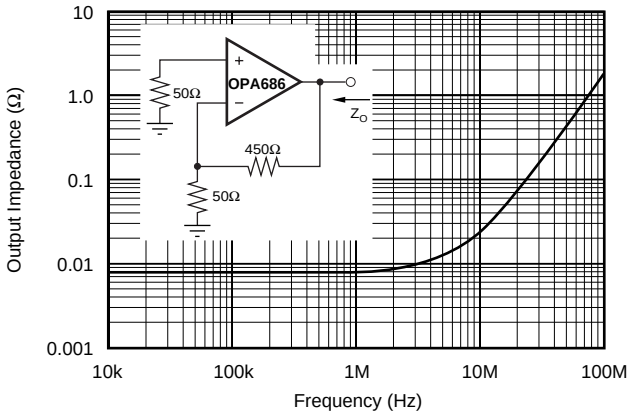
CMRR and PSRR



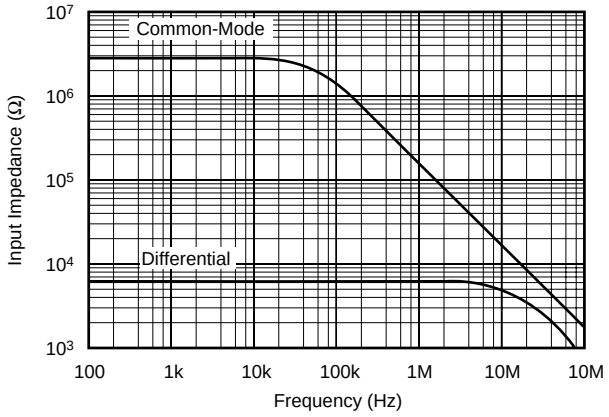
INPUT DC ERRORS vs TEMPERATURE



CLOSED-LOOP OUTPUT IMPEDANCE



DIFFERENTIAL and COMMON-MODE INPUT IMPEDANCE



APPLICATIONS INFORMATION

WIDEBAND, NON-INVERTING OPERATION

The OPA686 provides a unique combination of features—low input voltage noise along with a very low distortion output stage—to give one of the highest dynamic range op amps available. Its very high Gain Bandwidth Product (GBP) can be used either to deliver high signal bandwidths at high gains, or to deliver very low distortion signals at moderate frequencies and lower gains. To achieve the full performance of the OPA686, careful attention to PC board layout and component selection is required as discussed in the remaining sections of this data sheet.

Figure 1 shows the non-inverting gain of +10 circuit used as the basis of the Electrical Specifications and most of the Typical Performance Curves. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1), while output power (dBm) specifications are at the matched 50Ω load. The total 100Ω load at the output, combined with the 503Ω total feedback network load, presents the OPA686 with an effective output load of 83Ω for the circuit of Figure 1.

Voltage feedback op amps, unlike current feedback designs, can use a wide range of resistor values to set their gain. The circuit of Figure 1, and the specifications at other gains, use the constraint that R_G should always be set to 50Ω and R_F adjusted to get the desired gain. Using this guideline will guarantee that the noise added at the output due to Johnson noise of the resistors will not significantly increase the total noise over that due to the 1.3nV/$\sqrt{Hz}$ input voltage noise for the op amp itself.

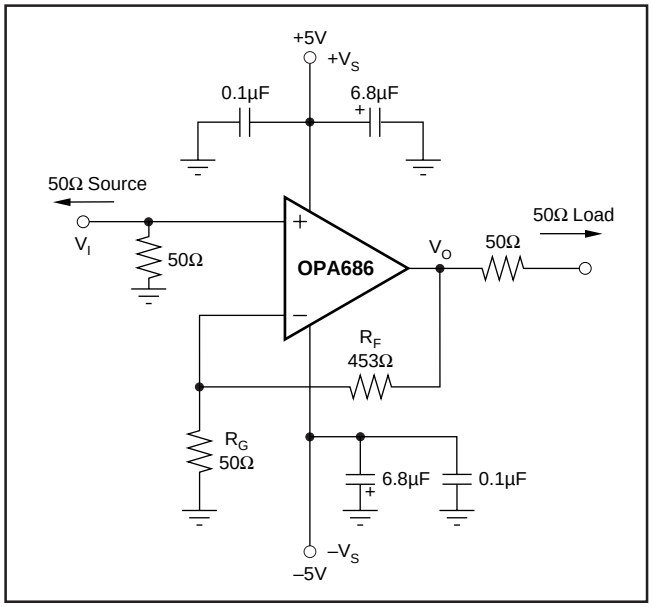


FIGURE 1. Non-Inverting, G = +10 Specification and Test Circuit.

WIDEBAND, INVERTING GAIN OPERATION

Operating the OPA686 as an inverting amplifier has several benefits and is particularly appropriate when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as the basis of the inverting mode Typical Performance Curves.

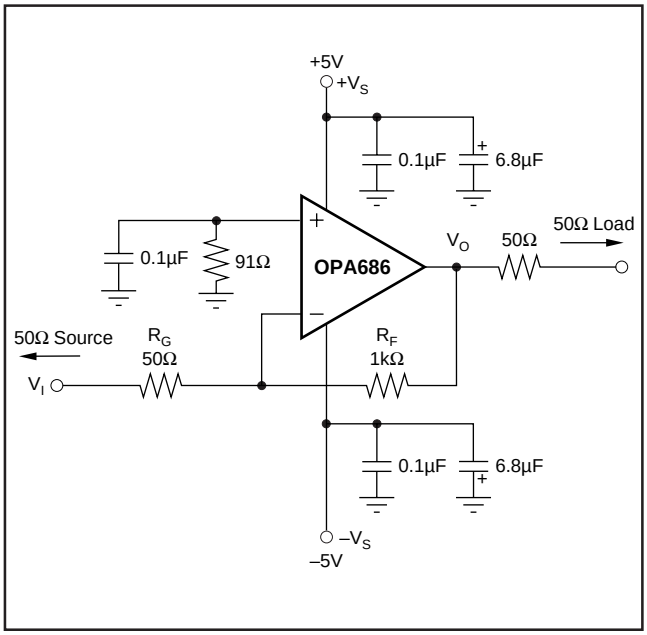


FIGURE 2. Inverting, G = –20 Characterization Circuit.

Driving this circuit from a 50Ω source, and constraining the gain resistor (R_G) to equal 50Ω, will give both a signal bandwidth and noise advantage. R_G acts as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain (V_O/V_I) for the circuit of Figure 2 is double that for Figure 1, the noise gains are in fact equal when the 50Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP of the amplifier. This can be seen in comparing the G = +10 and G = –20 small-signal frequency response curves. Both show approximately 250MHz bandwidth, but the inverting configuration of Figure 2 gives 6dB higher signal gain. If the signal source is actually the low impedance output of another amplifier, R_G should be increased to the minimum load resistance value allowed for that amplifier and R_F should be adjusted to achieve the desired gain. For stable operation of the OPA686, it is critical that this driving amplifier show a very low output impedance at frequencies beyond the expected closed-loop bandwidth for the OPA686.

WIDEBAND, HIGH SENSITIVITY, TRANSIMPEDANCE DESIGN

The high Gain Bandwidth Product (GBP) and the low input voltage and current noise for the OPA686 make it an ideal wideband transimpedance amplifier for low to moderate transimpedance gains. Very high transimpedance gains (> 100kΩ) will benefit from the low input noise current of a FET-input op amp such as the OPA655. Unity gain stability in the op amp is not required for application as a

transimpedance amplifier. One transimpedance design example is shown on the front page of the data sheet. Designs that require high bandwidth from a large area (high capacitance) detector with relatively low transimpedance gain will benefit from the low input voltage noise offered by the OPA686. This input voltage noise will be peaked up over frequency at the output by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements of the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain, R_F, and the GBP of the OPA686 (1600MHz). Figure 3 shows a design using a 50pF source capacitance diode and a 10kΩ transimpedance gain. With these three variables set (and including the parasitic input capacitance for the OPA686 added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response.

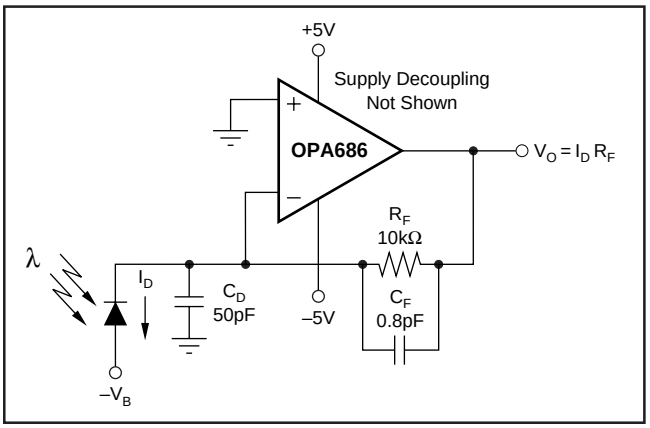


FIGURE 3. Wideband, Low Noise, Transimpendance Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$1/(2\pi R_F C_F) = \sqrt{(GBP/(4\pi R_F C_D))}$$

Adding the common-mode and differential mode input capacitance (1.0 + 2.0)pF to the 50pF diode source capacitance of Figure 3, and targeting a 10kΩ transimpedance gain using the 1600MHz GBP for the OPA686, will require a feedback pole set to 15.5MHz. This will require a total feedback capacitance of 1.0pF. Typical surface-mount resistors have a parasitic capacitance of 0.2pF, leaving the required 0.8pF value shown in Figure 3 to get the required feedback pole.

This will give an approximate –3dB bandwidth equal to:

$$f_{-3dB} = \sqrt{(GBP/2\pi R_F C_D)}Hz$$

The example of Figure 3 will give approximately 23MHz flat bandwidth using the 0.8pF feedback compensation.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent input noise current can be derived as:

$$I_{EQ} = \sqrt{I_N^2 + \frac{4kT}{R_F} + \left(\frac{E_N}{R_F}\right)^2 + \frac{\left(E_N 2\pi C_D F\right)^2}{3}}$$

Where:

I_{EQ} = Equivalent input noise current if the output noise is bandlimited to $F < 1/(2\pi R_F C_D)$

I_N = Input current noise for the op amp inverting input

E_N = Input voltage noise for the op amp

C_D = Diode capacitance

F = Bandlimiting frequency in Hz (usually a post filter prior to further signal processing)

Evaluating this expression up to the feedback pole frequency at 15.5MHz for the circuit of Figure 3, gives an equivalent input noise current of 6.4pA/√Hz. This is much higher than the 1.8pA/√Hz for just the op amp itself. This result is being dominated by the last term in the equivalent input noise expression. It is essential in this case to use a low voltage noise op amp. For example, if a slightly higher input noise voltage, but otherwise identical op amp were used instead of the OPA686 in this application (say 2.0nV/√Hz), the total input-referred current noise would increase to 9.5pA/√Hz.

LOW GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA686 while giving increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability while giving an easily controlled second-order low pass frequency response. Considering only the noise gain (non-inverting signal gain) for the circuit of Figure 4, the low frequency noise gain, (NG_1) will be set by the resistor ratios while the high frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high frequency noise gain. If this noise gain, determined by $NG_2 = 1+C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole, set by $1/R_F C_F$, is placed correctly, a very well controlled, 2nd-order low pass frequency response will result.

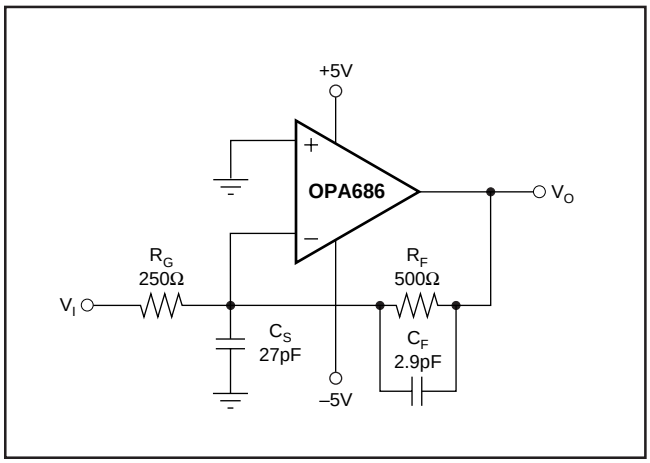


FIGURE 4. Broadband Low Gain Inverting External Compensation.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high frequency noise gain NG_2, which should be greater than the minimum stable gain for the OPA686. Here, a target NG_2 of 10.5 will be used. The second parameter is the desired low frequency signal gain, which also sets the low frequency noise gain NG_1. To simplify this discussion, we will target a maximally flat second-order low pass Butterworth frequency response (Q = 0.707). The signal gain of –2 shown in Figure 4 will set the low frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 3 in this example). Then, using only these two gains and the GBP for the OPA686 (1600MHz), the key frequency in the compensation can be determined as:

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right]$$

Physically, this Z_0 (10.6MHz for the values shown above) is set by $1/(2\pi \bullet R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0dB gain. The actual zero in the noise gain occurs at $NG_1 \bullet Z_0$ and the pole in the noise gain occurs at $NG_2 \bullet Z_0$. Since GBP is expressed in Hz, multiply Z_0 by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi \bullet R_F Z_O NG_2} \quad (= 2.86pF)$$

Finally, since C_S and C_F set the high frequency noise gain, determine C_S by [Using $NG_2 = 10.5$]:

$$C_S = (NG_2 - 1)\,C_F \qquad (= 27.2pF)$$

The resulting closed-loop bandwidth will be approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_O\ GBP} \qquad (= 130MHz)$$

For the values shown in Figure 4, the f_{-3dB} will be approximately 130MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_0$. The capacitor values shown in Figure 4 are calculated for $NG_1 = 3$ and $NG_2 = 10.5$ with no adjustment for parasitics.

Figure 5 shows the measured frequency response for the circuit of Figure 4. This shows the expected gain of –2 (6dB) with exceptional flatness through 70MHz and a –3dB bandwidth of 170MHz. Measured distortion into a 100Ω load shows > 5dB improvement through 20MHz over the performance shown in the Typical Performance Curves. Into a 500Ω load, the 5MHz, 2Vp-p, 2nd harmonic improves from –90dBc to –96dBc.

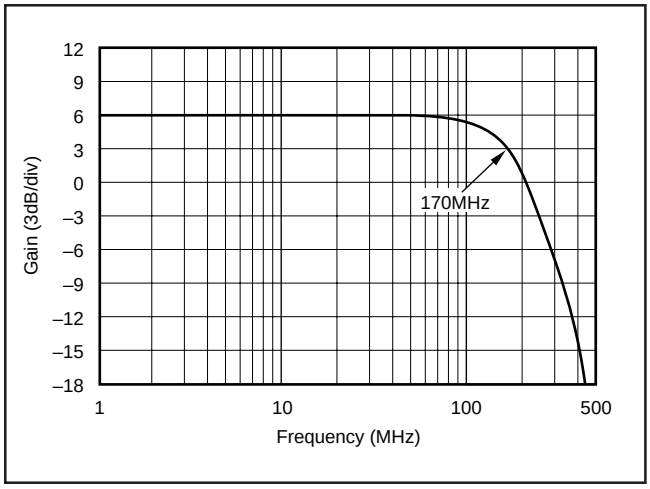


FIGURE 5. G = –2 Frequency Response with External Compensation.

LOW NOISE FIGURE, HIGH DYNAMIC RANGE "IF" AMPLIFIER

The low input noise voltage of the OPA686 and its high two-tone intercept can be used to good advantage as a fixed gain IF amplifier. While input noise figures in the 10dB range (for a matched 50Ω input) are easily achieved with just OPA686 alone, Figure 6 shows a technique which reduces the noise figure even further while providing a broadband, low gain IF amplifier stage using the OPA686.

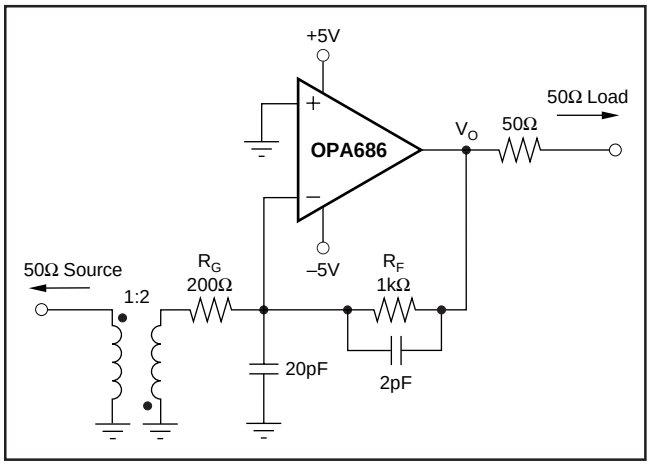


FIGURE 6. Low Noise Figure IF Amplifier.

Bringing the signal in through a step-up transformer to the inverting input gain resistor has several advantages for the OPA686. First, grounding the non-inverting input eliminates the contribution of the non-inverting input current noise to the output noise. Secondly, the non-inverting input voltage noise of the op amp is actually attenuated if reflected to the input side of R_G. Using the 1:2 (turns ratio) step up transformer reflects the 50Ω source impedance at

the primary through to the secondary as a 200Ω source impedance and likewise, the 200Ω R_G resistor is reflected through to the transformer primary as a 50Ω input matching impedance. The noise gain (NG) to the amplifier output is then 1+ 1000/400 = 3.5V/V. Taking the op amp's 1.3nV/$\sqrt{Hz}$ input voltage noise times this noise gain to the output, then reflecting this noise term to the input side of the R_G resistor, divides it by 5. This gives a net gain of 0.7 for the non-inverting input voltage noise when reflected to the input point for the op amp circuit. This is further reduced when referred back to the transformer primary.

The 14dB gain to the matched load for the circuit of Figure 6 is precisely controlled (±0.2dB) and gives a 6dB noise figure at the input of the transformer. The DC noise gain for this circuit (3.5) is below the specified minimum stable gain. This will improve the distortion performance at frequencies below 20MHz from those shown in the Typical Performance Curves. Adding the inverting compensation capacitors holds this configuration stable as described in the previous section. Measured results show 140MHz small-signal bandwidth for the circuit of Figure 6 with ±0.1dB flatness through 50MHz. The OPA686 will easily deliver a 2Vp-p ADC full-scale input at the matched 50Ω load. Two-tone testing at 20MHz for the circuit of Figure 6 (1Vp-p for each test tone) shows that the two-tone intermodulation intercept has improved to 40dBm versus the 35dBm shown in the Typical Performance Curves, giving a 72dBc SFDR for the two 4dBm test tones at the load .

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two PC boards are available to assist in the initial evaluation of circuit performance using the OPA686 in its two package styles. Both of these are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown in the table below.

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA686U	8-Pin SO-8	DEM-OPA68xU	MKT-351
OPA686N	5-Lead SOT23-5	DEM-OPA6xxN	MKT-348

Contact the Burr-Brown applications support line to request any of these boards.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA686 is available through either the Burr-Brown Internet web page (http://www.burr-brown.com) or as one model on a disk from the Burr-Brown Applications department (1-800-548-6132). The Applications department is also available for design assistance at this number. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA686 provides a very low input noise voltage while requiring a low 12mA quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 7 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

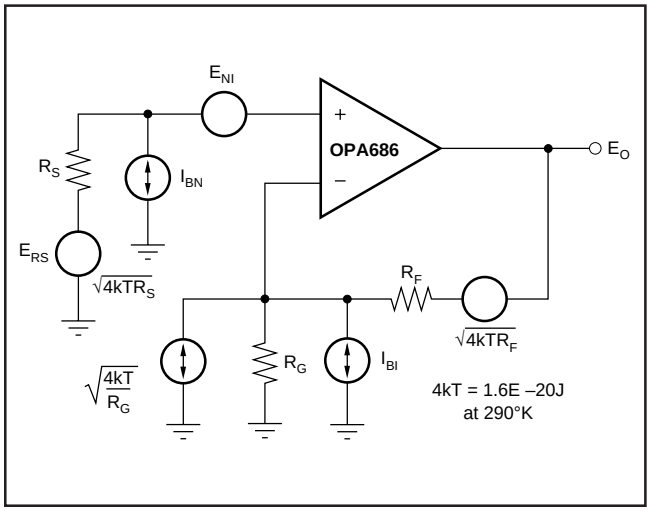


FIGURE 7. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then takes the square root to get back to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 7.

Equation 1

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = 1+R_F/R_G) will give the equivalent input-referred spot noise voltage at the non-inverting input as shown in Equation 2.

Equation 2

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Inserting high resistor values into Eq. 2 can quickly dominate the total equivalent input referred noise. A 105Ω source impedance on the non-inverting input will add a Johnson voltage noise term equal to that of the amplifier itself. As a simplifying constraint, set $R_G = R_S$ in Eq. 2 and assume an $R_S/2$ source impedance at the non-inverting input (where R_S is the signal's source impedance with another matching R_S to ground on the non-inverting input). This results in Eq. 3, where NG > 10 has been assumed to further simplify the expression.

Equation 3

$$E_N = \sqrt{(E_{NI})^2 + \frac{5}{4}(I_B R_S)^2 + 4kT\left(\frac{3R_S}{2}\right)}$$

Evaluating this expression for R_S = 50Ω will give a total equivalent input noise of 1.7nV/√Hz. Note that the NG has dropped out of this expression. This is valid only for NG > 10 as will typically be required by stability considerations.

FREQUENCY RESPONSE CONTROL

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factor), most high speed amplifiers will exhibit a more complex response with lower phase margin. The OPA686 is compensated to give a maximally flat 2nd-order Butterworth closed-loop response at a non-inverting gain of +10 (Figure 1). This results in a typical gain of +10 bandwidth of 250MHz, far exceeding that predicted by dividing the 1600MHz GBP by 10. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +40, the OPA686 will show the 40MHz bandwidth predicted using the simple formula and the typical GBP of 1600MHz.

Inverting operation offers some interesting opportunities to increase the available GBP. When the source impedance is matched by the gain resistor (Figure 2), the signal gain is $(1+R_F/R_G)$ while the noise gain for bandwidth purposes is $(1 + R_F/2R_G)$. This cuts the noise gain almost in half, increasing the minimum stable gain for inverting operation under these condition to –12 and the equivalent GBP to 3.2GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance which may be recommended to improve A/D linearity. A high speed, high open-loop gain amplifier like the OPA686 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA686. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA686 output pin (see Board Layout Guidelines).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA686 operating in a gain of +10, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads. As the signal gain is increased, the unloaded phase margin will also increase. Driving capacitive loads at higher gains will require lower R_S values than those shown for a gain of +10.

DISTORTION PERFORMANCE

The OPA686 is capable of delivering an exceptionally low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Performance Curves show the typical distortion under a wide variety of conditions. Most of these plots are limited to 110dB dynamic range. The OPA686's distortion, driving a 500Ω, load does not rise above –90dBc until either the signal level exceeds 2.0Vp-p and/or the fundamental frequency exceeds 5MHz. Distortion in the audio band is < –120dBc.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd harmonic will dominate the distortion with negligible a 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the non-inverting configuration, this is sum of $R_F + R_G$, while in the inverting configuration, it is just R_F (Figures 1 and 2). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the 2nd harmonic 12dB and the 3rd harmonic 18dB. Increasing the signal gain will also increase the 2nd harmonic distortion. Again, a 6dB increase in gain will increase the 2nd and 3rd harmonic by approximately 6dB even with constant

output power and frequency. Finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 100kHz. Starting from the –82dBc 2nd harmonic for a 5MHz, 2Vp-p fundamental into a 200Ω load at G = +10 (from the Typical Performance Curves), the 2nd harmonic distortion for frequencies lower than 100kHz will be approximately –82dBc – 20log(5MHz/100kHz) = –116dBc.

The OPA686 has extremely low 3rd-order harmonic distortion. This also gives a high two-tone, 3rd-order intermodulation intercept as shown in the Typical Performance Curves. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices. This matching network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA686 drives directly into the input of a high impedance device, such as an ADC, the 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum 6dBm. The intercept is used to predict the intermodulation spurious for two, closely-spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 – f_1|/2$, the two 3rd-order, close-in spurious tones will appear at $f_O \pm 3 \cdot \Delta f$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \cdot (IM3 – P_O)$ where IM3 is the intercept taken from the Typical Performance Curve and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 5MHz the OPA686 at a gain of +10 has an intercept of 48dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be 2Vp-p, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be 2 • (48 – 4) = 88dBc below the test-tone power level (–84dBm). If this same 2Vp-p, two-tone envelope were delivered directly into the input of an ADC—without the matching loss or the loading of the 50Ω network—the intercept would increase to at least 54dBm. With the same signal and gain conditions, but now driving directly into a light load, the spurious tones will then be at least 2 • (54 – 4) = 100dBc below the 4dBm test-tone power levels centered on 5MHz.

DC ACCURACY AND OFFSET CONTROL

The OPA686 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of its low ±1.5mV input offset voltage, careful attention to input bias current cancellation is also required. The low noise input stage of the OPA686 has a relatively high input bias current (10µA typical into the pins) but with a very close match between the two input currents—typically ±100nA input offset current. The total output offset voltage may be reduced considerably by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 20Ω series resistor into the non-inverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this will increase the source resistances for the non-inverting input bias current to 45Ω. Since this is now equal to the resistance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using the 453Ω feedback resistor, this output error will now be less than ±0.9µA • 453Ω = ±0.4mV over the full temperature range.

A fine-scale, output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to insure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be non-inverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the non-inverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal will set up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. Figure 8 shows one example of an offset adjustment for a DC-coupled signal path that will have minimum impact on the signal frequency response. In this case, the input is brought into an inverting gain resistor with the DC adjustment an additional current summed into the inverting node. The resistor values setting this offset adjustment are much larger than the signal path resistors. This will insure that this adjustment has minimal impact on the loop gain and hence, the frequency response.

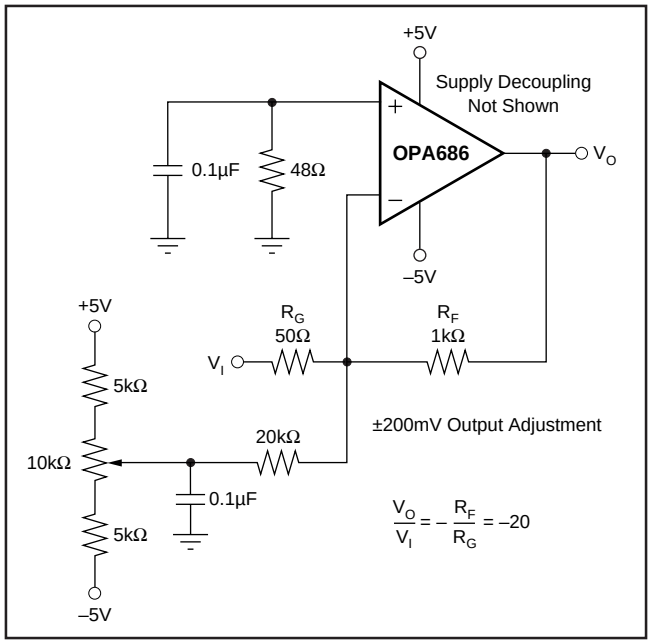


FIGURE 8. DC-Coupled, Inverting Gain of –20, with Output Offset Adjustment.

THERMAL ANALYSIS

The OPA686 will not require heatsinking or airflow in most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \cdot \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \cdot R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA686N (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load at $+2.5V_{DC}$.

$P_D = 10V\ (13.9mA) + 5^2/(4 \cdot (100\Omega \parallel 500\Omega)) = 214mW$

Maximum $T_J = +85°C + (0.21W \cdot 150°C/W) = 117°C$

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the OPA686 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA686. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be set the R_G be set to 50Ω. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA686 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA686 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot

of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high speed part like the OPA686 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA686 onto the board.

INPUT AND ESD PROTECTION

The OPA686 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 9.

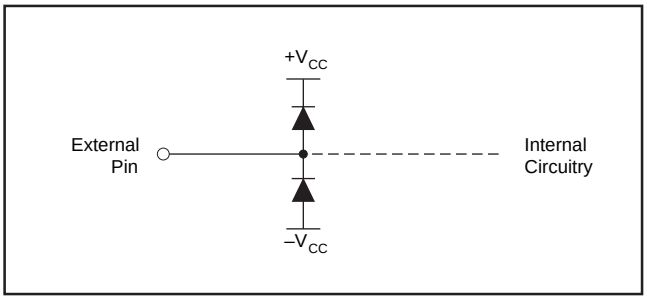


FIGURE 9. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA686), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA686N/250	LIFEBUY	SOT-23	DBV	5	250	None	CU NIPDAU	Level-3-250C-168 HR
OPA686N/3K	LIFEBUY	SOT-23	DBV	5	3000	None	CU NIPDAU	Level-3-250C-168 HR
OPA686U	LIFEBUY	SOIC	D	8	100	None	CU SNPB	Level-2-220C-1 YEAR
OPA686U/2K5	LIFEBUY	SOIC	D	8	2500	None	CU SNPB	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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