ALPHA & OMEGA SEMICONDUCTOR

AO4822A
Dual N-Channel Enhancement Mode Field Effect Transistor

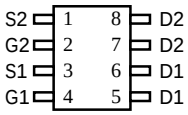
General Description

The AO4822A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard Product AO4822A is Pb-free (meets ROHS & Sony 259 specifications). AO4822AL is a Green Product ordering option. AO4822A and AO4822AL are electrically identical.*

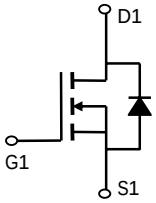
Features

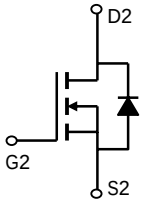
V_{DS} (V) = 30V
I_D = 8.5A (V_{GS} = 10V)
$R_{DS(ON)}$ < 16mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 26mΩ (V_{GS} = 4.5V)

UIS TESTED!
Rg,Ciss,Coss,Crss Tested



SOIC-8





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max 10 Sec	Max Steady State	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [AF]	T_A=25°C	I_D	8.5	6.8	A
	T_A=70°C		6.6	5.4	A
Pulsed Drain Current [B]		I_{DM}	30		A
Avalanche Current [C]		I_{AR}	16		A
Repetitive avalanche energy L=0.3mH [C]		E_{AR}	38		mJ
Power Dissipation	T_A=25°C	P_D	2	1.1	W
	T_A=70°C		1.28	0.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [AF]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		74	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	35	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.7	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8.5A		13.4	16	mΩ
		T_J=125°C		20	25	
		V_{GS}=4.5V, I_D=6A		19.5	26	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8.5A		23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		955	1250	pF
C_{oss}	Output Capacitance			145		pF
C_{rss}	Reverse Transfer Capacitance			112		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.5	0.85	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=8.5A		17	24	nC
Q_g(4.5V)	Total Gate Charge			9	12	nC
Q_{gs}	Gate Source Charge			3.4		nC
Q_{gd}	Gate Drain Charge			4.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.8Ω, R_{GEN}=3Ω		5	6.5	ns
t_r	Turn-On Rise Time			6	7.5	ns
$t_{D(off)}$	Turn-Off DelayTime			19	25	ns
t_f	Turn-Off Fall Time			4.5	6	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8.5A, dI/dt=100A/µs		16.7	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8.5A, dI/dt=100A/µs		6.7	10	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F.The current rating is based on the t ≤ 10s thermal resistance rating.
Rev 2: Sept. 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

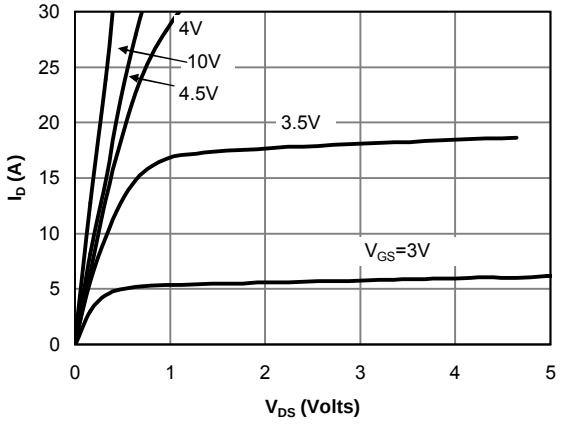


Fig 1: On-Region Characteristics

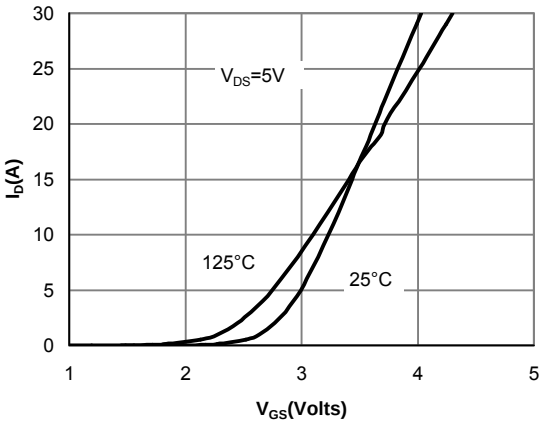


Figure 2: Transfer Characteristics

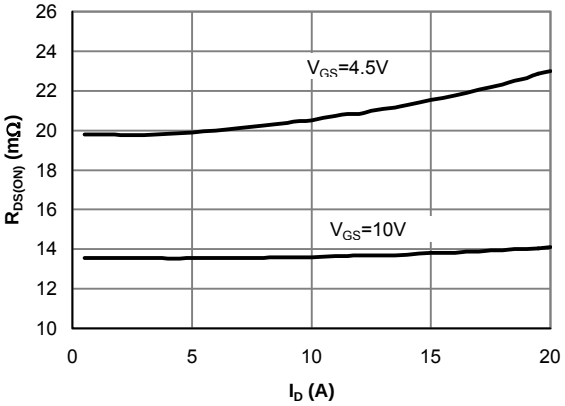


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

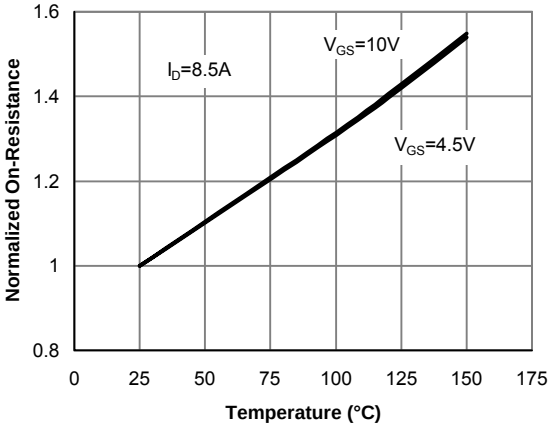


Figure 4: On-Resistance vs. Junction Temperature

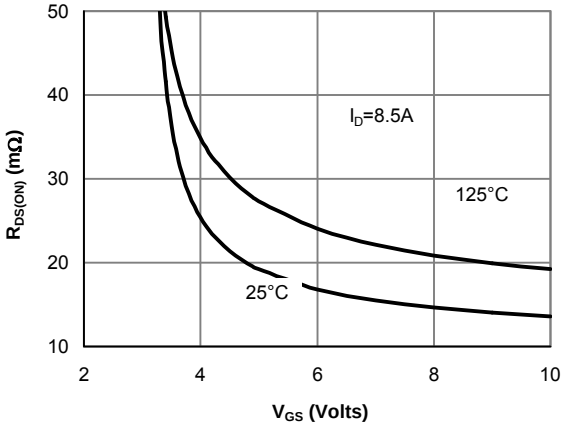


Figure 5: On-Resistance vs. Gate-Source Voltage

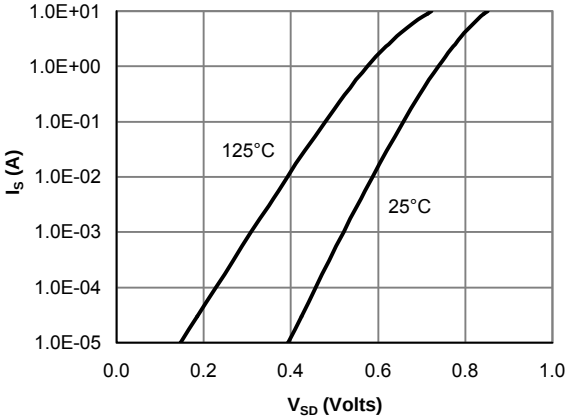


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

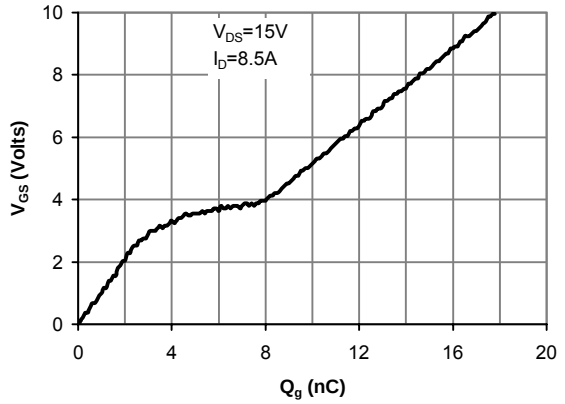


Figure 7: Gate-Charge Characteristics

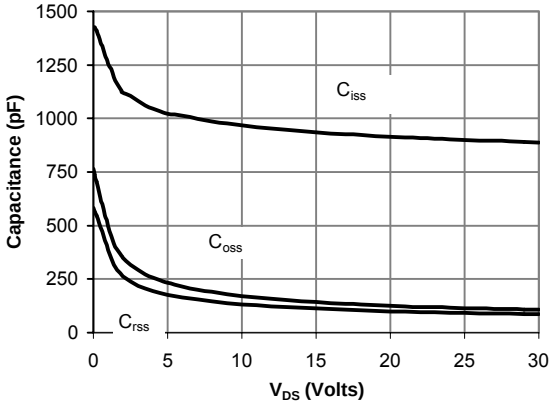


Figure 8: Capacitance Characteristics

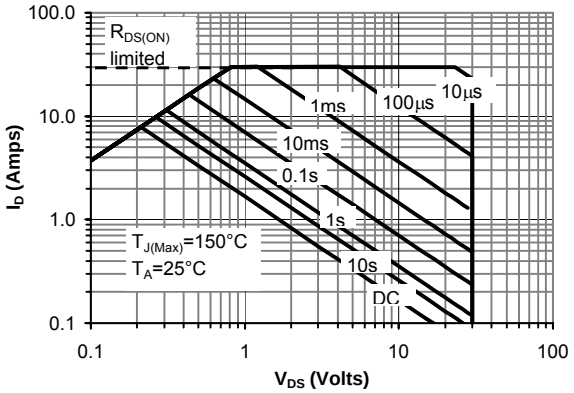


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

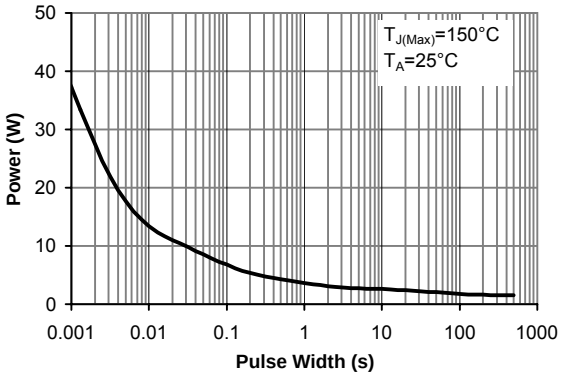


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

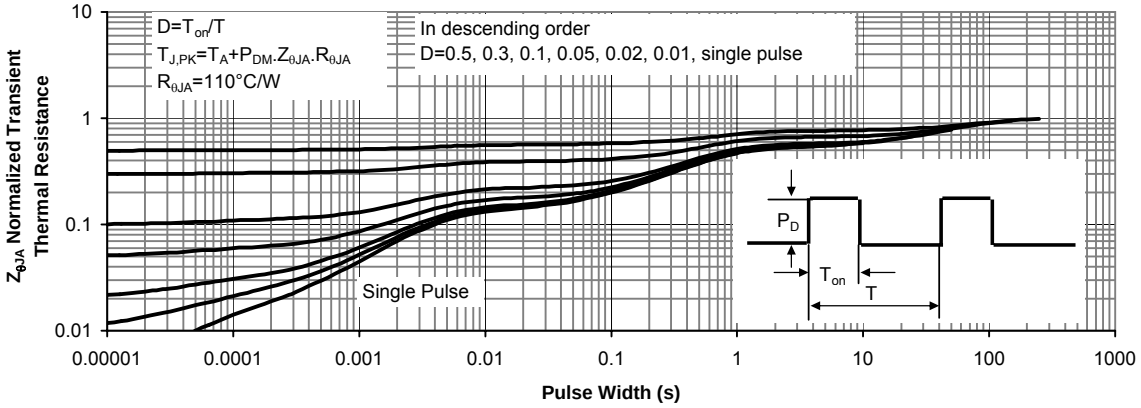


Figure 11: Normalized Maximum Transient Thermal Impedance