



Numonyx™ StrataFlash® Embedded Memory

Specification Update

June 2008

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This product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Revision History

Date	Version	Description
June 2008	09	removed the typo error in "affected documents/related documents", replaced with correct P30 datasheet name and ordering information.
April 2008	08	Applied Numonyx branding.
Jan 2008	007	added errata to allow successful erase operation in intensive erase suspend resume environment
June 2007	006	- Updated errata to allow synchronous burst operation with TSOP packages under specific conditions. - Updated the Device Command table. - Updated description on synchronous burst operation and added EOWL section. - Updated flowcharts - Corrected typos and provided text clarifications.
March 2006	005	Added errata Section 4, "512Mbit Top Boot Parameter Mapping" on page 8 Added Documentation Change Section 3, "1-Gbit Family reference removed" on page 15
January 2006	004	Added errata "64Mbit TSOP Address Pin A23 connection" .
November 2005	003	Added Errata 2: "TSOP Read Access Time (tAVAV, tAVQV, tELQV, tVLQV)" on page 8.
September 2005	002	Added Specification Change: Section 3, "512-Mbit Easy BGA Ball Height Changed" on page -10 Added Errata: Section 1, "TSOP Synchronous Burst Read" on page -8
August 2005	001	Document includes all known errata and specification changes to date (original version)

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata and specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Numonyx™ StrataFlash® Memory (P30) datasheet	306666

Nomenclature

Errata are design defects or errors. These may cause the Numonyx™ StrataFlash® memory behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Numonyx™ StrataFlash® memory components. Numonyx may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.
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Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document

Summary Table of Changes—Numonyx™ StrataFlash® Embedded Memory (P30)

Number	Page	Status	Errata
1	8	See Errata	"TSOP Synchronous Burst Read"
2	8	No Fix	"TSOP Read Access Time (tAVAV, tAVQV, tELQV, tVLQV)"
3	8	See Errata	"64Mbit TSOP Address Pin A23 connection"
4	8	See Errata	"512Mbit Top Boot Parameter Mapping"
5	8	See Errata	"w602: erase suspend resume operation"

Specification Changes

Number	Page	Specification Changes
1	10	"Removed Power Supply Sequencing Requirement"
2	10	"Capacitance Conditions Changed"
3	10	"512-Mbit Easy BGA Ball Height Changed"
4	11	"AC and DC Specification Changes to support Burst Operation on TSOP"

Specification Clarifications

Number	Page	Specification Clarifications
1	12	"Updated Numonyx-Specific Extended Query Table for Stacked Devices"
2	13	"Added Additional Memory Maps for Stacked Devices"

Documentation Changes

Number	Page	Document Revision	Documentation Changes
1	15	-001	Please see Section 1, "256-Mbit and 128-Mbit Bottom Parameter Memory Maps" on page 15
2	15	-001	Please see Section 2, "Programming Region Size for the 256-Mbit Device" on page 15
3	15	-002	Please see Section 3, "1-Gbit Family reference removed" on page 15
4	15	-009	"Burst Operation with TSOP" on page 15

Errata

1. TSOP Synchronous Burst Read

Problem: Synchronous burst read operation is currently not supported for the TSOP package.

Implication: Customers may experience read failures if synchronous burst mode is implemented with the TSOP package.

Workaround: Specific workaround(s) have been identified for this erratum as described under [“AC and DC Specification Changes to support Burst Operation on TSOP” on page 11](#) and [“Burst Operation with TSOP” on page 15](#). The synchronous read input signals (i.e. ADV# and CLK) should be tied off to support asynchronous reads otherwise.

Status: A workaround has been identified. Please refer to [“AC and DC Specification Changes to support Burst Operation on TSOP” on page 11](#) and [“Burst Operation with TSOP” on page 15](#) for more information.

2. TSOP Read Access Time (t_{AVAV} , t_{AVQV} , t_{ELQV} , t_{VLQV})

Problem: Read access speed of the 256M TSOP package has been changed to 95ns.

Implication: Customers may experience read failures if the read access is faster than 95ns on the 256M TSOP package.

Workaround: No workaround(s) have been identified for this erratum.

Status: A fix is under evaluation.

3. 64Mbit TSOP Address Pin A23 connection

Problem: Possible read errors in 64-Mbit density TSOP package configurations may occur in units marked with an FPO code less than or equal to A601xxxx. The 8-digit FPO marking is located on the second line on top of the package.

Implication: Customers may experience read failures if address pin A23 is connected to $V_{\frac{1}{2}}$ or is floated. A23 is an upper address select for densities above 64Mbit.

Workaround: Ground or drive address pin A23 low.

Status: This erratum does not apply to material marked with an FPO code of A602xxxx or later.

4. 512Mbit Top Boot Parameter Mapping

Problem: The 512Mbit Top Boot device in all EasyBGA packages has an incorrectly configured parameter block map. The device incorrectly maps the parameter blocks to the middle of the memory map instead of to the top and the bottom of the memory map.

Implication: Customer software may not function properly depending upon how the software is structured to operate with parameter blocks in the middle of the memory map.

Workaround: The customer may order the Bottom Boot option since 512Mbit Top and Bottom devices have an identical memory map.

Status: This erratum does not apply to material marked with an FPO code of A553xxxx or later on 512Mbit Easy BGA devices in leaded or Pb-free packages.

5. W602: erase suspend resume operation

- Problem:** P30 product may fail to erase in intensive erase/suspend/resume environments. This is due to an internal firmware issue that is exhibited in certain applications that require at least 3000 to 4000 erase/suspend/resume cycles during the erase of a single block.
- Implication:** Customer may see erase failure (SR reports "A0") during a background erase. This does not damage the device in any way, but data in the block may be disturbed from its original state.
- Workaround:** If such an erase failure occurs, customer should retry the erase with an increase to the Tres (W602) spec from 500uS to 1mS. If the device still fails, continue to increase Tres in increments of 500uS up to a maximum Tres of 2.5mS. Once the failing block passes, subsequent blocks should revert back to original erase algorithm and timing for Tres (500uS typical).
- Status:** This erratum does not apply to material marked with an FPO code dated x806xxxx or later.

Specification Changes

1. Removed Power Supply Sequencing Requirement

Issue: Removed the power-up requirement that V_{CC} should attain V_{CCMIN} before applying V_{CCQ} and V_{PP} if they are not connected together.

Old Specification:

Power supply sequencing is not required if V_{CC} , V_{CCQ} , and V_{PP} are connected together; If V_{CCQ} and/or V_{PP} are not connected to the V_{CC} supply, then V_{CC} should attain V_{CCMIN} before applying V_{CCQ} and V_{PP} . Device inputs should not be driven before supply voltage equals V_{CCMIN} .

New Specification:

Power supply sequencing is not required if V_{PP} is connected to V_{CC} or V_{CCQ} . Otherwise V_{CC} and V_{CCQ} should attain their minimum operating voltage before applying V_{PP} .

2. Capacitance Conditions Changed

Issue: The conditions for the capacitance table changed as shown below.

Symbol	Parameter	Signals	Min	Typ	Max	Unit	Condition	Note
C_{IN}	Input Capacitance	Address, Data, CE#, WE#, OE#, RST#, CLK, ADV#, WP#	2	6	7	pF	Typ temp = 25 °C, Max temp = 85 °C, $V_{CC} = (0\text{ V} - 2.0\text{ V})$, $V_{CCQ} = (0\text{ V} - 3.6\text{ V})$, Discrete silicon die	1,2,3
C_{OUT}	Output Capacitance	Data, WAIT	2	4	5	pF		

Notes:

- Capacitance values are for a single die; for 2-die and 4-die stacks multiply the capacitance values by the number of die in the stack.
- Sampled, not 100% tested.
- Silicon die capacitance only, add 1 pF for discrete packages.

3. 512-Mbit Easy BGA Ball Height Changed

Issue: The mechanical specifications for the 512-Mbit Easy BGA changed as shown in [Table 1](#).

Table 1. Easy BGA Package Dimensions (Sheet 1 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Package Height (64/128/256-Mbit)	A	-	-	1.200	-	-	0.0472	
Package Height (512-Mbit)	A	-	-	1.300	-	-	0.0512	
Ball Height	A1	0.250	-	-	0.0098	-	-	
Package Body Thickness (64/128/256-Mbit)	A2	-	0.780	-	-	0.0307	-	
Package Body Thickness (512-Mbit)	A2	-	0.910	-	-	0.0358	-	

Table 1. Easy BGA Package Dimensions (Sheet 2 of 2)

Product Information	Symbol	Millimeters			Inches			Notes
		Min	Nom	Max	Min	Nom	Max	
Ball (Lead) Width	b	0.330	0.430	0.530	0.0130	0.0169	0.0209	
Package Body Width	D	9.900	10.000	10.100	0.3898	0.3937	0.3976	1
Package Body Length	E	12.900	13.000	13.100	0.5079	0.5118	0.5157	1
Pitch	[e]	-	1.000	-	-	0.0394	-	
Ball (Lead) Count	N	-	64	-	-	64	-	
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039	
Corner to Ball A1 Distance Along D	S1	1.400	1.500	1.600	0.0551	0.0591	0.0630	1
Corner to Ball A1 Distance Along E	S2	2.900	3.000	3.100	0.1142	0.1181	0.1220	1

Notes:

1. See your local sales representative for Daisy Chain Evaluation Unit information..

4. AC and DC Specification Changes to support Burst Operation on TSOP

Issue: A note was added in the P30 Specification under Operating Conditions stating that 40Mhz burst operation on the TSOP package has a minimum operating Vcc value of 1.85V. The AC Read Specification table was also updated to support the TSOP synchronous burst operation as shown in [Table 2, "Clock Specifications" on page 11](#).

Table 2. Clock Specifications

R200	f_{CLK}	CLK frequency		-	52	MHz	1,3,5,6
			TSOP	-	40	MHz	
R201	t_{CLK}	CLK period		19.2	-	ns	
			TSOP	25	-	ns	
R202	$t_{CH/CL}$	CLK high/low time		5	-	ns	
R203	$t_{FCLK/RCLK}$	CLK fall/rise time		-	3	ns	

Specification Clarifications

1. Updated Numonyx-Specific Extended Query Table for Stacked Devices

Issue: The following information was added to the Numonyx-Specific Extended Query Table for stacked devices.

Offset ⁽¹⁾ P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h (P+1)h (P+2)h	3	Primary extended query table Unique ASCII string "PRI"	10A 10B: 10C:	--50 --52 --49	"P" "R" "I"
(P+3)h	1	Major version number, ASCII	10D:	--31	"1"
(P+4)h	1	Minor version number, ASCII	10E:	--34	"4"
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support (1=yes, 0=no) <i>bits 11–29 are reserved; undefined bits are "0." If bit 31 is "1" then another 31 bit field of Optional features follows at the end of the bit–30 field.</i> bit 0 Chip erase supported bit 1 Suspend erase supported bit 2 Suspend program supported bit 3 Legacy lock/unlock supported bit 4 Queued erase supported bit 5 Instant individual block locking supported bit 6 Protection bits supported bit 7 Pagemode read supported bit 8 Synchronous read supported bit 9 Simultaneous operations supported bit 10 Extended Flash Array Blocks supported bit 30 CFI Link(s) to follow bit 31 Another "Optional Features" field to follow	10F: 110: 111: 112:	--E6 --01 --00 See table below	No Yes Yes No No Yes Yes Yes No No See table below

Address	Discrete		512-Mbit			
	–B	–T	–B	–T		
	--	--	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
112:	--00	--00	--40	--00	--40	--00

Offset ⁽³⁾ P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+48)h (P+49)h (P+4A)h (P+4B)h	4	CFI Link Field bit definitions Bits 0–9 = Address offset (within 32Mbit segment) of referenced CFI table Bits 10–27 = nth 32Mbit segment of referenced CFI table Bits 28–30 = Memory Type Bit 31 = Another CFI Link field immediately follows	152: 153: 154: 155:	See table below	
(P+4C)h	1	CFI Link Field Quantity Subfield definitions Bits 0–3 = Quantity field (n such that n+1 equals quantity) Bit 4 = Table & Die relative location Bit 5 = Link Field & Table relative location Bits 6–7 = Reserved	156:		

Address	Discrete		512-Mbit			
	–B	–T	–B		–T	
	—	—	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
112:	--00	--00	--40	--00	--40	--00

2. Added Additional Memory Maps for Stacked Devices

Issue: Memory maps for both top parameter and bottom parameter 512-Mbit were added for clarification.
Diagrams updated to remove confusion. Added virtual addressing map.

Table 3. 512-Mbit Top Parameter Memory Map (Easy BGA and QUAD+ SCSP)

Die Stack Config.	Size (KB)	512-Mbit Flash (2x256-Mbit w/ 1CE)	
		Blk	Address Range
(Top Parameter Die)	32	258	1FFC000 - 1FFFFFF
	:	:	:
	32	255	1FF0000 - 1FF3FFF
	128	254	1FE0000 - 1FEFFFF
	:	:	:
	128	0	1000000 - 100FFFF
(Bot Parameter Die)	128	258	FF0000 - FFFFFFF
	:	:	:
	128	4	010000 - 01FFFF
	32	3	00C000 - 00FFFF
	:	:	:
	32	0	000000 - 003FFF

Table 4. 512-Mbit Bottom Parameter Memory Map (Easy BGA and QUAD+ SCSP)

Die Stack Config.	Size (KB)	512-Mbit Flash (2x256-Mbit w/ 1CE)	
		Blk	Address Range
(Top Parameter Die)	32	258	1FFC000 - 1FFFFFFF
	⋮	⋮	⋮
	32	255	1FF0000 - 1FF3FFFF
	128	254	1FE0000 - 1FEFFFFF
	⋮	⋮	⋮
	128	0	1000000 - 100FFFFF
(Bot Parameter Die)	128	258	FF0000 - FFFFFFFF
	⋮	⋮	⋮
	128	4	010000 - 01FFFF
	32	3	00C000 - 00FFFF
	⋮	⋮	⋮
	32	0	000000 - 003FFF

Note: Top and Bottom parameter Memory Maps are intended to be identical.

Documentation Changes

1. 256-Mbit and 128-Mbit Bottom Parameter Memory Maps

Issue: There was an error in the 256-Mbit and 128-Mbit Bottom Parameter Memory Maps. These were corrected.

2. Programming Region Size for the 256-Mbit Device

Issue: There was an error in the size of the Programming Regions for the 256-Mbit device. This was corrected to be 8-Mbit like the other densities.

3. 1-Gbit Family reference removed

Issue: The 1-Gbit product family was removed from the specification.

4. Burst Operation with TSOP

Issue: Synchronous burst was not previously permitted on TSOP packages for this product

Old Specification:

Synchronous burst read operation is currently not supported for the TSOP package. The synchronous read signals, ADV# and CLK, should be tied off to support asynchronous reads.

New Specification:

Synchronous burst read operation is permitted with all options of the P30 256 Mbit TSOP package when the clock frequency does not exceed 40 Mhz and the device does not operate below a V_{cc} of 1.85V min. Only 256 Mbit TSOP devices support synchronous burst operation on the TSOP package at this time.

