HARMONY Data Sheet

1Mb: MT75W8Y136HBB
2Mb: MT75W16Y136HBB

For the latest data sheet, please refer to the Micron Web site:
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FEATURES

- 16K and 8K x 136-bit full TCAMs
- Configurable as 8K/4K x 272 or 32K/16K x 68
- 68-bit interface operates at 13.6 Gb/s
- Sustains 100 million searches per second on a 34-bit, 68-bit, or 136-bit field
- Performs 50 million searches per second in 272-bit configuration
- Holds multiple word widths within the same device
- Provides synchronous pipelined operation
- Cascades up to 31 TCAMs without performance degradation or additional logic
- Allows glueless interface to industry-standard synchronous SRAMs
- Supports IEEE 1149.1 JTAG Test Access
- 1.8V and 3.3V power supply
- 272-ball HSBGA package

GENERAL DESCRIPTION

The Micron® Harmony device is a high-performance, pipelined, synchronous, ternary content addressable memory (TCAM) device, which is available in two configurations:

- 1Mb version, organized as 8K x 136 bits
- 2Mb version, organized as 16K x 136 bits

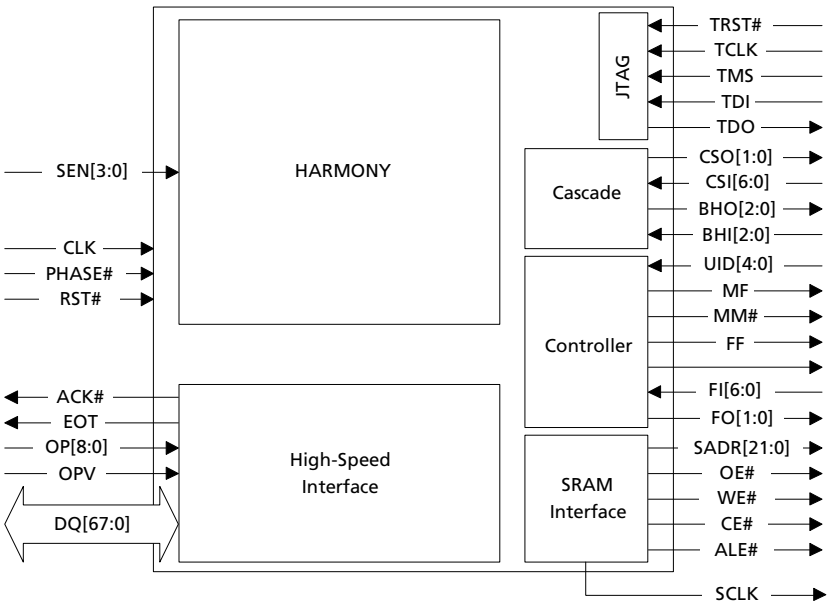
Additionally, the organization is flexible; the 2Mb Harmony device can be reconfigured as 32K x 68 bits or 8K x 272 bits, and the 1Mb Harmony device can be reconfigured as 16K x 68 bits or 4K x 272 bits.

Harmony sustains 100 million searches per second when organized as 136 bit wide or 68 bit wide, and 50 million searches per second when organized as 272 bit wide. Harmony also supports a search table of 34 bits with the help of the global mask registers (GMRs).

This high-speed device can be used in a variety of networking and communications applications, such as longest-prefix match (CIDR), MPLS, and Layer 2, 3, and 4 protocols.

The flexibility of the Harmony device allows the use of multiple search tables within the same device. It simultaneously compares data against an entire pre-stored array of addresses, providing a performance advantage by reducing search times an order-of-magnitude over typical binary or tree-based search algorithms. This Harmony device can be designed into many applications, but it is particularly well suited to performing highly intensive search operations.

Figure 1. Harmony Block Diagram



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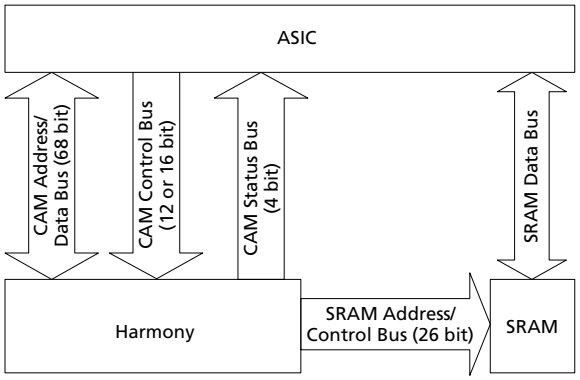
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FUNCTIONAL DESCRIPTION

The Harmony Block Diagram (Figure 1) consists of the following components: TCAM, high-speed I/O interface, cascade control, SRAM interface, test assess port, and the instruction and DQ bus interface. Figure 2 illustrates how Harmony is typically connected to other devices in a system.

Figure 2. Typical Harmony Connections



Harmony has four major buses that interface with other devices: the TCAM address/data bus, the TCAM control bus, the TCAM status bus, and the SRAM address/control bus. Other interfaces include a cascade interface that is used when multiple Harmony chips are cascaded to increase the table size and a JTAG interface.

ADDRESS AND DATA BUS

The TCAM address/data bus is a 68-bit bidirectional bus that performs one I/O operation per clock cycle.

Note: TCAM operations require two or four clock cycles each, so if the system clock is 200 MHz, an I/O operation is performed every 5ns. However, each TCAM operation requires 10 or 20ns for completion, depending on the operation.

DATA BUS DQ[67:0]

The Data Bus DQ[67:0] is used for data transfer to and from the TCAM array, which comprise data and mask arrays. The DQ bus transports the search data during the SEARCH operation. The DQ bus also transports addressing and data during the READ/WRITE operations of the TCAM array and the internal registers. Additionally, the DQ bus carries the address information for the SRAM bus.

INSTRUCTION BUS

The instruction bus OP[8:0] carries the instruction and its associated parameters. The description of each instruction and the related parameters are listed in "Harmony Instructions" on page 17.

Each instruction execution requires two clock cycles, but the bidirectional DQ[67:0] bus runs every cycle, providing a simple double data rate I/O. A second port provides the address and control lines necessary to drive an external SRAM. SEARCH operations drive the resulting match address on the SRAM address lines, allowing associated data to be stored in the external SRAM rather than the internal device memory. READ and WRITE operations also drive the SRAM address lines with the address of the TCAM word being read or written.

SRAM INTERFACE

The SRAM interface section drives the ADDRESS and CONTROL signals required to access the external SRAM. Harmony can generate a synchronous output clock (SCLK) to perform SRAM accesses. Using the SCLK signal, Harmony reduces the amount of required interface logic by synchronously driving the SRAM ADDRESS and CONTROL signals. When cascaded, the Harmony device, which contains a match in its results register, drives the SRAM bus. However, when no match exists, the last Harmony device of the cascade (LRAM = 1) drives the SRAM bus. Also, when cascaded, this section inserts pipeline delays for the SRAM address and SRAM control for Harmony. The SRAM data bus is connected to the appropriate host ASIC; therefore, SRAM data does not pass through Harmony.

SRAM Addressing

The SRAM address consists of information obtained from the DQ bus and either the lowest match address from a SEARCH instruction or the address supplied by the Instruction Register. The interface timing and control selects the address from the Instruction Register by asserting the applicable READ or WRITE instruction. During a READ or WRITE instruction to the SRAM, if the identification (UID) is the global address, then the last TCAM on the SRAM bus of the depth-cascaded devices drives the SRAM signals (LCAM = 1).

CASCADING HARMONY DEVICES

Harmony devices can be cascaded to provide additional depth. Up to 31 devices can be cascaded without any performance degradation. Harmony performs the necessary arbitration to determine which of the cascaded devices drives the SRAM bus, thereby eliminating bus contention. Each device in the cascade is assigned a unique ID number, which helps identify the device that has found the match.

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Cascade Control

The cascade control section drives the CASCADE OUTPUT (CSO) signal when the Harmony devices are depth cascaded. Harmony also contains the control logic to determine if the entry in a single device is full or if the table consisting of multiple devices is full. In addition, the cascade control section provides support for multiple matches. Although the cascade control section does not drive the validity of matches, the success of matches, multiple matches, or the required SRAM signals (these signals are located in the controller section of the block diagram), it does contain the control logic to enable the output for these signals.

The diagram showing the cascading of eight devices is shown in Figure 23 on page 34.

Cascading CSO[1:0] and CSI[6:0] Signals

With eight devices cascaded, the search table can be either 128K x 136 bits, 256K x 68 bits, or 64K x 272 bits wide. Figure 23 on page 34 shows the pin connections between the cascaded Harmony devices.

Each Harmony device asserts the CASCADE OUT signals CSO[0] and CSO[1] to inform the downstream devices of the result. The CASCADE IN signals CSI[6:0] for a device are connected to the CSO signals of the upstream devices.

Note: The host ASIC must program the table size TLSZ[3:2] bits in the Instruction Register to "01" for each of the devices in a cascade, as described in Figure 7 on page 12.

Depth Cascading for a FULL Signal

FULL OUT FO[0] and FO[1] are the same logical signal. When eight Harmony devices are cascaded, one of these FULL signals must be connected to the FI signals of up to four downstream devices. Bit[0] of each of the 68-bit entries indicates if the entry in the data array is empty or occupied. The "Write To Next Free Address" instruction uses this information.

Each signal of the FI[6:0] bus is connected to the FO[0] or FO[1] output of the upstream cascaded device, to generate the FULL FLAG FF. Figure 24 on page 35 shows the interconnections of these signals between the cascaded devices.

DUAL DATA RATE CLOCK

The dual data rate clock, configured as cycle A and cycle B, allows the DQ bus interface to operate at double speed while maintaining 100 MHz search rates even though the I/O width is less than the data width. Hence, only 68 pins, instead of 136 pins, are required to support 136-bit data words. Furthermore, Harmony can perform consecutive searches on 136-bit data words. The PHASE# signal ensures that these double-speed operations are correctly aligned with Harmony.

Master Clock (CLK)

Harmony receives the master clock CLK, which has a maximum frequency of 200 MHz.

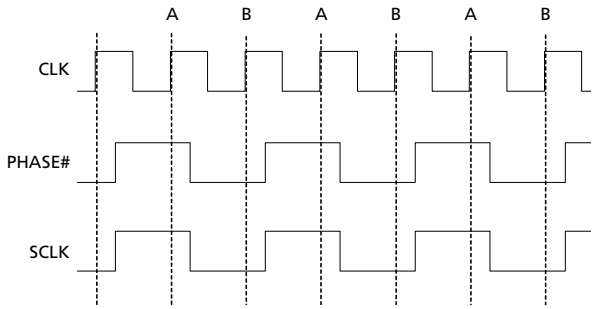
PHASE# Signal

The PHASE# signal runs at half the frequency of the master clock and generates the internal clock (see Figure 3). The Harmony uses this divided clock for internal operations.

SRAM Clock (SCLK)

The SCLK is an output clock and is generated for the SRAM bus. Because this clock is generated from the internal clock, it allows users to perform the SRAM READ and WRITE operations synchronous to the Harmony device.

Figure 3. Relationship Between CLK, PHASE#, and SCLK Signals



POWER MANAGEMENT

The power management feature within Harmony reduces power dissipation by limiting SEARCH operations to selected portions of the TCAM. Predetermined portions of data can be selected and isolated for a SEARCH instruction. The input pins (SEN[3:0]) independently control four equal sections of the device. To disable power management, set bit 0 of the Configuration Register or connect SEN[3:0] to V_{SS}.

RESET FUNCTION

Hardware Reset

RST# is the reset pin on Harmony. Driving this pin LOW performs a hardware reset and initializes the Harmony device to a known state.

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Software Reset

Bit[0] in the Instruction Register and the reset pin work in a similar way. When Bit[0] is set to "1," it generates an internal reset pulse lasting for eight clock cycles and then automatically resets to "0."

Please refer to the Micron Application Note: "Initialization of Harmony TCAM."

JTAG INTERFACE AND TEST ACCESS PORT

The Harmony test access port provides an interface for manufacturing tests and consists of the boundary scan access port used to support the standard JTAG IEEE 1149.1. See page 6 for more details on JTAG interface and test access port.

HARMONY SIGNALS

Table 1: Harmony Signal Nomenclature

SYMBOL	TYPE	DESCRIPTION
CLOCKS AND RESET		
CLK	I	**Master Clock**. Harmony samples all the control and data signals either on the positive edge of CLK, or on the positive of CLK when PHASE# is LOW.
PHASE#	I	**PHASE#**. This signal runs at half the frequency of CLK and generates an internal clock from CLK.
SCLK	T[1]	**SRAM Clock**. This signal is the clock for the external SRAM bus. It runs at half the speed of the input CLK, going LOW on the CLK positive edge that PHASE# is HIGH. The SRAM clock must be enabled by the SCE bit in the Configuration Register.
RST#	I	**Reset**. Driving RST# LOW initializes the device to a known state.
INSTRUCTION AND DQ BUS		
OP[8:0]	I	**Instruction Bus**. OP[1:0] specifies the instruction. OP[8:2] contains the instruction parameters. The descriptions of individual instructions explain the details of the parameters. The encoding of instructions based on the [1:0] fields are: 00:READ 01:WRITE 10:SEARCH 11:WRITE NEXT FREE ADDRESS
OPV	I	**Op-Code Valid**. OPV qualifies the instruction bus. 0:No Instruction, 1:Instruction
DQ[67:0]	I/O	**Address/Data Bus**. DQ[67:0] carries the read and write address and data during REGISTER, DATA, and MASK ARRAY operations. It carries the compare data during SEARCH operations. It also carries TCAM array, SRAM, or regular address during READ and WRITE operations.
ACK	T[1]	**Read Acknowledge**. ACK indicates that valid data is available on the DQ bus during REGISTER, DATA WORD, AND WORD MASK ARRAY READ operations, or the data is available on the SRAM data bus during operations.
EOT	T[1]	**End of Transfer**. EOT indicates the end of burst transfer during READ or WRITE burst operations.
MF	T[1]	**Match Flag**. When asserted, MF indicates that the device is selected in a SEARCH operation. MM# must be enabled by the MME bit in the Configuration Register.
MV	T[1]	**Match Flag Valid**. When asserted, MV qualifies the match flag and multi-match flag signals.
MM#	T[1]	**Multi-Match Flag**. When asserted, indicates that two or more matches were found. MM# must be enabled by the MME bit in the Configuration Register. MM# may be left unconnected, but if used it should be connected to V_{DDQ} with a 10KΩ resister.
SEN[3:0]	I	**Search Enable**. SEN[3:0] controls which pages within the TCAM array participate in SEARCH operations. These pins have pull-down resistors, so they may be left unconnected. They must be enabled by the SENE bit in the Configuration Register.
SRAM INTERFACE		
SADR[21:0]	T[1]	**SRAM Address**. SADR contains address lines to access external SRAMs that contains associative data. See Table 26 and Table 27 on page 32 for SRAM bus addressing details.
CE#	T[1]	**SRAM Chip Enable**. CE# is the chip enable control for external SRAMs.
WE#	T[1]	**SRAM Write Enable**. WE# is the write enable control for external SRAMs.
OE#	T[1]	**SRAM Output Enable**. OE# is the output enable control for external SRAMs.
ALE#	T[1]	**Address Latch Enable**. ALE# is the latch enable control for external SRAMs.

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Table 1: Harmony Signal Nomenclature (Continued)

SYMBOL	TYPE	DESCRIPTION
CASCADE INTERFACE		
CSI[6:0]	I	**Cascade In**. These pins depth-cascade the device to form a larger table size. One signal of this bus is connected to the CSO[1] or CSO[0] of each of the upstream devices in a block. Connect all unused CSI pins to a logic 0. For more information, see "The UID bits correspond to the UID bits of the TCAM device driving the SRAM, and provide for continuous addressing of a larger SRAM from multiple Harmony devices. OP[8:6] bits (in the 1Mb Harmony device) and OP[8:7] bits (in the 2Mb Harmony device) allow page addressing when large amounts of SRAM are required for each TCAM address. For 136-bit SEARCH and WRITE operations, SADR[0] is always "0." For 272-bit SEARCHES, SADR[1:0] is "00."" on page 32.
CSO[1:0]	O	**Cascade Out**. CSO[1] and CSO[0] are the same logical signal. CSO[1] or CSO[0] is connected to one input of the CSI bus of up to four downstream devices (in a block that contains up to eight devices).
FI[6:0]	I	**Full In**. Each signal in this bus is connected to FO[0] or FO[1] of an upstream device to generate the FF signal for the depth-cascaded block. Connect all unused FI signals to logic 1.
FO[1:0]	O	**Full Out**. FO[1] and FO[0] are the same logical signal. One of these two signals must be connected to the FI of up to four downstream devices in a depth-cascaded table. Bit[0] in the TCAM array indicates if the entry is full (1) or empty (0).This signal is asserted if all bits in the TCAM array are "1s."
BHI[2:0]	I	**Block Hit In**. These pins are used for cascading more than eight devices. They must be tied to V_{SS} if cascading eight or fewer devices.
BHO[2:0]	O	**Block Hit Out**. These pins are used for cascading more that eight devices. Output is NC if cascading eight or fewer devices.
FF	O	**Full Flag**. When asserted, this signal indicates that the table consisting of all depth-cascaded devices is full.
DEVICE IDENTIFICATION		
UID[4:0]	I	**Device Identification**. The binary-encoded device ID for a depth-cascaded system starts at 00000 and goes up to 11110. 11111 is reserved for a special broadcast address that selects all cascaded TCAMs in the system. On a broadcast read-only, the device with the LCAM bit set to "1" responds.
TEST ACCESS PORT PINS		
TDI	I	Test Data In. Internal pull-up to V_{DDQ}.
TCK	I	Test Clock. Tie to V_{DDQ} if JTAG port not used.
TDO	T[1]	Test Data Out
TMS	I	Test Mode Select. Internal pull-up to V_{DDQ}.
TRST#	I	Reset. Internal pull-up to V_{DDQ}.
POWER AND GROUND		
V_{DD}		Supply voltage for core (1.8V)
V_{DDQ}		Supply voltage for I/O (3.3V)
V_{SS}		Ground

[1] T = Three-state

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Table 2: Harmony Signals in Signal Name Order

SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)
ACK	V2	DQ27	A12	FI3	M4	SADR8	E20	V_{DDQ}	J19
ALE#	N18	DQ28	W12	FI4	N1	SADR9	G18	V_{DDQ}	J2
BHI0	J1	DQ29	B11	FI5	P1	SCLK	M20	V_{DDQ}	L19
BHI1	K4	DQ30	U11	FI6	N2	TCK	D3	V_{DDQ}	M3
BHI2	K2	DQ31	A10	FO0	P4	TDI	C2	V_{DDQ}	N19
BHO0	L1	DQ32	V11	FO1	R2	TDO	C1	V_{DDQ}	R3
BHO1	L2	DQ33	B10	MF	U18	TMS	D2	V_{DDQ}	T20
BHO2	L3	DQ34	W11	MM#	V19	TRST#	E4	V_{DDQ}	U14
CE#	N20	DQ35	C10	MV	U19	UID0	D1	V_{DDQ}	U3
CLK	L17	DQ36	V10	OE#	M18	UID1	E3	V_{DDQ}	V12
CSI0	F3	DQ37	A9	OP0	P18	UID2	E1	V_{DDQ}	V15
CSI1	G4	DQ38	U10	OP1	R19	UID3	E2	V_{DDQ}	V17
CSI2	F2	DQ39	C9	OP2	P17	UID4	F4	V_{DDQ}	V9
CSI3	G2	DQ40	Y9	OP3	R18	V_{DD}	A11	V_{DDQ}	W5
CSI4	H3	DQ41	D9	OP4	R17	V_{DD}	A15	V_{DDQ}	W7
CSI5	H2	DQ42	W9	OP5	T19	V_{DD}	A6	V_{DDQ}	Y11
CSI6	H1	DQ43	A8	OP6	T18	V_{DD}	B18	V_{SS}	D13
CSO0	J4	DQ44	U9	OP7	U20	V_{DD}	B2	V_{SS}	D17
CSO1	J3	DQ45	B8	OP8	V20	V_{DD}	B9	V_{SS}	D4
DQ0	U16	DQ46	W8	OPV	P19	V_{DD}	F1	V_{SS}	D8
DQ1	D16	DQ47	D7	PHASE#	M19	V_{DD}	F20	V_{SS}	H17
DQ2	Y18	DQ48	V8	RST#	T4	V_{DD}	K1	V_{SS}	H4
DQ3	A18	DQ49	B6	SEN0	W4	V_{DD}	K17	V_{SS}	J10
DQ4	W18	DQ50	Y7	SEN1	W3	V_{DD}	K3	V_{SS}	J11
DQ5	C16	DQ51	B7	SEN2	V5	V_{DD}	L20	V_{SS}	J12
DQ6	U15	DQ52	V7	SEN3	V3	V_{DD}	R1	V_{SS}	J9
DQ7	B16	DQ53	A5	SADR0	C18	V_{DD}	R20	V_{SS}	K9
DQ8	V16	DQ54	U7	SADR1	B20	V_{DD}	T3	V_{SS}	K10
DQ9	D15	DQ55	C6	SADR10	G19	V_{DD}	V18	V_{SS}	K11
DQ10	Y17	DQ56	V6	SADR11	F19	V_{DD}	V4	V_{SS}	K12
DQ11	C15	DQ57	A4	SADR12	H18	V_{DD}	W13	V_{SS}	L9
DQ12	W16	DQ58	U6	SADR13	G20	V_{DD}	Y10	V_{SS}	L10
DQ13	B15	DQ59	C5	SADR14	H20	V_{DD}	Y15	V_{SS}	L11
DQ14	V14	DQ60	Y5	SADR15	J17	V_{DD}	Y6	V_{SS}	L12
DQ15	B14	DQ61	B4	SADR16	J18	V_{DDQ}	A17	V_{SS}	M10
DQ16	W14	DQ62	Y4	SADR17	J20	V_{DDQ}	A7	V_{SS}	M11
DQ17	A14	DQ63	C4	SADR18	K18	V_{DDQ}	B13	V_{SS}	M12
DQ18	W15	DQ64	Y3	SADR19	K19	V_{DDQ}	C7	V_{SS}	M9
DQ19	C13	DQ65	A3	SADR2	C20	V_{DDQ}	D10	V_{SS}	N17
DQ20	V13	DQ66	U5	SADR20	K20	V_{DDQ}	D11	V_{SS}	N4
DQ21	A13	DQ67	D5	SADR21	L18	V_{DDQ}	D14	V_{SS}	U13
DQ22	Y14	EOT	V1	SADR3	C19	V_{DDQ}	D20	V_{SS}	U17
DQ23	C12	FF	U2	SADR4	D19	V_{DDQ}	D6	V_{SS}	U4
DQ24	Y13	FI0	L4	SADR5	F17	V_{DDQ}	E17	V_{SS}	U8
DQ25	B12	FI1	M1	SADR6	E18	V_{DDQ}	G17	V_{SS}	W1
DQ26	U12	FI2	M2	SADR7	F18	V_{DDQ}	G3	WE#	M17

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Table 3: Harmony Signals in Ball Designation Order

BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL	BALL NUMBER(S)	SYMBOL
A3	DQ65	D2	TMS	J1	BHI0	M19	PHASE#	V2	ACK
A4	DQ57	D3	TCK	J2	VDDQ	M20	SCLK	V3	SEN3
A5	DQ53	D4	VSS	J3	CSO1	N1	FI4	V4	VDD
A6	VDD	D5	DQ67	J4	CSO0	N2	F16	V5	SEN2
A7	VDDQ	D6	VDDQ	J9	VSS	N4	VSS	V6	DQ56
A8	DQ43	D7	DQ47	J10	VSS	N17	VSS	V7	DQ52
A9	DQ37	D8	VSS	J11	VSS	N18	ALE#	V8	DQ48
A10	DQ31	D9	DQ41	J12	VSS	N19	VDDQ	V9	VDDQ
A11	VDD	D10	VDDQ	J17	SADR15	N20	CE#	V10	DQ36
A12	DQ27	D11	VDDQ	J18	SADR16	P1	FI5	V11	DQ32
A13	DQ21	D13	VSS	J19	VDDQ	P4	FO0	V12	VDDQ
A14	DQ17	D14	VDDQ	J20	SADR17	P17	OP2	V13	DQ20
A15	VDD	D15	DQ9	K1	VDD	P18	OP0	V14	DQ14
A17	VDDQ	D16	DQ1	K2	BHI2	P19	OPV	V15	VDDQ
A18	DQ3	D17	VSS	K3	VDD	R1	VDD	V16	DQ8
B2	VDD	D19	SADR4	K4	BHI1	R2	FO1	V17	VDDQ
B4	DQ61	D20	VDDQ	K9	VSS	R3	VDDQ	V18	VDD
B6	DQ49	E1	UID2	K10	VSS	R17	OP4	V19	MM#
B7	DQ51	E2	UID3	K11	VSS	R18	OP3	V20	OP8
B8	DQ45	E3	UID1	K12	VSS	R19	OP1	W1	VSS
B9	VDD	E4	TRST#	K17	VDD	R20	VDD	W3	SEN1
B10	DQ33	E17	VDDQ	K18	SADR18	T3	VDD	W4	SEN0
B11	DQ29	E18	SADR6	K19	SADR19	T4	RST#	W5	VDDQ
B12	DQ25	E20	SADR8	K20	SADR20	T18	OP6	W7	VDDQ
B13	VDDQ	F1	VDD	L1	BHO0	T19	OP5	W8	DQ46
B14	DQ15	F2	CSI2	L2	BHO1	T20	VDDQ	W9	DQ42
B15	DQ13	F3	CSI0	L3	BHO2	U2	FF	W11	DQ34
B16	DQ7	F4	UID4	L4	FI0	U3	VDDQ	W12	DQ28
B18	VDD	F17	SADR5	L9	VSS	U4	VSS	W13	VDD
B20	SADR1	F18	SADR7	L10	VSS	U5	DQ66	W14	DQ16
C1	TDO	F19	SADR11	L11	VSS	U6	DQ58	W15	DQ18
C2	TDI	F20	VDD	L12	VSS	U7	DQ54	W16	DQ12
C4	DQ63	G2	CSI3	L17	CLK	U8	VSS	W18	DQ4
C5	DQ59	G3	VDDQ	L18	SADR21	U9	DQ44	Y3	DQ64
C6	DQ55	G4	CSI1	L19	VDDQ	U10	DQ38	Y4	DQ62
C7	VDDQ	G17	VDDQ	L20	VDD	U11	DQ30	Y5	DQ60
C9	DQ39	G18	SADR9	M1	FI1	U12	DQ26	Y6	VDD
C10	DQ35	G19	SADR10	M2	FI2	U13	VSS	Y7	DQ50
C12	DQ23	G20	SADR13	M3	VDDQ	U14	VDDQ	Y9	DQ40
C13	DQ19	H1	CSI6	M4	F13	U15	DQ6	Y10	VDD
C15	DQ11	H2	CSI5	M9	VSS	U16	DQ0	Y11	VDDQ
C16	DQ5	H3	CSI4	M10	VSS	U17	VSS	Y13	DQ24
C18	SADR0	H4	VSS	M11	VSS	U18	MF	Y14	DQ22
C19	SADR3	H17	VSS	M12	VSS	U19	MV	Y15	VDD
C20	SADR2	H18	SADR12	M17	WE#	U20	OP7	Y17	DQ10
D1	UID0	H20	SADR14	M18	OE#	V1	EOT	Y18	DQ2

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Table 4: Ball Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC	NC	DQ65	DQ57	DQ53	VDD	VDDQ	DQ43	DQ37	DQ31	VDD	DQ27	DQ21	DQ17	VDD	NC	VDDQ	DQ3	NC	NC	A
B	NC	VDD	NC	DQ61	NC	DQ49	DQ51	DQ45	VDD	DQ33	DQ29	DQ25	VDDQ	DQ15	DQ13	DQ7	NC	VDD	NC	SADR1	B
C	TDO	TDI	RES'D	DQ63	DQ59	DQ55	VDDQ	NC	DQ39	DQ35	RES'D	DQ23	DQ19	NC	DQ11	DQ5	NC	SADR0	SADR3	SADR2	C
D	UID0	TMS	TCK	VSS	DQ67	VDDQ	DQ47	VSS	DQ41	VDDQ	VDDQ	NC	VSS	VDDQ	DQ9	DQ1	VSS	NC	SADR4	VDDQ	D
E	UID2	UID3	UID1	TRST#													VDDQ	SADR6	NC	SADR8	E
F	VDD	CSI2	CSI0	UID4													SADR5	SADR7	SADR11	VDD	F
G	NC	CSI3	VDDQ	CSI1													VDDQ	SADR9	SADR10	SADR13	G
H	CSI6	CSI5	CSI4	VSS													VSS	SADR12	NC	SADR14	H
J	BHI0	VDDQ	CSO1	CSO0					VSS	VSS	VSS	VSS					SADR15	SADR16	VDDQ	SADR17	J
K	VDD	BHI2	VDD	BHI1					VSS	VSS	VSS	VSS					VDD	SADR18	SADR19	SADR20	K
L	BHO0	BHO1	BHO2	FI0					VSS	VSS	VSS	VSS					CLK	SADR21	VDDQ	VDD	L
M	FI1	FI2	VDDQ	FI3					VSS	VSS	VSS	VSS					WE#	OE#	PHASE#	SCLK	M
N	FI4	FI6	NC	VSS													VSS	ALE#	VDDQ	CE#	N
P	FI5	NC	NC	FO0													OP2	OP0	OPV	NC	P
R	VDD	FO1	VDDQ	NC													OP4	OP3	OP1	VDD	R
T	NC	NC	VDD	RST#													NC	OP6	OP5	VDDQ	T
U	NC	FF	VDDQ	VSS	DQ66	DQ58	DQ54	VSS	DQ44	DQ38	DQ30	DQ26	VSS	VDDQ	DQ6	DQ0	VSS	MF	MV	OP7	U
V	EOT	ACK	SEN3	VDD	SEN2	DQ56	DQ52	DQ48	VDDQ	DQ36	DQ32	VDDQ	DQ20	DQ14	VDDQ	DQ8	VDDQ	VDD	MM#	OP8	V
W	VSS	NC	SEN1	SEN0	VDDQ	NC	VDDQ	DQ46	DQ42	NC	DQ34	DQ28	VDD	DQ16	DQ18	DQ12	NC	DQ4	NC	NC	W
Y	NC	NC	DQ64	DQ62	DQ60	VDD	DQ50	NC	DQ40	VDD	VDDQ	NC	DQ24	DQ22	VDD	NC	DQ10	DQ2	NC	NC	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Note: Balls C3 and C11 are reserved for manufacturing test. Reserved balls should remain unconnected or tied to Vss.

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TCAM ARCHITECTURE

CONTENT ADDRESSABLE MEMORY

The TCAM array of the 2Mb Harmony consists of 16,384, 136-element ternary words, and the 1Mb Harmony consists of 8,192, 136-element ternary words, arranged so that each ternary element contains a data bit and a mask bit. The combination of data and mask bits determine whether the ternary element is a "0," "1," or "X" ("Don't Care"). Internally, bit 0 determines if the ternary word contains valid data; when the bit is set to "0," the word is available because it does not contain valid data. This bit is used to determine the next free address in the device.

A priority encoder generates the address of the word with the lowest address that satisfies the match criteria, using the searched data words, TCAM array words, and the specified global mask register.

DATA PATH DESCRIPTION

TCAM Array Architecture

The 1Mb and 2Mb Harmony devices contain a TCAM array comprised of data and ternary mask storage cells. The Harmony TCAM array is physically organized as four 136-bit wide quadrants, each 2K or 4K words deep, as shown in Figure 4. The TCAM array contains the data array and mask array.

Data Array

The storage cells of the data array hold the "0" and "1" data for each bit in the TCAM array. The DATA array is accessed through the READ CAM data and WRITE CAM data instructions.

Mask Array

Each cell in the data array has a corresponding mask bit associated with it. A "1" in a mask array bit forces SEARCH operations to match the data stored in the data array. A "0" in a mask array bit causes SEARCH operations to ignore the corresponding bit in the data array, effectively masking out that bit and allowing it to always match the search data. Therefore, the resulting value of that bit is "0," "1," or "X" ("Don't Care").

TCAM Array Quadrants

The Harmony TCAM array is physically organized as four quadrants. At 136 bits per word, each quadrant is 2K words deep for a 1Mb device and 4K words deep for a 2Mb device, as shown in Figure 4.

Each quadrant can be set to a different size by programming the configuration bits, CFG[16:9] in the Instruction Register. Two bits configure each quadrant as shown in Table 5.

Each quadrant can be organized into one of the table sizes shown in Table 6. Initially, the configuration bits have values of 00000000b providing four quadrants of 4K x 68 bits for the 1Mb device and 8K x 68 bits for the 2Mb device.

Figure 4. TCAM Array Quadrants

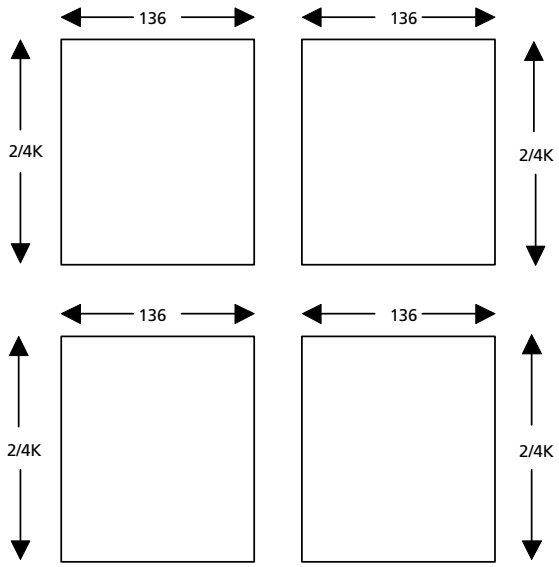


Table 5: Configuration Bits For Each Quadrant

CFG BITS	FUNCTION	68-BIT WORD SEGMENT ADDRESSES	
		1Mb	2Mb
10:9	These bits configure the address space within the first quadrant	0 to 4K -1	0 to 8K -1
12:11	These bits configure the address space within the second quadrant	4K to 8K -1	8K to 16K -1
14:13	These bits configure the address space within the third quadrant	8K to 12K -1	16K to 24K -1
16:15	These bits configure the address space within the fourth quadrant	12K to 16K -1	24K to 32K -1

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Table 6: Configuration Bits

CONFIGURATION BITS	QUADRANT SIZE	
	1Mb	2Mb
00	4K x 68 bits	8K x 68 bits
01	2K x 136 bits	4K x 136 bits
10	1K x 272 bits	2K x 272 bits

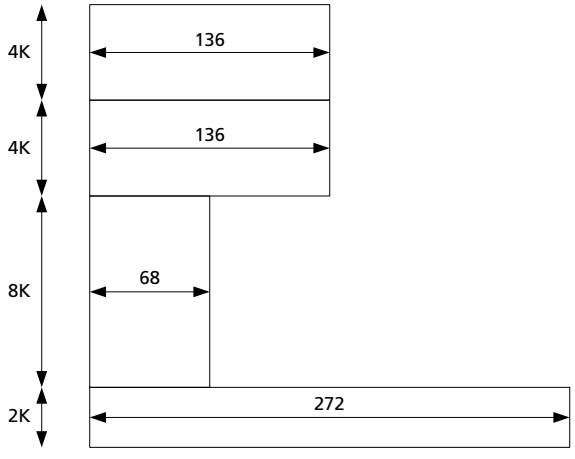
Multiple Search Table Configuration

Each Harmony quadrant may be configured individually to a width of 68, 136, or 272 bits. For example, if the CFG bits [16:9] are set to 10000101 then a 2Mb device would be configured to support tables in these widths: two quadrants of 4K x 136 bits, one quadrant of 8K x 68 bits, and one quadrant of 2K x 272 bits, respectively, as shown in Figure 5.

TCAM Array Addressing

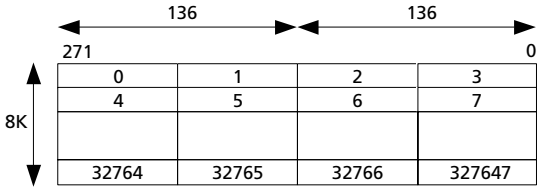
READ and WRITE access to the TCAM array is based on 68-bit segments. The 1Mb Harmony addresses are 0–16,383 and the 2Mb Harmony addresses are 0–32,767. The address range for each quadrant is shown in Table 5. Figures 6, 7, and 8 illustrate the segment address configuration into 272-, 136-, and 68-bit words. SEARCH operations report the lowest segment address of the matching word. For example, in a 136-bit search, the LSB of the match index is “0;” in a 272-bit search, the two LSBs are “0.”

Figure 5. Different Width Example



CFG = 10000101

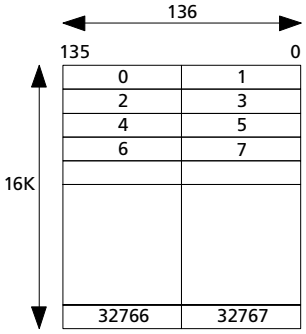
Figure 6. 272-Bit (Double-Word) Configuration (2Mb)



CFG = 10101010
(272-Bit Configuration)

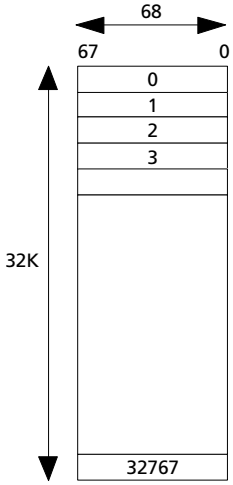
Note: The WRITE NEXT FREE ADDRESS operation is not supported in 272-bit mode.

Figure 7. 136-Bit (Single-Word) Configuration (2Mb)



CFG = 01010101
(136-Bit Configuration)

Figure 8. 68-Bit (Half-Word) Configuration (2Mb)



CFG = 00000000
(68-Bit Configuration)

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Depth Cascading to Create Larger Logical Tables

Some high-performance applications require larger tables than can be provided by one device. For these specific applications, up to eight Harmony devices can be depth cascaded to form larger table sizes without a loss of throughput or external glue logic.

When more than one Harmony device is required, the host ASIC must set the TLSZ field of the Instruction Register to "01" and LCAM (bit 7 in the Instruction Register) to "1" in the last Harmony device of the depth-cascaded chain. The LCAM bit of all previous devices in the depth-cascaded chain must then be set to "0." Similarly, the last TCAM on the SRAM bus must have LRAM (bit 8 in the Configuration Register) set to "1." The LRAM bit of the other Harmony devices must then be set to "0." Harmony performs all of the necessary arbitration to determine which device drives the SRAM bus.

When the TLSZ field is set to "1," the MF, MM#, and MV signals have five clock cycles of latency. When a single Harmony device is used, the TLSZ field of the Instruction Register can be set to "0" to reduce the latency from five or six, to four clock cycles. Although the latency of the searches increases proportionally with the table sizes, the search rate remains constant. For each search, if the device determines a match within the device, then the CSO[1] and CSO[0] signals are asserted.

REGISTER DESCRIPTIONS

The Harmony device contains 16 comparand registers, the global mask register (consisting of nine registers), result, instruction, information, burst read, burst write, next free address, and configuration registers. Table 7 provides an overview of the Harmony registers, which are listed in ascending address order. Each register group is described in the following subsections. Figure 9 shows the data path and relationships between the registers, the TCAM array, and the DQ I/O port.

COMPARAND REGISTERS

The device contains sixteen 136-bit comparand registers dynamically selected in every SEARCH operation to store the comparand presented on the DQ bus. These registers are used later by the WRITE NEXT FREE ADDRESS.

In Cycle A of the SEARCH instruction, Harmony stores the search data bits[135:68]) in the even-number comparand registers. In Cycle B, Harmony stores the search data bits[67:0] in the odd-numbered comparand registers. See Figure 10 on page 13.

Table 7: Register Overview

ADDRESS	ABBREVIATION	TYPE	NAME
0–31	CMPR[0–31]	R	Sixteen 136-bit comparand registers. Stores comparands from the DQ bus for writing later.
32–47	GMR[0-7]	R/W	Eight 136-bit global mask registers
48–55	RR[0–7]	R	Eight result registers
56	INSTR	R/W	Instruction register
57	INFO	R	Information register
58	RBAR	R/W	Burst read address register
59	WBAR	R/W	Burst write address register
60	NFA	R	Next free address register
61	CONFIG	R/W	Configuration register
62–63	N/A	N/A	Reserved

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Figure 9. Internal Datapath Diagram of the Harmony Registers

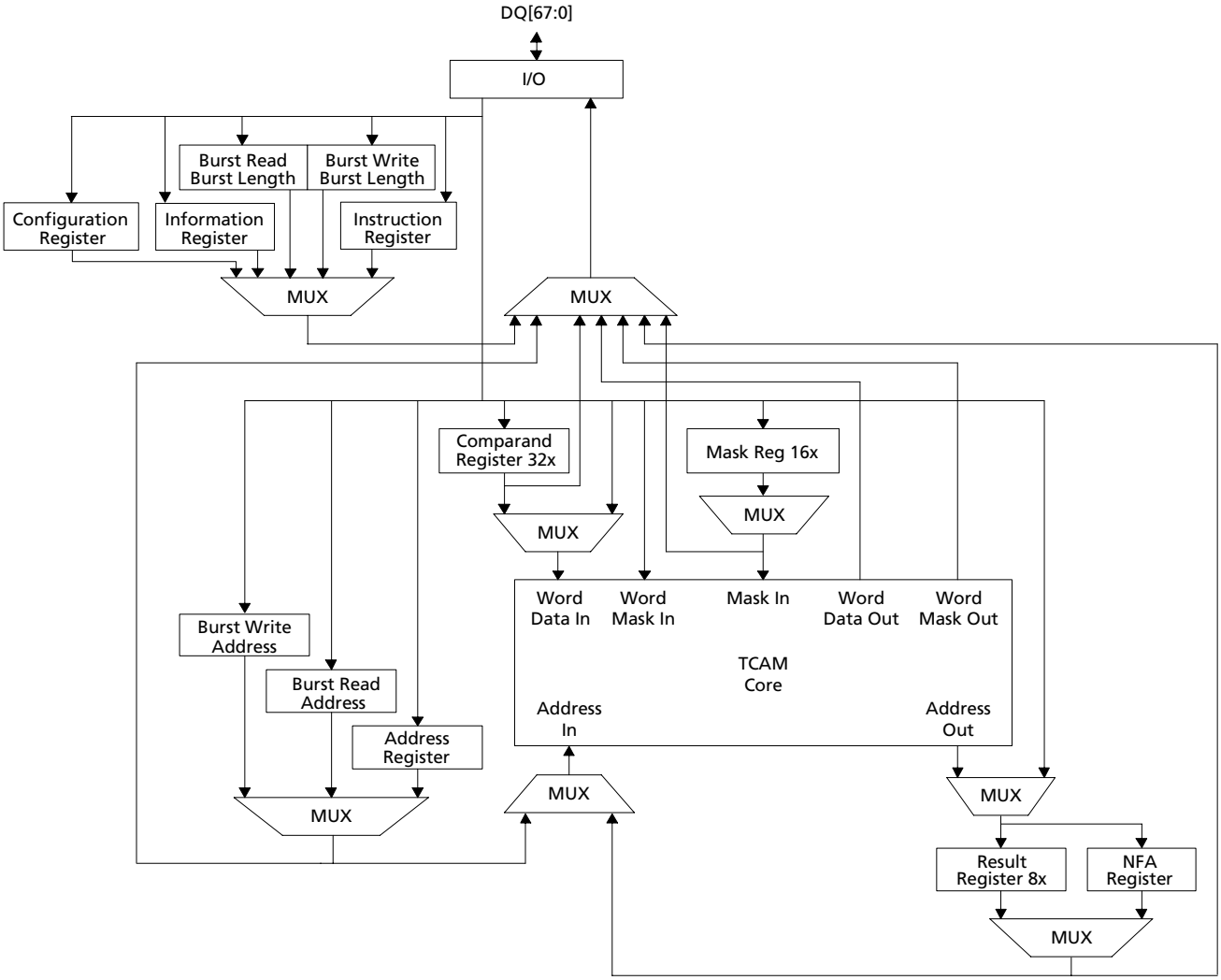
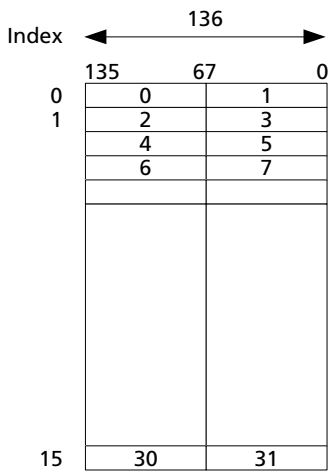


Figure 10. Comparand Registers Address and Usage



GLOBAL MASK REGISTERS

The device contains eight 136-bit global mask registers dynamically selected in every SEARCH operation to select the search subfield. Figure 11 on page 14 specifies the address of these registers. The 3-bit global search or write index supplied on the instruction bus applies one of eight global masks during the SEARCH and WRITE operations, as shown in 11.

Table 8: Comparand Register

BIT(S)	NAME	INIT VALUE	DESCRIPTION
67:0	Comp	0	Comparand Value

Table 9: Comparand Mask Register

BIT(S)	NAME	INIT VALUE	DESCRIPTION
67:0	Mask	0	Global Mask Value

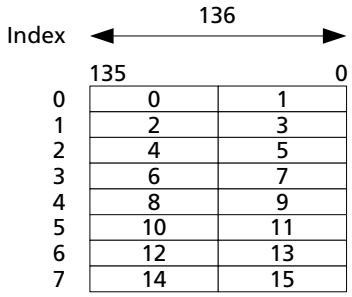
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Note that in a 68-bit configuration, the host must program the even and odd mask registers with the same value; Harmony uses even-numbered mask registers as global masks.

A mask bit in the global mask registers is used during SEARCH and WRITE operations. In SEARCH operations, setting the mask bit to "1" enables compares; setting the mask bit to "0" disables compares (forced match) at the current bit position. In WRITE operations to the data or mask array, setting the mask bit to "1" enables writes; setting the mask bit to "0" disables writes at the current bit position.

Figure 11. Addressing the Global Mask Register



SEARCH and WRITE Command Global Mask Selection

During a SEARCH operation, the search data bit, data bit, mask bit, and the global mask bit are used to generate a match at each bit position (see Table 10). A search is successful when an entry match occurs on all bit positions.

Table 10: SEARCH Bit Position Truth Table

GLOBAL MASK	TCAM MASK	TCAM DATA	SEARCH DATA	MATCH
0	x	x	x	Yes
1	0	x	x	Yes
1	1	0	0	Yes
1	1	1	0	No
1	1	0	1	No
1	1	1	1	Yes

RESULT REGISTERS

The device contains eight result registers to hold the lowest match address (LMA) found during a SEARCH operation. The SEARCH instruction specifies which result register to use during Cycle B of the SEARCH instruction.

The host can then use this register to access the data or mask of the word at the LMA or the external SRAM data by using the index as part of the address (See "SRAM Addressing" on page 3). The device with a valid bit set performs a READ or WRITE operation. All other devices suppress the operation.

Table 11: Result Register (1Mb)

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[13:0]	INDEX	x	**Index**. This is the address of the 68-bit entry where a successful search occurs. The device updates this field if it has a successful search. In 136-bit, the LSB is 0; in a 272-bit configuration, the two LSBs are "00."
[30:14]	N/A	0	**Reserved.**
[31]	VALID	0	**Valid**. The device sets this bit to "1" if it is a global winner (first Harmony downstream with a match) in a SEARCH operation.
[67:32]	N/A	0	**Reserved.**

Table 12: Result Register (2Mb)

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[14:0]	INDEX	x	**Index**. This is the address of the 68-bit entry where a successful search occurs. The device updates this field if it has a successful search. In 136-bit, the LSB is "0"; in a 272-bit configuration, the two LSBs are "00."
[30:15]	N/A	0	**Reserved.**
[31]	VALID	0	**Valid**. The device sets this bit to "1" if it is a global winner (first Harmony downstream with a match) in a SEARCH operation.
[67:32]	N/A	0	**Reserved.**

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INSTRUCTION REGISTER

Table 13: Instruction Register

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[0]	SRST	0	**Software Reset**. If "1," this bit resets the device with the same effect as a hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to a "0" if written with a "1."
[1]	DEVE	0	**Device Enable**. If "0," the device does not perform any SEARCH, WRITE, WRITE NEXT FREE ADDRESS, and READ operations, and it keeps the SRAM bus in three-state condition, forcing the cascade interface outputs to "0."
[3:2]	TLSZ	01	**Table Size**. The host must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the SEARCH and WRITE NEXT FREE ADDRESS operations, as well as the accesses to the SRAM (SADR[21:0], CE#, OE#, WE#, ALE#, MV, MF, MM#, and ACK). Once programmed, the search latency stays constant. **Number of Devices** **CLK** 00:1 device 4 01:2-8 devices 5 10:9-31 devices 6 11:Reserved
[6:4]	RLAT	000	**Latency of match Signals**. This field adds latency to the MF, MV, MM#, and ACK signals by the following number of CLK cycles during SEARCH operations. 000:0 100:4 001:1 101:5 010:2 110:6 011:3 111:7
[7]	LCAM	0	**Last TCAM in Table**. This device is the last TCAM in the depth-cascaded table. In the event of a search failure, the device with this bit set drives the match signals as follows: MF = 0, MV = 1 During nonsearch cycles, the device with this bit set drives the signals as follows: MF = 0, MV = 0
[8]	LRAM	0	**Last TCAM on this SRAM Bus**. This device is the last TCAM on this SRAM bus. In cycles where a TCAM does not drive the SRAM bus, the device with this bit set drives the SRAM bus (SADR, CE#, and WE#) in their inactive state. This bit sets a default driver for the SRAM control signals (SADR, CE#, WE#, and OE#). OE# is always asserted or deasserted.
[16:9]	CFG	00000000	**Table Configuration**. The device is internally divided into four quadrants, each of which can be configured as 8K x 68, 4K x 136, or 2K x 272 as follows: 00:8K x 68 (2Mb) 01:4K x 136 (2Mb) 10:2K x 272 (2Mb) 11:Reserved Bits[10:9] apply to configuring the first quadrant in the address space. Bits[12:11] apply to configuring the second quadrant in the address space. Bits[14:13] apply to configuring the third quadrant in the address space. Bits[16:15] apply to configuring the fourth quadrant in the address space.
[67:17]	N/A	0	**Reserved.**

INFORMATION REGISTER

Table 14: Information Register

BIT(S)	NAME	VALUE	DESCRIPTION
[11:0]	MFD	000100110011	**Manufacturer ID**. These bits include the JTAG bit LSB = 1.
[27:12]	DEVID	1Mb = 1010110100000010 2Mb = 1010110100000001	**Device Identification**. These bits indicate the device identification number.
[31:28]	RVSN	0001	**Revision Number.** This is the current device revision number. This number increments by one for each revision of the device.
[67:32]	N/A		**Reserved.**

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BURST READ ADDRESS REGISTER

The burst read address register fields must be programmed before each burst READ operation.

Table 15: Burst Read Address Register

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[14:0]	ADDR	0	**Address**. This is the starting address of the location of the TCAM array during a BURST READ operation. It automatically increments by one for each successive READ of the TCAM array. Bit 14 is reserved (set to "0") in the 1Mb device.
[18:15]	N/A	0	**Reserved.**
[27:19]	BLEN	0	**Length of Burst Access**. The device can READ from 4 up to 511 locations in a burst mode. Up to the maximum number of devices, this decrements back to 0.
[67:28]	N/A	0	**Reserved.**

BURST WRITE ADDRESS REGISTER

The burst write address register fields must be programmed before BURST WRITE operations.

Table 16: Burst Write Address Register

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[14:0]	ADDR	0	**Address**. This is the starting address of the location of the TCAM array during a BURST WRITE operation. It automatically increments by one for each successive WRITE of the TCAM array. Bit 14 is reserved (set to "0") in the 1Mb device.
[18:15]	N/A	0	**Reserved.**
[27:19]	BLEN	0	**Length of Burst Access**. The device provides the capability to write from 4 up to 511 locations in a burst mode. Up to the maximum number of devices, this decrements back to 0.
[67:28]	N/A	0	**Reserved.**

NEXT FREE ADDRESS REGISTER

Bit 0 of each entry (regardless of width) is a special bit designated for use in the operation of the WRITE NEXT FREE ADDRESS instruction. In 68-bit configurations, bit 0 indicates whether a location is full (bit set to "1") or empty (bit set to "0"). Every WRITE and WRITE NEXT FREE ADDRESS instruction loads the address of the first 68-bit location that contains a "0" in the entry's bit 0. This is stored in the Next Free Address Register. When the bits of the LSB in a device are set to "1," Harmony asserts FO[1:0] to "11." FF should also be set to "1" in each data word.

In 136-bit configurations, the LSB of this register is always set to "0." Regardless of the configured word width, the host must set bit 0 of each word to "0" (empty) or "1" (full) to indicate the full/empty status of each entry.

Table 17: Next Free Address Register

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[14:0]	IDX	0	**Index.**
[67:15]	N/A	0	**Reserved.**

CONFIGURATION REGISTER

Table 18: Configuration Register

BIT(S)	NAME	INITIAL VALUE	DESCRIPTION
[0]	SENE	0	**Enable Search Enable**. When this bit is set to "1," SEN[3:0] are enabled. These pins are individual quadrant enables. When SENE is set to "0," the SEN[3:0] pins have no effect.
[1]	MME	0	**Multi-Match Enable**. When this bit is set to "1," the MM# output is enabled. Otherwise, the MM# is disabled (three-state).
[2]	SCE	0	**SCLK Enable**. When this bit is set to "1," the SCLK output is enabled. Otherwise, the SCLK output is disabled (three-state).
[67:3]	N/A	0	**Reserved.**

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HARMONY INSTRUCTIONS

INSTRUCTION							OP[8:0] BUS				DQ[67:0] BUS							
TYPE	WIDTH	DATA SOURCE	DATA DESTINATION	ADDRESS SOURCE	ADDRESS DESTINATION	CYCLE	OP[8:6]	OP[5:3]	OP[2]	OP[1:0]	DQ[67:30]	DQ[29]	DQ[28:26]	DQ[25:21]	DQ[20:19]	DQ[18:15]	DQ[14:6]	DQ[5:0]
Read CAM Data Direct	68	CAM Array	DQ[67:0]	DQ[14:0]	N/A	1A/B	X	X	0	00	X	0	X	UID	00	X	Address[14:0]	
						2A/B	X	X	X	X	High-Z							
Read CAM Mask Direct	68	CAM Array	DQ[67:0]	DQ[14:0]	N/A	1A/B	X	X	0	00	X	0	X	UID	01	X	Address[14:0]	
						2A/B	X	X	X	X	High-Z							
Read CAM Data Indirect	68	CAM Array	DQ[67:0]	RR	N/A	1A/B	X	X	0	00	X	1	RR	UID	00	X		
						2A/B	X	X	X	X	High-Z							
Read CAM Mask Indirect	68	CAM Array	DQ[67:0]	RR	N/A	1A/B	X	X	0	00	X	1	RR	UID	01	X		
						2A/B	X	X	X	X	High-Z							
Read CAM Data Burst	68	CAM Array	DQ[67:0]	RBAR	N/A	1A/B	X	X	1	00		X		UID	00	X		
						2A/B	X	X	X	X	High-Z							
Read CAM Mask Burst	68	CAM Array	DQ[67:0]	RBAR	N/A	1A/B	X	X	1	00		X		UID	01	X		
						2A/B	X	X	X	X	High-Z							
Read SRAM Direct	68	N/A	N/A	DQ[14:0]	SADR[21:0]	1A/B	SADR[21:19]	X	0	00	X	0	X	UID	10	X	Address[14:0]	
						2A/B	X	X	X	X	High-Z							
Read SRAM Indirect	68	N/A	N/A	RR	SADR[21:0]	1A/B	SADR[21:19]	X	0	00	X	1	RR	UID	10	X		
						2A/B	X	X	X	X	High-Z							
Read Register	68	Register	DQ[67:0]	N/A	N/A	1A/B	X	X	0	00		X		UID	11	X		REG
						2A/B	X	X	X	X	High-Z							
Write CAM Data Direct	68	DQ[67:0]	CAM Array	DQ[14:0]	N/A	1A/B	X	GMR	0	01	X	0	X	UID	00	X	Address[14:0]	
						2A/B	X	X	X	X	Data[67:0]							
Write CAM Mask Direct	68	DQ[67:0]	CAM Array	DQ[14:0]	N/A	1A/B	X	GMR	0	01	X	0	X	UID	01	X	Address[14:0]	
						2A/B	X	X	X	X	Data[67:0]							
Write CAM Data Indirect	68	DQ[67:0]	CAM Array	RR	N/A	1A/B	X	GMR	0	01	X	1	RR	UID	00	X		
						2A/B	X	X	X	X	Data[67:0]							
Write CAM Mask Indirect	68	DQ[67:0]	CAM Array	RR	N/A	1A/B	X	GMR	0	01	X	1	RR	UID	01	X		
						2A/B	X	X	X	X	Data[67:0]							
Write Data Burst	68	DQ[67:0]	CAM Array	WBAR	N/A	1A/B	X	GMR	1	01		X		UID	00	X		
						2A/B	X	X	X	X	Data[67:0]							
Write Mask Burst	68	DQ[67:0]	CAM Array	WBAR	N/A	1A/B	X	GMR	1	01		X		UID	01	X		
						2A/B	X	X	X	X	Data[67:0]							
Write SRAM Direct	68	N/A	N/A	DQ[14:0]	SADR[21:0]	1A/B	SADR[21:19]	X	0	01	X	0	X	UID	10	X	Address[14:0]	
						2A/B	X	X	X	X	X							
Write SRAM Indirect	68	N/A	N/A	RR	SADR[21:0]	1A/B	SADR[21:19]	X	0	01	X	1	RR	UID	10	X		
						2A/B	X	X	X	X	X							
Write Register	68	DQ[67:0]	Register	N/A	N/A	1A/B	X	X	0	01		X		UID	11	X		REG
						2A/B	X	X	X	X	Data[67:0]							
Search	68	DQ[67:0]	CAM Array, CR	N/A	SADR[21:0]	1A	SADR[21:19]	GMR	0	10	Data[67:0]							
						1B	RR	CR		10	Data[67:0]							
Search	136	DQ[67:0]	CAM Array, CR	N/A	SADR[21:0]	1A	SADR[21:19]	GMR	0	10	Data[135:68]							
						1B	RR	CR		10	Data[67:0]							
Search	272	DQ[67:0]	CAM Array	N/A	SADR[21:0]	1A	SADR[21:19]	GMR	1	10	Data[271:204]							
						1B	RR	CR		10	Data[203:136]							
						2A	SADR[21:19]	GMR	X	10	Data[135:68]							
						2B	RR	CR		10	Data[67:0]							
Write NFA	68	CR	CAM Array	NFA	SADR[21:0]	1A	SADR[21:19]	CR		11	X							
						1B	XX0	CR		11	X							
Write NFA	136	CR	CAM Array	NFA	SADR[21:0]	1A	SADR[21:19]	CR		11	X							
						1B	XX1	CR		11	X							

CR = Comparand Register GMR = Global Mask Register NFA = Next Free Address Register RBAR = Read Burst Address Register REG = Register Address RR = Result Register WBAR = Write Burst Address Register

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Table 19: Instruction Set Overview

INSTRUCTION	DATA SOURCE	DATA DESTINATION	PARAMETER 1	PARAMETER 2	THROUGHPUT (CLK CYCLES)
Search (68/136-bit)	CAM data bus (DQ[67:0])	SRAM address bus SADR[21:0]	Global Mask Register	Data width = 68 or 136	2
Search (272-bit)	CAM Data Bus (DQ[67:0])	SRAM address bus SADR[21:0]	Global Mask Register	N/A	4
Read (68-bit)	CAM data, CAM mask, or SRAM	CAM data bus, SRAM data bus (DQ[67:0])/SADR[21:0]	Read address = Input address, lowest match address	Single (N =1) or Burst (N> = 4)	6+4*N
Read Register (68-bit)	Register	CAM data bus, SRAM data bus (DQ[678:0])	Register number	N/A	10
Write (68-bit)	CAM data bus (DQ[67:0])	CAM data, CAM mask, or SRAM	Write address = Input address, lowest match address	Single (N = 1) or Burst (N> = 4)	4+2*N
Write Register (68 bit)	CAM data bus (DQ[67:0])	Register	Register number	N/A	6
Write Next Free Address 68/136-bit)	Comparand Register	CAM data	Data width = 68 or 136	N/A	4

INSTRUCTION CODES

A master device, such as a controller, issues instructions to Harmony using the OP-CODE VALID (OPV) signal and the instruction bus. The following subsections describe the functions of the instructions. Table 19 provides an overview of the instructions that can be performed by Harmony. Harmony implements four basic instructions. OP[1:0] applies the instructions to the device when the OPV signal is kept HIGH for two CLK cycles. These two CLK cycles are designated as Cycle A (PHASE# HIGH at rising edge of CLK) and Cycle B (PHASE# LOW).

The OP[8:2] field passes the parameters of the instruction in Cycles A and B. The controller must align the instructions with the PHASE# and CLK signals.

Table 20: Instruction Pipeline

INSTRUCTION	TOTAL CLK CYCLES	CLK CYCLE 1A	CLK CYCLE 1B	CLK CYCLE 2A	CLK CYCLE 2B	CLK CYCLE 3A/B	CLK CYCLE 4A/B	CLK CYCLE 5A/B	CLK CYCLE 6A/B	CLK CYCLE 7A/B
Search (68-bit)	2	Search data 67:0 (input)	Search data 67:0 (input)	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Search (136-bit)	2	Search data 135:68 (input)	Search data 67:0 (input)	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Search (272-bit)	4	Search data 271:204 (input)	Search data 203:136 (input)	Search data 135:68 (input)	Search data 67:0 (input)	N/A	N/A	N/A	N/A	N/A
Read (single)	5	Read address (input)	Read address (input)	<None>	<None>	<None>	<None>	Data (output)	<None>	N/A
Read (burst)	6+4*N	Read address (input)	Read address (input)	<None>	<None>	<None>	<None>	Data (output)	<None>	Data (output)
Write (single)	4	Write address (input)	Write address (input)	Write data 67:0 (input)	Write data 67:0 (input)	<None>	N/A	N/A	N/A	N/A
Write (burst)	4+2*N	Write address	Write address	Write data 1 67:0 (input)	Write data 1 67:0 (input)	Write data 2 67:0 (input)	Write data 3 67:0 (input)	Write data 4 67:0 (input)	<None>	N/A
Write (NFA)	4	<None> (OP only)	<None> (OP only)	<None>	<None>	N/A	N/A	N/A	N/A	N/A

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INSTRUCTIONS AND INSTRUCTION PARAMETERS

Table 21 lists the instruction bus fields that contain Harmony instruction parameters and their respective cycles. Each instruction is described in more detail in the subsections that follow the table. See Table 10 on page 14 for the Bit Position Truth Table used during SEARCH instructions

Table 21: Instruction Parameters

INSTRUCTION	CYCLE	8	7	6	5	4	3	2	1	0
READ	A	SADR[21][1]	SADR[20][1]	SADR[19][1]	0	0	0	0 = Single 1 = Burst	0	0
	B	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
WRITE	A	SADR[21][1]	SADR[20][1]	SADR[19][1]	Global mask register index			0 = Single 1 = Burst	0	1
	B	0	0	0	Global mask register index			0 = Single 1 = Burst	0	1
SEARCH	A	SADR[21]	SADR[20]	SADR[19]	Global mask register index			68-bit or 136-bit: 0 272-bit: 1 in first Cycle 0 in second Cycle	1	0
	B	Result register index[2:0]			Comparand register index				1	0
WRITE NEXT FREE ADDRESS[2]	A	SADR[21]	SADR[20]	SADR[19]	Comparand register index				1	1
	B	0	0	Mode 0:68-bit 1:136-bit	Comparand register index				1	1

SADR[19] is only available on the 1Mb Harmony device. This bit is "X" ("Don't Care") on the 2Mb device.

[1] For SRAM reads and writes only. For all other READ and WRITE instructions, these bits are "X" ("Don't Care").
[2] The WRITE NEXT FREE ADDRESS instruction is not supported when the table width is 272 bits. A word in use must have bit 0 set to "1." An empty word must have bit 0 set to "0."

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SEARCH INSTRUCTIONS

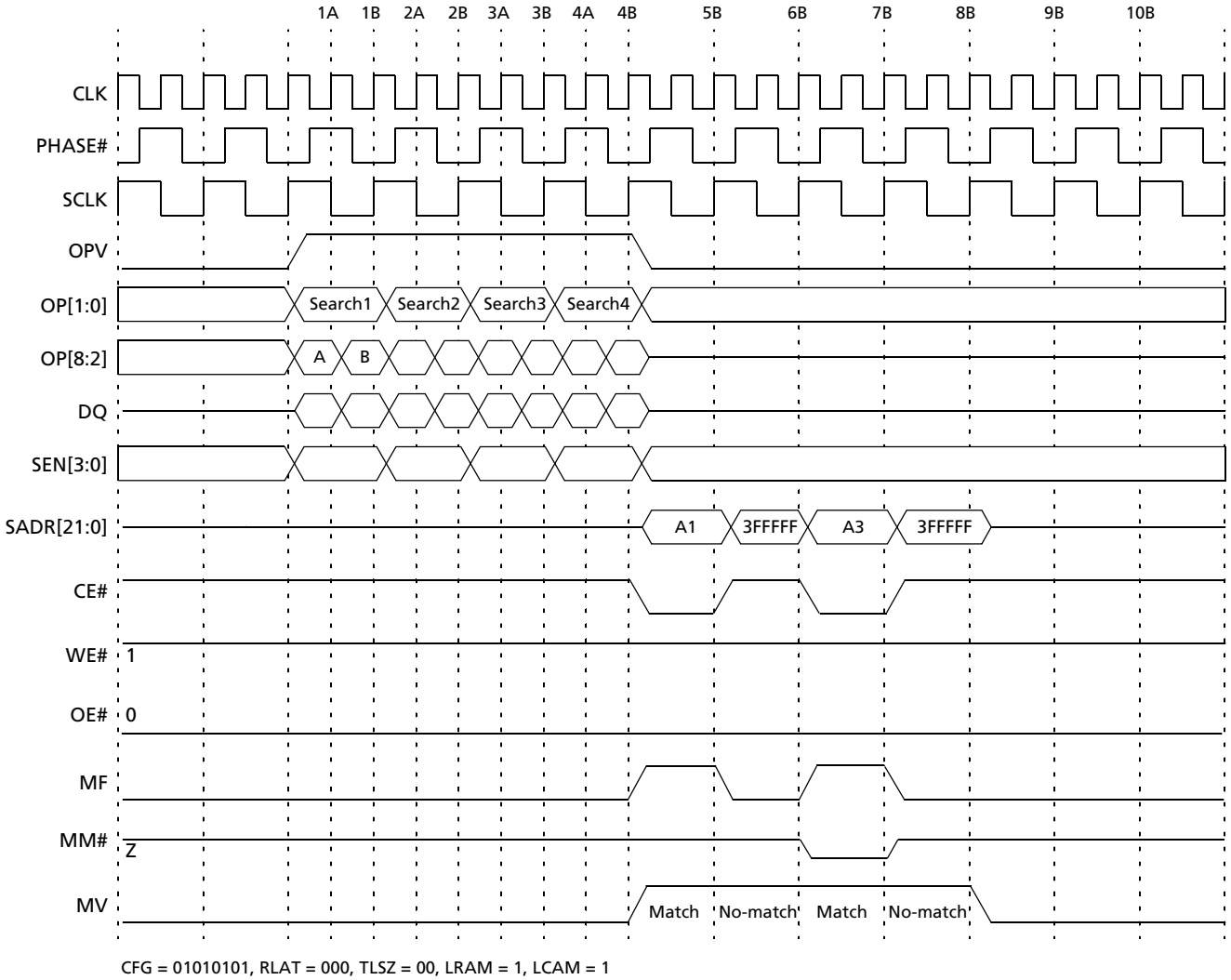
136-Bit Full Word Search Instruction

In the first cycle of full word searches, the host drives the OPV HIGH and applies the instruction on OP[8:0]. For the SEARCH operation, OP[5:3] carries the index to the Global Mask Register, whereas OP[8:6] carries the address to be matched on SADR[21:19]. DQ[67:0] then transports the data to compare with the TCAM array's [135:68] field.

In the second cycle, the host drives the OPV HIGH and applies the instruction to OP[8:0], and OP[5:2] transports the index to the Comparand Registers and then sends the full 136-bit word (which was presented during the first and second cycles) to the DQ bus. OP[8:6] carries the index to the Result Register to store the matching index and the match valid flag, while DQ[67:0] carries the data to be compared with TCAM array bits 0-67. The results of the SEARCH instruction then appear as a pipelined cycle.

The pipelined SEARCH instruction completes in two clock cycles. All SRAM interface signals, MV, MF, and MM# shift to the right for different values of TLSZ. Additionally, MV, MF, and MM# shift to the right for different values of RLAT. See Table 13 on page 15 and for the TLSZ and RLAT shift values

Figure 12. 136-Bit SEARCH Operation Timing Diagram



CFG = 01010101, RLAT = 000, TLSZ = 00, LRAM = 1, LCAM = 1

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68-Bit Half Word SEARCH Instruction

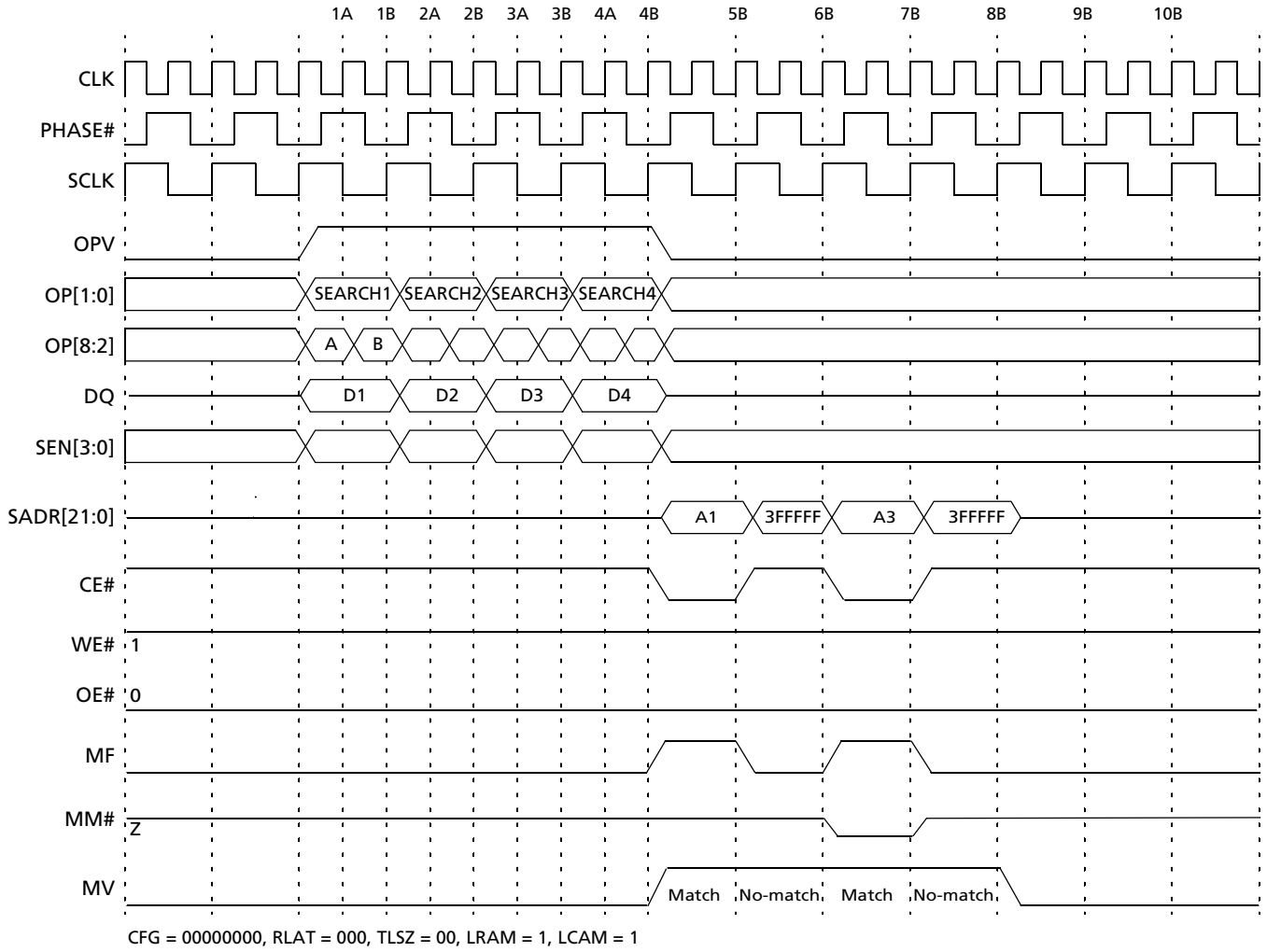
In the first cycle of half-word searches, the host drives the OPV HIGH and applies the instruction to OP[8:0]. For the SEARCH instruction, OP[5:3] carries the index to the Global Mask Register, while OP[8:6] carries the address to be output on SADR[21:19]. The DQ[67:0] then transports the data to be compared with the TCAM array's [67:0] field.

In the second cycle, the host drives the OPV HIGH and applies the instruction to the OP[8:0] field. The OP[5:2] transports the index to the Comparand Registers to be stored, and then sends the half 68-bit word, which was presented during the first and second cycles, to the DQ bus. The OP[8:6] transports the index to the Result Register to store the match index and the match valid flag. The full word SEARCH instruction completes in four clock cycles after an initial latency search of four clock cycles; however, because the instruction is pipelined, searches can be performed every two cycles.

All SRAM interface signals, MV, MF, and MM# shift to the right for different values of TLSZ. Additionally, MV, MF, and MM# shift to the right for different values of RLAT. See Table 13 on page 15 for the TLSZ and RLAT shift values.

Note: In the 68-bit configuration, the host must supply the same data on DQ[67:0] during the first and second cycles.

Figure 13. 68-Bit SEARCH Operation Timing Diagram



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272-Bit Double Word SEARCH Instruction

The double word SEARCH instruction completes in four clock cycles after an initial latency search of four clock cycles. However, because the instruction is pipelined, searches can be performed every two cycles.

During the first cycle, the host drives the OPV HIGH and applies the instruction on OP[8:0]. In this cycle OP[2] must be set to "1." OP[5:3] carries the Global Mask Register index to be applied to field [271:136] of the search data, while DQ[67:0] carries the data to be compared with the TCAM array's field of [271:204].

During the second cycle, the host also drives the OPV HIGH and applies the instruction on OP[8:0], while DQ[67:0] carries the data to be compared with the TCAM array's field of [203:136].

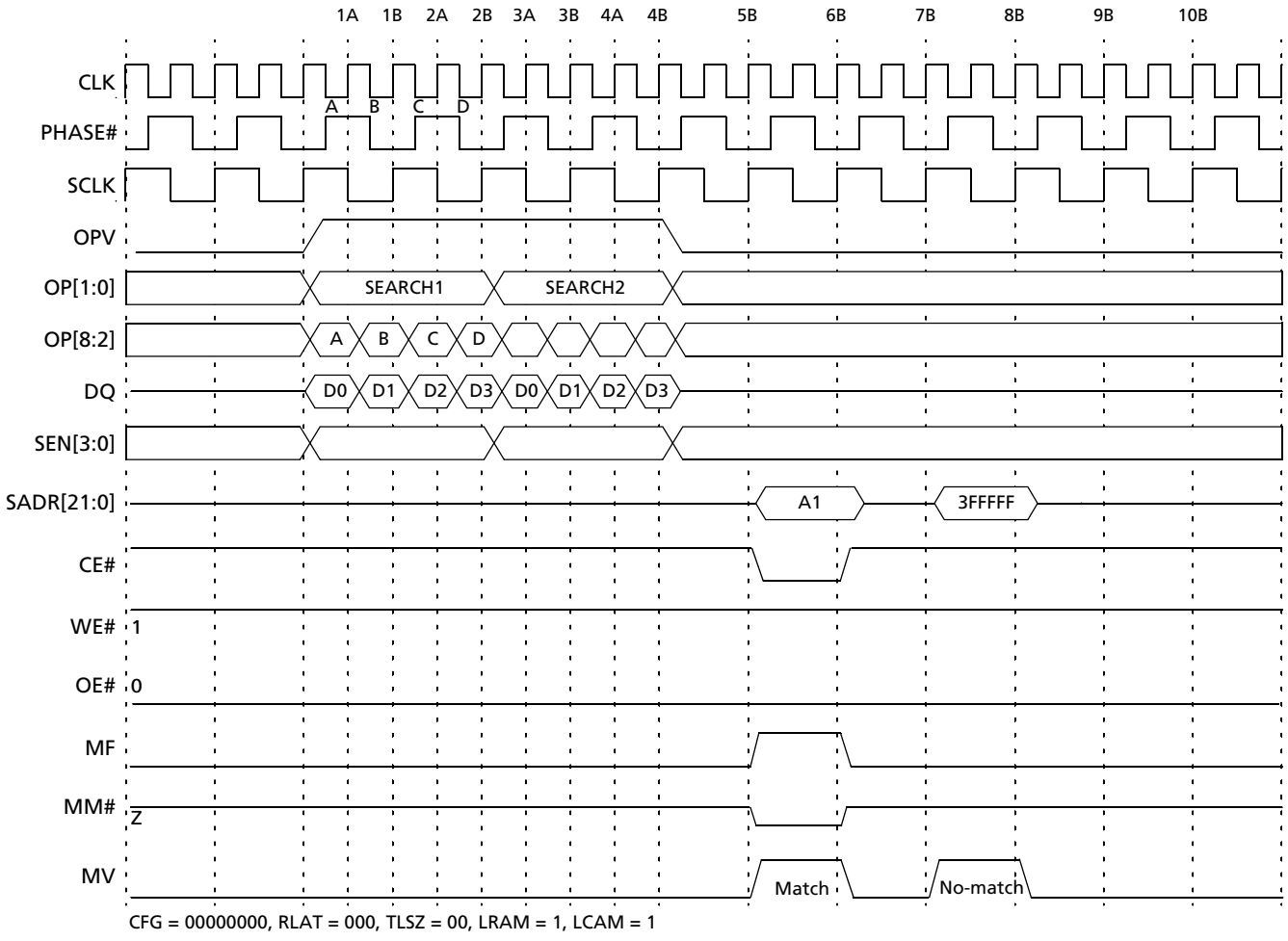
During the third cycle, the host continues to drive the OPV HIGH and to apply the instruction on OP[8:0]. In this cycle, OP[2] must be set to "0." OP[5:3] carries the Global Mask Register index to be applied to field [135:0] of the search data. OP[8:6] carries the address to be supplied on SADR[21:19] if the device has a successful match. The DQ[67:0] carries the data to be compared with the [135:68] field of the TCAM array.

During the fourth cycle, the host continues to drive OPV HIGH and applies the instruction on OP[8:0]. The DQ[67:0] carries the data to be compared against the [67:0] field of the TCAM array.

In the 272-bit configuration, the SEARCH instruction is completed in four clock cycles. The SEARCH instruction results appear as a pipelined cycle with its latency measured from the second cycle of the instruction.

For all SRAM interface signals, MV and MF shift to the right for different values of TLSZ. Additionally, MV, MF, and MM# shift to the right for different values of RLAT. See Table 13 on page 15 for the TLSZ and RLAT shift values.

Figure 14. 272-Bit SEARCH Operation Timing Diagram



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READ Instruction

The READ instruction parameters are detailed in Tables 22 and 23. Harmony can perform single location reads of the TCAM array or registers, or burst reads of the TCAM array. In addition, associated data stored in an external SRAM can be accessed a single location at a time.

Table 22: READ Instruction Parameters

INSTRUCTION PARAMETER OP[2]	READ INSTRUCTION	DESCRIPTION
0	SINGLE READ	Reads a single location of the TCAM array, external SRAM, or device registers. All access information is applied on the DQ bus.
1	BURST READ	Reads a block of locations from the TCAM array as a burst. The internal register (RBAR) specifies the starting address and the length of the data transfer from the TCAM array, and it auto-increments the address for each access. All other access information is applied on the DQ bus.

Note: The device registers and external SRAM can only be read in single-read mode.

Table 23: TCAM or SRAM Single READ Address Format

	DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:15]	DQ [14:6]	DQ [5:0]
TCAM Single Read	Reserved	0:Direct 1:Indirect	Result Register index (applicable when DQ[29] is indirect)	UID	0:TCAM	0:Data 1:Mask	Reserved	DQ[29] = 0. This field carries address of data location. DQ[29] = 1. The Result Register specified on DQ[28:26] supplies the address of the data location. DQ[14] is reserved (= 0) on the 1Mb Harmony device.	
TCAM Burst Read	Reserved							"Don't Care." These bits come from the Burst Read Address Register, which increments for each access.	
SRAM Single Read	Reserved	0:Direct 1:Indirect	Result Register index (applicable when DQ[29] is indirect)		1:SRAM	0		DQ[29] = 0. This field carries address of data location. DQ[29] = 1. The Result Register specified on DQ[28:26] supplies the address of the data location. DQ[14] is reserved (= 0) on the 1Mb Harmony device.	
Register Read	Reserved				11:Register		Reserved		Register Address

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Single READ Instruction

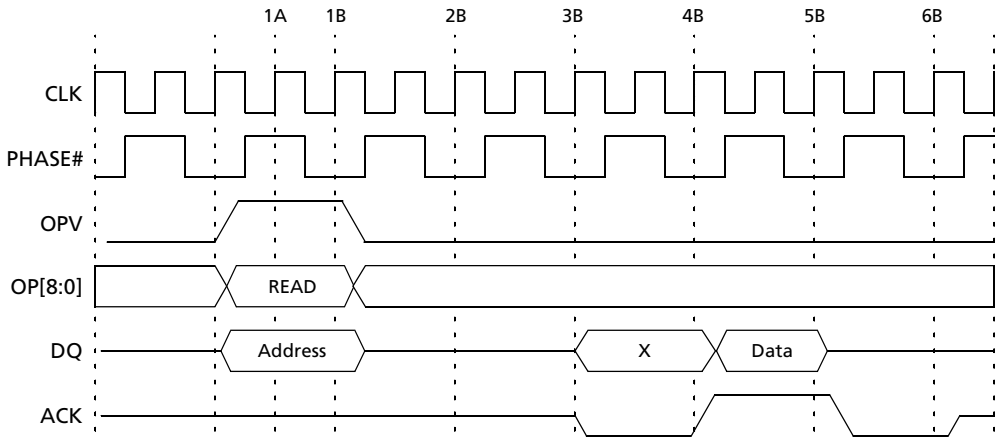
During the first cycle, the host ASIC configures the OP[1:0] (OP[2] = 0) using OPV = 1 and applies the READ instruction while the DQ bus supplies the address. The host selects the device for which UID[4:0] matches the DQ[25:21] lines or the last chained Harmony of the cascade when DQ[25:21] = 11111. The host ASIC also supplies SADR[21:19] on OP[8:6] in the first cycle of the READ instruction, if the READ has been applied to an external SRAM.

For the next two cycles, the host ASIC holds the DQ[67:0] bus in a three-stated, High-Z mode. Afterward, in the fourth cycle, the device selected by the host drives the DQ[67:0] bus and pulls the ACKNOWLEDGE (ACK) signal from Z to LOW. In the fifth cycle, the device selected by the host drives data to be read from the addressed location on DQ[67:0] and asserts the ACK signal HIGH.

Lastly, the selected device tri-states DQ[67:0] and deasserts ACK LOW. At termination of the last cycle, the selected device three-states the ACK, completes the single READ instruction, and prepares Harmony for the next instruction.

The READ instruction, configured as a SINGLE READ (OP[2] = 0) or as a BURST READ (OP[2] = 1), reads the TCAM array, SRAM, or register location.

Figure 15. Single Location READ



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Burst READ Instruction

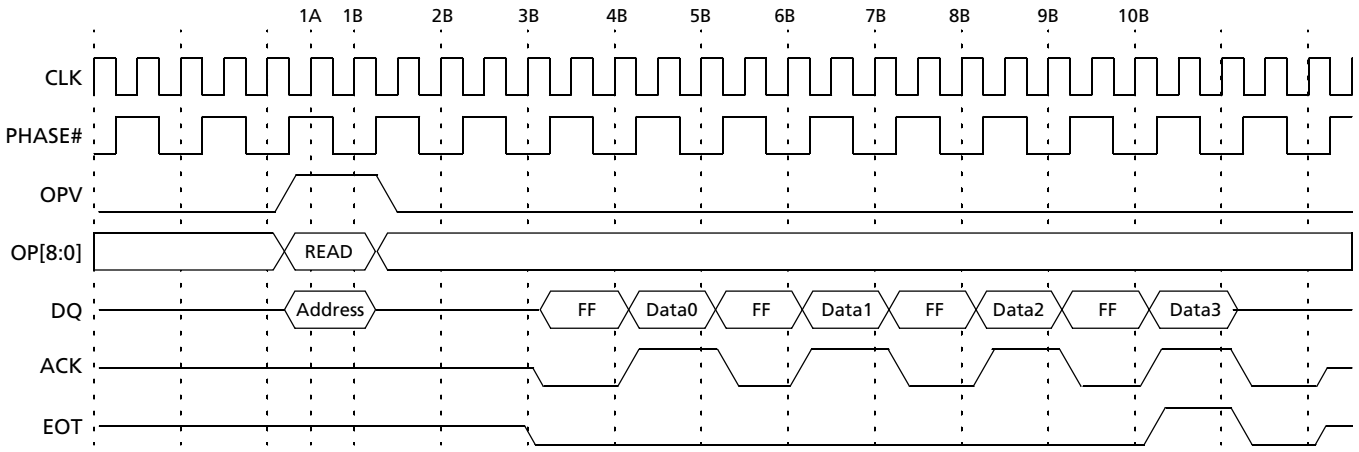
The burst length (BLEN) field of the Burst Read Address (RBAR) Register determines the latency of the BURST READ instruction. The BURST READ instruction completes in four clock cycles, plus twice the number of burst accesses. Note that before initiating the burst READ instruction, the host must first program the Burst Read Address Register with the start address and the length of transfer. The following sequence delineates the clock cycles required of the READ instruction:

In the first cycle, the host ASIC configures the OP[1:0] (OP[2] = 1), using OPV = 1 and applies the READ instruction, while the DQ bus supplies the address. The host then selects the device for which UID[4:0] matches the DQ[25:21] lines or the last chained device when DQ[25:21] = 11111.

For the next two cycles the host three-states (High-Z) DQ[67:0]. In the fourth cycle, the device selected by the host drives DQ[67:0] to signal the end of transfer (EOT), and deassert ACK from Z to LOW. In the fifth cycle, the selected device (selected by the host) drives the data to be read from the addressed location on DQ[67:0] and asserts ACK signal back HIGH. These fourth and fifth cycles are repeated until all of the specified accesses in the burst length (BLEN) field of the Burst Read Address Register are depleted.

On the last transfer, the selected device drives DQ[67:0] to a three-stated position, asserts the END OF TRANSFER (EOT) signal HIGH, and deasserts ACK to LOW. At the termination of the last cycle, cycle 4 + 2n (where n is the number of burst accesses), the selected device three-states the ACK signal, completes the BURST READ instruction, and prepares Harmony for the next instruction.

Figure 16. Data and Mask Burst READ (BLEN = 4)



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SRAM READ Instruction

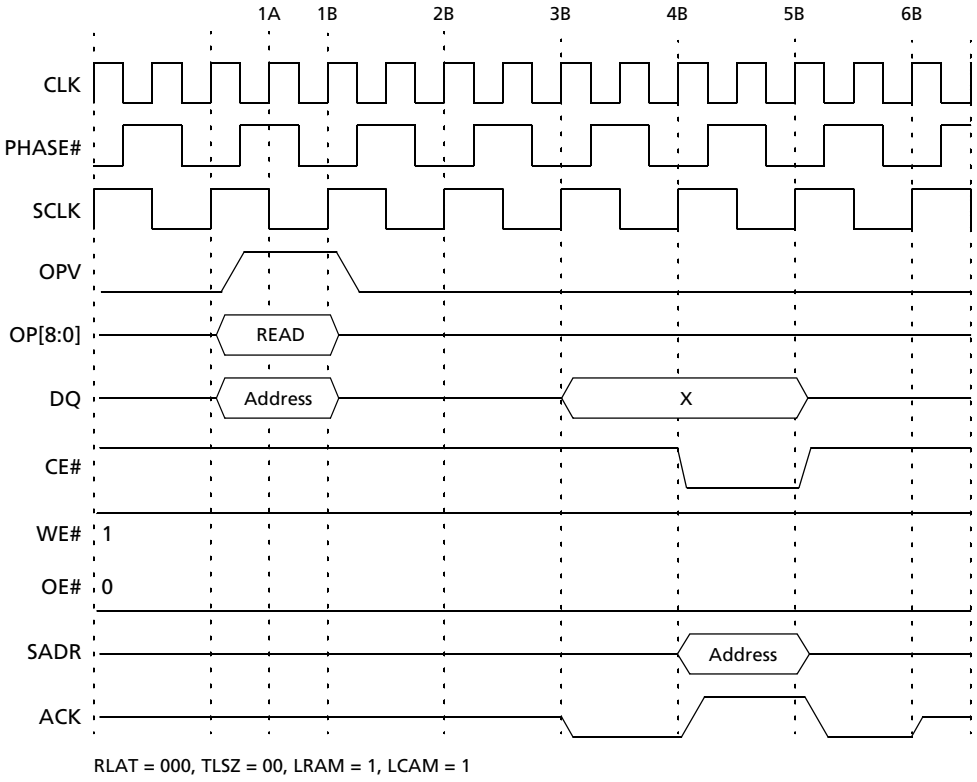
Associative data stored in the external SRAM is accessed by SRAM READ instructions. An instruction completes in six cycles, as described below.

In the first cycle, the host applies the READ instruction on OP[1:0] and sets the instruction data valid to 1 (OPV = 1). The DQ bus then supplies the appropriate address, sets DQ[20:19] to 10, and selects the SRAM address. The host selects the device for which the UID[4:0] matches DQ[25:21] and supplies SADR[21:19] to OP[8:6]. In the second and third cycles, the host three-states DQ[67:0].

In the fourth cycle, the selected device starts to drive DQ[67:0] and drives the ACK signal from High-Z to LOW. In the fifth cycle, the selected device drives the read address on SADR[21:0]; it also drives ACK HIGH, CE# LOW, and ALE# LOW. In the sixth cycle, the selected device three-states CE#, SADR, and the DQ bus and continues to drive ACK LOW. At the end of sixth cycle, the selected device three-states ACK.

SADR[13:0] contains the address supplied on the DQ bus during access to Harmony. Furthermore, OP[8:6] transports signals from the instruction bus to the SRAM[21:19] address bus.

Figure 17. SRAM READ Cycle



RLAT = 000, TLSZ = 00, LRAM = 1, LCAM = 1

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WRITE Instruction

The WRITE instruction can be configured as a SINGLE WRITE (OP[2] = 0) in a TCAM array, register, or external SRAM location; or to TCAM array locations as a BURST WRITE (OP[2] = 1) by using the internal auto-incrementing Burst Write Address Register. The SINGLE WRITE instruction can be completed in only three cycles. However, the BURST WRITE operation requires an additional cycle for each successive WRITE.

Table 24: WRITE Instruction Parameters

INSTRUCTION PARAMETER OP[2]	WRITE INSTRUCTION	DESCRIPTION
0	SINGLE WRITE	Writes a single location of the TCAM array, external SRAM, or device registers. All access information is applied on the DQ bus.
1	BURST WRITE	Writes a block of locations to the TCAM array as a burst. The Internal Register (RBAR) specifies the starting address and the length of the data transfer from the TCAM array, and it auto-increments the address for each access. All other access information is applied on the DQ bus.

Note: The Device Registers and external SRAM can only be written in single-write mode.

Table 25: TCAM or SRAM Single WRITE Address Format

	DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20]	DQ [19]	DQ [18:15]	DQ [14:6]	DQ [5:0]
TCAM Single Write	Reserved	0:Direct 1:Indirect	Result Register index (applicable when DQ[29] is indirect)	UID	0:TCAM	0:Data 1:Mask	Reserved	DQ[29] = 0. This field carries address of data location. DQ[29] = 1. The Result Register specified on DQ[28:26] supplies the address of the data location. DQ[14] is reserved (= 0) on the 1Mb Harmony device.	
TCAM Burst Write	Reserved							"Don't Care." These bits come from the Burst Write Address Register, which increments for each access.	
SRAM Single Write	Reserved	0:Direct 1:Indirect	Result Register index (applicable when DQ[29] is indirect)		1:SRAM	0		DQ[29] = 0. This field carries address of data location. DQ[29] = 1. The Result Register specified on DQ[28:26] supplies the address of the data location. DQ[14] is reserved (= 0) on the 1Mb Harmony device.	
Register Write	Reserved				11:Register		Reserved		Register Address

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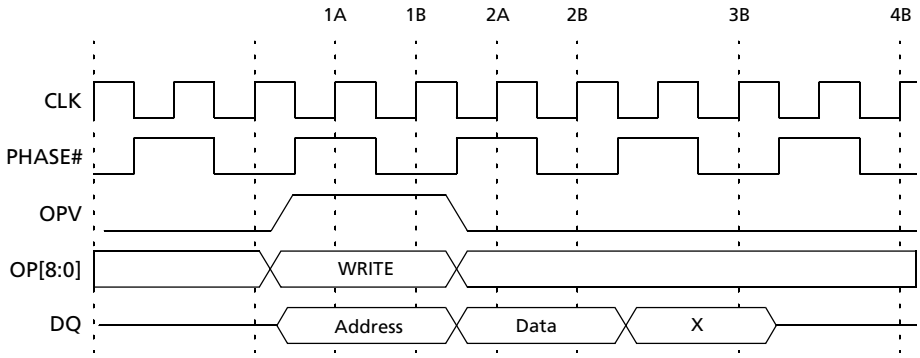
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Single WRITE Instruction

In the first cycle, the host applies the WRITE instruction on the OP[1:0] (OP[2] = 0), using OPV = 1 and the supplied address on the DQ bus. The host also supplies the index to the Global Mask Register to mask the WRITE instruction to the TCAM array's location in OP[5:3]. For the WRITE instruction, the host selects the device for which UID[4:0] matches DQ[25:21] or all connected devices when DQ[25:21] = 11111.

In the second cycle, the host drives DQ[67:0] with the data to be written to the TCAM array, external SRAM, or register location of the selected device. The third cycle is an idle cycle, and soon after this idle period the device is ready for the next instruction.

Figure 18. WRITE Cycle



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BURST WRITE Instruction

The BURST WRITE instruction operates for the number of burst accesses specified by the burst length (BLEN) field of the Burst Write Address Register, plus two additional clock cycles. Note that before initiating the BURST WRITE instruction, the host must program the Burst Write Address Register with the start address and the length of transfer, as indicated in the BLEN field. The following summarizes the sequence of the BURST WRITE instruction

In the first cycle, the host applies the WRITE instruction on OP[1:0] (OP[2] = 1) with OPV = 1 and the supplied address on the DQ bus. The host also supplies the index to the Global Mask Register to mask the WRITE to the TCAM array locations in OP[5:3]. The host then selects the device for which UID[4:0] matches the DQ[25:21] or all devices when DQ[25:21] = 11111.

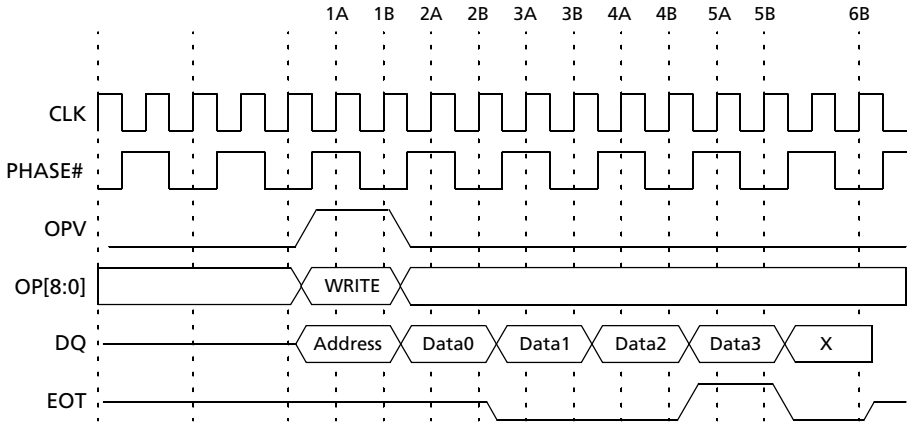
In the second cycle, the host drives DQ[67:0] with the data to be written to the TCAM array location of the selected device. On DQ[67:0], the host only writes the data to the corresponding subfield that has its mask bit set to "1" in the Global Mask Register. This is specified by the index OP[5:3] and supplied in the first cycle.

From the third cycle to the number of burst accesses (indicated by the BLEN field), plus one additional access (n^{th} cycle +1), the host drives DQ[67:0] with the data to be written to the TCAM array's next location (addressed by the auto-increment address field of the Burst Write Address Register).

This (the address?) is specified by the OP[5:3] index and supplied by the first cycle. The selected device drives the EOT signal LOW from the third to the n^{th} cycle. Afterward, the selected device drives this same signal HIGH one cycle after the n^{th} cycle. This value, n, is specified by the BLEN field of the Burst Write Address Register.

Two cycles after the n^{th} cycle, the selected device drives the EOT signal LOW. Afterward, when the cycle terminates, the selected device drives the EOT signal to a Z state, and prepares Harmony for the next instruction.

Figure 19. Data and Mask Burst WRITE (BLEN = 4)



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SRAM WRITE Instruction

The SRAM WRITE instruction enables and writes associative data contained in external SRAM. An SRAM WRITE instruction completes in three clock cycles on the DQ bus.

In the first cycle, the host ASIC applies the WRITE instruction on CMD[1:0] (with CMD[2] = 0), and sets the OP-CODE VALID signal to "1" (CMDV = 1). The DQ bus then supplies the SRAM address and sets DQ[20:19] to 10. The host ASIC selects the device for which the UID[4:0] matches DQ[25:21]; it selects the device with LCAM bit set when DQ[25:21] = 11111. The second and third cycles are necessary WAIT cycles.

SRAM WRITE Instruction

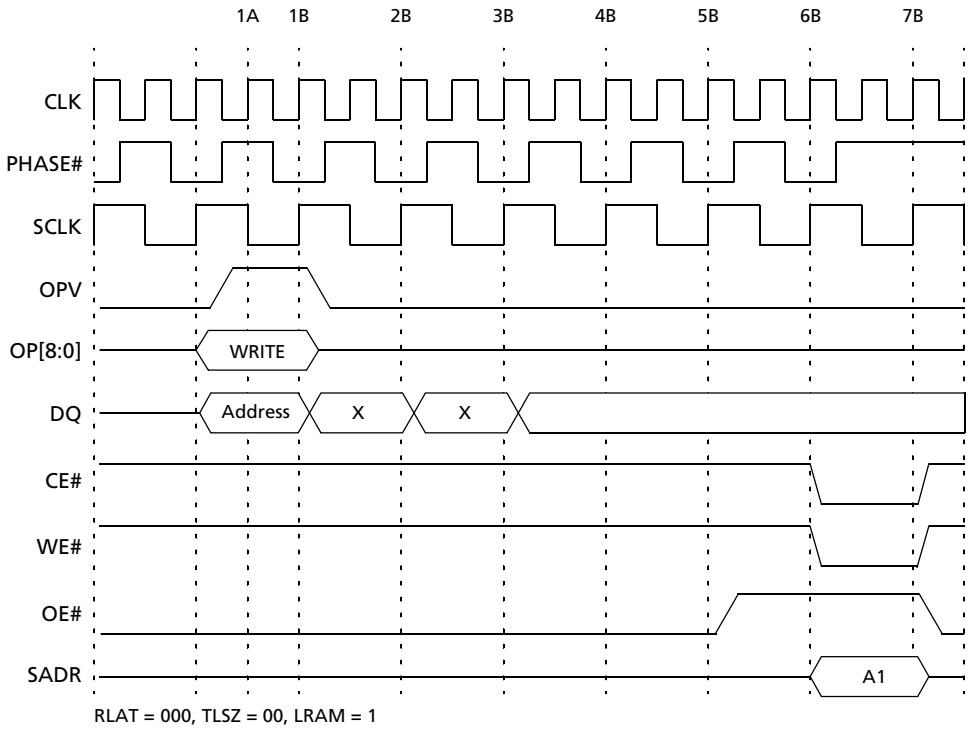
Associative data stored in external SRAM is accessed by SRAM WRITE instructions. An instruction completes in six cycles. The following delineates the instruction sequence.

In the first cycle, the host applies the WRITE instruction on OP[1:0], and sets the instruction data valid to "1" (OPV = 1). The DQ bus then supplies the appropriate address, sets DQ[20:19] to 10, and selects the SRAM address. The host selects the device for which the UID[4:0] matches DQ[25:21] and supplies SADR[21:19] to OP[8:6]. In the second and third cycles, the host three-states DQ[67:0].

In the fourth cycle, the selected device starts to drive DQ[67:0] and drives the ACK signal from High-Z to LOW. In the fifth cycle, the selected device drives the WRITE address on SADR[21:0]; it also drives ACK HIGH, CE# LOW, and ALE# LOW. In the sixth cycle, the selected device three-states CE#, SADR, and the DQ bus and continues to drive ACK LOW. At the end of sixth cycle, the selected device three-states ACK.

SADR[13:0] contains the address supplied on the DQ bus during access to Harmony. Furthermore, OP[8:6] transports signals from the instruction bus to the SRAM[21:19] address bus.

Figure 20. SRAM WRITE Cycle



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WRITE NEXT FREE ADDRESS Instruction

The WRITE NEXT FREE ADDRESS instruction can be completed in the following two clock cycles:

In the first half of the first cycle, the host applies the WRITE NEXT FREE ADDRESS instruction on OP[1:0] and sets the instruction data valid to "1" (OPV = 1). OP[5:2] specifies the index of the even and odd Comparand Registers to be written in the 136-bit configuration. In the 68-bit configuration, the even-numbered comparands are specified by this index. OP[8:6] transports the bits to be driven on SADR[21:19] during the SRAM WRITE. In the second half of the first cycle, the host continues to drive OPV to "1," OP[1:0] to "11," and OP[5:2] with the even and odd comparand indexes. OP[6] equals "0" for half-word searches of the next free address, and equals one for full word searches of the next free address.

In the second cycle, the host sets the INSTRUCTION DATA VALID signal to "0" (OPV = 0). After the completion of the second cycle, the TCAM is ready for the next instruction. The search latency of the SRAM WRITE instruction is the same as the search latency to the instruction; it is measured from the second cycle of the WRITE NEXT FREE ADDRESS instruction.

When the host applies the WRITE NEXT FREE ADDRESS instruction, specifying the appropriate comparand register, Harmony writes the specified comparand in the next free location in the depth-cascaded table. The next free location is the first entry in Harmony with its bit [0] set to "0." If all the entries within the first Harmony are occupied (bit[0] = 1), then the first entry with bit[0] = 0 in a downstream Harmony in a group of cascaded devices is the next free location.

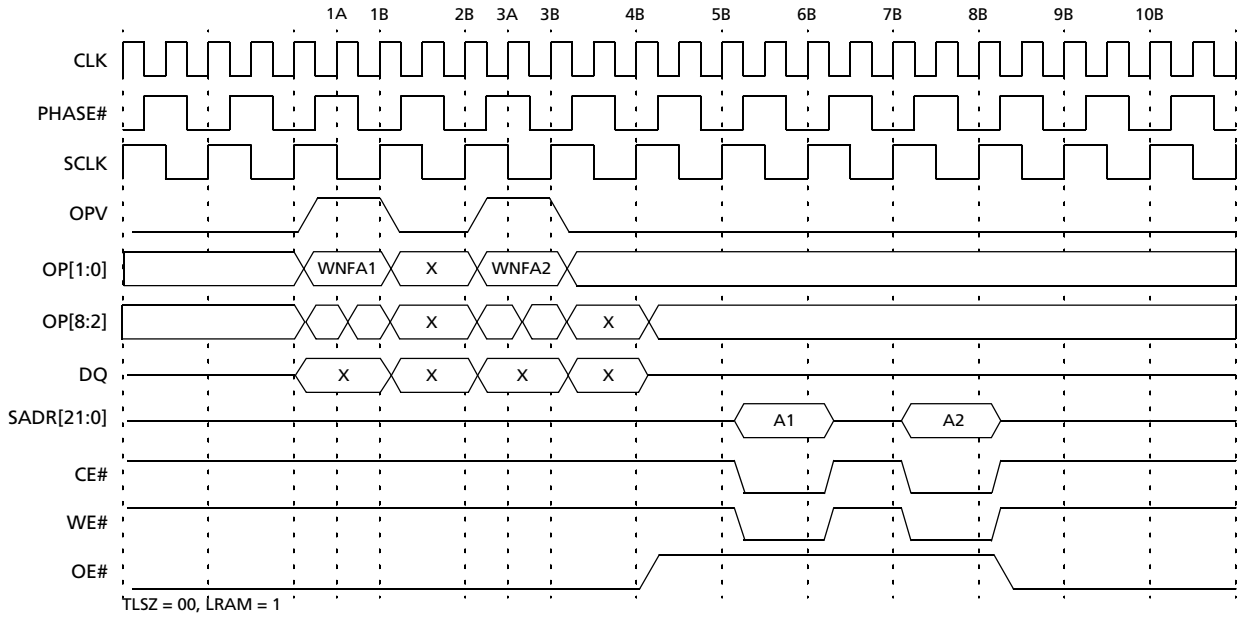
In a 136-bit configuration, bit[0] in both the even and the odd locations must be set to "0" when empty. However a "1" in bit[0] in either the even or odd location indicates that the 136-bit word is full. As a result, only one bit (bit[0] in either the even or odd location) is needed to indicate validity, but bit[0] of both the even or odd location must be "0" for the WRITE NEXT FREE instruction to write at that 136-bit word.

When configured for depth cascading, the FF signal indicates to the host when no more entries can be written and when all entries within a group of cascaded devices are occupied. Harmony updates the signal to the TCAM array after each WRITE or WRITE NEXT FREE ADDRESS instruction.

When configured for full words, the WRITE NEXT FREE ADDRESS instruction writes to both the even and odd Comparand Registers in the data locations and uses the Next Free Address (NFA) Register as the address. It generates a WRITE to the external SRAM and also uses the NFA Register as a portion of the SRAM address.

When configured for half-words, the WRITE NEXT FREE ADDRESS instruction writes only to the even Comparand Register within the data location and uses the NFA Register as the address. It generates a WRITE to the external SRAM and also uses the NFA Register as a portion of the SRAM address. The WRITE NEXT FREE ADDRESS instruction only supports 68 or 136 words and does not support multiple search tables of different widths in depth cascaded configurations. Therefore, all tables must be single, equal-width tables.

Figure 21. WRITE NFA



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SRAM ADDRESSING

The external SRAM address, SADR[21:0], is generated from several sources, as shown in Tables 26 and 27. SADR[13:0] (in the 1Mb Harmony device) and SADR[14:0] (in the 2Mb Harmony device) correspond to the word locations within an individual Harmony device. For SEARCH operations, the index bits are the same as the index field in the Result Register specified as part of the SEARCH instruction.

The UID bits correspond to the UID bits of the TCAM device driving the SRAM, and provide for continuous addressing of a larger SRAM from multiple Harmony devices. OP[8:6] bits (in the 1Mb Harmony device) and OP[8:7] bits (in the 2Mb Harmony device) allow page addressing when large amounts of SRAM are required for each TCAM address. For 136-bit SEARCH and WRITE operations, SADR[0] is always "0." For 272-bit SEARCHES, SADR[1:0] is "00."

Table 26: SRAM Addressing for 1Mb Harmony

INSTRUCTION	SRAM OPERATION	SADR[21:19]	SADR[18:14]	SADR[13:0]
SEARCH	READ	OP[8:6]	UID[4:0]	Index[13:0]
WRITE NEXT FREE ADDRESS	WRITE			NFA[13:0]
READ	READ			DQ[13:0]
WRITE	WRITE			
INDIRECT ACCESS	WRITE/READ			RR[13:0]

Table 27: SRAM Addressing for 2Mb Harmony

INSTRUCTION	SRAM OPERATION	SADR[21:20]	SADR[19:15]	SADR[14:0]
SEARCH	READ	OP[8:7]	UID[4:0]	Index[14:0]
WRITE NEXT FREE ADDRESS	WRITE			NFA[14:0]
READ	READ			DQ[14:0]
WRITE	WRITE			
INDIRECT ACCESS	WRITE/READ			RR[14:0]

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APPLICATION INFORMATION

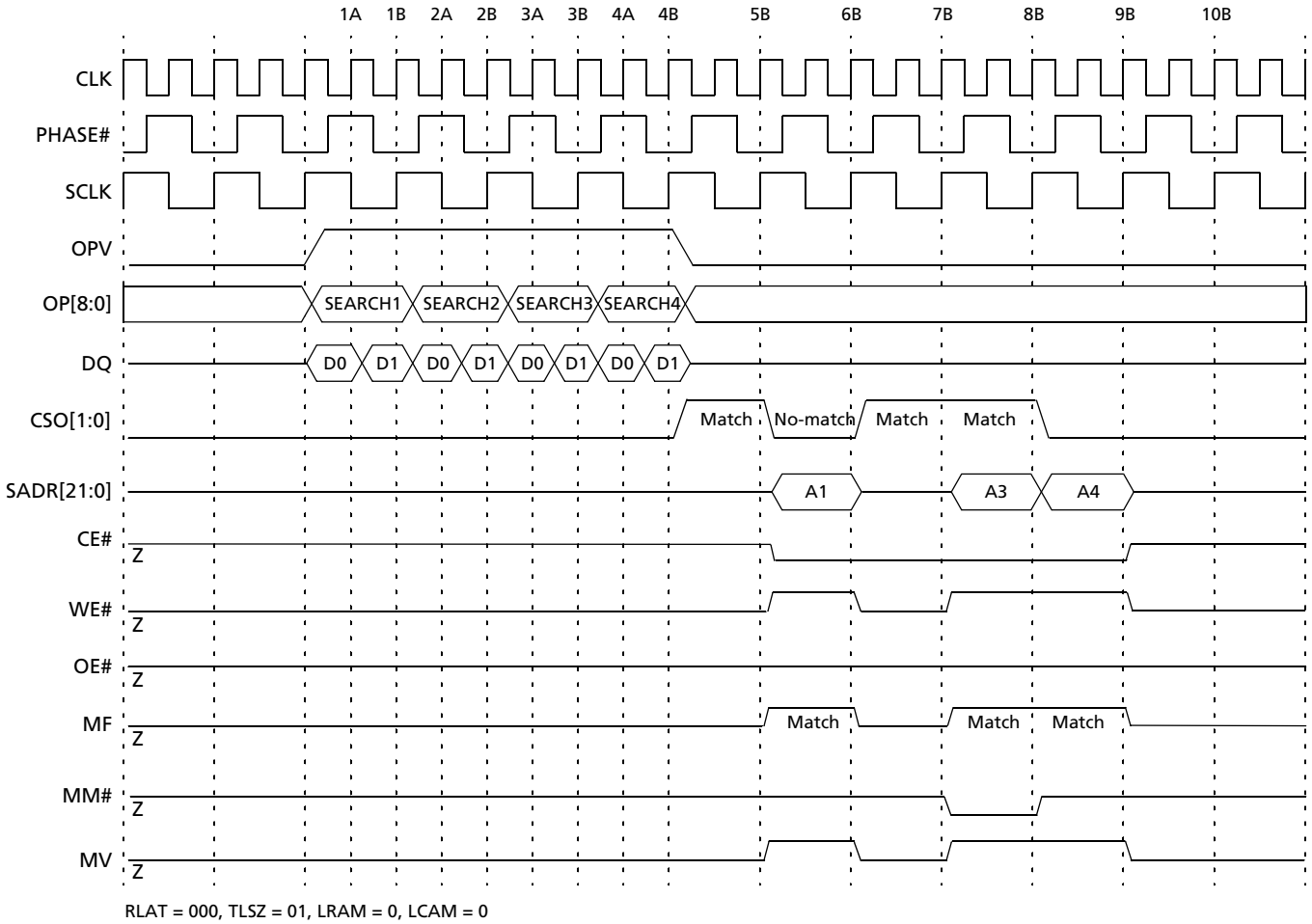
DEPTH CASCADING

The Harmony search engine can depth-cascade up to 31 devices. Harmony performs the necessary arbitration to determine which device drives the SRAM bus, thereby eliminating bus contention. The latency of the searches increases as the table size increases; however, the search rate remains constant, as shown in Figure 22.

Eight Devices

Figure 23 on page 34 shows how up to eight devices can cascade to form a 128K x 68, 64K x 136, or 32K x 272 bit table, and also shows the interconnection between the devices for depth-cascading. Additionally, the host ASIC must program the table size (TLSZ) field to 01. For each search, when a device determines a local match within the device, it asserts the CSO[1:0] signals.

Figure 22. Arbitration for a Group of Cascaded Devices

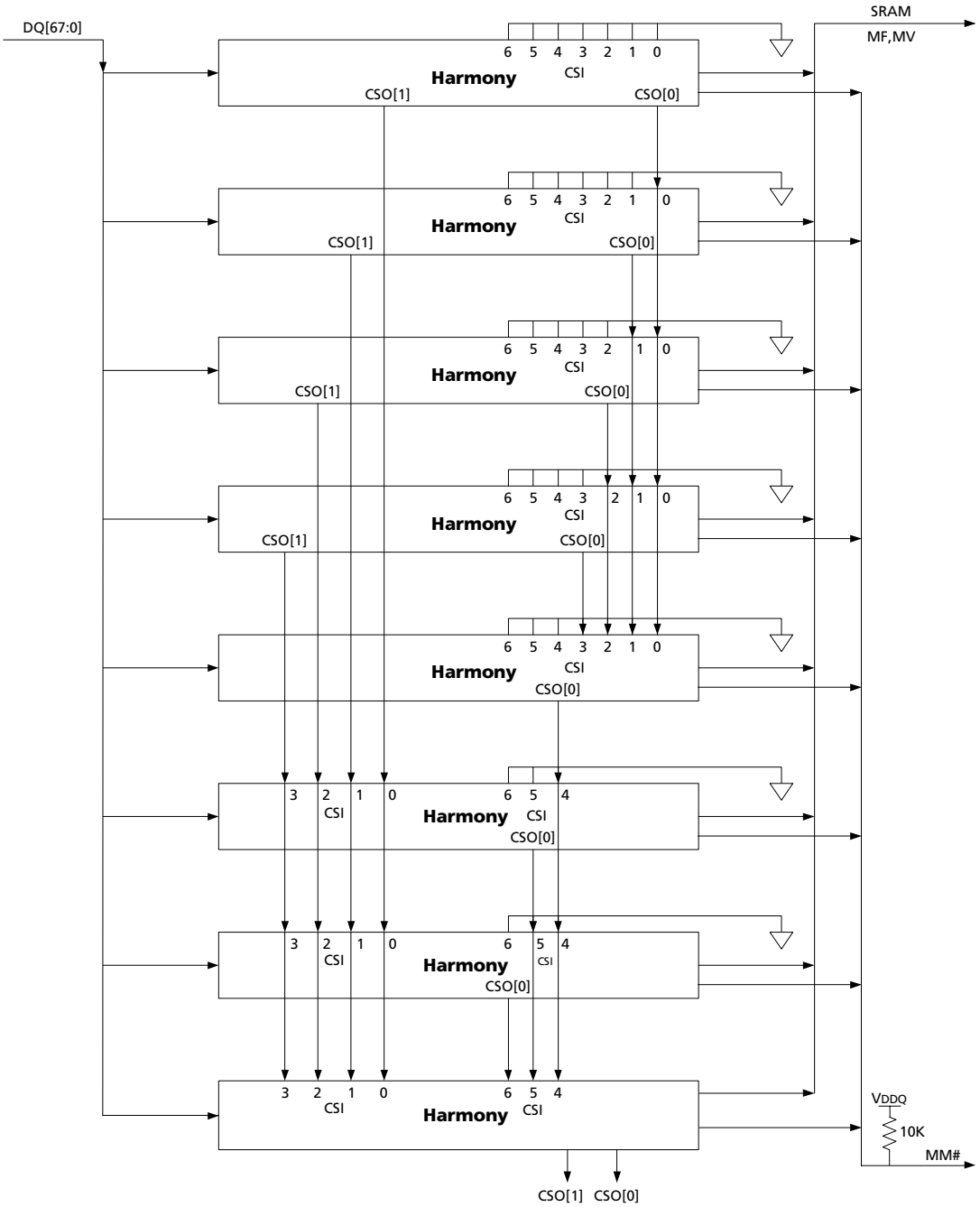


RLAT = 000, TLSZ = 01, LRAM = 0, LCAM = 0

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Figure 23. Depth Cascading Eight Harmony Devices



Search (68-bit Configuration with LCAM = 1)

The device is configured to be the last in the depth-cascaded table by setting LCAM to "1" in the Instruction Register. The device with LCAM set to "1" drives the MV, MF, and MM# signals in cycles when upstream devices do not drive these signals. The Harmony device, with its LCAM bit set, drives MV, MF, and MM# during a search with a no match or with nonsearch instructions.

Search (68-bit Configuration with LRAM = 1)

The device is configured to be last on the SRAM bus by setting LRAM to "1" in the instruction register. In a cycle where the upstream Harmony does not drive the SRAM bus, the last SRAM bus device (with LRAM = 1) drives the SRAM control signals (SADR, CE#, WE#, ALE#) when they are active. When set to "1," the LRAM bit sets the default driver for the SRAM control signals (SADR, CE#, WE#, and ALE#).

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Depth-Cascading to Generate Full

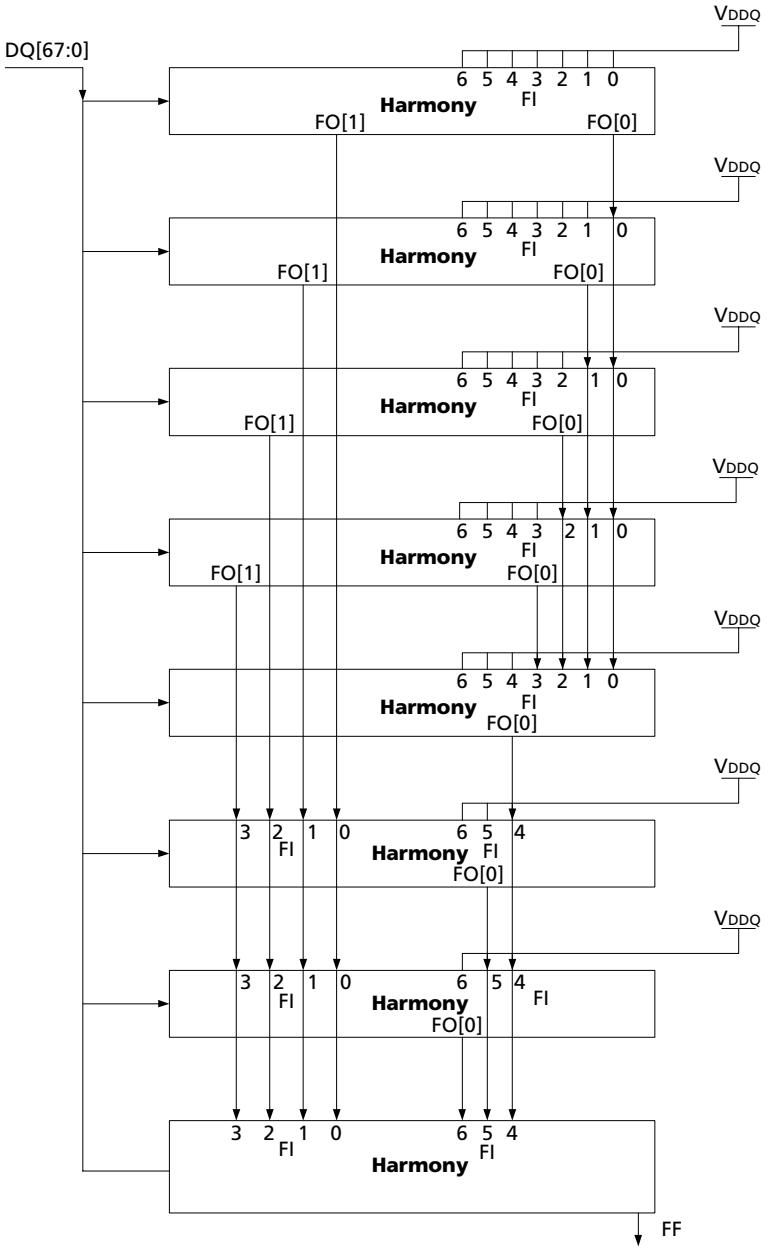
Bit 0 of each entry, regardless of width, is designated as a special bit (1 = Full; 0 = Empty). For each WRITE NEXT FREE ADDRESS or WRITE to the TCAM array, a device asserts FO[1] and FO[0] when no empty locations exist. FF is asserted when the device is full and all FI inputs are HIGH.

Note: The BHI and BHO pins are used when more than eight devices are cascaded; otherwise, these pins are not connected or tied to ground.

Arbitration

Four cycles after the SEARCH instruction, each device drives CSO[1:0] with the match result of the search. At the next cycle, all downstream devices know the outcome of the search in all upstream devices. When any upstream device has a match, all subsequent devices defer driving the SRAM bus. When a search or no match occurs, the Harmony device, with its LRAM bit set (the last in the chain), drives the SRAM bus signals. Also, the device with LCAM set to "1" is the default driver of the MV, MF, and MM# signals.

Figure 24. Full Generation in a Cascaded Table



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INITIALIZATION

After a hard or soft reset, the Device Register and internal state machines are placed in a known state. However, the contents of the TCAM must still be initialized. The minimum required initialization sets bit 0 of each TCAM word to "0," indicating that the word does not contain valid data. In addition, the table configuration bits of the Instruction Register must be initialized to indicate the width of the each of the four addressable sections.

The last TCAM in the table bit (LCAM) of the Instruction Register must be set to "1" in the last device of the cascaded block; the LCAM bit must be set to "0" in all other devices. In addition, the last TCAM on the SRAM bus (LRAM) must be set to "1" in the last device of the cascaded block; the LRAM must be set to "0" in all other devices.

For single Harmony configurations, the Table Size bits (bits 2 and 3 of the Instruction Register) should be set to "00" to reduce the latency from five clock cycles to four. Finally, the Mask Registers must be initialized to values that depend on the specific application.

Note: Reset initializes all mask registers to "0s," guaranteeing a word-for-word match regardless of data values contained in the TCAM array.

POWER SUPPLY SEQUENCING

Power must be applied in sequence. The higher voltage (V_{DDQ}, 3.3V) is applied first, and the lower voltage (V_{DD}, 1.8V) is applied immediately thereafter. The delay time depends on the relative slew rates of the two supplies. Note that if the lower supply slews considerably faster than the higher voltage, it is not desirable to go above the higher voltage supply.

When it is not possible to guarantee that V_{DDQ} powers up first, an external Schottky diode between the two supplies keeps the V_{DDQ} supply within a small voltage drop of the V_{DD} supply. This prevents any parasitic paths from turning on and causing problems. The anode goes to the lower voltage supply and the cathode goes to the higher voltage supply.

32-BIT SEARCH APPLICATIONS

Harmony can efficiently store and search 32-bit and narrower data fields, such as those found in 32-bit IPv4 addresses, 28- or 24-bit ATM VPI/VCI pairs, and 20-bit MPLS labels. Using the technique described here, a single 2Mb Harmony device can store up to 64K IPv4 entries and search them at the same rate as 68- and 136-bit entries.

The quadrants that store the narrow entries are configured for 68-bit searches, and data is stored with two 32-bit entries per 68-bit word. To enable a single-cycle search for a given entry, the entries are divided between the upper half (bits 67:34) or the lower half (bits 33:0) of the 68-bit word based on one of the bits of the entry itself. The bit chosen for this selection function should be in a bit position that is never subject to local (ternary) or global masking, and it should have a fairly equal probability of being a one or a zero to ensure that the entries are nearly evenly distributed between the upper and lower halves of the 68-bit words. (For IPv4, such a bit may be found in the most significant byte of the IP address, although it will not be one of the three or four most significant bits.)

To perform the search, one of two Global Mask Registers (GMRs) is specified as part of the 68-bit SEARCH instruction. One GMR is configured to search the upper half of the 68-bit words, and the other GMR is configured to search the lower half. The same bit position that selected whether words are stored in the upper or lower half now selects the Mask Register that is used for the SEARCH operation. The control logic checks the state of this bit on the search key (the incoming IPv4 address to be matched) and issues the op-code that includes the appropriate GMR. When using this technique, it is only necessary to search the upper or lower halves of the 68-bit entry to find the matching entry in a single SEARCH operation.

Figure 25. 32 Bit Searches

	67-36	35	34	33-2	1	0
DQ	IP Address	1	1	IP Address	0	1
GMR[A]	all 0	0	1	all 1	1	1
GMR[B]	all 1	1	0	all 0	1	1
TCAM Array	/32 IPv4addr1	1	1	/32 IPv4addr2	0	1
	/28 IPv4addr3	1	1	/28 IPv4addr4	0	1
	(empty)	0	1	/24 IPv4addr6	0	1
	/20 IPv4addr5	1	0	(empty)	0	1
	(empty)	0	0	(empty)	0	1
	(empty)	x	x	(empty)	x	0

Bit[0]: Word valid (1 = valid)
Bit[1]: Table management (0 = IPv4)
Bit[34]: Lower segment valid (1 = valid)
Bit[35]: Upper segment valid (1 = valid)
GMR[A]: Search lower segment
GMR[B]: Search upper segment

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Within each 68-bit word, each half must have its own validity information. While this can be done by placing an invalid or reserved address (such as all "1"s or all "0"s) in each unused half, it is just as easy to dedicate one bit in each half as a validity indicator. If bit[0] of each word that is used for one of these entries is set to "1," it is still possible to use the WRITE NEXT FREE ADDRESS instruction with other tables that might be stored in the same device. Even if one more bit is set to "0" as a table indicator (all other tables would have a "1" in this position and use additional bits to discriminate among themselves), 32-bits remain available for each upper-half and lower-half entry. A map of this scheme is shown in Figure 25. Note that it is unnecessary to use specific bits for upper- or lower-half entries; any bits can be used for any function except that bit[0] must be used for the word validity bit to avoid conflicts with the WRITE NFA mechanism (if it is used in the application).

For Technical Notes about Harmony and other Micron TCAM products, check www.micron.com/tcam or consult with your local Micron Field Applications Engineer.

TEST ACCESS PORT

The Harmony test access port provides an interface for manufacturing tests and consists of the boundary scan access port used to support the standard JTAG IEEE 1149.1.

The Harmony fully supports the test access port (TAP) and boundary scan architecture, as specified in the IEEE JTAG standard 1149.1. The pins for this interface are: TCK, TMS, TRST# and TDI, and TDO.

Table 28 describes the operations that the test access port controller supports, and Table 29 describes the TAP device ID Register. A BSDL file is available online at www.micron.com/TCAM.

Note: To functionally disable the JTAG interface, connect the TCK, TMS, TDI, and TRST# to V_{DDQ}.

Table 28: JTAG-Supported Operations

INSTRUCTION	STATUS	DESCRIP[TION
Sample/Preload	Mandatory	This operation loads the values of signals passing to and from the I/O pins into the boundary scan shift register. It provides a snapshot of the functional operation.
EXTEST	Mandatory	This operation uses boundary scan values shifted in from the Test Access Port to test the connections which are external to the device.
BYPASS	Mandatory	This operation bypasses the internal JTAG Registers for this device.
IDCODE	Optional	This operation outputs the TAP Device ID Register (see Table 29).

Table 29: TAP Device ID Register

FIELD	RANGE	INITIAL VALUE	DESCRIPTION
Revision #	[31:28]	0001	Revision Number. This number increments by one for each revision of the device.
Part #	[27:12]	1010 1101 0000 0010	This field indicates the device identification number (2Mb)
MFD	[11:1]	000 1001 1001	Manufacturer ID
LSB	[0]	1	Least Significant Bit

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD} = 2.5V V_{DDQ} = 4.6V
Voltage on all other pins	Input = 6V Output = 4.6V
Temperature under bias	-40°C to +125°C
Storage Temperature	-65°C to +125°C
DC Output Current	TBD

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to maximum ratings for extended periods of time may reduce reliability. Functionality at or above these conditions is not implied.

All voltages referenced to V_{SS}.

OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN.	TYPICAL	MAX.	UNITS
V_{DD}	Operating supply voltage		1.7	1.8	1.9	Volts
V_{DDQ}	I/O supply voltage		3.135	3.3	3.465	Volts
V_{IH}	Input high voltage		2.0		5.5	Volts
V_{IL}	Input low voltage		-0.3		0.8	Volts
T_A	Ambient operating temperature	Commercial	0		70	C°

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{DD}	V_{DD} supply current	-66		2300	mA	Average operating current at maximum frequency. Transient peak currents may exceed these values.
		-83		TBD		
		-100		TBD		
I_{DDQ}	V_{DDQ} supply current @ 3.3V	-66		200	mA	Average operating current at maximum frequency. Transient peak currents may exceed these values. Applies only for outputs in three-state.
		-83		TBD		
		-100		TBD		
V_{OH}	Output high voltage		2.4		V	I_{OH} = 8mA, V_{DDQ} = 3.3V
V_{OL}	Output low voltage			0.4	V	I_{OL} = 8mA, V_{DDQ} = 3.3V
I_{IZ}	Input leakage current		-10	10	µA	$V_{SS} \leq V_{IN} \leq V_{DDQ}$
			-100	10	µA	V_{IN} = Vss; TMS, TDI, TRST#
			-10	100	µA	V_{IN} = V_{DDQ}; SEN
I_{OZ}	Output leakage current		-10	10	µA	$V_{SS} \leq V_{OUT} \leq V_{DDQ}$; Applies only for outputs in three-state.

CAPACITANCE

SYMBOL	PARAMETER	MAX.	UNIT	NOTES
Cin	Input Capacitance	6	pF	F = 1 MHz, V_{IN} = 0V
Cout	Output Capacitance	6	pF	F = 1 MHz, V_{OUT} = 0V

HSBG THERMAL RESISTANCE

SYMBOL	PARAMETER	AIR FLOW	TYP	UNIT
Θ_{JA}	Thermal Resistance (Junction to Ambient)	0m/s	14.7	°C/W
		1m/s	13.3	
		2m/s	10.9	
Θ_{JC}	Thermal Resistance (Junction to Case)	N/A	4.3	

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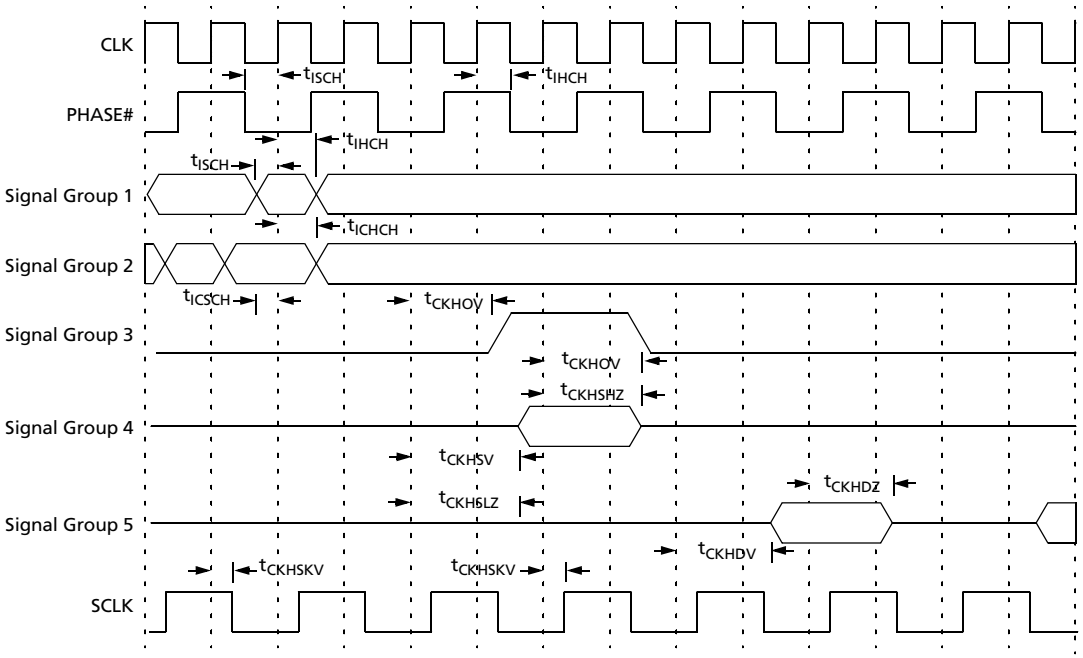
AC TIMING WAVEFORMS

Table 30: AC Timing Parameters

ROW	SYMBOL	-66		-83		-100		UNIT	DESCRIPTION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	f_{CLK}		133		166		200	MHz	CLK Max frequency
2	t_{CKHI}	2.9		2.4		2.0		ns	CLK high pulse; worst-case 40%/60% duty cycle[1]
3	t_{CKLO}	2.9		2.4		2.0		ns	CLK low pulse; worst-case 40%/60% duty cycle[1]
4	t_{ISCH}	1.8		1.5		1.5		ns	Input Setup Time to CLK rising edge
5	t_{IHCH}	0.6		0.5		0.5		ns	Input Hold Time to CLK rising edge
6	t_{ICSCH}	4.2		3.5		3.5		ns	Cascaded Input Setup Time to CLK rising edge [6]
7	t_{ICHCH}	0.6		0.5		0.5		ns	Cascaded Input Hold Time to CLK rising edge [6]
8	t_{CKHOV}		10.2		8.5		8.0	ns	Rising edge of CLK to CSO, FO, BHO, FF valid [2, 6]
9	t_{CKHDV}		11.4		9.5		8.5	ns	Rising edge of CLK to DQ valid [3, 6]
10	t_{CKHDZ}	1.2	8.4	1.0	7.0	1.0	7.0	ns	Rising edge of CLK to DQ three-state [4, 5, 6]
11	t_{CKHSV}	3.6	11.4	3.0	9.5	3.0	8.5	ns	Rising edge of CLK to SRAM bus valid [3, 6]
12	t_{CKHSHZ}		3.6		3.0		3.0	ns	Rising edge of CLK to SRAM bus High-Z [4, 5, 6]
13	t_{CKHSLZ}		3.6		3.0		3.0	ns	Rising edge of CLK to SRAM bus LOWZ [4, 5, 6]
14	t_{CKHSKV}	7.0	16.4	7.0	14.5	7.0	13.5	ns	Rising edge of CLK to SCLK valid

[1] t_{CKKHI} and t_{CKKLO} duty cycle values are based on 20-80 percent signal levels.
[2] Based on an AC load of 30pF.
[3] Except when noted, all values are based on AC load 50pF measured at 1.5V reference levels.
[4] Based on AC load of 10pF, 50-W DC loading and measured at 200mV from steady state.
[5] These parameters are sampled and are not 100 percent tested.
[6] Measured from the rising edge of CLK when PHASE# is LOW.

Figure 26. AC Timing Waveforms

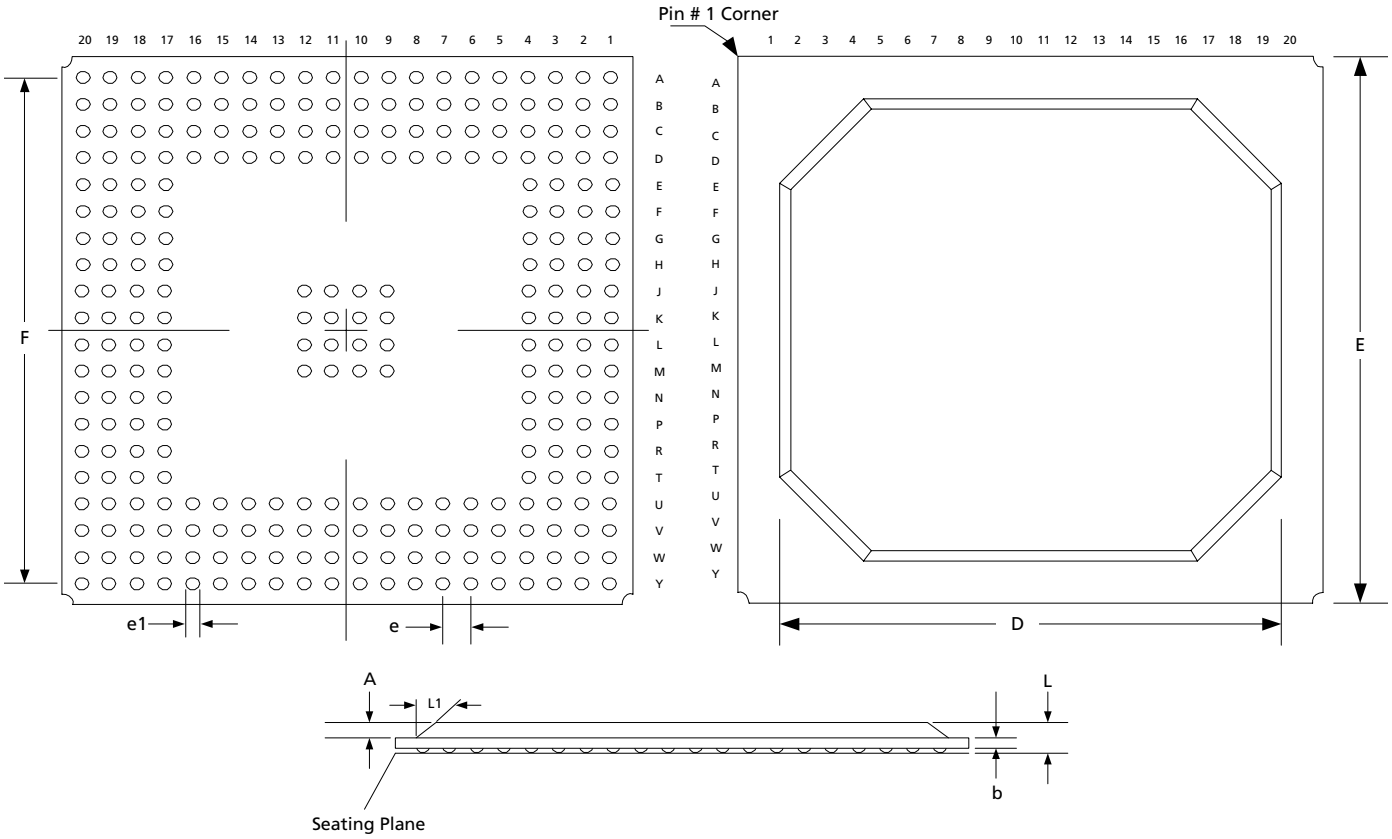


Signal Group 1: OP[8:0], OPV, RST#, DQ (write), SEN[3:0]
SIgnal Group 2: CSI[6:0], FI[6:0], BHI[2:0]
Signal Group 3: CSO[1:0], FO[1:0], FF, MF, MM#, MV, BHO[2:0]
Signal Group 4: CE#, OE#, WE#, ALE#, SADDR
Signal Group 5: DQ (READ), ACK, EOT

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PACKAGING INFORMATION



272-Ball HSBGA Dimensions

	DIM. A	DIM. b	DIM. D	DIM. E	DIM. e	e1	DIM. F	DIM. L	L1
MIN.	1.17	0.56	24.00	26.80	1.27	0.60	24.13	2.20	30° (TYP)
NOM.				27.00		0.75		2.33	
MAX.				27.20		0.90		2.46	

Note: All dimensions shown in mm.

ORDERING INFORMATION

PART NUMBER	DENSITY	SEARCH RATE	PACKAGE	TEMPERATURE	VOLTAGE
MT75W8Y136HBB-66 MT75W8Y136HBB-83 MT75W8Y136HBB-100	1Mb	66 MSps 83 MSps 100 MSps	272-Ball HSBGA	0 - 70°	1.8V/3.3V
MT75W16Y136HBB-66 MT75W16Y136HBB-83 MT75W16Y136HBB-100	2Mb	66 MSps 83 MSps 100 MSps			

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