NXP Semiconductors
User's Guide

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i.MX 8M EVK Board Hardware User's Guide

1. Introduction

This document is the hardware User's Guide for the i.MX 8M Evaluation Kit (EVK) based on the NXP Semiconductor's i.MX 8MDQLQ Applications Processor. This board is fully supported by NXP Semiconductor. This manual includes system setup and debugging, and provides detailed information on the overall design and usage of the EVK board from a hardware system perspective.

1.1. Board overview

The EVK board is a platform designed to showcase the most commonly used features of the i.MX 8MDQLQ Applications Processor in a small, low cost package. The i.MX 8M EVK board is an entry level development board, which gives the developer the option of becoming familiar with the processor before investing a large amount of resources in more specific designs.

Table 1 lists the features of the i.MX 8M EVK board.

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Table 1. Board features

Processor	NXP Applications Processor	MIMX8MQ6DVAJZAA
DRAM memory	Micron 3 GB LPDDR4	MT53B768M32D4NQ-062 WT:B
Mass storage	Micron 16 GB eMMC5.0	MTFC16GAKAECN-2M WT
	Micron 32 MB QSPI NOR	MT25QL256ABA1EW9
	MicroSD card connector	SD3.0 supported
Power	NXP PMIC PF4210 + Discrete DCDC/LDO	
Display interface	HDMI 2.0a Connector	
	DSI interface (Mini-SAS connector)	
Ethernet	1 GB Ethernet with RJ45 connector	
USB	x1 USB (2.0/3.0) Type-C connector	
	x1 USB (2.0/3.0) host connector	
Audio connectors	3.5 mm Stereo Headphone output	
Debug connectors	JTAG (10-PIN header)	
	MicroUSB for UART debug	
Camera	CSI interface (Mini-SAS connector)	
WiFi/Bluetooth	x1 on board WiFi/BT module	
	x1 M.2 slot (KEY-E type)	
Buttons	ONOFF, RESET	
LED Indicators	Power status, UART	
Expansion Port	FPC connector (SAI ports)	
PCB	3.937-inch x 3.937-inch (10 cm x 10 cm), 10-layer board	

1.2. Board contents

The i.MX 8M EVK contains the following items:

- i.MX 8M EVK board
- USB Cable (x1 Standard USB TYPE-A to MicroUSB TYPE-B connector; x1 Standard USB TYPE-A to USB TYPE-C connector)
- 12V/5.0A Power Supply
- Quick Start Guide

1.3. Board revision history

- Rev A0/A1
- Rev B1/B2
- Rev B3

The board assembly version will be printed on a label, usually attached to the bottom side. The assembly version will be the letter designation following the schematic revision: 700-29615 REV _.

2. Specifications

This section provides the detailed information about the electrical design and practical considerations that go into the EVK board. **Figure 1** describes each block in the high-level block diagram of the EVK board.

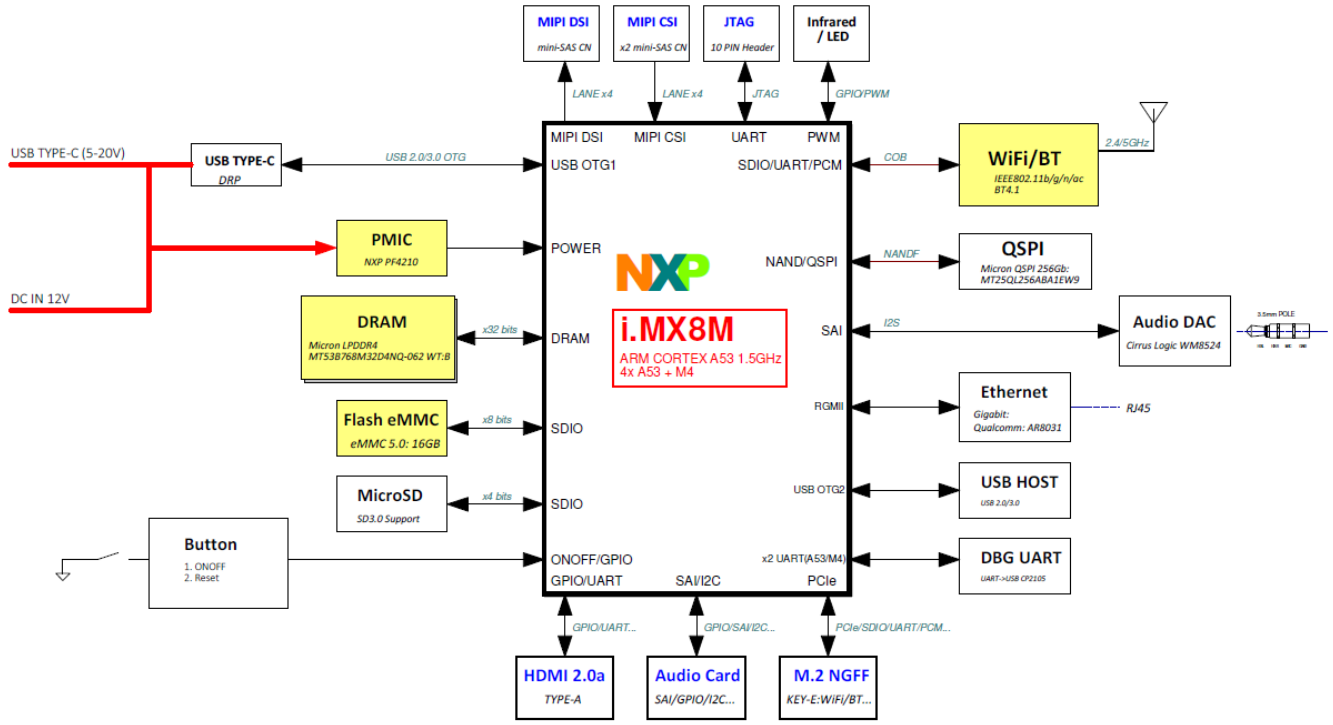


Figure 1. MCIMX8M-EVK block diagram

Figure 2 shows the overview of the i.MX 8M EVK board.

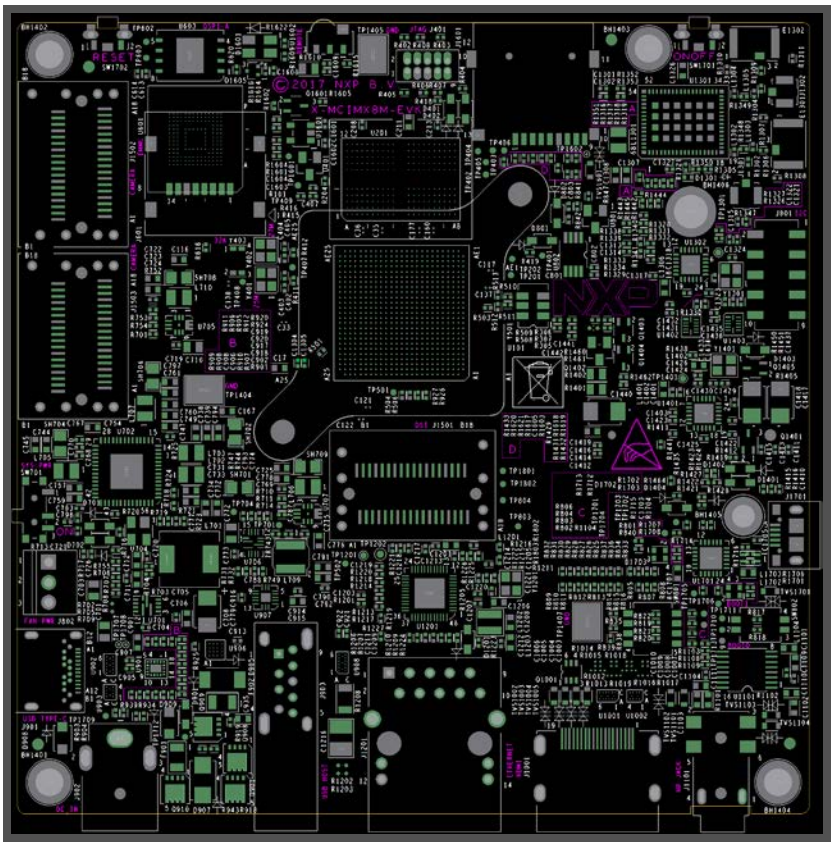


Figure 2. i.MX 8M EVK board overview

2.1. Processor

The i.MX 8MDQLQ processors represent NXP Semiconductor's latest achievement in integrated multimedia-focused products offering high performance processing with a high degree of functional integration, targeted towards the growing market of connected devices. The i.MX 8MDQLQ processor features NXP's advanced implementation of the Quad ARM Cortex®-A53+ ARM Cortex®-M4 core, which operates at speeds up to 1.5 GHz. i.MX 8MDQLQ includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor provides a 32-bit DDR3/LVDDR3/DDR4/LPDDR4 memory interface and other interfaces for connecting peripherals, such as HDMI, LCD, WLAN, Bluetooth™, GPS and camera sensors.

For more detailed information about the processor, please refer to the datasheet and reference manual on www.nxp.com/i.MX8M.

2.2. Boot mode operations and selections

The i.MX 8MDQLQ Applications Processor can be the boot configuration selected on SW802 or by the boot configuration stored on internal eFUSE. Alternatively, the i.MX 8MDQLQ can download a program image from a USB connection when configured in serial downloader mode. The method used to determine where the processor finds its boot information is from two dedicated BOOT MODE pins. **Table 2** shows the values used in the two methods.

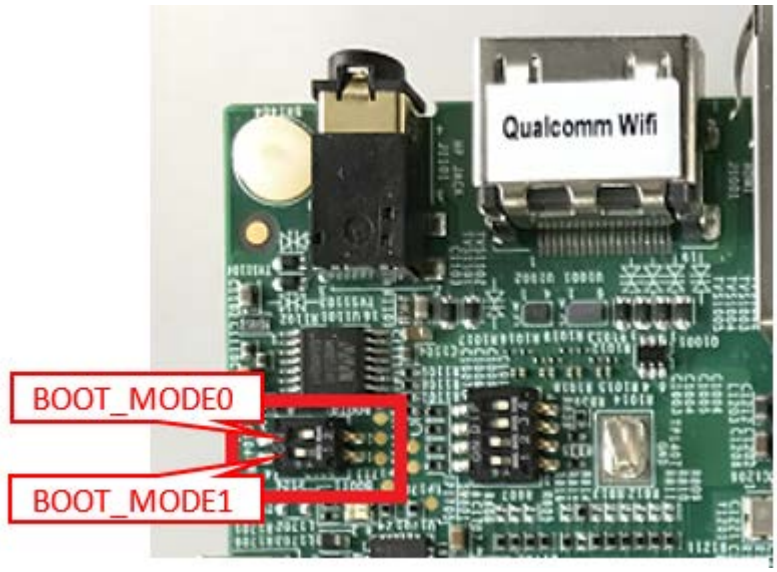


Figure 3. Boot mode

Table 2. Boot mode pin settings

BOOT_MODE1	BOOT_MODE 0	Boot source
0	0	Boot from fuses
0	1	Serial downloader
1	0	Internal boot
1	1	Reserved

It is important for the developer to remember that these two pins are tied to the BOOT modules, therefore, on i.MX 8M EVK board, use a dual-switch (SW802) to select the input voltage of these two pins, 0 or 3.3 V. If the developer wants to boot the program Image from the Fuses Mode, the position of the switch 1 and 2 must be set to OFF, it is the same principle to choose the Serial Downloader Module or Internal Boot Module to load bootable code into the processor.

If the method of determining the bootable source code is selected to be from the hardware, then the developer must set the switch S802:MODE0 to OFF, MODE1 to ON, and the four i.MX 8MDQLQ pins must be set on the EVK board as **Table 3** and **Figure 4**.

Table 3. Boot mode setting

BOOT configuration	SW801
Boot from EMMC	0010
Boot from SD2	1100

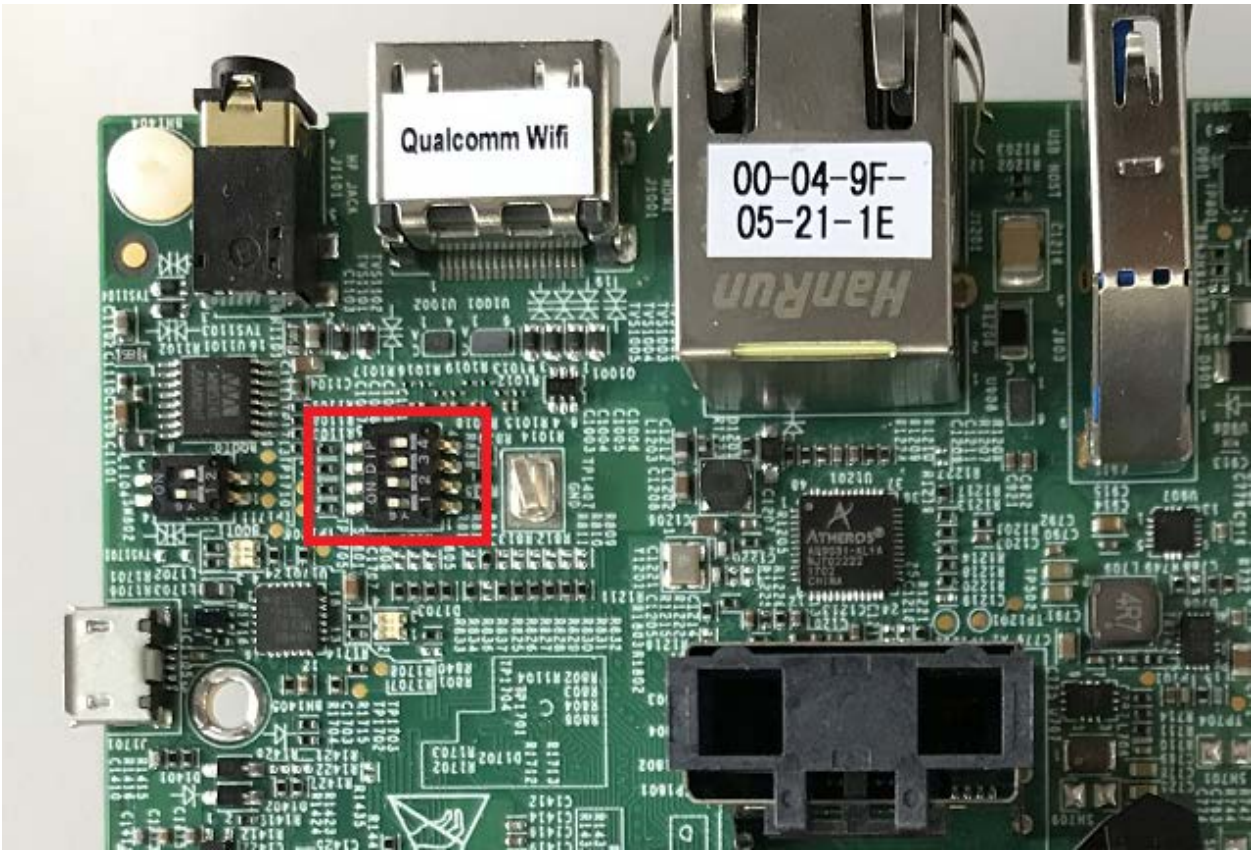


Figure 4. Boot mode setting

On the i.MX 8M EVK board, the default boot mode is from eMMC device. There is one SD connector on the board. The board will check the eMMC connector first and then the SD connector. If you put the boot card into SD connector, and set the boot configuration as “BOOT from SD2”, the board will boot from the SD by default.

NOTE

For more information about the boot module, such as the meaning of every bit of the Boot Switch, please refer to i.MX 8MDQLQ Reference Manual on www.nxp.com/i.MX8M.

2.3. Power tree

There is a +12 V external wall power supply that needs to be connected to the i.MX 8M EVK board at connector J902. The other powers from internal adapters, on the EVK board, use discrete device to power the system. **Figure 5** shows the power tree.

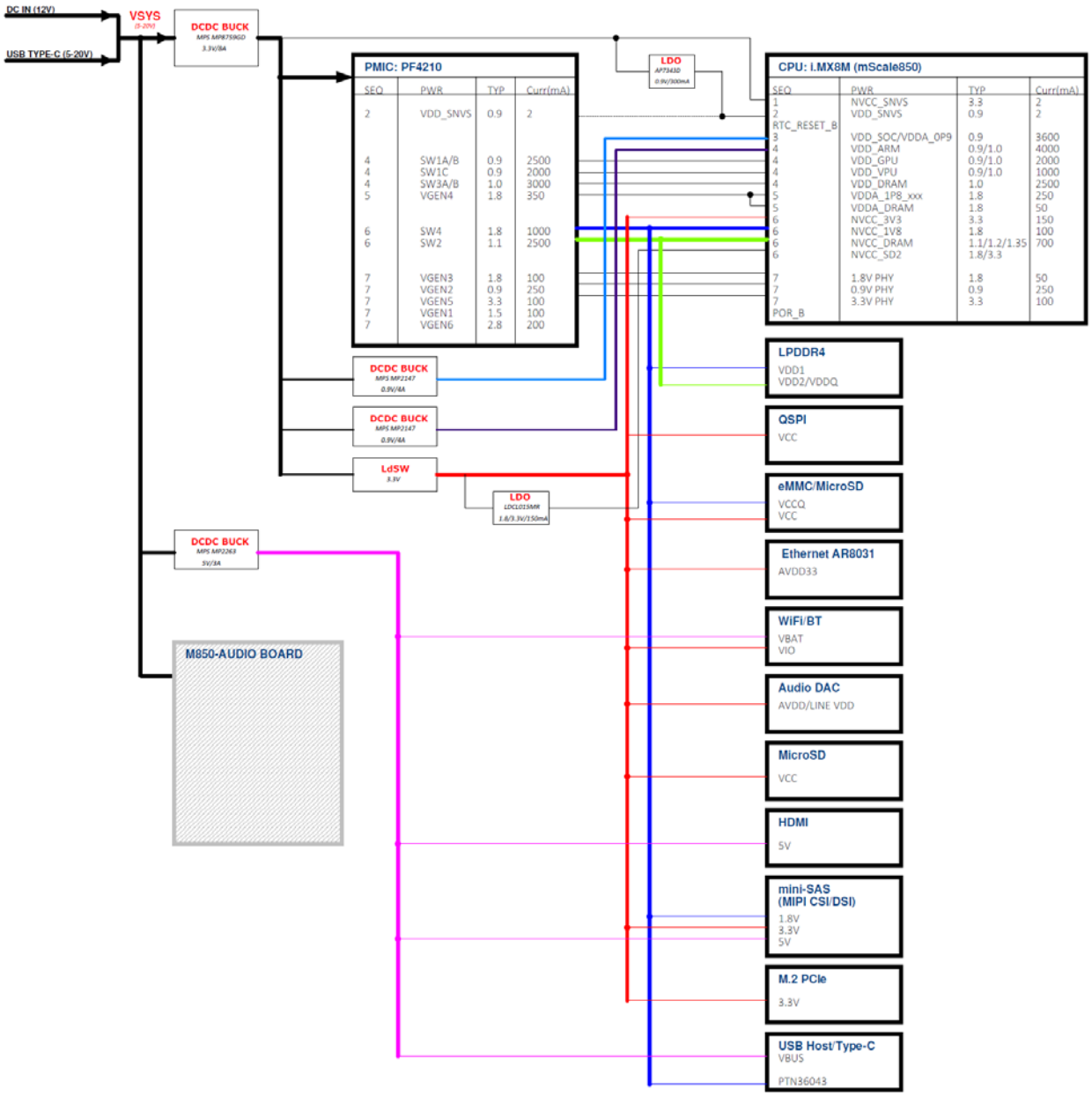


Figure 5. Power tree diagram

In **Figure 5**, the developer can get all the voltage supply rails used on the EVK board. When some modules are not working, the developer needs to test whether the voltage of this module is correct. **Table 4** lists the power rails on the board.

Table 4. Power rails

mScale850		SRC TYPE	Value
SEQ	PWR rail		
1	NVCC_SNVS		3.3
2	VDD_SNVS		0.9
RTC_RESET_B			
3	VDD_SOC/VDDA_0P9	DC/DC BUCK	0.9
4	VDD_ARM	DC/DC BUCK	0.9/1.0
4	VDD_GPU	PMIC PF4210	0.9/1.0
4	VDD_VPU	PMIC PF4210	0.9/1.0
4	VDD_DRAM	PMIC PF4210	1.0
5	VDDA_1P8_xxx	PMIC PF4210	1.8
5	VDDA_DRAM	PMIC PF4210	1.8
6	NVCC_3V3	DC/DC BUCK	3.3
6	NVCC_1V8	PMIC PF4210	1.8
6	NVCC_DRAM	PMIC PF4210	1.1/1.2/1.35
7	NVCC_SD2	LDO	1.8/3.3
8	1.8V PHY	PMIC PF4210	1.8
8	0.9V PHY	PMIC PF4210	0.9
8	3.3V PHY	PMIC PF4210	3.3
POR_B			

NOTE

If an alternate power supply is used (not the original power supply), it should be no more than 20 V; otherwise the board will not work.

2.4. LPDDR4 DRAM memory

The i.MX 8M EVK board has one **768 Meg × 32 (4 channels × 16 I/O)** LPDDR4 SDRAM chip (MT53B768M32D4NQ-062 WT:B) for a total of 3 GB RAM memory.

In the physical layout, the LPDDR4 chip is placed on the TOP side, the data traces are not necessarily connected to the LPDDR4 chips in sequential order, but for ease of routing, are connected as best determined by the layout and other critical traces.

The DRAM_VREF can be created by a simple voltage divider using 1.5 K Ohm 1% resistors and 0.1uF capacitors for stability. The relatively smaller-value resistors provide enough current to maintain a steady mid-point voltage. The calibration resistors used by the LPDDR4 chips and processor are 240 Ohm 1% resistors.

2.5. SD card slot (J1601)

There is one MicroSD card connectors (J1601) on the i.MX 8M EVK board. J1601 on the i.MX 8M EVK board is the TF slot for SD2 interface. By default, this MicroSD connector supports one 4-bit SD3.0 card or MMC card.

2.6. eMMC memory (U601)

The eMMC interface is connected to uSDHC1 of i.MX 8M. It can support eMMC 5.0, eMMC and hinge type. MicroSD socket are co-layout, and the eMMC device is populated by default on the EVK board. To boot from eMMC, you need to change the Boot-mode switch (SW801) settings as shown in **Table 3**.

2.7. Ethernet connector (J1201)

There is one gigabit Ethernet module on the i.MX 8MDQLQ processor. The developer can use the ENET connector to send/receive the ENET signals. The Ethernet subsystem of the i.MX 8M EVK board is provided by the Qualcomm AR8031 Ethernet Transceiver (U1201). The Ethernet Transceiver (or PHY) receives standard RGMII Ethernet signals from the MAC-NET core of the i.MX 8MDQLQ Applications Processor. The processor takes care of all Ethernet protocols at the MAC layer and above. The PHY is only responsible for the Link Layer formatting. The PHY receives the clock signal from the ENET_TXC pin of i.MX 8MDQLQ processor.

When the developer uses the i.MX 8M EVK board for the first time, he must set the MAC address for the EVK board. The MAC address is printed on the connector very clearly, and the developer just needs to set MAC address same as it.

2.8. USB connector (J901, J903)

The i.MX 8MDQLQ Applications Processors contain two USB 2.0/3.0 OTG controllers, with two integrated USB PHY. On the EVK board, one is used for USB host port and the other for the USB TYPE-C port.

2.9. Audio input/output (J1101)

The main Audio DAC used on the EVK board is CIRRUS LOGIC Low Power, high quality Stereo DAC, WM8524. The digital interface between i.MX 8MDQLQ and WM8524 includes three signals: SYNC_CLK, BCLK, and DACDAT. The i.MX 8MDQLQ also provides the MCLK to WM8960.

i.MX 8M EVK includes one headphone interface (J1101). J1101 is a 3.5 mm 4-pole (or TRRS) phone jack.

2.10. UART connector (J1701)

The i.MX 8MDQLQ Applications Processor has four independent UART Ports (UART1 – UART4). Usually the developer can use a DB9 connector and a level shifter such as MAX3232 to complete the UART debug circuit. Nowadays, many computers may not have a RS-232 DB9 connector, so on the EVK board, SILICON LABS’s CP2105, there is a USB to Serial UART IC to cover the UART signal to the USB signal.

On the EVK board, UART1_TXD & UART1_RXD are used to output serial debugging information for A53-core. UART2_TXD & UART2_RXD are used to output serial debugging information for M4-core. No RTS or CTS signals are sent from the Processor to the Debug connector as these signals are ignored by most applications. The required terminal settings to receive debug information during the boot cycle are as shown in **Table 5**.

Table 5. Terminal setting parameters

Data Rate	115,200 Baud
Data bits	8
Parity	None
Stop bits	1

2.11. JTAG connector (J401)

The i.MX 8MDQLQ Applications Processor accepts five JATG signals from an attached debugging device on dedicated pins. A sixth pin on the processor accepts a board HW configuration input, specific to the EVK board only. The five JTAG signals used by the processor are:

- JTAG_TCK TAP Clock
- JTAG_TMS TAP Machine State
- JTAG_TDI TAP Data In
- JTAG_TDO TAP Data Out
- JTAG_nTRST TAP Reset Request (Active Low)

2.12. Extension port (J1801)

One Expansion port (J1801) is provided on the EVK board to generate audio card connector, and the developer can use the processor to perform audio features development.

2.13. MIPI-CSI/MIPI-DSI connector (J1501, J1502, J1503)

The i.MX 8MDQLQ processor supports dual MIPI-CSI and single MIPI-DSI. The connectors are designed to support camera and LCD. The connectors are as shown in **Figure 6**.

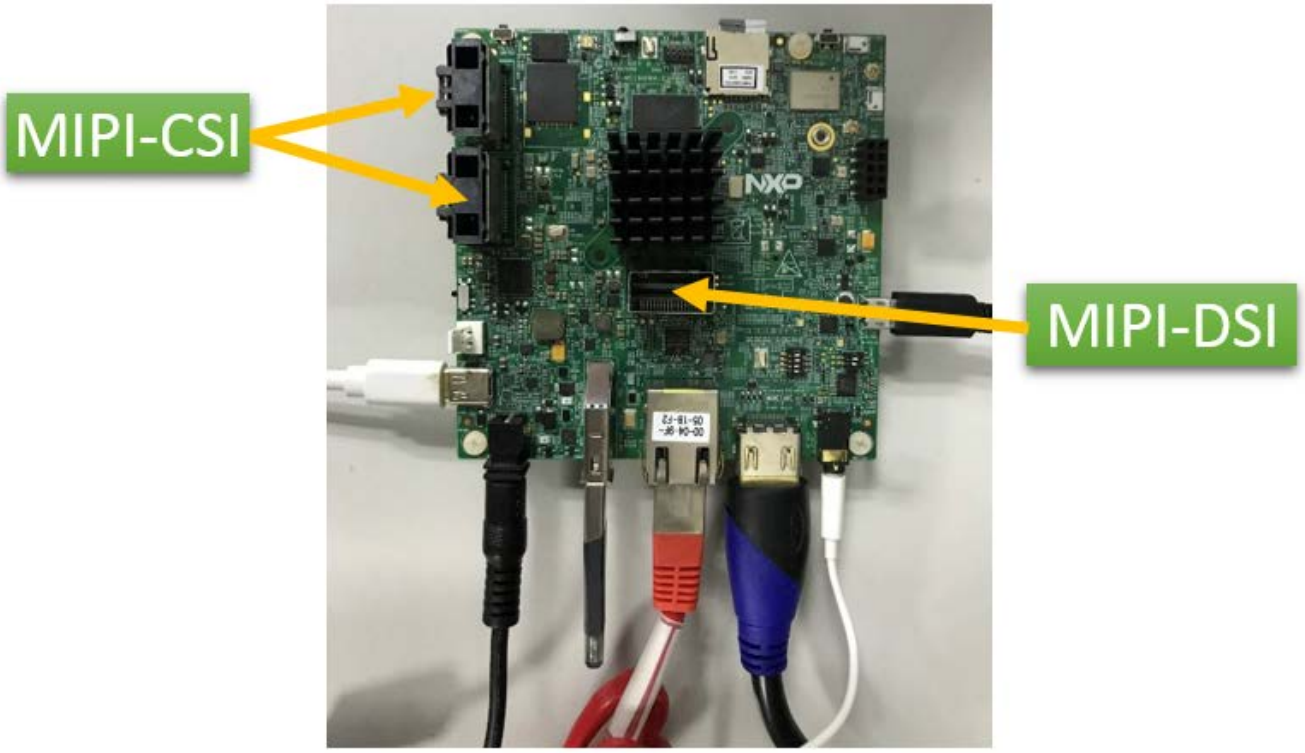


Figure 6. MIPI-DSI/CSI connector

2.14. User interface buttons

There are two user interface buttons on the EVK board.

2.14.1. Power button (SW1701)

The chip supports the use of a button input signal to request main SoC power state changes (i.e. ON or OFF) from the PMU.

ON/OFF can be configured as debounce, OFF-to-ON time, and max timeout. The debounce and OFF-to-ON time can be configured as 0, 50, 100 and 500 ms. Debounce is used to generate the power-off interrupt. In the ON state, if ON/OFF button is held longer than the debounce time, the power-off interrupt is generated. OFF-to-ON time supports the time it takes to request power-on after a button has been held longer than the configured time. In the OFF state, if ON/OFF button is held longer than the OFF-to-ON time, the state will transit from OFF to ON. Max timeout can be configured as 5 s, 10 s, 15 s and disable. Max timeout can also be the time for requesting power down after ON/OFF button has been held for the defined time.

2.14.2. Reset button (SW1702)

In the ON state, holding the RESET button (SW1702) will force to reset the power rails except the VDD_SNVS on the i.MX 8M EVK board. The i.MX 8MDQLQ applications processor will be immediately turned off and reinitiate a boot cycle from the OFF state.

2.15. WiFi/BT (U1301/J1401)

The MCIMX8M EVK board has two ways to support WiFi/BT function:

1. Chip on board WiFi: LBEE5U91CQ-TEMP;
2. M.2 WiFi/BT card.

Both ways share the same UART interface for BT function, so the BT function cannot be used at the same time. For WiFi, there are two standalone PCIe interfaces for this purpose, and WiFi function can be used at the same time.

2.16. User interface LED indicators

There are two LED indicators on the board. These LEDs have the following functions:

- Main Power Supply (D1601)
  - Green – CPU is running on OD mode.
  - Red – WALL_12V_DC_JACK is provided and SW701 is powered on.
  - OFF – The board is powered off.
- UART (D1702/D1703)
  - Green light flashing – The UART data transmitted to PC.
  - Orange light flashing – The UART data received from PC.

2.17. HDMI connector (J1001)

The i.MX 8M EVK board has a Type-A HDMI connector that can playback 4K video.

3. PCB information

The overall dimensions of the i.MX 8M EVK board PCB are shown in **Figure 3**. The EVK board is made with standard 10-layer technology. The material used was FR-4, and the PCB stack-up information is shown in **Table 6.**

Table 6. Board stack up information

Layer	Description	Coppoer (Oz.)	Dielectric thickness (mil)
1	Signal	0.333	
	Dielectric		TU768P:2.741mil
2	GND	1	
	Dielectric		TU768P:3.94mil
3	Power	1	
	Dielectric		TU768P:4.409mil
4	Signal	1	
	Dielectric		TU768P:3.94mil
5	GND	1	3.0
	Dielectric		TU768P:4.491mil
6	Signal	1	
	Dielectric		TU768P:3.94mil
7	GND	1	
	Dielectric		TU768P:4.465mil
8	Signal	1	
	Dielectric		TU768P:3.94mil
9	GND	1	
	Dielectric		TU768P:2.743mil
10	Signal	0.333	

3.1. EVK design files

You can download the schematics, layout file, gerber files, and BOM from www.nxp.com/i.MX8M.

NOTE

The CPU dies when the temperature is over 95°C due to some use cases. It is strongly recommended to install fans on the heatsink to avoid any potential damages to the PCBA. You can get fans from www.nxp.com/i.MX8M.

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