

MNADC12062M-X REV 0A0

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12-BIT, 1MHz, 75mW A/D CONVERTER WITH INPUT MULTIPLEXER AND SAMPLE/HOLD

General Description

Using an innovative multistep conversion technique, the 12-bit ADC12062 CMOS analog-to-digital converter digitizes signals at a 1MHz sampling rate while consuming a maximum of only 75mW on a single +5V supply. The ADC12062 performs a 12-bit conversion in three lower-resolution "flash" conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12062 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 100uW.

Industry Part Number

ADC12062M

NS Part Numbers

ADC12062MW-QML

Prime Die

ADC12062

Controlling Document

5962-9559301QXA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description Temp (°C)

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Built-in sample-and-hold
- Single +5V supply
- Single channel or 2 channel multiplexer operation
- Low Power Standby mode

KEY SPECIFICATIONS

- | | |
|---|---------------|
| - Sampling rate | 1 MHz (min) |
| - Conversion time | 740 nS (typ) |
| - Signal-to-Noise Ratio, $f_{in} = 100$ kHz | 69.5 dB (min) |
| - Power dissipation ($f_s = 1$ MHz) | 75 mW (max) |
| - No missing codes over temperature | Guaranteed |

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications
- Waveform digitizers

(Absolute Maximum Ratings)

(Note 1, 2)

Supply Voltage (Vcc = DVcc = AVcc)	-0.3V to +6V
Voltage at Any Input or Output	-0.3V to Vcc + 0.3V
Input Current at Any Pin (Note 3)	25mA
Package Input Current (Note 3)	50mA
Power Dissipation (Note 4)	875mW
ESD Susceptibility (Note 5)	1500V
Soldering Information (10 seconds)	300 C
Storage Temperature Range	-65 C to +150 C
Maximum Junction Temperature (Tjmax)	150 C
Thermal Resistance ThetaJA (Still Air)	45 C/W
(500LF/Min Air flow)	27 C/W
ThetaJC	7.5 C/W

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: All voltages are measured with respect to Gnd (Gnd = Agnd = Dgnd), unless otherwise specified.
- Note 3: When the input voltage (Vin) at any pin exceeds the power supply rails (Vin < Gnd or Vin > Vcc) the absolute value of current at that pin should be limited to 25mA or less. The 50mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.
- Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax, ThetaJA and the ambient temperature TA. The maximum allowable power dissipation at any temperature is $P_d = (T_{jmax} - T_A) / \Theta_{JA}$ or the number given in the absolute maximum ratings, whichever is lower. In most cases the maximum derated power dissipation will be reached only during fault conditions.
- Note 5: Human body model, 100pF discharged through a 1.5K Ohm resistor.

Recommended Operating Conditions

(Note 1, 2)

Temperature Range

$$T_{min} \leq T_A \leq T_{max}$$
$$-55\text{ }^{\circ}\text{C} \leq T_A \leq +125\text{ }^{\circ}\text{C}$$

Supply Voltage Range
(DV_{CC} = AV_{CC})

4.5V to 5.5V

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: All voltages are measured with respect to Gnd (Gnd = Agnd = Dgnd), unless otherwise specified.

Electrical Characteristics

CONVERTER CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: DVcc = AVcc = +5V, Vref+(sense) = +4.096V, Vref-(sense) = Agnd, and fs = 1MHz.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	Resolution					12	Bits	1, 2, 3
	Differential Linearity Error				-0.8	+0.8	LSB	1
					-0.95	+0.95	LSB	2, 3
	Integral Linearity Error		1		-1.0	+1.0	LSB	1
			1		-1.5	+1.5	LSB	2, 3
	Offset Error				-1.25	+1.25	LSB	1
					-2.0	+2.0	LSB	2, 3
	Full Scale Error				-1.0	+1.0	LSB	1
					-1.5	+1.5	LSB	2, 3
	Power Supply Sensitivity	DVcc = AVcc = 5V $\pm$ 10%			-1.0	+1.0	LSB	1, 2, 3
Rref	Reference Resistance				500	1000	Ohms	1, 2, 3
Vref(+)	Vref+(sense) Input Voltage					AVcc	V	1, 2, 3
Vref(-)	Vref-(sense) Input Voltage				Agnd		V	1, 2, 3
Vin	Input Voltage Range	To Vin1, Vin2, or ADC IN			Agnd - 0.05V	AVcc + 0.05V	V	1, 2, 3
	ADC IN Input Leakage	Agnd to AVcc - 0.3V				3	uA	1, 2, 3
	MUX On-Channel Leakage	Agnd to AVcc - 0.3V				3	uA	1, 2, 3
	MUX Off-Channel Leakage	Agnd to AVcc - 0.3V				3	uA	1, 2, 3

Electrical Characteristics

DYNAMIC CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: DVcc = AVcc = +5V, Vref+(sense) = +4.096V, Vref-(sense) = AGND, Rs = 250hms, fin = 100KHz, 0dB from fullscale, fs = 1MHz

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SINAD	Signal-to-Noise Plus Distortion Ratio		2		68.0		dB	4, 5, 6
SNR	Signal-to-Noise Ratio		2, 3		69.5		dB	4, 5, 6
THD	Total Harmonic Distortion		2, 4			-74	dBc	4
			2, 4			-70	dBc	5, 6
ENOB	Effective Number of Bits		2, 5		11.0		Bits	4, 5, 6

DC ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: DVcc = AVcc = +5V, Vref+(sense) = +4.096V, Vref-(sense) = Agnd, fs = 1MHz.

Vin(1)	Logical "1" Input Voltage	DVcc = AVcc = +5.5V			2.0		V	1, 2, 3
Vin(0)	Logical "0" Input Voltage	DVcc = AVcc = +4.5V				0.8	V	1, 2, 3
Iin(1)	Logical "1" Input Current					1.0	uA	1, 2, 3
Iin(0)	Logical "0" Input Current					1.0	uA	1, 2, 3
Vout(1)	Logical "1" Output Voltage	DVcc = AVcc = +4.5V, Iout = -360uA			2.4		V	1, 2, 3
		DVcc = AVcc = +4.5V, Iout = -100uA			4.25		V	1, 2, 3
Vout(0)	Logical "0" Output Voltage	DVcc = AVcc = +4.5V, Iout = 1.6mA				0.4	V	1, 2, 3
Iout	TRI-STATE @ Output Leakage Current	Pins DB0-DB11				3	uA	1, 2, 3
Dlcc	DVcc Supply Current					3	mA	1, 2, 3
Alcc	AVcc Supply Current					12	mA	1, 2, 3

Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: DVcc = AVcc = +5V, Vref+(sense) = +4.096V, Vref-(sense) = Agnd, fs = 1MHz.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fs	Maximum Sampling Rate (1/tTHROUGHPUT)				1		MHz	9, 10, 11
tconv	Conversion Time (S/H Low to EOC High)				600	980	nS	9, 10, 11
ts/ñ	S/H Pulse Width				5	550	nS	9, 10, 11
teoc	S/H Low to EOC Low				60	125	nS	9, 10, 11
tacc	Access Time (RD Low or OE High to Data Valid)	Cl = 100pF				20	nS	9, 10, 11
t1h, t0h	TRI-STATE Control (RD High or OE Low Databus TRI-STATE)	Rl = 1k ohm, Cl = 10pF				40	nS	9, 10, 11
tīnñh	Delay from RD Low to INT High	Cl = 100pF				60	nS	9, 10, 11
tīnñl	Delay from EOC High to INT Low	Cl = 100pF			-35	-10	nS	9, 10, 11
tupdate	EOC High to New Data Valid					15	nS	9, 10, 11
tms	Multiplexer Address Setup Time (MUX Address Valid to EOC Low)				50		nS	9, 10, 11
tmh	Multiplexer Address Hold Time (EOC Low to MUX Address Invalid)				50		nS	9, 10, 11
tñss	CS Setup Time (CS Low to RD Low, S/H Low, or OE High)				20		nS	9, 10, 11
tñsh	CS Hold Time (CS High after RD High, S/H High, or OE low)				20		nS	9, 10, 11

Note 1: Integral Linearity Error is the maximum deviation from a straight line between the measured offset and full scale endpoints.

Note 2: Dynamic testing of the ADC12062 is done using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies.

Note 3: The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

(Continued)

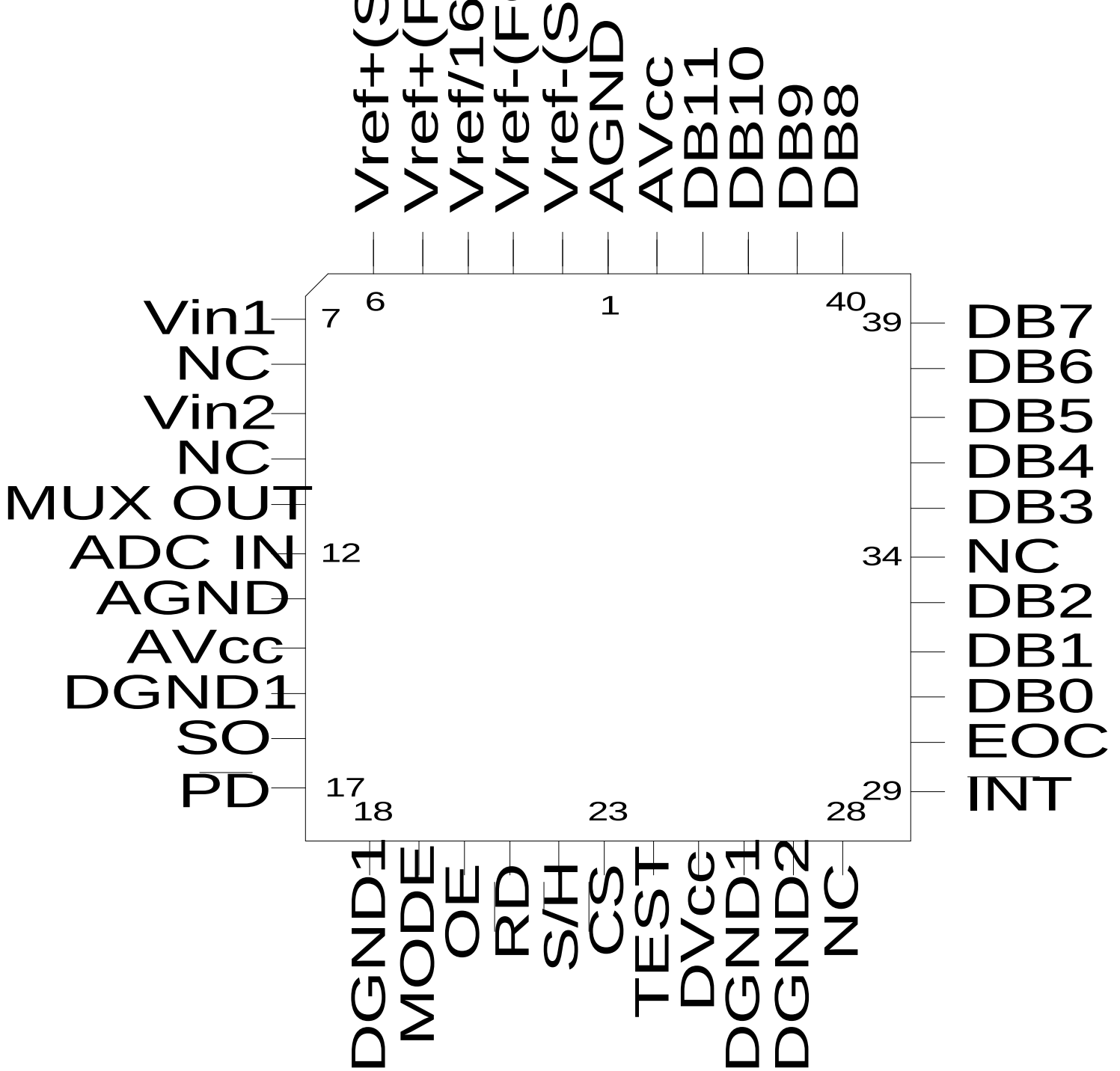
Note 4: The contributions from the first nine harmonics are used in the calculation of the THD.

Note 5: Effective Number of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation $ENOB = (SINAD - 1.76)/6.02$.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
6309HRA1	CERQUAD, 44LD, STRAIGHT (B/I CKT)
P000005A	CERQUAD, 44LD, STRAIGHT (PIN OUT)
WA44ARB	CERQUAD, 44LD, STRAIGHT(P/P DWG)

See attached graphics following this page.



ADC12062MW/883
CONNECTION DIAGRAM
44 - LEAD QUAD F/P
(TOP VIEW)
P000005A

