
ALINX ALTER Core Board AC4075 User Manual



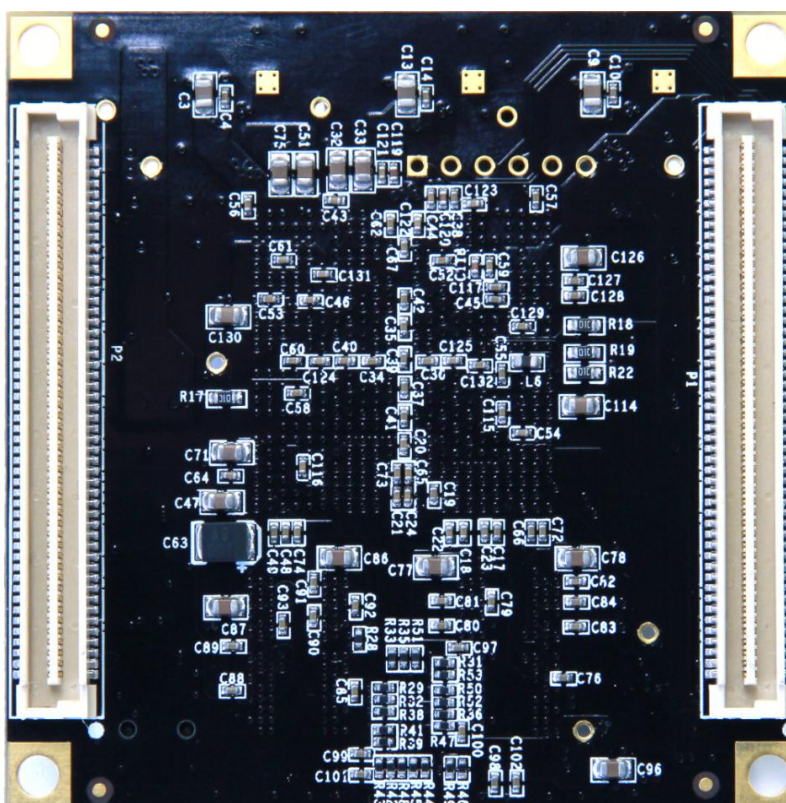
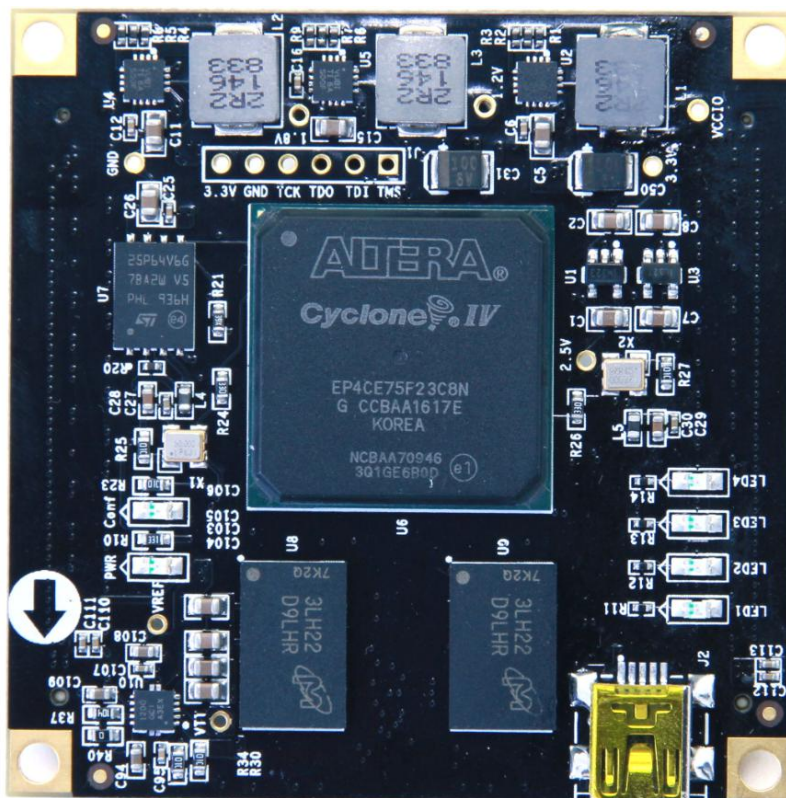
Version Record

Version	Date	Release By	Description
Rev 1.0	2020-11-07	Rachel Zhou	First Release

Table of Contents

Version Record.....	2
Part 1: AC4075 core board.....	4
Part 2: DDR2 DRAM.....	5
Part 3: SPI Flash.....	7
Part 4: FPGA Power Supply.....	9
Part 5: Expansion Ports.....	11
Part 6: Power interface on Core Board.....	14
Part 7: Crystal oscillator on Core Board.....	15
Part 8: LED Light on Core Board.....	16
Part 9: Structure Diagram.....	19

Part 1: AC4075 core board



FPGA+ 2DDR2 core board is based on ALTERA CYCLONE IV series EP4CE75F23C8. This chip develops a high-performance core board with high speed, high bandwidth and high capacity. It is suitable for video image processing and high-speed data acquisition.

This core board uses two pieces of MICRON's MT47H64M16HR-3IT DDR2 chip with a total capacity of 2Gbit; two DDR2s form a 32-bit bus mode, and the read/write data bandwidth between FPGA and DDR2 is up to 8.5Gb; this configuration can satisfy 4 channels of 1080p video processing needs.

This core board extends 168 IO ports (73 pairs of LVDS differential), which is a good choice for users who need a lot of IO. Moreover, the FPGA chip to the interface is treated with the same length, and the core board size is only 60*60 (mm), which is very suitable for secondary development.

Part 2: DDR2 DRAM

Figure 2-1 detailed part of the DDR2 schematic (For details, please refer to the schematic provided by us.)

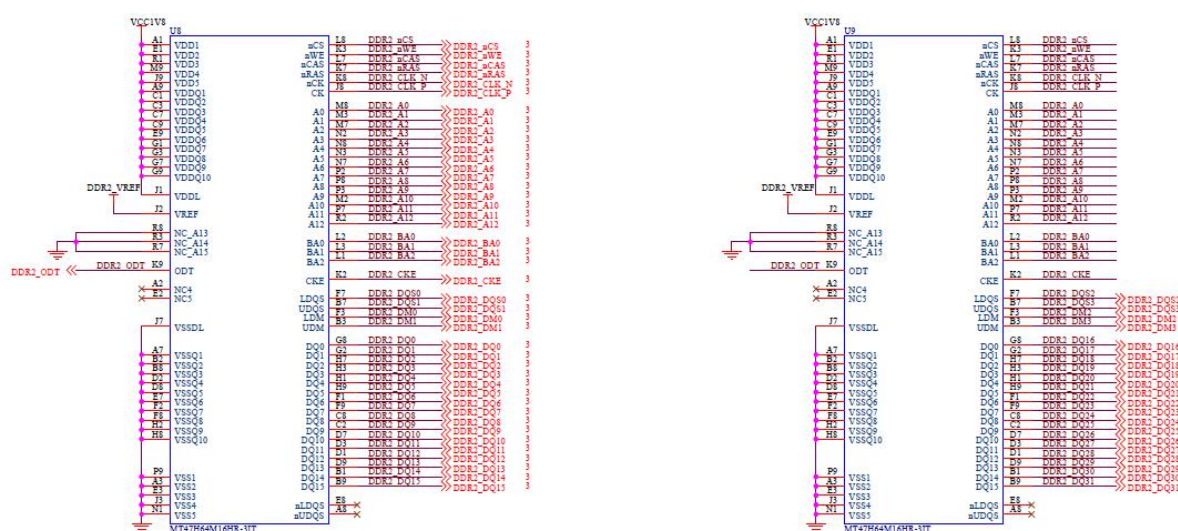


Figure 2-1: DDR2 schematic

Further, in order to allow DDR2 work properly, it is necessary to provide a reference voltage VREF and the termination voltage VTT is DDR2 DDR2 chip

DDR2_A[4]	AA4	DDR2_BA[2]	AB10
DDR2_A[5]	U15	DDR2_nCAS	Y17
DDR2_A[6]	Y4	DDR2_CKE	AA8
DDR2_A[7]	AA19	DDR2_CLK_P	Y14
DDR2_A[8]	AB3	DDR2_CLK_N	Y15
DDR2_A[9]	U16	DDR2_DQ[16]	AB18
DDR2_A[10]	Y6	DDR2_DQ[17]	W15
DDR2_nRAS	U14	DDR2_DQ[18]	W17
DDR2_nWE	AB6	DDR2_DQ[19]	AB16
DDR2_ODT	AA17	DDR2_DQ[20]	V14
DDR2_DM[0]	AA7	DDR2_DQ[21]	AB20
DDR2_DM[1]	V5	DDR2_DQ[22]	V15
DDR2_DM[2]	AA16	DDR2_DQ[23]	T15
DDR2_DM[3]	A10	DDR2_DQ[24]	AA15
DDR2_DQ[0]	Y10	DDR2_DQ[25]	AA13
DDR2_DQ[1]	AB7	DDR2_DQ[26]	AB15
DDR2_DQ[2]	AA9	DDR2_DQ[27]	AA14
DDR2_DQ[3]	AB8	DDR2_DQ[28]	AB13
DDR2_DQ[4]	U10	DDR2_DQ[29]	U12
DDR2_DQ[5]	V11	DDR2_DQ[30]	AB14
DDR2_DQ[6]	Y8	DDR2_DQ[31]	W13
DDR2_DQ[7]	W10	DDR2_DQS[0]	AB9
DDR2_DQ[8]	V8	DDR2_DQS[1]	V10
DDR2_DQ[9]	AA5	DDR2_DQS[2]	V13
DDR2_DQ[10]	Y7	DDR2_DQS[3]	Y13
DDR2_DQ[11]	W7		
DDR2_DQ[12]	W6		
DDR2_DQ[13]	U9		
DDR2_DQ[14]	Y3		
DDR2_DQ[15]	W8		

Part 3: SPI Flash

The AC4075 FPGA core board is equipped with one 64MBit SPI FLASH,

and the model is M25P64, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of SPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, core application code and other user data files. The specific models and related parameters of SPI FLASH are shown in Table 3-1.

Position	Model	Capacity	Factory
U8	M25P64	64M Bit	ST

Table 3-1: SPI FLASH Specification

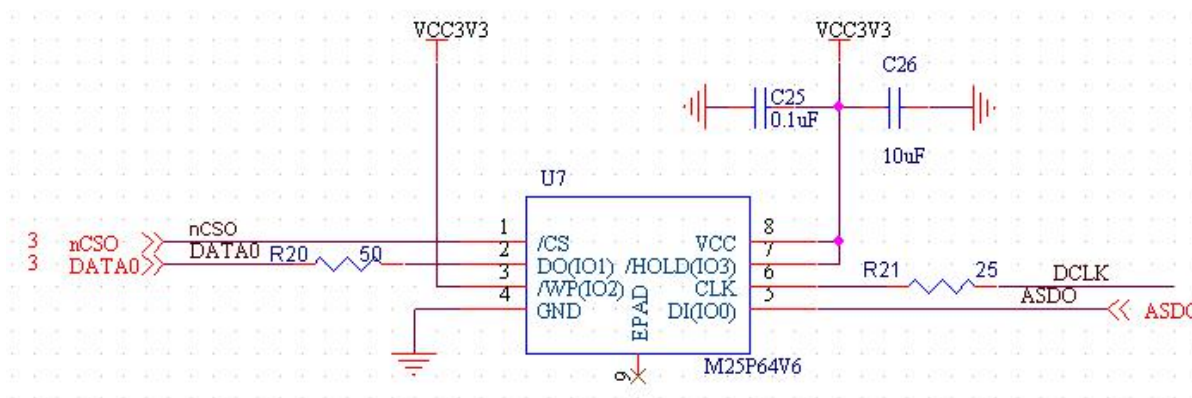


Figure 3-1: SPI Flash schematic

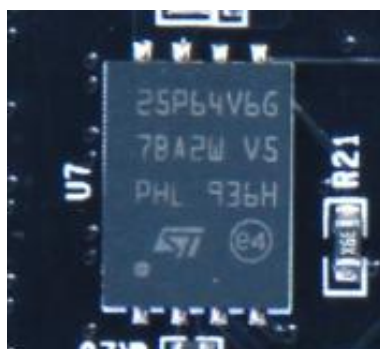


Figure 3-2: M25P64 chip on the FPGA Board

SPI Flash pin assignments:

Pin Name	FPGA Pin
DCLK	K2

nCSO	E2
DATA0	K1
ASDO	D1

Part 4: FPGA Power Supply

In order for FGPA to work properly, we need to provide 3.3V, 1.8V, 2.5V, 1.2V and VCCIO five-way power for the FPGA. Let's talk about the power pin portion of the FPGA, which includes the power pins for each bank, the core voltage pins, the analog voltage, and the phase-locked loop power supply pins.

VCCINT is the FPGA core power supply pin, connected to 1.2V; VCCIO is the power supply voltage of each BANK of the FPGA, where VCCIO1 is the power supply pin of the BANK1 of the FPGA. Similarly, VCCIO2~VCCIO8 are the power supply of the BANK2~BANK8 of the FPGA respectively. In the AC4040 core board, VCCIO3 and VCCIO4 are connected to 1.8V, because BANK3 and BANK4 are IOs connected to DDR2. The other BANK (BANK1~2, BANK5~8) voltages are connected to the adjustable VCCIO, which enables the BANK IO voltage of the FPGA to be flexibly adjusted. By adjusting the resistance value of the VCCIO power supply part, different output voltages are obtained, so that the FPGA core The board's IO level can be applied to different voltages (the default VCCIO voltage is 3.3V). In addition, with DDR2 on the core board, a termination power supply VTT and a reference power supply VREF for DDR2 are required.

The power supply (VCCIO, 1.2V, 1.8V) with three large current requirements on the FPGA development board adopts the TLV62130RGT DCDC chip imported from TI Company of the United States. It has high efficiency, small size, no heat, can provide large current, small ripple, etc. It is an excellent power solution for FPGA; a large number of high-grade imported

capacitors are used to ensure the system's power supply is stable and reliable. The three-way DCDC power supply circuit is designed as follows:

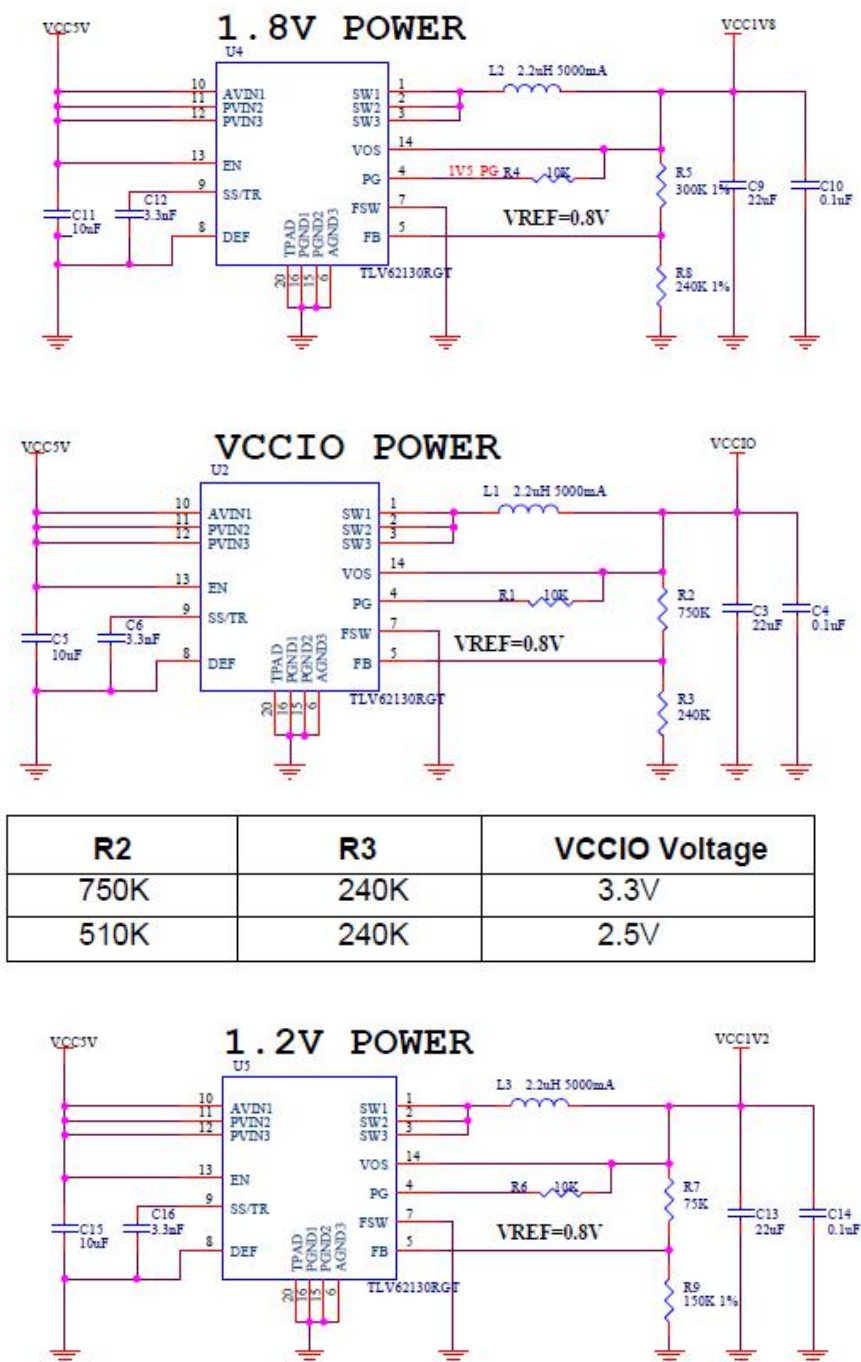


Figure 4-1: DC-DC Power Supply Schematic

The other two channels (3.3V and 2.5V) use less LDO chips SPX3819M5-L-3-3 and SPX3819M5-L-2-5 because of the low current required.

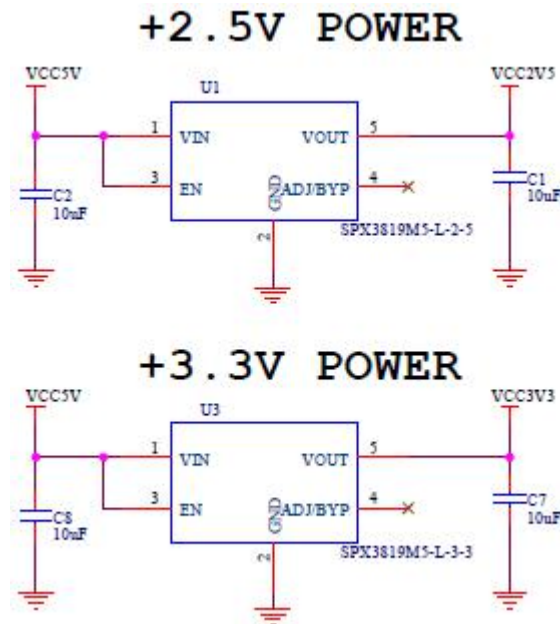


Figure 4-2: LDO Power Supply Schematic



Figure 4-3: Power Supply Circuit on the Core Board

Part 5: Expansion Ports

The core board has a total of two high-speed expansion ports, which is connected with the FPGA carrier board by two 100-pin inter-board connectors. The inter-board connector uses AMP Tyco board-to-board connector 5177984-4, with a PIN pitch of 0.8mm, and a male connector with a height of 5mm. It is connected with the female AMP connector 5177983-4 of the FPGA carrier board, which is configured for high speed data communication.

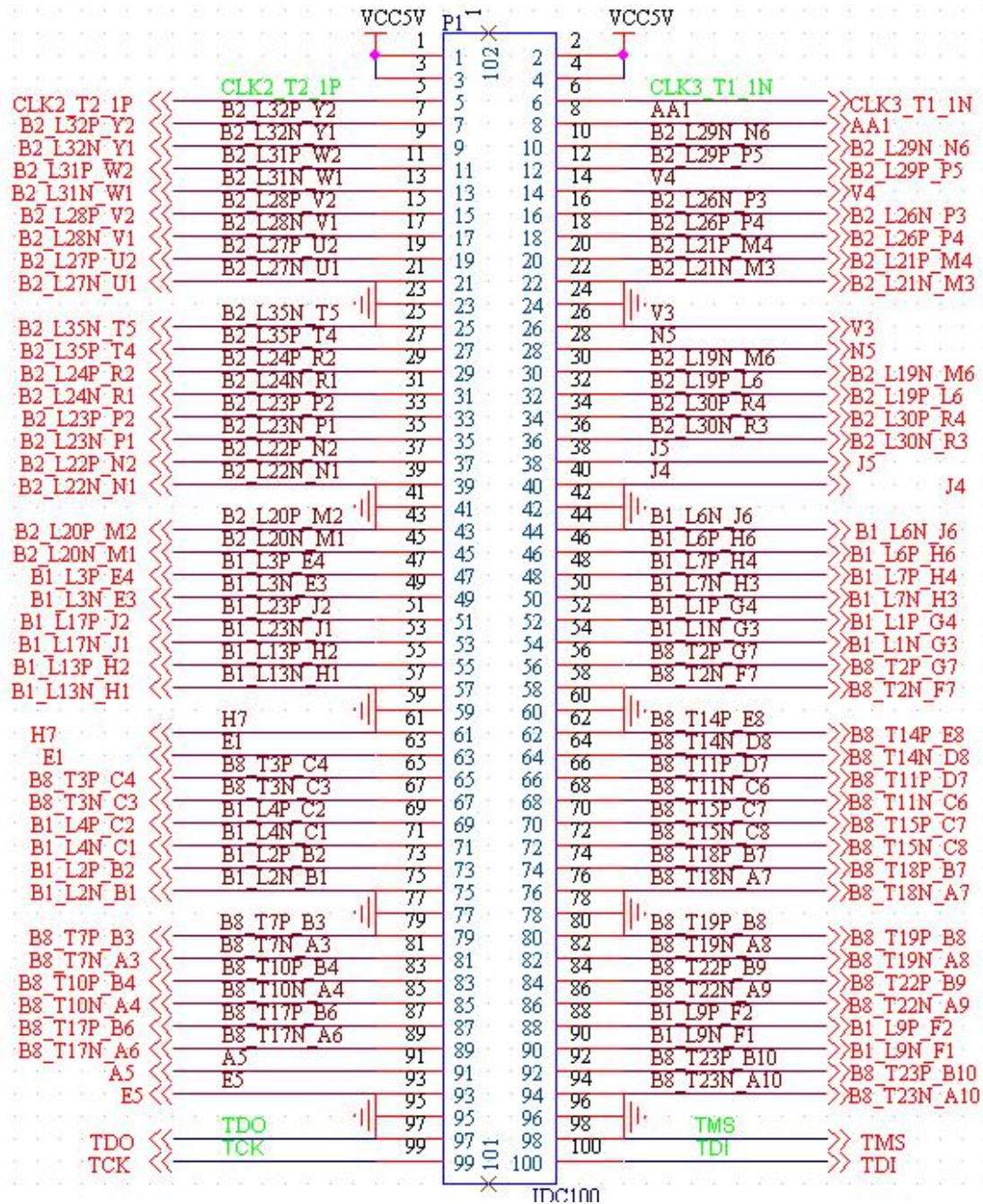


Figure 5-1: Expansion Ports P1

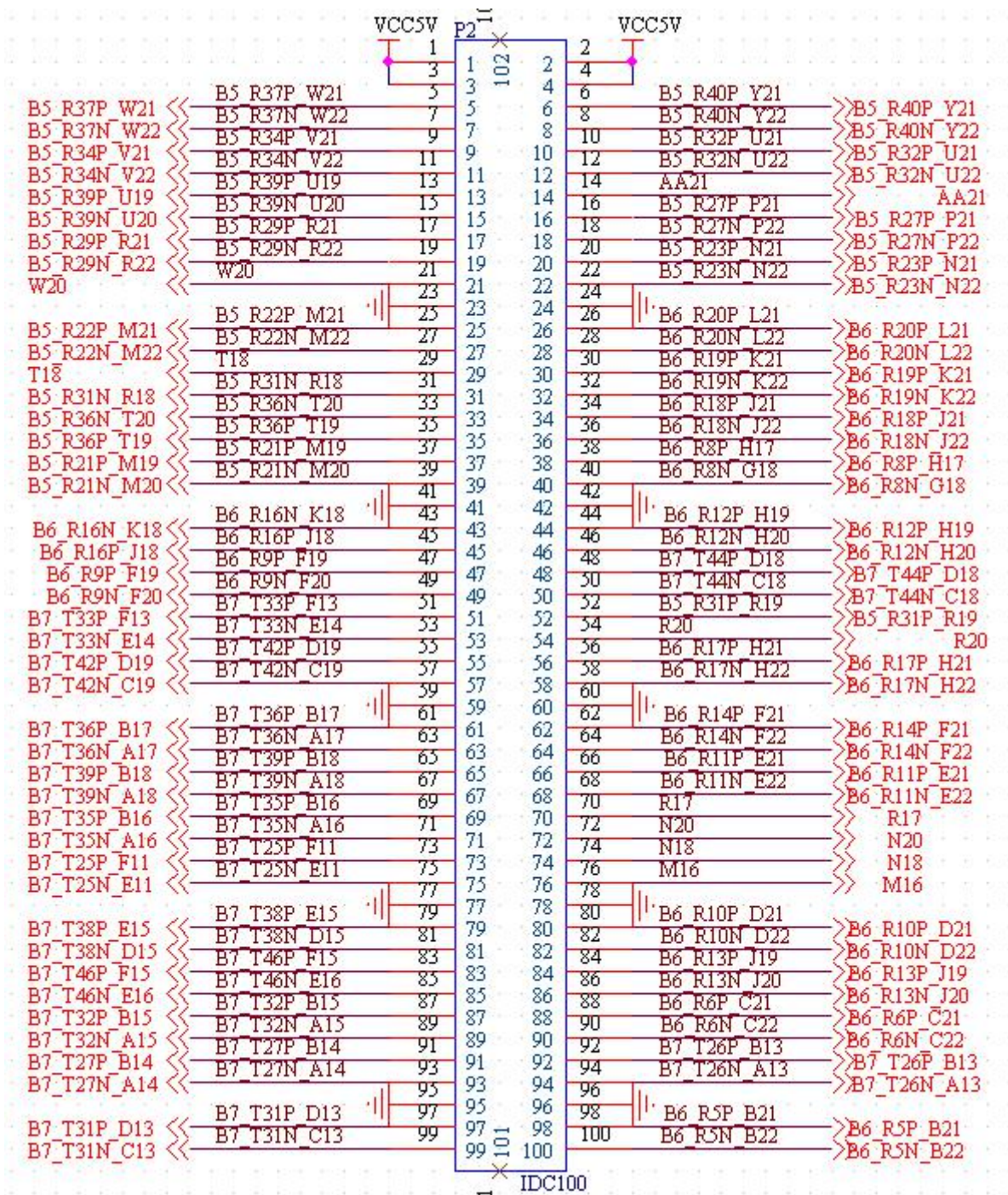


Figure 5-2: Expansion Ports P2

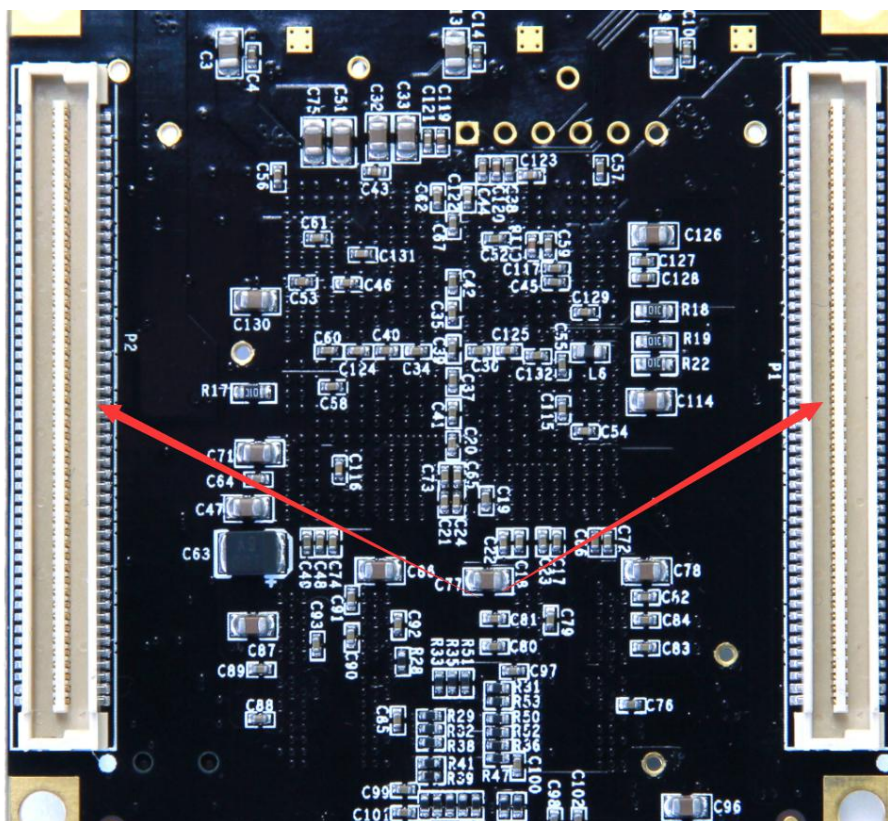


Figure 5-3: Expansion Ports P1&P2 on the Core Board

Part 6: Power interface on Core Board

In order to make the core board work normally, the FPGA expansion board needs to provide a +5V power supply to the core board through the expansion ports. The power supply voltage of the core board ranges from 4.5V to 5.5V, and the current is about 1A. In order to ensure a certain margin, the FPGA carrier board It is best to provide 5V 2A current. The FPGA carrier board provide the 5V power input to the core board through pin 1 to 4 of the expansion port P1, P2.

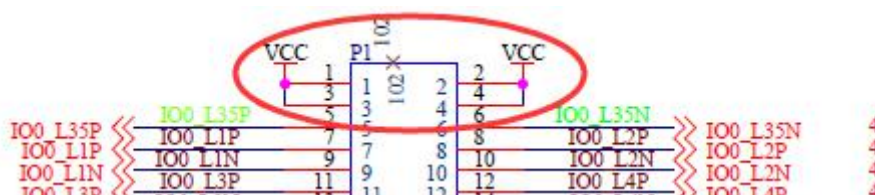


Figure 6-1: Power input pin

If you need to debug the core board separately, power the core board through the Mini USB port (J2) of the core board, the Mini USB cable is connected to the USB port of the computer. When the user supplies power to the core board through the Mini USB port (J2), it cannot be powered through the carrier board. Otherwise, current conflict may occur and the USB interface of the computer may be burned out.

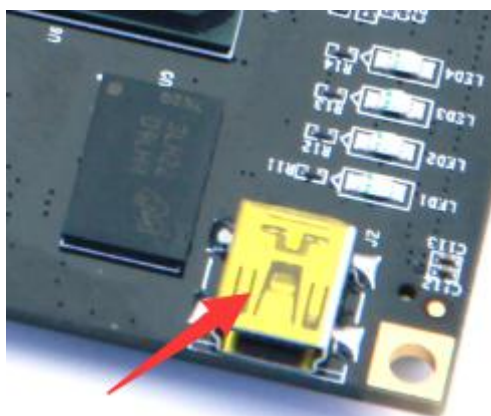


Figure 6-2: Mini USB on the Core Board

Part 7: Crystal oscillator on Core Board

The core board carries a 50M active crystal oscillator and a 27M active crystal oscillator. The 50MHz clock is connected to the G1 pin of the FPGA, and the 27MHz clock is connected to the T22 pin of the FPGA.

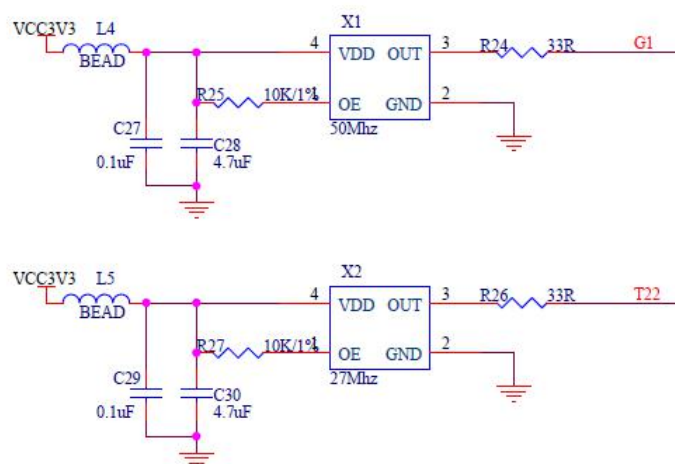


Figure 7-1: Crystal oscillator Schematic

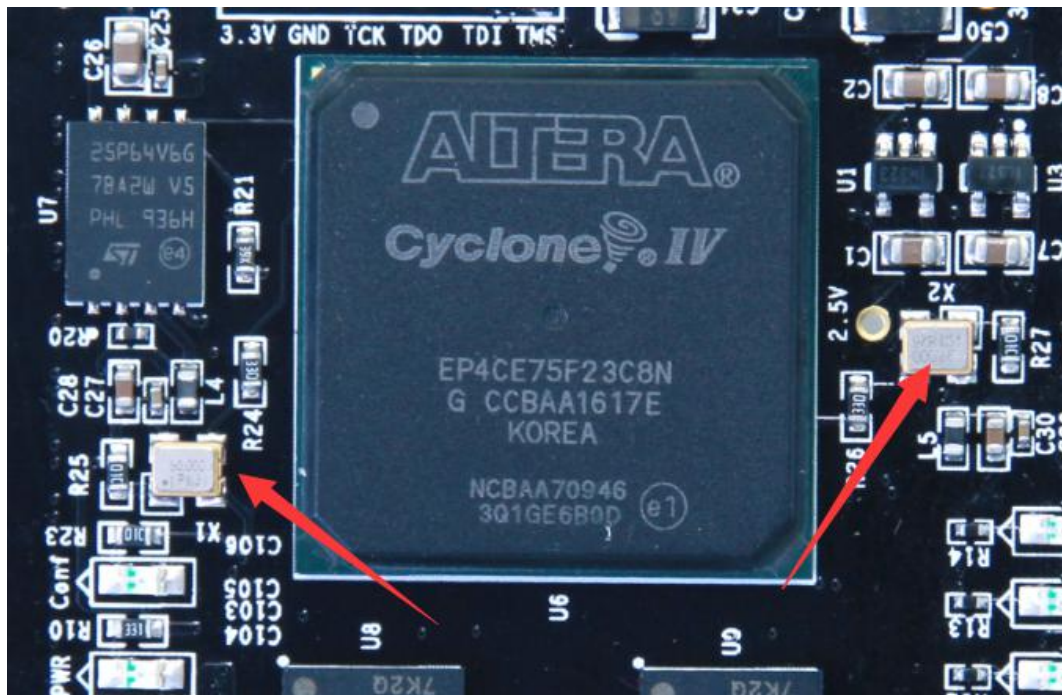


Figure 7-2: Crystal oscillator on the Core Board

Crystal oscillator Pin Assignment

Input Clock	FPGA Pin
50MHz	G1
27MHz	T22

Part 8: LED Light on Core Board

There are 6 red LED lights on the AC4075 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and four are the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate.

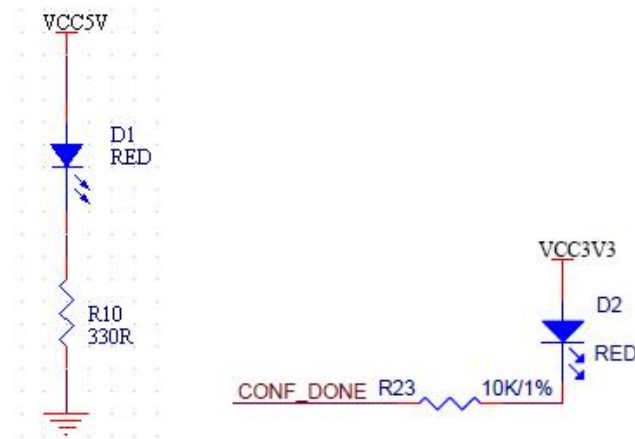


Figure 8-1: Power Indicator and Configure Indicator schematic



Figure 8-2: Power Indicator and Configure Indicator on the Core Board

The schematic diagram of the four user LED sections is shown below. In Figure 8-3, When the FPGA pin output is logic 0, the LED will be lit.

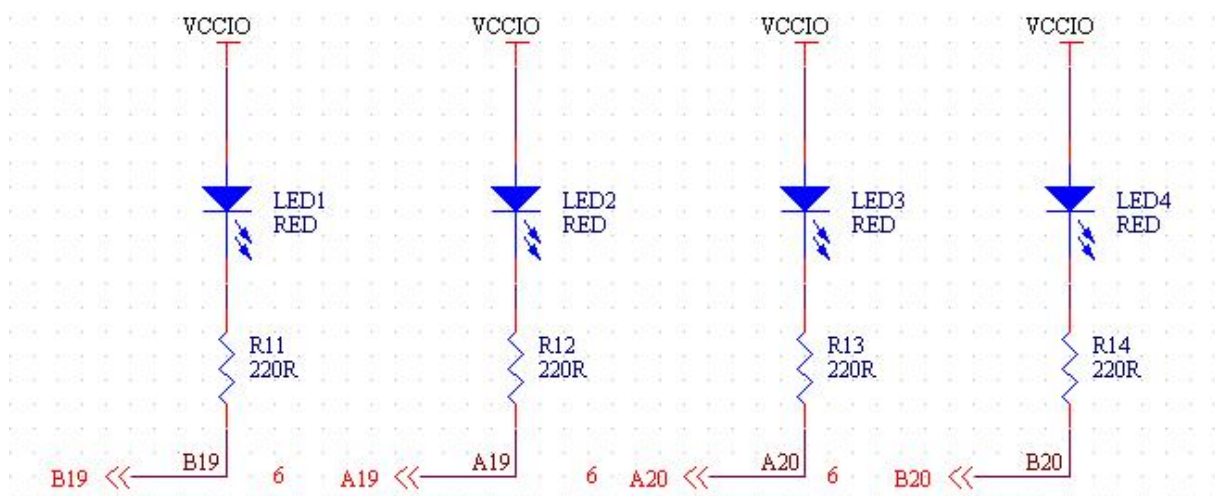


Figure 8-3: User LED Schematic

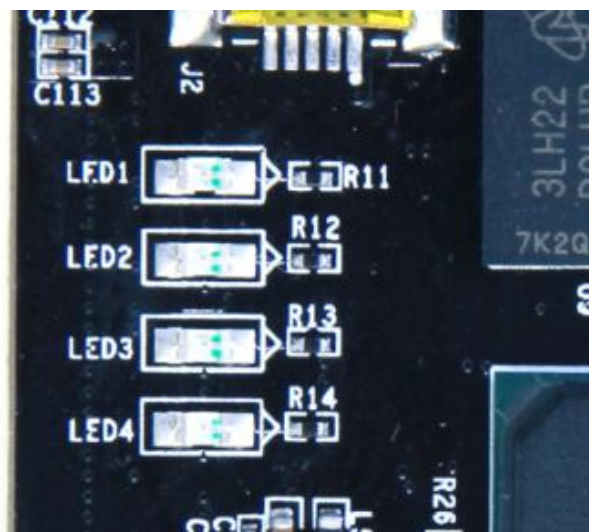


Figure 1-8-4: User LED on the Core Board

User LEDs Pin Assignment

LED Name	FPGA Pin
LED0	B19
LED1	A19
LED2	A20
LED3	B20

Part 9: Structure Diagram

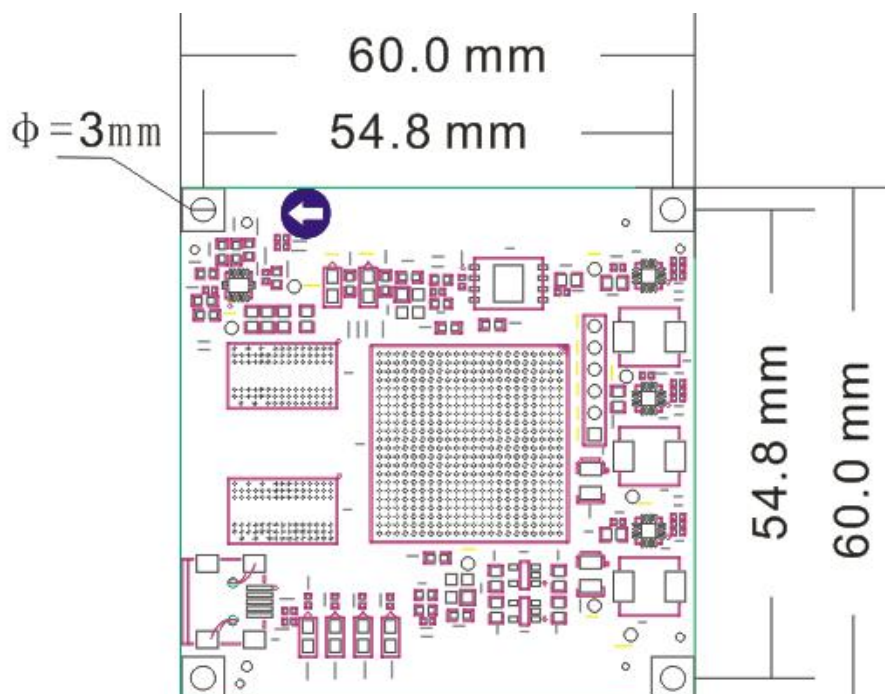


Figure 1-9-1: AC4040 FPGA Core board (Top view)

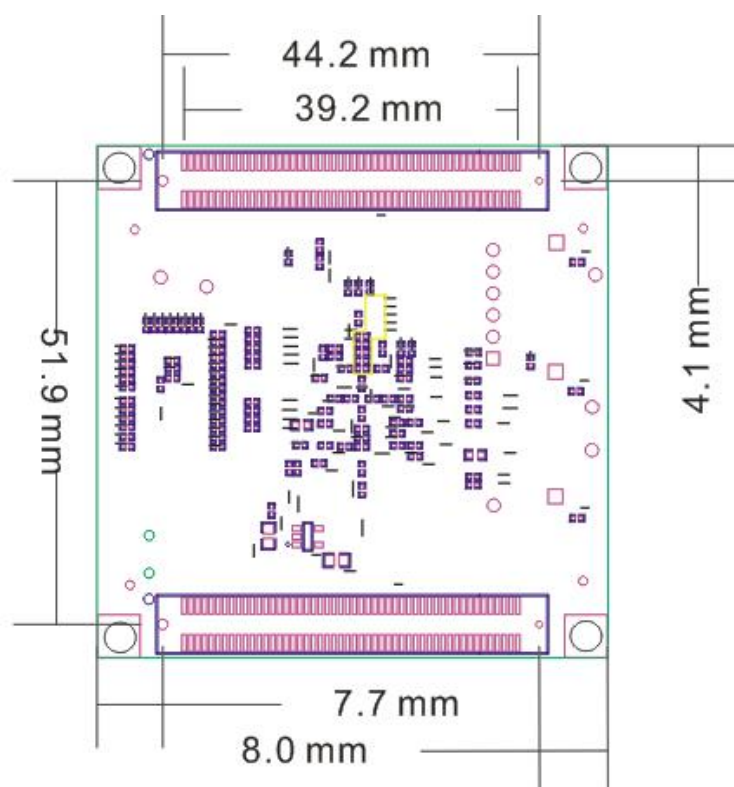


Figure 1-9-2: AC4040 FPGA Core board (Top view)