



DATA SHEET

Preliminary

O K I O P T I C A L C O M P O N E N T S

OD9652N

10-Gbps Optical Receiver Module

October 2001

Oki Semiconductor

Document Reference: JOG-00885, Rev. 1

ML7033**Preliminary****Dual-Channel Line Card CODEC****GENERAL DESCRIPTION**

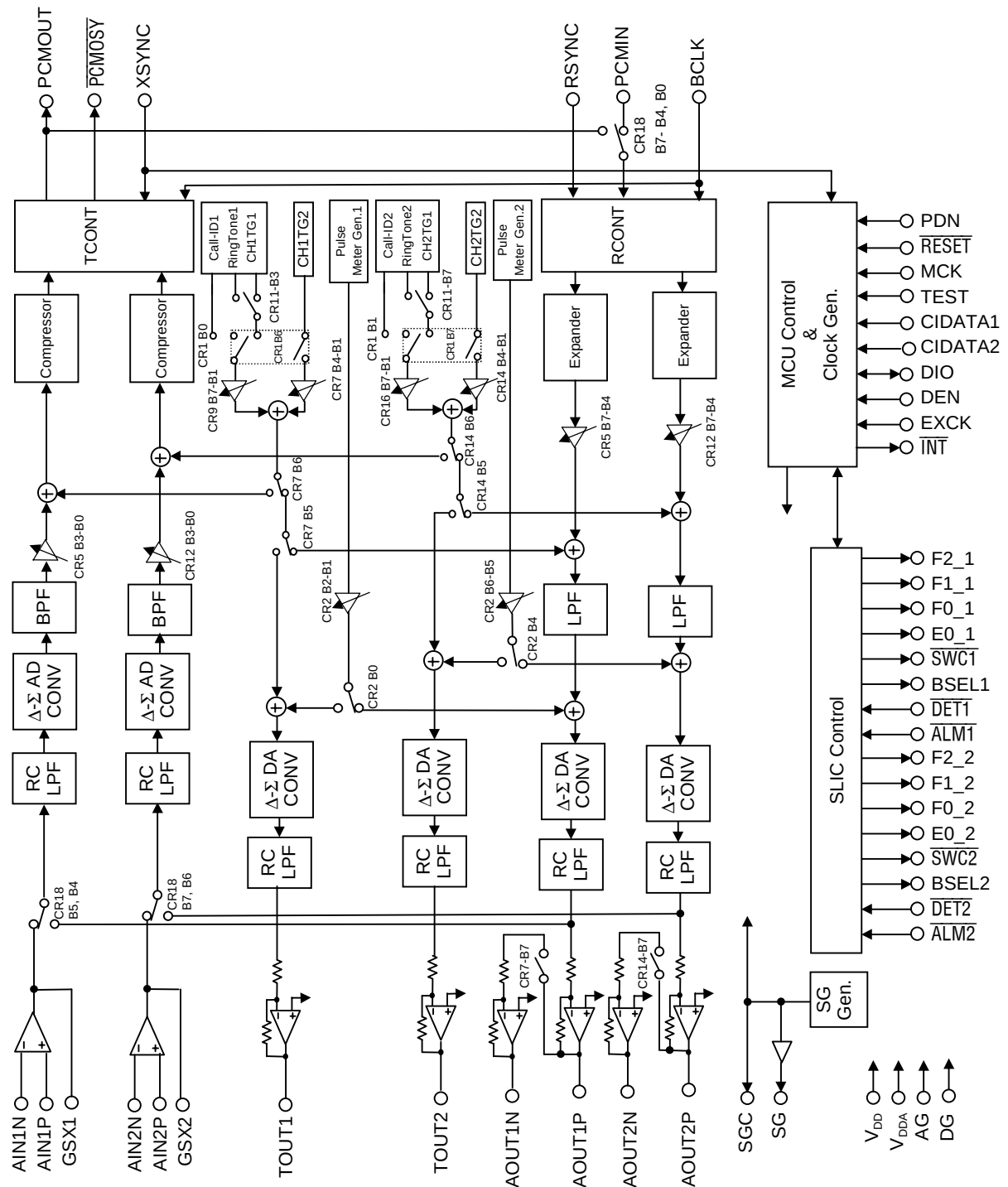
The ML7033 is a 2-channel Line Card CODEC CMOS IC for voice signals ranging from 300 to 3400 Hz. This device contains 2-channel analog-to-digital (A/D) and digital-to-analog (D/A) converters on a single chip. The ML7033 is designed especially for a single power supply and low power applications and achieves a reduced footprint.

The ML7033 is best suited for line card applications with easy interface to subscriber line interface circuits (SLICs). Especially Intersil HC5518x series.

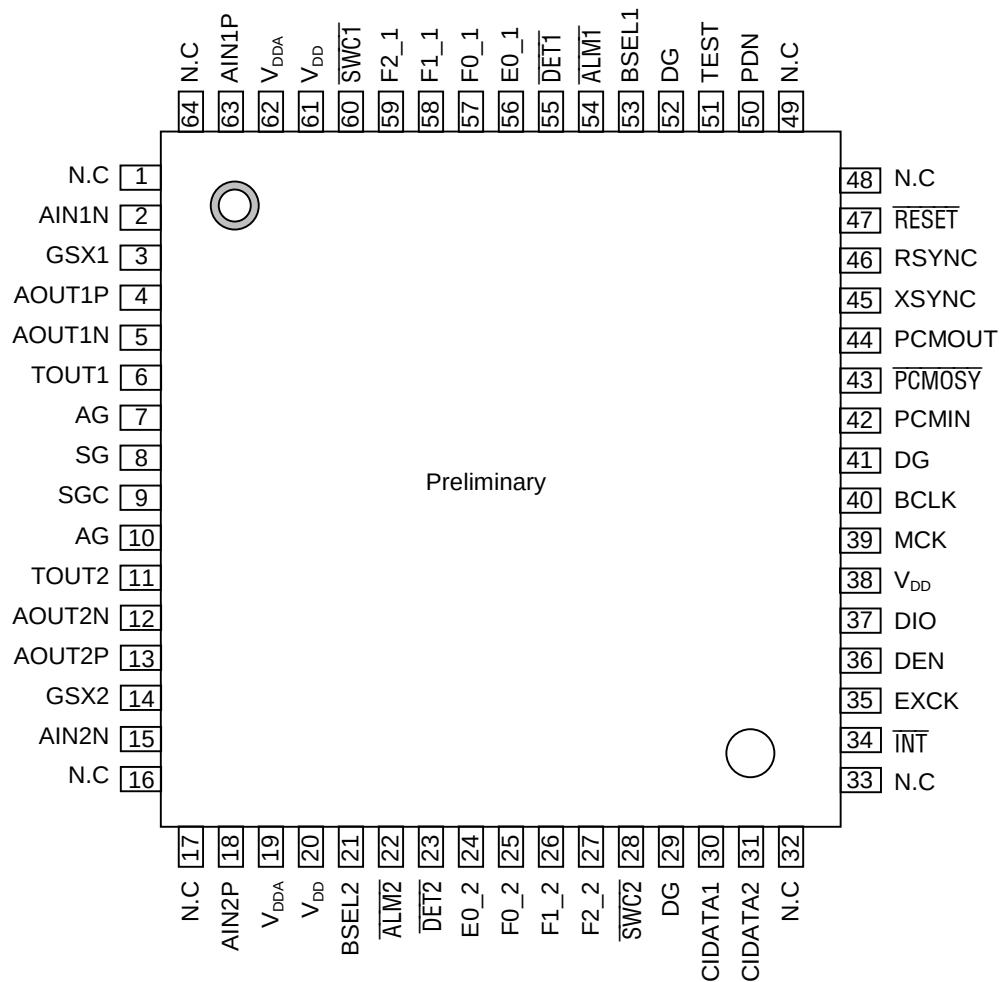
FEATURES

- Seamlessly interfaces with Intersil HC5518x series
- Single 5-V Power Supply Operation
- Using Δ - Σ ADC and DAC Technique
- ITU-T companding law - μ -law/A-law/Linear
- DSP filter response adjustment for modem application
- Low power consumption
 - 2-channel operating mode: 115 mW (typical) 180 mW (max)
 - 1-channel operating mode: 80 mW (typical) 115 mW (max)
 - Power down mode: 0.1 mW (typical) 0.25 mW (max); PDN = "0"
- Power on reset
- Dual tone generators (300 to 3400 Hz per 10 Hz step), Adjustable gain
 - Call progress tone, DTMF tone capable
- Ringing tone generator (15 to 50 Hz per 1 Hz step), Adjustable gain
- Pulse metering tone generator (12 kHz, 16 kHz), Adjustable gain
- Caller ID tone generator (ITU-T V.23, Bell 202)
- Analog and digital loop back
- Time-slot assignment
- Serial MCU interface
- Master clock: 2.048 MHz/4.096 MHz selectable
- Serial PCM transmission data rate: 256k to 4096k
- Adjustable transmit/receive gain
- Built-in reference voltage supply
- Differential or single ended analog output selectable
- Package: 64-pin plastic QFP (QFP64-P-1414-0.80-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	N.C	—	—
2	AIN1N	I	Channel-1 Transmit Op-amp Input Negative
3	GSX1	O	Channel-1 Transmit Op-amp Output
4	AOUT1P	O	Channel-1 Receive Output Positive
5	AOUT1N	O	Channel-1 Receive Output Negative
6	TOUT1	O	Channel-1 Tone Output
7	AG	—	Analog Ground
8	SG	O	Signal Ground for External Circuit
9	SGC	O	Signal Ground for Internal Circuit
10	AG	—	Analog Ground
11	TOUT2	O	Channel-2 Tone Output
12	AOUT2N	O	Channel-2 Receive Output Negative
13	AOUT2P	O	Channel-2 Receive Output Positive
14	GSX2	O	Channel-2 Transmit Op-amp Output
15	AIN2N	I	Channel-2 Transmit Op-amp Input Negative
16	N.C	—	—
17	N.C	—	—
18	AIN2P	I	Channel-2 Transmit Op-amp Input Positive
19	V _{DDA}	—	Power Supply
20	V _{DD}	—	Power Supply
21	BSEL2	O	Output for SLIC2 Battery Select
22	ALM2	I	Input from SLIC2 Thermal Detector
23	DET2	I	Input from SLIC2 Switch Hook or Ring Trip Detector
24	E0_2	O	Output for SLIC2 Detector Select
25	F0_2	O	Mode Control Output for SLIC2 F0
26	F1_2	O	Mode Control Output for SLIC2 F1
27	F2_2	O	Mode Control Output for SLIC2 F2
28	SWC2	O	Output for SLIC2 Ring relay Driver Control
29	DG	—	Digital Ground
30	CIDATA1	I	Call ID Data Input for Channel 1
31	CIDATA2	I	Call ID Data Input for Channel 2
32	N.C	—	—
33	N.C	—	—
34	INT	O	Interrupt Output (from SLIC status)
35	EXCK	I	MCU Interface Data Clock Input
36	DEN	I	MCU Interface Data Enable Input
37	DIO	I/O	MCU Interface Control Data Input/Output

Pin	Symbol	Type	Description
38	V _{DD}	—	Power Supply
39	MCK	I	Master Clock (2.048/4.096 MHz)
40	BCLK	I	PCM Data Shift Clock
41	DG	—	Digital Ground
42	PCMIN	I	PCM Data Input
43	PCMO _{SY}	O	PCM Data Synchronizing Output for Time-Slot Assignment
44	PCMOUT	O	PCM Data Output
45	XSYNC	I	Transmit Synchronizing Signal
46	RSYNC	I	Receive Synchronizing Signal
47	RESET	I	Reset for Control Register
48	N.C	—	—
49	N.C	—	—
50	PDN	I	Power Down Control
51	TEST	I	Internal Test Input (keep “0” during normal operation)
52	DG	—	Digital Ground
53	BSEL1	O	Output for SLIC1 Battery Select
54	ALM ₁	I	Input from SLIC1 Thermal Detector
55	DET ₁	I	Input from SLIC1 Switch Hook or Ring Trip Detector
56	E0_1	O	Output for SLIC1 Detector Select
57	F0_1	O	Mode Control Output for SLIC1 F0
58	F1_1	O	Mode Control Output for SLIC1 F1
59	F2_1	O	Mode Control Output for SLIC1 F2
60	SWC ₁	O	Output for SLIC1 Ring Relay Driver Control
61	V _{DD}	—	Power Supply
62	V _{DDA}	—	Analog Power Supply
63	AIN1P	I	Channel-1 Transmit Op-amp Input Positive
64	N.C	—	—

Control Register Assignment

Register	Address					Data								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	Filter2 SEL	Filter1 SEL	MCK SEL	SHORT	LIN	ALAW	MODE1	MODE0	R/W
CR1	0	0	0	0	1	CH2TG ON	CH1TG ON				CID FMT	CID CH2 ON	CID CH1 ON	R/W
CR2	0	0	0	1	0	PMG2 FRQ	PMG2 LV1	PMG2 LV0	PMG2 TOUT2	PMG1 FRQ	PMG1 LV1	PMG1 LV0	PMG1 TOUT1	R/W
CR3	0	0	0	1	1	TSAE	TSAC	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0	W
CR4	0	0	1	0	0	DET2 TIM3	DET2 TIM2	DET2 TIM1	DET2 TIM0	DET1 TIM3	DET1 TIM2	DET1 TIM1	DET1 TIM0	R/W
CR5	0	0	1	0	1	LV1R3	LV1R2	LV1R1	LV1R0	LV1X3	LV1X2	LV1X1	LV1X0	R/W
CR6	0	0	1	1	0	F2_1	F1_1	F0_1	SWC1	BSEL1	E0_1	DET1*	ALM1*	R/W
CR7	0	0	1	1	1	AOUT1 SEL	CH1TG2 TX	CH1TG2 TOUT1	CH1TG2 LV3	CH1TG2 LV2	CH1TG2 LV1	CH1TG2 LV0	CH1TG2 _8	R/W
CR8	0	1	0	0	0	CH1TG2 _7	CH1TG2 _6	CH1TG2 _5	CH1TG2 _4	CH1TG2 _3	CH1TG2 _2	CH1TG2 _1	CH1TG2 _0	R/W
CR9	0	1	0	0	1	CH1TG1 LV6	CH1TG1 LV5	CH1TG1 LV4	CH1TG1 LV3	CH1TG1 LV2	CH1TG1 LV1	CH1TG1 LV0	CH1TG1 _8	R/W
CR10	0	1	0	1	0	CH1TG1 _7	CH1TG1 _6	CH1TG1 _5	CH1TG1 _4	CH1TG1 _3	CH1TG1 _2	CH1TG1 _1	CH1TG1 _0	R/W
CR11	0	1	0	1	1	CH2 RING	CH2TG1 TRP2	CH2TG1 TRP1	CH2TG1 TRP0	CH1 RING	CH1TG1 TRP2	CH1TG1 TRP1	CH1TG1 TRP0	R/W
CR12	0	1	1	0	0	LV2R3	LV2R2	LV2R1	LV2R0	LV2X3	LV2X2	LV2X1	LV2X0	R/W
CR13	0	1	1	0	1	F2_2	F1_2	F0_2	SWC2	BSEL2	E0_2	DET2*	ALM2*	R/W
CR14	0	1	1	1	0	AOUT2 SEL	CH2TG TX	CH2TG TOUT2	CH2TG2 LV3	CH2TG2 LV2	CH2TG2 LV1	CH2TG2 LV0	CH2TG2 _8	R/W
CR15	0	1	1	1	1	CH2TG2 _7	CH2TG2 _6	CH2TG2 _5	CH2TG2 _4	CH2TG2 _3	CH2TG2 _2	CH2TG2 _1	CH2TG2 _0	R/W
CR16	1	0	0	0	0	CH2TG1 LV6	CH2TG1 LV5	CH2TG1 LV4	CH2TG1 LV3	CH2TG1 LV2	CH2TG1 LV1	CH2TG1 LV0	CH2TG1 _8	R/W
CR17	1	0	0	0	1	CH2TG1 _7	CH2TG1 _6	CH2TG1 _5	CH2TG1 _4	CH2TG1 _3	CH2TG1 _2	CH2TG1 _1	CH2TG1 _0	R/W
CR18	1	0	0	1	0	CH2 LOOP1	CH2 LOOP0	CH1 LOOP1	CH1 LOOP0	TEST3	TEST2	TEST1	TEST0	R/W
CR19	1	0	0	1	1	TEST11	TEST10	TEST9	TEST8	TEST7	TEST6	TEST5	TEST4	R/W

*: Read only bit

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	−0.3 to +7.0	V
Analog Input Voltage	V_{AIN}	—	−0.3 to $V_{DD}+0.3$	V
Digital Input Voltage	V_{DIN}	—	−0.3 to $V_{DD}+0.3$	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	—	−40	—	+85	°C
High Level Input Voltage	V_{IH}	All Digital Input Pins	2.2	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	0.8	V
MCK Frequency	F_{MCK}	MCK = 2.048 MHz (MCK SEL = "0")	−0.01%	2048	+0.01%	kHz
		MCK = 4.096 MHz (MCK SEL = "1")	−0.01%	4096	+0.01%	kHz
BCLK Frequency	F_{BCLK}	BCLK	256	—	4096	kHz
Sync Pulse Frequency	F_{SYNC}	XSYNC, RSYNC	−0.01%	8	+0.01%	kHz
Clock Duty Ratio	D_{CLK}	MCK, BCLK	40	50	60	%
Digital Input Rise Time	t_{IR}	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time	t_{IF}		—	—	50	ns
MCK to BCLK Phase Difference	t_{MB}	MCK, BCLK	—	—	50	ns
Transmit Sync Pulse Setting Time	t_{XS}	BCLK to XSYNC	50	—	—	ns
	t_{SX}	XSYNC to BCLK	50	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLK to RSYNC	50	—	—	ns
	t_{SR}	RSYNC to BCLK	50	—	—	ns
Sync Pulse Width	t_{WS}	XSYNC, RSYNC, SHORT = "0"	1 BCLK	—	125 μ s – 1BCLK	μ s
		XSYNC, RSYNC, SHORT = "1"	210	—	1BCLK	ns
PCMOUT Set-up Time	t_{DS}	PCMOUT	50	—	—	ns
PCMOUT Hold Time	t_{DH}	PCMOUT	50	—	—	ns
Digital Output Load	R_{DL}	Pull-up Resistor, PCMOUT	0.5	—	—	k Ω
	C_{DL1}	PCMOUT	—	—	50	pF
	C_{DL2}	Other output pins	—	—	50	pF
Bypass Capacitor for SGC	C_{SG}	SGC to AG	0.1	—	—	μ F

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I _{DD1}	2CH Operating Mode, No Signal	—	23.0	35.0	mA
	I _{DD2}	1CH Operating Mode, No Signal	—	16.0	22.0	mA
	I _{DD4}	Power Down Mode, PDN = "0"	—	25.0	50.0	μA
High Level Input Leakage Current	I _{IH}	All Digital Input Pins V _I = V _{DD}	—	0.1	5.0	μA
Low Level Input Leakage Current	I _{IL}	All Digital Input Pins V _I = 0 V	–5.0	–0.1	—	μA
Digital Output Low Voltage	V _{OL1}	PCMOUT, Pull-up = 0.5 kΩ	0	0.2	0.4	V
	V _{OL2}	Other output pins, I _{OL} = –0.4 mA	0	0.2	0.4	V
Digital Output High Voltage	V _{OH}	I _{OH} = 0.4 mA	2.5	—	—	V
Digital Output Leakage Current	I _O	PCMOUT High Impedance State	—	—	10	μA
Input Capacitance	C _{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SG, SGC Output Voltage	V _{SG}	SGC to AG 0.1 μF	—	2.4	—	V
SG, SGC Rise Time	t _{SGC}	SGC to AG 0.1 μF Rise time to 90% of max. level	—	—	10	ms
SG Output Load Resistance	R _{LSG}	SG	10	—	—	kΩ

Transmit Analog Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R _{INX}	AIN1N, AIN1P, AIN2N, AIN2P	—	10	—	MΩ
Output Load Resistance	R _{LGX}	GSX1, GSX2 with respect to SGC *1	20	—	—	kΩ
Output Load Capacitance	C _{LGX}		—	—	30	pF
Output Amplitude	V _{OGX}		—	—	2.226	V _{pp}
Offset Voltage	V _{OSGX}		–50	—	50	mV

*1 –3.0 dBm (600Ω) = 0 dBm0, 3.17 dBm0 (μ-law) = 2.226 V_{pp}

Receive Analog Interface Characteristics(V_{DD} = 4.75 to 5.25 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Load Resistance	R _{LAO}	AOUT1P, AOUT1N, AOUT2P, AOUT2N (each) with respect to SG	20	—	—	kΩ
	R _{LTO}	TOUT1, TOUT2 (each) with respect to SG	10	—	—	kΩ
Output Load Capacitance	C _{LAO}	AOUT1P, AOUT1N, AOUT2P, AOUT2N, TOUT1, TOUT2	—	—	50	pF
Output Amplitude	V _{OAO}	AOUT1P, AOUT1N, AOUT2P, AOUT2N, TOUT1, TOUT2, R _{LAO} = 20 kΩ with respect to SG	—	—	3.4 *2	V _{pp}
Offset Voltage	V _{OSAO}	AOUT1P, AOUT1N, AOUT2P, AOUT2N, TOUT1, TOUT2 with respect to SG	-100	—	100	mV

*2 0.658 dBm (600Ω) = 0 dBm0, 3.17 dBm0 (μ-law) = 3.4 V_{pp}

AC Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
		Freq. (Hz)	Level (dBm0)					
Transmit Frequency Response	Loss T1	60	0	GSXn to PCMOUT (Attenuation)	25	45	dB	
	Loss T2	300			−0.15	0.15		0.20
	Loss T3	1020			Reference			
	Loss T4	3000			−0.15	0.02		0.20
	Loss T5	3300			−0.15	0.1		0.80
	Loss T6	3400			0	0.6		0.80
Receive Frequency Response	Loss R1	100	0	PCMIN to AOUTn (Attenuation)	−0.15	0.04	dB	
	Loss R2	1020			Reference			
	Loss R3	3000			−0.15	0.07		0.2
	Loss R4	3300			−0.15	0.2		0.8
	Loss R5	3400			0	0.6		0.8
Transmit Signal to Distortion Ratio	SDT1	1020	3	GSXn to PCMOUT *2	36	43	dB	
	SDT2		0		36	40		
	SDT3		−30		36	38		
	SDT4		−40		30	32		
	SDT5		−45		25	29		
Receive Signal to Distortion Ratio	SDR1	1020	3	PCMIN to AOUTn *2	36	42	dB	
	SDR2		0		36	39		
	SDR3		−30		36	39		
	SDR4		−40		30	33		
	SDR5		−45		25	30		
Transmit Gain Tracking	GTT1	1020	3	GSXn to PCMOUT	−0.2	0.02	dB	
	GTT2		−10		Reference			
	GTT3		−40		−0.2	0.06		0.2
	GTT4		−50		−0.6	0.4		0.6
	GTT5		−55		−1.2	0.4		1.2
Receive Gain Tracking	GTR1	1020	3	PCMIN to AOUTn	−0.2	0	dB	
	GTR2		−10		Reference			
	GTR3		−40		−0.2	−0.02		0.2
	GTR4		−50		−0.6	−0.1		0.6
	GTR5		−55		−1.2	−0.2		1.2

*2 C-message Filter is used

AC Characteristics (Continued)

(V_{DD} = 4.75 to 5.25 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)					
Idle Channel Noise	NIDLE _T	—	—	Analog input =SGC *2 AINn to PCMOUT Gain = 1 (μ-law)	—	9	15	dBnc0
	NIDLE _R	—	—	PCMIN = 'FF'h (μ-law) PCMIN = 'D5'h (A-law) PCMIN = all '0'(linear) *2 PCMIN to AOUTn	—	4	10	
Absolute Level (Initial Difference)	AV _T /AV _R	1020	0	GSXn to PCMOUT V _{DD} = 5 V, Ta = 25°C	0.511	0.548	0.587	Vrms
				PCMIN to AOUTn (Single-ended) V _{DD} = 5 V, Ta = 25°C	0.806	0.835	0.864	
Absolute Level (Deviation of Temperature and Power)	AV _{TT} AV _{RT}					V _{DD} = 4.75 to 5.25 V Ta = −40 to 85°C	−0.3 −0.3	— —
Absolute Delay	T _D	1020	0	A to A Mode BCLK = 2048 kHz	—	0.58	0.6	ms
Transmit Group Delay	T _{GD} T1	500	0	*3	—	0.26	0.75	ms
	T _{GD} T2	600			—	0.16	0.35	
	T _{GD} T3	1000			—	0.02	0.125	
	T _{GD} T4	2600			—	0.05	0.125	
	T _{GD} T5	2800			—	0.07	0.75	
Receive Group Delay	T _{GD} R1	500	0	*3	—	0.00	0.75	ms
	T _{GD} R2	600			—	0.00	0.35	
	T _{GD} R3	1000			—	0.00	0.125	
	T _{GD} R4	2600			—	0.09	0.125	
	T _{GD} R5	2800			—	0.12	0.75	
Cross Talk Attenuation	CR _T	1020	0	Trans to Receive	75	83	—	dB
	CR _R			Receive to Trans	75	80	—	
	CR _{CH}			Channel to Channel	75	78	—	
Discrimination	DIS	4.6 to 72k	0	0 to 4 kHz	30	32	—	dB
Out of Band Spurious	OBS	300 to 3.4K	0	4.6 to 1000 kHz	—	−37.5	−35	dB
Signal Frequency Distortion	SFD _T	1020	0	0 to 4 kHz	—	−50	−40	dBm0
	SFD _R				—	−48	−40	
Intermoduration Distortion	IMD _T	fa = 470	−4	2 fa − fb	—	−50	−40	dBm0
	IMD _R	fb = 320			—	−54	−40	
Power Supply Noise Rejection Ratio	PSR _{T1}	0 to 4k	100 mVrms	*4	40	44	—	dB
	PSR _{T2}	4 to 50k			50	55	—	
	PSR _{R1}	0 to 4k			40	45	—	
	PSR _{R2}	4 to 50k			50	56	—	

*3 Minimum value of the group delay distortion

*4 The measurement under idle channel noise

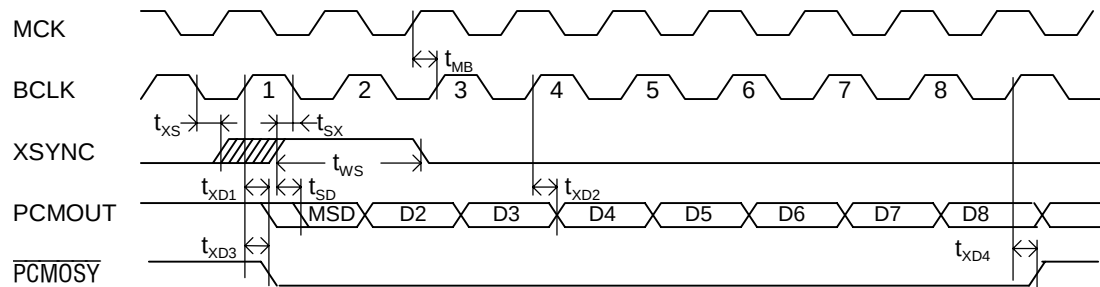
AC Characteristics (Continued)

(V_{DD} = 4.75 to 5.25 V, Ta = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t _{SD}	PCMOUT	—	—	100	ns
	t _{XD1}	Pull-up resistor = 0.5 kΩ	—	—	100	
	t _{XD2}	C _L = 50 pF and 1 LSTTL	—	—	100	
	t _{XD3}	$\overline{\text{PCMOSY}}$, C _L = 50 pF	—	—	100	ns
	t _{XD4}		—	—	100	
PCMOUT Operation Delay Time	t _{DDO}	Time of operation start after power on	—	4	—	ms
AOUTn/TOUn Signal Output Delay Time	t _{DAO}	Time of base band signal output start after power on	—	4	—	ms
Serial Port I/O Setting Time	t ₁	Cload = 50 pF	50	—	—	ns
	t ₂		50	—	—	ns
	t ₃		50	—	—	ns
	t ₄		50	—	—	ns
	t ₅		100	—	—	ns
	t ₆		50	—	—	ns
	t ₇		50	—	—	ns
	t ₈		—	—	50	ns
	t ₉		50	—	—	ns
	t ₁₀		50	—	—	ns
	t ₁₁		—	—	50	ns
EXCK Clock Frequency	f _{EXCK}	EXCK	0.5	—	10	MHz
SLIC Interface Delay Time	t ₂₀		—	—	200	ns
	t ₂₁		—	20	—	μs
	t ₂₂		—	—	200	ns
	t ₂₃		—	—	200	ns
	t ₂₄		—	—	225	ms

TIMING DIAGRAM

Long Frame Sync Mode (SHORT = "0")



Short Frame Sync Mode (SHORT = "1")

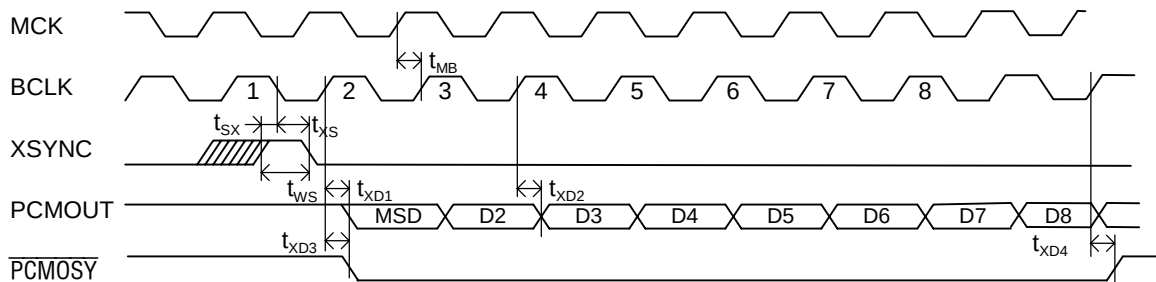
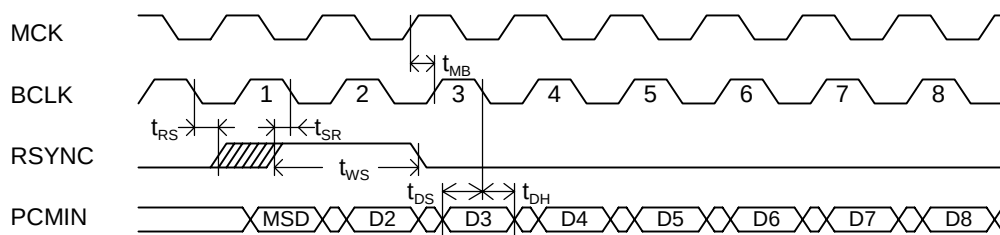


Figure 1 Transmit Side Timing Diagram

Long Frame Sync Mode (SHORT = "0")



Short Frame Sync Mode (SHORT = "1")

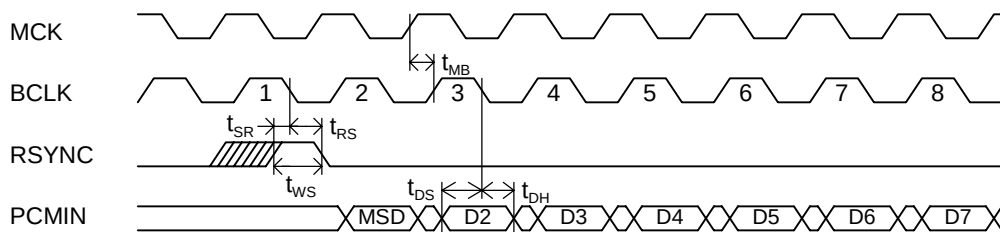
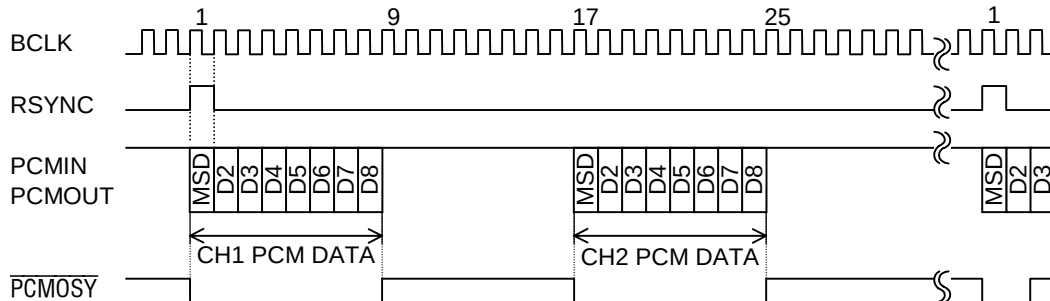
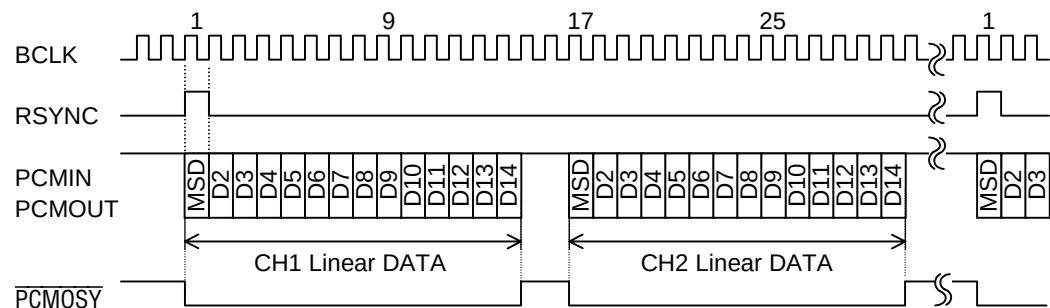
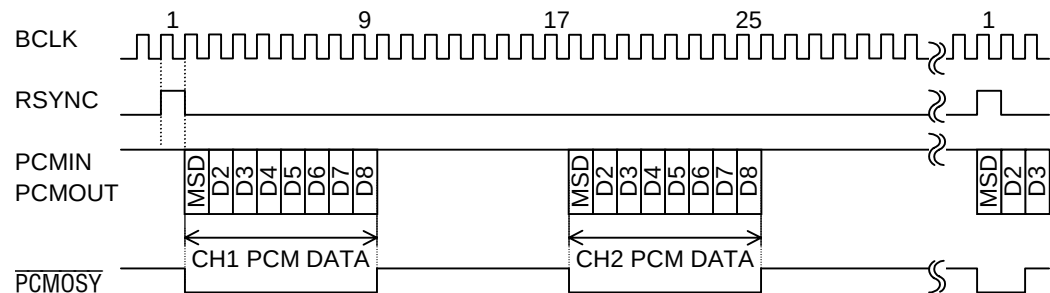
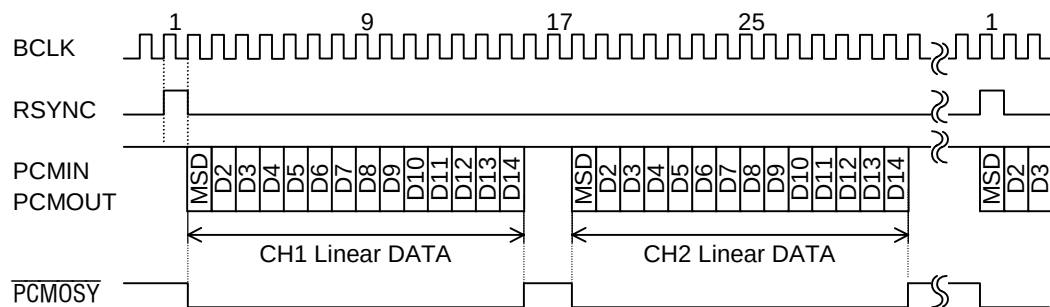


Figure 2 Receive Side Timing Diagram

PCM Mode (LIN = "0") & Long Frame Sync Mode (SHORT = "0")**Linear Mode (LIN = "1") & Long Frame Sync Mode (SHORT = "0")****PCM Mode (LIN = "0") & Short Frame Sync Mode (SHORT = "1")****Linear Mode (LIN = "1") & Short Frame Sync Mode (SHORT = "1")****Figure 3 PCM Interface Bit Configuration**

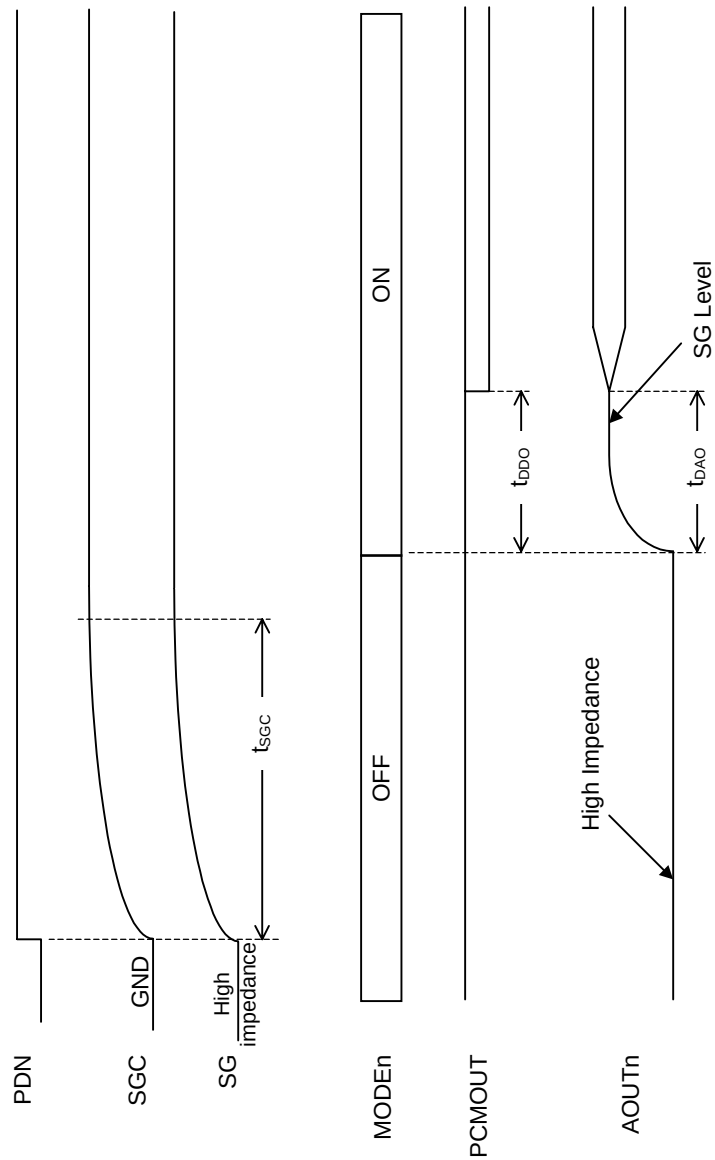


Figure 4 SGC, PCMOUT and AOUT Output Timing

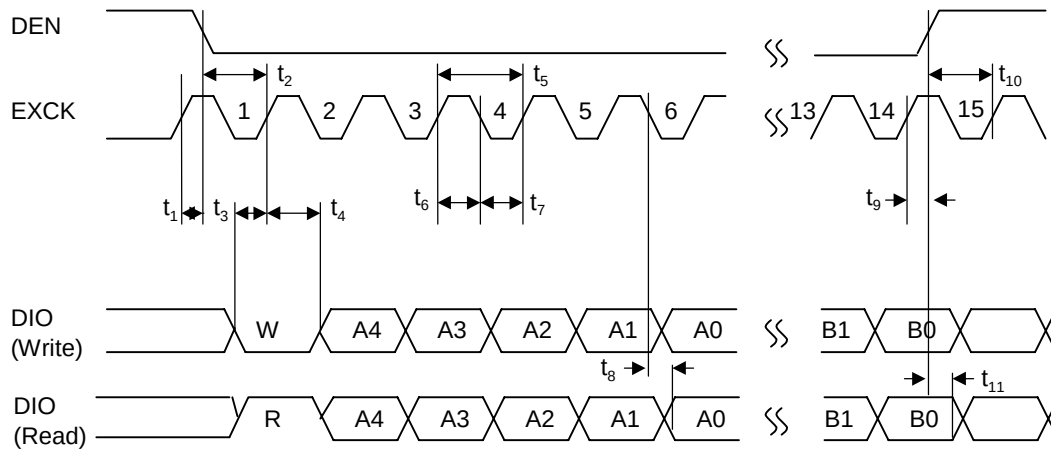


Figure 5 Serial Control Port Interface

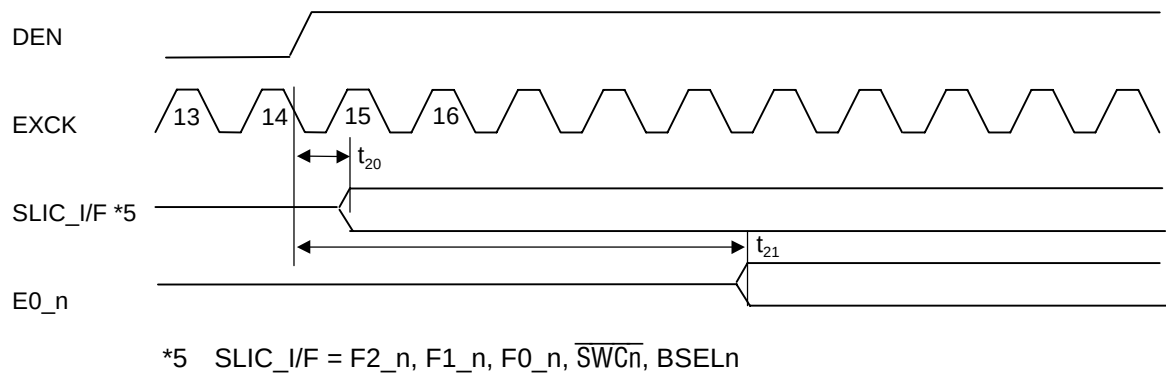


Figure 6 SLIC Interface Timing 1 (to SLIC)

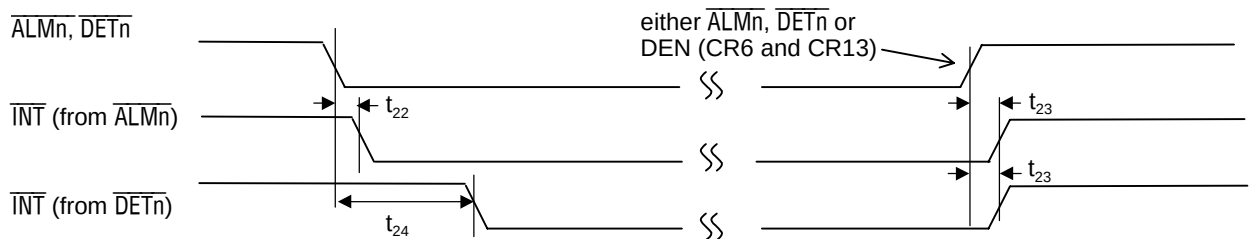


Figure 7 SLIC Interface Timing 2 (from SLIC)

* $\overline{INT}$ will be released either of the following case.

- (1) $\overline{ALMn}$ or $\overline{DETn}$ goes high. (PDN = 1), $\overline{ALMn}$ and $\overline{DETn}$ are all high. (PDN = 0)
- (2) Both SLIC 1 control (CR6) and SLIC 2 control (CR13) are read by MCU.

FUNCTIONAL DESCRIPTION

Pin Functional Description

AIN1N, AIN1P, AIN2N, AIN2P, GSX1, GSX2

AIN1N, AIN1P, AIN2N and AIN2P are the transmit analog inputs for Channels 1 and 2.

GSX1 and GSX2 are the transmit level adjustments for Channels 1 and 2.

AIN1N, AIN1P, AIN2N and AIN2P are inverting and non-inverting inputs for the op-amp; GSX1 and GSX2 are connected to the output of the op-amp and are used to adjust the level, as shown below.

When not using AIN1N, AIN1P, AIN2N and/or AIN2P, connect AIN1N to GSX1, AIN1P to SGC, AIN2N to GSX2, and AIN2P to SGC. During power down mode, the GSX1 and GSX2 outputs are at a high impedance.

In the case of the analog input 2.226 V_{pp} at GSX pin with digital output +3.17 dBm0 (μ-law).

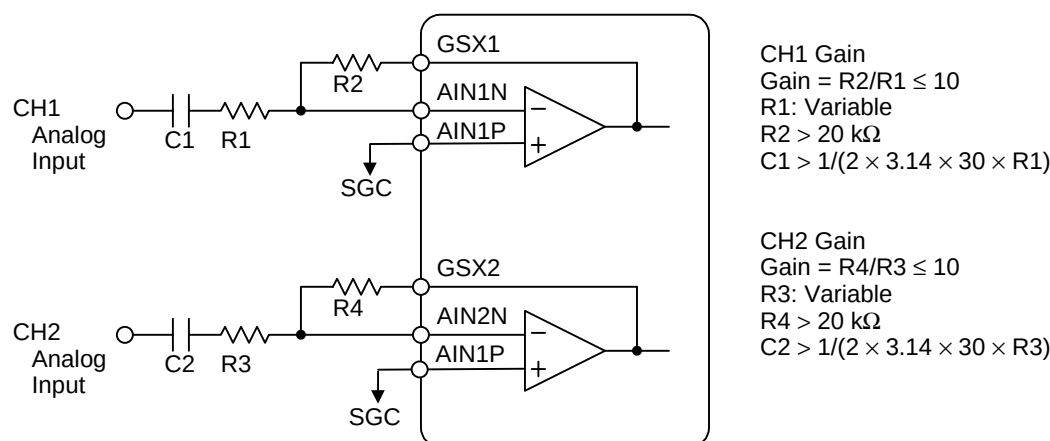


Figure 8 Example of Analog Input Setting Schematic

AOUT1P, AOUT1N, AOUT2P, AOUT2N

AOUT1P and AOUT1N are the receive analog output from Channel 1 and AOUT2P and AOUT2N are output from Channel 2.

When AOUT1 SEL (CR7-B7) is logic low ("0"), AOUT1P is a single-ended output from channel 1 and AOUT1N is at high impedance.

While AOUT2 SEL (CR14-B7) is logic low ("0"), AOUT2P is a single-ended output from channel 2. AOUT2N is at high impedance.

When AOUT1 SEL (CR7-B7) is logic high ("1"), AOUT1P and AOUT1N are differential output from channel 1. While AOUT2 SEL (CR14-B7) is logic high ("1"), AOUT2P and AOUT2N are differential output from channel 2.

The output signal from each pin has an amplitude of 3.4 V_{pp} above and below the signal ground voltage (SG).

When the digital signal of +3.17 dBm0 is input to PCMIN, it can drive a load of 20 kΩ or more.

During power saving or power down mode, these outputs are at a high impedance.

TOUT1, TOUT2

TOUT1 is the tone analog output from Channel 1 and TOUT2 is output from Channel 2.

The output signal has an amplitude of 2.5 V_{pp} above and below the signal ground voltage (SG).

During power saving or power down mode, these outputs are at a high impedance.

V_{DDA}, V_{DD}

Power supply for +5 V.

V_{DDA} is a power supply for an analog circuit of the system. V_{DD} is a power supply for a digital circuit of the system. V_{DDA} pin should be used a bypass capacitor of 0.1 μ F with excellent high frequency characteristics should be connected between V_{DDA} pin and AG pin.

V_{DDA} is separate from V_{DD} internally. The V_{DDA} pin must be connected to the V_{DD} pin on the printed circuit board.

AG, DG

AG is a ground for the analog signal circuits. DG is a ground for the digital signal circuits.

DG is separate from AG internally. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor. Connect a 0.1 μ F capacitor with excellent high frequency characteristics should be connected between the AG pin and the SGC pin. This pin is only for internal schematic.

During power down mode, this outputs is at the voltage level of AG with about 50 k Ω impedance.

SG

SG level output for external parts.

The output voltage from this pin is 2.4 V, as same as SGC pin. During power down mode, this output is at a high impedance.

MCK

Master clock input.

The frequency must be 2.048 or 4.096 MHz selected by MCK SEL (CR0-B5).

BCLK

Shift clock signal input for the PCMIN and PCMOUT signals.

The frequency, equal to the data rate, is 256 to 4096 kHz. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK). Please refer to Figure 1 about the phase difference of MCK and BCLK.

RSYNC

Receive synchronizing signal input.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK).

XSYNC

Transmit synchronizing signal input.

The PCM output signal from the PCMOUT pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal synchronizes all timing signals of all section. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK).

PCMIN

PCMIN is a data input pin.

The voice band signal is converted to an analog signal in synchronization with the RSYNC signal and BCLK. The analog signal of channel 1 is output from AOUT1 pin and the analog signal of channel 2 is output from AOUT2 pin.

When the Long Frame Sync Mode (SHORT = "0"), the start of the PCM data (Channel 1's MSD) is identified at the rising edge of RSYNC.

When the Short Frame Sync Mode (SHORT = "1"), the start of the PCM data (Channel 1's MSD) is identified at the falling edge of RSYNC.

PCMOUT

PCMOUT is a data output pin.

The output signal is output from Channel 1's MSD bit in a sequential order, synchronizing with the rising edge of the BCLK signal.

When the Long Frame Sync Mode (SHORT = "0"), the first bit of PCMOUT may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

When the Short Frame Sync Mode (SHORT = "1"), the first bit of PCMOUT may be output at the falling edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state during power down state.

A pull-up resistor must be connected to this pin because it is an open drain output.

PCMOSY

PCM Data Synchronizing Output for Time-Slot Assignment.

The output data PCMOUT is synchronized by this signal while in Time-Slot Assignment mode. The low level output of this signal indicates PCM data is available from the PCMOUT pin. This signal is used to control the TRI-STATE Enable of a backplane line-driver.

Table 1 The output cording format at the PCM Mode (LIN = "0")

INPUT/OUTPUT Level	PCMIN/PCMOUT															
	ALAW = "0" (μ-law)								ALAW = "1" (A-law)							
	MSD	D2	D3	D4	D5	D6	D7	D8	MSD	D2	D3	D4	D5	D6	D7	D8
+Full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
+0	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
−0	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
−Full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Table 2 The output cording format at the Linear Mode (LIN = "1")

INPUT/OUTPUT Level	PCMIN/PCMOUT													
	MSD	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
+Full scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1
+1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
−1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
−Full scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0

PDN

Power down control signal.

When PDN is at logic low ("0"), both Channel 1 and Channel 2 circuits are in the power down state. Also, all control registers except SLIC interface are in an initial state (logic "0" level). The SLIC interface registers are same state as before power down. While power down state, interrupt function (INT pin) is available from output of SLIC. During normal operation mode, set this pin to logic high ("1") level.

The power down mode is controlled by MODE1 (CR0-B1) and MODE0 (CR0-B0) Ored with the signal from the PDN pin. Power down function (PDN = "0") is valid even if MODE1 and/or MODE0 is logic high ("1") level.

RESET

Reset signal for control register.

When RESET is at logic low ("0"), all control registers are in an initial state (logic "0" level). During normal operation mode, set this pin to logic high ("1") level.

Table 3 Condition of PCMOUT by the Power Control at the PCM Mode (LIN = "0")

PDN	MODE1	MODE0	ALAW	CH2 PCM Data	CH1 PCM Data
0	0/1	0/1	0/1	High impedance *5	High impedance *5
1	0	0	0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
			1	1 1 0 1 0 1 0 1	1 1 0 1 0 1 0 1
1	0	1	0	1 1 1 1 1 1 1 1	Operate
			1	1 1 0 1 0 1 0 1	Operate
1	1	0	0	Operate	1 1 1 1 1 1 1 1
			1	Operate	1 1 0 1 0 1 0 1
1	1	1	0	Operate	Operate
			1	Operate	Operate

Table 4 Condition of PCMOUT by the Power Control at the Linear Mode (LIN = "1")

PDN	MODE1	MODE0	ALAW	CH2 Linear Data	CH1 Linear Data
0	0/1	0/1	0/1	High impedance *5	High impedance *5
1	0	0		ALL "0"	ALL "0"
1	0	1		ALL "0"	Operate
1	1	0		Operate	ALL "0"
1	1	1		Operate	Operate

Table 5 Condition of the Analog Output by the Power Control

PDN	MODE1	MODE0	GSX1	GSX2	AOUT1	AOUT2	SG	SGC	MCU Interface (CR6, CR13)	MCU Interface (ELSE)
0	0/1	0/1	High Impedance	High Impedance	High Impedance	High Impedance	High Impedance	*6	Operate	"0"
1	0	0	High Impedance	High Impedance	High Impedance	High Impedance	High Impedance	*6	Operate	Operate
1	0	1	Operate	High Impedance	Operate	High Impedance	Operate	Operate	Operate	Operate
1	1	0	High Impedance	Operate	High Impedance	Operate	Operate	Operate	Operate	Operate
1	1	1	Operate	Operate	Operate	Operate	Operate	Operate	Operate	Operate

*5 The data will be 'H' by external pull-up resistor.

*6 The voltage level of AG with about 50 kΩ

F2_n, F1_n, F0_n

Mode Control Output for SLIC1 and SLIC2 (Intersil HC5518x series)

These output signals are input of SLIC devices with the same pin names. Table 6 shows the operating modes of SLIC devices. It is possible to connect these pins to same pins on the SLIC directly. These pins are available while power down state (PDN = "0").

E0_n

Detector Output for SLIC1 and SLIC2 (Intersil HC5518x series)

These output signals indicate detector output select for SLIC devices. Refer to Table 6. Hold timer (20 μ s) operates automatically. It is possible to connect this pin to same pin on the SLIC directly. This pin is available while power down state (PDN = "0"). However hold timer is ignored in this state.

Table 6 SLIC Device Operating Modes

Operating Mode	F2	F1	F0	E0 = 1	E0 = 0	Description
Low Power Standby	0	0	0	SHD	GKD	Standby mode
Forward Active	0	0	1	SHD	GKD	Forward battery loop feed
Unbalanced Ringing	0	1	0	RTD	RTD	Unbalanced ringing mode
Reverse Active	0	1	1	SHD	GKD	Reverse battery loop feed
Ringing	1	0	0	RTD	RTD	Balanced ringing mode
Forward Loop Back	1	0	1	SHD	GKD	Test mode
Tip Open	1	1	0	SHD	GKD	For PBX type application
Power Denial	1	1	1	n/a	n/a	Device shutdown

SHD: Switch Hook Detection

RTD: Ring Trip Detection

GKD: Ground Key Detection

BSELn

Battery select output for SLIC1 and SLIC2 (Intersil HC5518x series)

These output signals control SLIC battery select function. A logic low ("0") selects the low battery on the SLIC device. A logic high ("1") selects the high battery on the SLIC device. It is possible to connect this pin to same pin on the SLIC directly. This pin is available while power down state (PDN = "0").

SWCn

Switch control output for SLIC1 and SLIC2 (Intersil HC5518x series)

These output signals control SLIC switch control. A logic low ("0") enables the switch and a logic high ("1") disables the switch. It is possible to connect this pin to same pin on the SLIC directly. This pin is available while power down state (PDN = "0").

DETn

Inputs from SLIC (Intersil HC5518x series) Switch Hook or Ring Trip Detector

These input signals indicate either a switch hook, ground key, or a ring trip output operation from the SLIC devices. Debounce timer for each channel can be selected by DETn TIM3 through DETn TIM0. It is possible to connect this pin to same pin on the SLIC directly. This pin is available while power down state (PDN = "0"). However debounce timer is ignored while this state.

ALMn

Inputs from SLIC (Intersil HC5518x series) thermal shutdown output

These input signals indicate SLIC die temperature has exceeded safe operating temperature and SLIC device has been powered down automatically. In the event the safe die temperature of SLIC is exceeded, the ALM input will go logic low ("0") and DET will go logic high ("1"). It is possible to connect this pin to same pin on the SLIC directly. This pin is available while power down state (PDN = "0").

INT

Interrupt output

This output signal indicates either the SLIC is under detector output condition or thermal shutdown alarm condition. When SLIC device detects either switch hook, ground key, or ring trip, or is under thermal shutdown alarm condition, the INT pin goes logic low ("0"). Interrupt function doesn't include debounced timer when PDN pin is logic low ("0").

INT will be released either of the following case. Refer to Figure 7.

- (1) ALMn or DETn goes high. (PDN=1), ALMn and DETn go high. (PDN = 0)
- (2) Both SLIC 1 control register (CR6) and SLIC 2 control register (CR13) are read by MCU.

DEN, EXCK, DIO

Serial control ports for MCU interface.

Reading and writing data is performed by an external MCU through these pins. Eight registers with eight bits are provided on the devices. DEN is the “Enable” control signal input. EXCK is the data shift clock input. DIO is the address and data input or output. Figure 9 shows the input or output timing diagram. For EXCK, please employ a continuous clock or a more than 15 shot of clock.

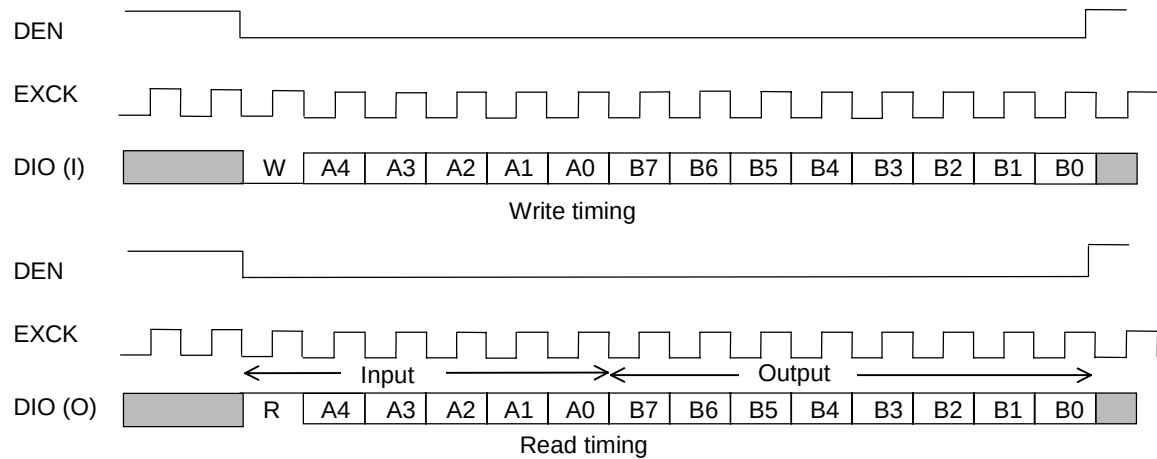


Figure 9 MCU Interface Timing Diagram

CIDATA1, CIDATA2

Input data for Caller ID generation.

CIDATA1 is data input for channel 1 and CIDATA2 is data input for channel 2.

While in a Caller ID tone generation mode (CID CH2 ON [CR1-B1] = “1” or CID CH1 ON [CR1-B0] = “1”), the input signal of CIDATA is modulated by CID_FMT (CR1-B2) based on either ITU-T V.23 or Bell 202 and output from AOUTn pin. Caller ID generation data is generated by CH1TG1 and CH2TG1 and it is possible to change the tone level by control register setting.

TEST

Input for internal test.

Keep logic low (“0”) level during normal operation.

Power-On Description

While power on status, the following chart will be recommended.

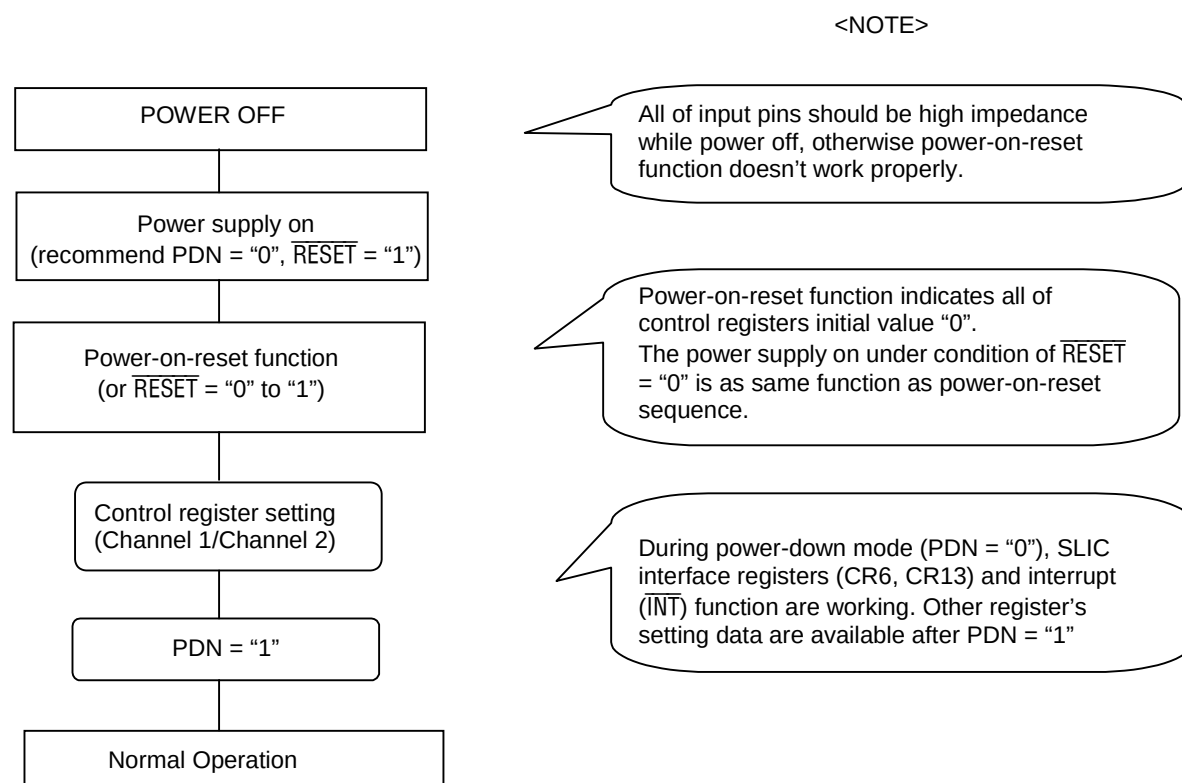


Figure 10 Power-ON Chart

Control Registers Functional Description

CR0 (Basic operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	Filter1 SEL	Filter2 SEL	MCK SEL	SHORT	LIN	ALAW	MODE1	MODE0

B7 (Filter1 SEL) ... Transmit and receive filter of CH1 select;

B6 (Filter2 SEL) ... Transmit and receive filter of CH2 select;

0/basd on ITU-T_G.714 filter, 1/high_modem performance bandwidth filter

B5 (MCK SEL) ... MCK frequency select; 0/2.048 MHz, 1/4.096 MHz

B4 (Short) ... Short frame synchronous interface select. Refer to Figure 3;

0/Long frame synchronous interface, 1/Short frame synchronous interface

B3 (LIN) ... PCM interface linear mode select;

0/PCM data, 1/14-bit linear (2's complement) data

B2 (ALAW) ... PCM companding law select; 0/ μ -law, 1/A-law

B1, B0 (MODE1, MODE0) ... Functional mode setting;

Power down mode (B1 = B0 = "0") indicates power down function except register reset.

Power down mode (B1 = B0 = "0") is valid even if PDN pin is "1" (power on) level.

Table 7 Mode Setting for CH1 and CH2

MODE1	MODE0	PDN	$\overline{\text{RESET}}$	Power of Channel		Register	
				CH2	CH1	CR6, CR13	else
—	—	0/1	0	OFF	OFF	"0"	"0"
—	—	0	1	OFF	OFF	Available	*7
0	0	1	1	OFF	OFF	Available	Available
0	1	1	1	OFF	ON	Available	Available
1	0	1	1	ON	OFF	Available	Available
1	1	1	1	ON	ON	Available	Available

*7 Only write and read sequence are available

CR1 (Tone generator ON and Caller ID tone control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	CH2TG ON	CH1TG ON				CID FMT	CID CH2 ON	CID CH1 ON

B7 (CH2TG ON) ... Tone generator on Channel 2 enable: 0/OFF, 1/ON

B6 (CH1TG ON) ... Tone generator on Channel 1 enable: 0/OFF, 1/ON

B5, B4, B3: not used.

B2 (CID FMT) ... Caller ID generator format select;
0/ITU-T V.23 format (1: 1300 Hz, 0: 2100 Hz),
1/Bell 202 format (1: 1200 Hz, 0: 2200 Hz)

B1 (CID CH2 ON) ... Caller ID generator for channel 2 ON; 0/OFF, 1/ON

B0 (CID CH1 ON) ... Caller ID generator for channel 1 ON; 0/OFF, 1/ON

CR2 (Pulse meter tone generator setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	PMG2 FRQ	PMG2 LV1	PMG2 LV0	PMG2 TOUT2	PMG1 FRQ	PMG1 LV1	PMG1 LV0	PMG1 TOUT1

B7 (PMG2 FRQ) ... Pulse meter tone 2 frequency select; 0/12 kHz, 1/16 kHz

B6, B5 (PMG2 LV1, PMG2 LV0) ... Pulse meter tone 2 level setting;
(B6, B5): (0,0) = OFF, (0, 1) = 0.5 Vpp, (1, 0) = 1.0 Vpp, (1, 1) = 1.5 Vpp

B4 (PMG2 TOUT2) ... Pulse meter tone 2 output pin select; 0/AOUT2 pin (Mix to voice signal), 1/TOUT2 pin

B3(PMG1 FRQ) ... Pulse meter tone 1 frequency select; 0/12 kHz, 1/16 kHz

B2, B1 (PMG1 LV1, PMG1 LV0) ... Pulse meter tone 1 level setting;
(B6, B5): (0, 0) = OFF, (0, 1) = 0.5 Vpp, (1, 0) = 1.0 Vpp, (1, 1) = 1.5 Vpp

B0 (PMG1 TOUT1) ... Pulse meter tone 1 output pin select; 0/AOUT1 pin (Mix to voice signal), 1/TOUT1 pin

*Prohibition: No rising while the tone falling (within 10 ms).

CR3 (Time slot assignment control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	TSAE	TSAC	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0

* CR3 is a write only register.

B7 (TSAE) ... Time slot assignment enable; 0/Time slot assignment OFF, 1/Time slot assignment ON
During OFF (TSAE = '0'), Channel 1 is assigned to Slot 0 and Channel 2 is assigned to Slot 2 as a default.

B6 (TSAC) ... Time slot assignment channel select; 0/Channel 1 data select, 1/channel 2 data select

B5 to B0 (TSA5 to TSA0) ... Time slot assignment position select. From 0 (000000) to 63 (111111) slot can be available.

In case of 14 bit linear mode, only even slot (0, 2, 4, ..., 62) can be available. In any mode, both transmit side and receive side are available on the same slot.

Example) CH1 = slot 0 (000000), CH2 = slot 3 (000011)

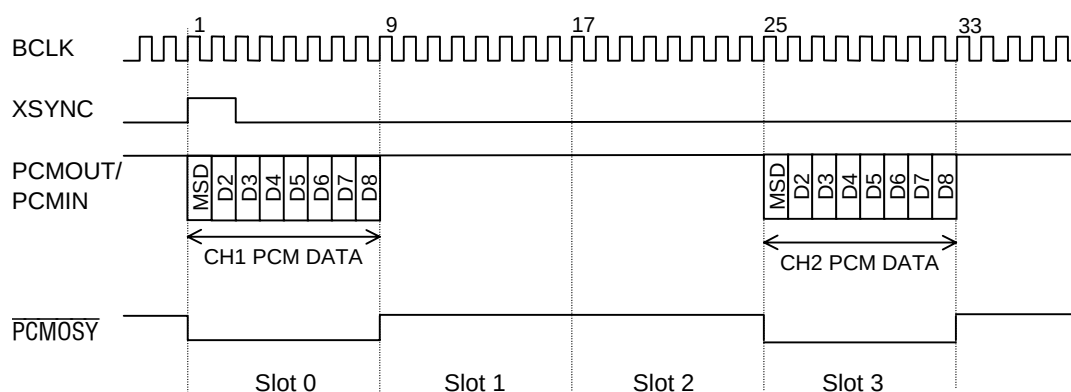


Figure 11 Example of Time Slot Assignment: CH1 = Slot 0, CH2 = Slot 3

CR4 (Debounced timer select)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DET2 TIM3	DET2 TIM2	DET2 TIM1	DET2 TIM0	DET1 TIM3	DET1 TIM2	DET1 TIM1	DET1 TIM0

B7, B6, B5, B4 (DET2 TIM3, TIM2, TIM1, TIM0): Debounce timer for CH2

... debounce timer from DET2 input to DET2 bit (CR13-B1) setting
Debounce timer is available while power on state (PDN = "1").

B3, B2, B1, B0 (DET1 TIM3, TIM2, TIM1, TIM0): Debounce timer for CH1

... debounce timer from DET1 input to DET1 bit (CR6-B1) setting
Debounce timer is available while power on state (PDN = "1").

The timer value is calculated by the equation of [Decimal (B7, B6, B5, B4) * 15] or [Decimal (B3, B2, B1, B0) * 15].

Refer to Table 8.

Table 8 Debounce Timer Setting

B7/B3	B6/B2	B5/B1	B4/B0	Timer (ms)
0	0	0	0	0
0	0	0	1	15
0	0	1	0	30
0	0	1	1	45
0	1	0	0	60
:	:	:	:	:
0	1	1	1	105
1	0	0	0	120
1	0	0	1	135
:	:	:	:	:
1	1	1	1	225

CR5 (CH1 transmit/receive level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	LV1R3	LV1R2	LV1R1	LV1R0	LV1X3	LV1X2	LV1X1	LV1X0

B7, B6, B5, B4 (LV1R3, LV1R2, LV1R1, LV1R0) ... Receive side level adjustment for CH1.
Refer to Table 9.

B3, B2, B1, B0 (LV1X3, LV1X2, LV1X1, LV1X0) ... Transmit side level adjustment for CH1.
Refer to Table 9.

Table 9 Receive and Transmit Level Adjustment

LV1R3/LV1X3	LV1R2/ LV1X2	LV1R1/LV1X1	LV1R0/LV1X0	Level (dBm0)
0	0	0	0	0.0
0	0	0	1	-1.0
0	0	1	0	-2.0
0	0	1	1	-3.0
0	1	0	0	-4.0
0	1	0	1	-5.0
0	1	1	0	-6.0
0	1	1	1	-7.0
1	0	0	0	-8.0
1	0	0	1	-9.0
1	0	1	0	-10.0
1	0	1	1	-11.0
1	1	0	0	-12.0
1	1	0	1	-13.0
1	1	1	0	-14.0
1	1	1	1	OFF

CR6 (SLIC 1 control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	F2_1	F1_1	F0_1	$\overline{\text{SWC1}}$	BSEL1	E0_1	$\overline{\text{DET1}}$	$\overline{\text{ALM1}}$

B7, B6, B5 (F2_1, F1_1, F0_1) ... Mode setting for SLIC1. Refer to table 6.

B4 (SWC1) ... Switch control for SLIC1; 0/switch enable, 1/switch disable

B3 (BSEL1) ... Battery select for SLIC1; 0/low battery, 1/high battery

B2 (E0_1) ... Detector output select for SLIC1. Refer to table 6.
Hold timer (20 μ s) always works from this bit to E0_1 output pin.

B1 (DET1) ... Detector output from SLIC1. Read only bit; 0/detect, 1/not detect
Debounce timer value is set by CR4.

B0 (ALM1) ... Thermal Shutdown Alarm from SLIC1. Read only bit; 0/detect, 1/not detect

CR7 (CH1 Tone generator 2 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	AOUT1 SEL	CH1TG 2 TX	CH1TG 2 TOUT1	CH1TG2 LV3	CH1TG2 LV2	CH1TG2 LV1	CH1TG2 LV0	CH1TG2 _8

CR8 (CH1 Tone generator 2 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	CH1TG2 _7	CH1TG2 _6	CH1TG2 _5	CH1TG2 _4	CH1TG2 _3	CH1TG2 _2	CH1TG2 _1	CH1TG2 _0

CR7-B7 (AOUT1 SEL) ... AOUT1P, AOUT1N output functionality select:
 0/AOUT1P: Single ended output, AOUT1N: at high impedance
 1/AOUT1P and AOUT1N are differential output

B6 (CH1TG1 TX) ... Tone generator in channel 1 transmission select;
 0/Receive side output, 1/Transmit side output

B5 (CH1TG1 TOUT1) ... Tone generator in channel 1 receive side output pin select;
 0/output from AOUT1 pin, 1/output from TOUT1 pin

B4, B3, B2, B1 (CH1TG2LV3, TG2LV2, TG2LV1, TG2LV0) ... Level of tone generator 2 in channel 1 setting.
 Refer to Table 10.

Table 10 Tone Generator 2 Level Adjustment

B4 TG2LV3	B3 TG2LV2	B2 TG2LV1	B1 TG2LV0	Level (dBm0)
0	0	0	0	OFF
0	0	0	1	-12.0
0	0	1	0	-11.0
0	0	1	1	-10.0
0	1	0	0	-9.0
0	1	0	1	-8.0
0	1	1	0	-7.0
0	1	1	1	-6.0
1	0	0	0	-5.0
1	0	0	1	-4.0
1	0	1	0	-3.0
1	0	1	1	-2.0
1	1	0	0	-1.0
1	1	0	1	0.0
1	1	1	0	+1.0
1	1	1	1	+2.0

CR7-B0, CR8-B7 to B0 (CH1TG2_8 to CH1TG2_0) ... Channel 1 TG2 frequency select. Refer to Table 11.

The tone generator 2 frequency can varied from 300 to 3400 Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)/10] to hex

Example) expected frequency = 1500 Hz

decimal of [expected frequency (Hz)/10] = 150d

hex of [150d] = 096h

setting data = (CR7-B0, CR8-B7,, CR8-B0) = (0, 1, 0, 0, 1, 0, 1, 1, 0)

Table 11 Tone Generator Frequency Setting

Frequency (Hz)	decimal	hex	CR7	CR8							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

* There is no guarantee that out of range setting frequency between 300 Hz and 3400 Hz.

CR9 (CH1 tone generator 1 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	CH1TG1 LV6	CH1TG1 LV5	CH1TG1 LV4	CH1TG1 LV3	CH1TG1 LV2	CH1TG1 LV1	CH1TG1 LV0	CH1TG1 _8

CR10 (CH1 tone generator 1 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	CH1TG1 _7	CH1TG1 _6	CH1TG1 _5	CH1TG1 _4	CH1TG1 _3	CH1TG1 _2	CH1TG1 _1	CH1TG1 _0

CR9-B7, B6, B5, B4, B3, B2, B1 (CH1TG1LV6, TG1LV5, TG1LV4, TG1LV3, TG1LV2, TG1LV1, TG1LV0)

... Level of tone generator 1 setting. Refer to Table 12.

The level is calculated by the following equation.

Level (dBm0) = decimal (B7, B6, B5, B4, B3, B2, B1) * 0.1 – 12.2

decimal (B7, B6, B5, B4, B3, B2, B1) = $B7 * 64 + B6 * 32 + B5 * 16 + B4 * 8 + B3 * 4 + B2 * 2 + B1$

Example) (B7, B6, B5, B4, B3, B2, B1) = (1, 0, 0, 0, 0, 0, 0)

decimal (B7, B6, B5, B4, B3, B2, B1) = 64

Level = $6.4 - 12.2 = -5.8$ [dBm0]

Table 12 Tone Generator 1 Level Adjustment

B7 TG1LV6	B6 TG1LV5	B5 TG1LV4	B4 TG1LV3	B3 TG1LV2	B2 TG1LV1	B1 TG1LV0	Level (dBm0)
0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	-12.1
0	0	0	0	0	1	0	-12.0
0	0	0	0	0	1	1	-11.9
0	0	0	0	1	0	0	-11.8
:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	-5.9
1	0	0	0	0	0	0	-5.8
1	0	0	0	0	0	1	-5.7
:	:	:	:	:	:	:	:
1	1	1	1	0	1	0	0.0
1	1	1	1	0	1	1	0.1
1	1	1	1	1	0	0	0.2
1	1	1	1	1	0	1	0.3
1	1	1	1	1	1	0	0.4
1	1	1	1	1	1	1	0.5 (= 1.25 V _{op})

CR9-B0, CR10-B7 to B0 (CH1TG1_8 to CH1TG1_0) ... TG1 in channel 1 frequency select.

When CH1RING is logic low ("0"), all of these bits are valid. Refer to Table 13.

The tone generator 1 frequency can varied from 300 to 3400 Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)/10] to hex

Example) expected frequency = 1500 Hz

decimal of [expected frequency (Hz)/10] = 150d

hex of [150d] = 096h

setting data = (CR9-B0, CR10-B7, ..., CR10-B0) = (0, 1, 0, 0, 1, 0, 1, 0, 1, 1, 0)

Table 13 Tone Generator Frequency Setting (CH1RING = "0")

Frequency (Hz)	decimal	hex	CR9	CR10							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

* There is no guarantee that out of range setting frequency between 300 Hz and 3400 Hz.

When CH1RING is logic high (“1”), CR10-B5 to B0 decide frequency for ringing.

Refer to Table 14.

The tone generator 1 frequency can varied from 15 to 50 Hz per 1Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)] to hex

Example) expected frequency = 20 Hz

decimal of [expected frequency (Hz)] = 20d

hex of [20d] = 014h

setting data = (CR10-B5B4, B3, B2, B1, B0) = (0, 1, 0, 1, 0, 0)

Table 14 Tone Generator Frequency Setting (CH1RING = “1”)

Frequency (Hz)	decimal	hex	CR9	CR10							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
15	15	0Fh	—	—	—	0	0	1	1	1	1
16	16	10h	—	—	—	0	1	0	0	0	0
17	17	11h	—	—	—	0	1	0	0	0	1
18	18	12h	—	—	—	0	1	0	0	1	0
19	19	13h	—	—	—	0	1	0	0	1	1
20	20	14h	—	—	—	0	1	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
48	48	30h	—	—	—	1	1	0	0	0	0
49	49	31h	—	—	—	1	1	0	0	0	1
50	50	32h	—	—	—	1	1	0	0	1	0

* There is no guarantee that out of range setting frequency between 15 Hz and 50 Hz.

CR11 (Ringing_ON and Trapezoid crest factors control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	CH2 RING	CH2TG1 TRP2	CH2TG1 TRP1	CH2TG1 TRP0	CH1 RING	CH1TG1 TRP2	CH1TG1 TRP1	CH1TG1 TRP0

B7 (CH2 RING) ... Channel 2 Ringing tone function select
 0/CH2TG1 works as a normal tone generator
 1/CH2TG1 works as a ringing tone generator
 The frequency and level of CH2TG1 are set by Channel 2 TG1 setting register.

B6, B5, B4 (CH2TG1 TRP2, TG1 TRP1, TG1 TRP0) ... Trapezoid crest factors select; Refer to Table 15.
 These bits are valid while ringing mode. CH2RING = '1'

B3 (CH1 RING) ... Channel 1 Ringing tone function select
 0/CH1TG1 works as a normal tone generator
 1/CH1TG1 works as a ringing tone generator
 The frequency and level of CH1TG1 are set by Channel 1 TG1 setting register.

B2, B1, B0 (CH1TG1 TRP2, TG1 TRP1, TG1 TRP0) ... Trapezoid crest factors select; Refer to Table 15.
 These bits are valid while ringing mode. CH1RING = '1'

Table 15 Crest Factor Setting

B6/B2 TG1 TRP2	B5/B1 TG1 TRP1	B4/B0 TG1 TRP0	Crest Factor
0	0	0	OFF
0	0	1	1.225
0	1	0	1.250
0	1	1	1.275
1	0	0	1.300
1	0	1	1.325
1	1	0	1.350
1	1	1	1.375

CR12 (CH2 transmit/receive level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	LV2R3	LV2R2	LV2R1	LV2R0	LV2X3	LV2X2	LV2X1	LV2X0

B7, B6, B5, B4 (LV2R3, LV2R2, LV2R1, LV2R0) ... Receive side level adjustment for CH2. Refer to Table 16.

B3, B2, B1, B0 (LV2X3, LV2X2, LV2X1, LV2X0) ... Transmit side level adjustment for CH2. Refer to Table 16.

Table 16 Receive and Transmit Level Adjustment

LV2R3/ LV2X3	LV2R2/ LV2X2	LV2R1/ LV2X1	LV2R0/ LV2X0	Level (dBm0)
0	0	0	0	0.0
0	0	0	1	-1.0
0	0	1	0	-2.0
0	0	1	1	-3.0
0	1	0	0	-4.0
0	1	0	1	-5.0
0	1	1	0	-6.0
0	1	1	1	-7.0
1	0	0	0	-8.0
1	0	0	1	-9.0
1	0	1	0	-10.0
1	0	1	1	-11.0
1	1	0	0	-12.0
1	1	0	1	-13.0
1	1	1	0	-14.0
1	1	1	1	OFF

CR13 (SLIC 2 control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	F2_2	F1_2	F0_2	SWC2	BSEL2	E0_2	DET2	ALM2

B7, B6, B5 (F2_2, F1_2, F0_2) ... Mode setting for SLIC2. Refer to table 6.

B4 (SWC2) ... Switch control for SLIC2; 0/switch enable, 1/switch disable

B3 (BSEL2) ... Battery select for SLIC2; 0/low battery, 1/high battery

B2 (E0_2) ... Detector output select for SLIC2. Refer to table 6.
Hold timer (20 μ s) always works from this bit to E0_1 output pin.

B1 (DET2) ... Detector output from SLIC2. Read only bit; 0/detect, 1/not detect
Debounce timer value is set by CR4.

B0 (ALM2) ... Thermal Shutdown Alarm from SLIC2. Read only bit; 0/detect, 1/not detect

CR14 (CH2 tone generator 2 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	AOUT2 SEL	CH2TG2 TX	CH2TG2 TOUT2	CH2TG2 LV3	CH2TG2 LV2	CH2TG2 LV1	CH2TG2 LV0	CH2TG2 _8

CR15 (CH2 tone generator 2 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	CH2TG2 _7	CH2TG2 _6	CH2TG2 _5	CH2TG2 _4	CH2TG2 _3	CH2TG2 _2	CH2TG2 _1	CH2TG2 _0

CR14-B7 (AOUT2 SEL) ... AOUT2P, AOUT2N output functionality select:
 0/AOUT2P: Single ended output, AOUT2N: at high impedance
 1/AOUT2P and AOUT2N are differential output

B6 (CH2TG TX) ... Tone generator on channel 2 transmission select;
 0/Receive side output, 1/Transmit side output

B5 (CH2TG TOUT2) ... Tone generator on channel 2 receive side output pin select;
 0/output from AOUT2 pin, 1/output from TOUT2 pin

B4, B3, B2, B1 (CH2TG2LV3, TG2LV2, TG2LV1, TG2LV0) ... Level of tone generator 2 in channel 2 setting.
 Refer to Table 17.

Table 17 Tone Generator 2 Level Adjustment

B4 TG2LV3	B3 TG2LV2	B2 TG2LV1	B1 TG2LV0	Level (dBm0)
0	0	0	0	OFF
0	0	0	1	-12.0
0	0	1	0	-11.0
0	0	1	1	-10.0
0	1	0	0	-9.0
0	1	0	1	-8.0
0	1	1	0	-7.0
0	1	1	1	-6.0
1	0	0	0	-5.0
1	0	0	1	-4.0
1	0	1	0	-3.0
1	0	1	1	-2.0
1	1	0	0	-1.0
1	1	0	1	0.0
1	1	1	0	+1.0
1	1	1	1	+2.0

CR14-B0, CR15-B7 to B0 (CH2TG2_8 to CH2TG2_0) ... TG2 in channel 2 frequency select. Refer to Table 18.

The tone generator 2 frequency can varied from 300 Hz to 3400 Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)/10] to hex

Example) expected frequency = 1500 Hz

decimal of [expected frequency (Hz)/10] = 150d

hex of [150d] = 096h

setting data = (CR14-B0, CR15-B7,, CR15-B0) = (0, 1, 0, 0, 1, 0, 1, 1, 0)

Table 18 Tone Generator Frequency Setting

Frequency (Hz)	decimal	hex	CR14	CR15							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

* There is no guarantee that out of range setting frequency between 300 Hz and 3400 Hz.

CR16 (CH2 tone generator 1 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	CH2TG1 LV6	CH2TG1 LV5	CH2TG1 LV4	CH2TG1 LV3	CH2TG1 LV2	CH2TG1 LV1	CH2TG1 LV0	CH2TG1 _8

CR17 (CH2 tone generator 1 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	CH2TG1 _7	CH2TG1 _6	CH2TG1 _5	CH2TG1 _4	CH2TG1 _3	CH2TG1 _2	CH2TG1 _1	CH2TG1 _0

CR16-B7, B6, B5, B4, B3, B2, B1(CH2TG1LV6, TG1LV5, TG1LV4, TG1LV3, TG1LV2, TG1LV1, TG1LV0)

... Level of tone generator 1 setting. Refer to Table 19.

The level is calculated by the following equation.

Level (dBm0) = decimal (B7, B6, B5, B4, B3, B2, B1) * 0.1 – 12.2

decimal (B7, B6, B5, B4, B3, B2, B1) = B7 * 64 + B6 * 32 + B5 * 16 + B4 * 8 + B3 * 4 + B2 * 2 + B1

Example) (B7, B6, B5, B4, B3, B2, B1) = (1, 0, 0, 0, 0, 0, 0)

decimal (B7, B6, B5, B4, B3, B2, B1) = 64

Level = 6.4 – 12.2 = –5.8 [dBm0]

Table 19 Tone Generator 1 Level Adjustment

B7 TG1LV6	B6 TG1LV5	B5 TG1LV4	B4 TG1LV3	B3 TG1LV2	B2 TG1LV1	B1 TG1LV0	Level (dBm0)
0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	–12.1
0	0	0	0	0	1	0	–12.0
0	0	0	0	0	1	1	–11.9
0	0	0	0	1	0	0	–11.8
:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	–5.9
1	0	0	0	0	0	0	–5.8
1	0	0	0	0	0	1	–5.7
:	:	:	:	:	:	:	:
1	1	1	1	0	1	0	0.0
1	1	1	1	0	1	1	0.1
1	1	1	1	1	0	0	0.2
1	1	1	1	1	0	1	0.3
1	1	1	1	1	1	0	0.4
1	1	1	1	1	1	1	0.5 (= 1.25 V0p)

CR16-B0, CR17-B7 to B0 (CH2TG1_8 to CH2TG1_0) ... TG1 in channel 2 frequency select.

When CH2RING is logic low ("0"), all of these bits are valid. Refer to Table 20.

The tone generator 1 frequency can varied from 300 to 3400 Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)/10] to hex

Example) expected frequency = 1500 Hz

decimal of [expected frequency (Hz)/10] = 150d

hex of [150d] = 096h

setting data = (CR16-B0, CR17-B7,, CR17-B0) = (0, 1, 0, 0, 1, 0, 1, 1, 0)

Table 20 Tone Generator Frequency Setting (CH2RING = "0")

Frequency (Hz)	decimal	hex	CR16	CR17							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

* There is no guarantee that out of range setting frequency between 300 Hz and 3400 Hz.

When CH2RING is logic high (“1”), CR17-B5 to B0 decide frequency for ringing.

Refer to Table 21.

The tone generator 1 frequency can varied from 15 to 50 Hz per 1 Hz.

The frequency is decoded using the following equation;

Setting data (hex) = convert from decimal of [expected frequency (Hz)] to hex

Example) expected frequency = 20 Hz

decimal of [expected frequency (Hz)] = 20d

hex of [20d] = 014h

setting data = (CR17-B5B4, B3, B2, B1, B0) = (0, 1, 0, 1, 0, 0)

Table 21 Tone Generator Frequency Setting (CH2RING = “1”)

Frequency (Hz)	decimal	hex	CR16	CR17							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
15	15	0Fh	—	—	—	0	0	1	1	1	1
16	16	10h	—	—	—	0	1	0	0	0	0
17	17	11h	—	—	—	0	1	0	0	0	1
18	18	12h	—	—	—	0	1	0	0	1	0
19	19	13h	—	—	—	0	1	0	0	1	1
20	20	14h	—	—	—	0	1	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
48	48	30h	—	—	—	1	1	0	0	0	0
49	49	31h	—	—	—	1	1	0	0	0	1
50	50	32h	—	—	—	1	1	0	0	1	0

* There is no guarantee that out of range setting frequency between 15 Hz and 50 Hz.

CR18 (Test control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	CH2 LOOP1	CH2 LOOP0	CH1 LOOP1	CH1 LOOP0	TEST3	TEST2	TEST1	TEST0

B7, B6 (CH2 LOOP1, CH2 LOOP0) ... Loop-back test for channel 2 select;

(B7, B6): (0, 0 or 1) = loop-back OFF

(1, 0) = Digital loop back test for CH2. PCMOUT signal connects to PCMIN node.

(1, 1) = Analog loop back test for CH2. AOUT2 signal connects to GSX2 node.

* Loop-back test is available only under condition of both XSYNC and RSYNC are the same signal.

B5, B4 (CH1 LOOP1, CH1 LOOP0) ... Loop-back test for channel 1 select;

(B5, B4): (0, 0 or 1) = loop-back OFF

(1, 0) = Digital loop back test for CH1. PCMOUT signal connects to PCMIN node.

(1, 1) = Analog loop back test for CH1. AOUT1 signal connects to GSX1 node.

* Loop-back test is available only under condition of both XSYNC and RSYNC are the same signal.

B3 to B0 (TEST3 to TEST0) ... Internal test select; When writing data, write "0".

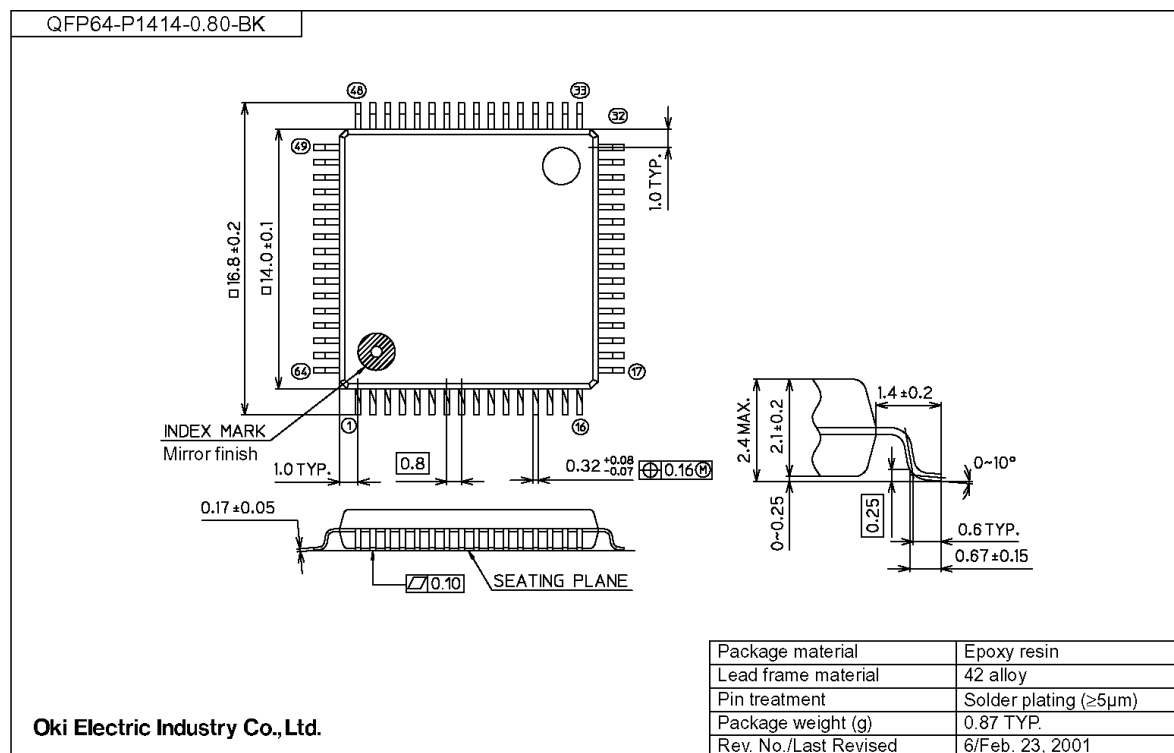
CR19 (Test control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR19	TEST11	TEST10	TEST9	TEST8	TEST7	TEST6	TEST5	TEST4

B7 to B0 (TEST11 to TEST4) ... Internal test select; When writing data, write "0".

PACKAGE DIMENSIONS

(Unit: mm)

**Notes for Mounting the Surface Mount Type Package**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters outside the specified maximum ratings or operation outside the specified operating range.

Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges, including but not limited to operating voltage, power dissipation, and operating temperature.

The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property or death or injury to humans. Such applications include, but are not limited to: traffic control, automotive, safety, aerospace, nuclear power control, and medical, including life support and maintenance.

Certain parts in this document may need governmental approval before they can be exported to certain countries. The purchaser assumes the responsibility of determining the legality of export of these parts and will take appropriate and necessary steps, at their own expense, for export to another country.

Copyright 2001 Oki Semiconductor

Oki Semiconductor reserves the right to make changes in specifications at anytime and without notice. This information furnished by Oki Semiconductor in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Oki Semiconductor for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Oki.



Oki REGIONAL SALES OFFICES

Silicon Solutions

Northwest Area

785 N. Mary Avenue
Sunnyvale, CA 94085
Tel: 408/720-8940
Fax: 408/720-8965

North Central Area

300 Park Blvd., Suite 365
Itasca, IL 60143
Tel: 630/250-1313
Fax: 630/250-1414

Northeast Area

138 River Road
Shattuck Office Center
Andover, MA 01810
Tel: 978/688-8687
Fax: 978/688-8896

Southwest Area

2171 Campus Drive, Suite 320
Irvine, CA 92612
Tel: 949/752-1843
Fax: 949/752-2423

Southeast Area

1590 Adamson Parkway, Suite 220
Morrow, GA 30260
Tel: 770/960-9660
Fax: 770/960-9682

South Central Area

Park Creek II
2007 N. Collins Blvd., Suite 305
Richardson, TX 75080
Tel: 972/238-5450
Fax: 972/238-0268

Oki Web Site:

<http://www.okisemi.com>

Oki Stock No: 320288-001

Oki Semiconductor

Corporate Headquarters

785 N. Mary Avenue
Sunnyvale, CA 94085-2909
Tel: 408/720-1900
Fax: 408/720-1918