User's Manual

飞凌嵌入式 FORLINX EMBEDDED

FETMX6UL-C2

OKMX6UL-C2

ARM Cortex-A7

Embedded Development Platform

Hardware Manual

Forlinx Embedded Technology Co. Ltd. www.forlinx.net

1

Address: 2699 Xiangyang North Avenue, Baoding, Hebei, China. TEL:0312-3102663 FAX:0312-3112651

Product Features

1. NXP i.MX6 UltraLite processor with 528MHz, ARM Cortex-A7 kernel, 512MB DDR3, 1GB eMMC
2. Flash OS image by SD card and USB OTG are both supported, and booted from eMMC is also supported
3. Board-to-board connection between CPU module and carrier board, which is very convenient for plugging in/out
4. Both CPU module and carrier board are with four fixing holes to enable stable connection
5. With on-board dual CAN port, WIFI&BT module, ESAM and dual fast Ethernet

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Attentions



MUST READ BEFORE WORKING WITH i.MX6UL

Product Operation Environment:

Power Supply: DC 5V
Working Temperature: 0 - 85℃
Humility: 10–95%（Non-condensing）

- Hot-plug of CPU module and peripheral modules is strictly prohibited.
- Please follow all the warnings and instructions marked on the product.
- Please keep the product dry. Once splashed or immersed by any liquid, cut off the power and dry it out immediately.
- Please store and operate the product in ventilating conditions to avoid damages brought by over high temperature.
- Please do not use or store the product in dusty or untidy conditions.
- Please do not use or store the product in alternate cold and hot conditions to avoid condensing which will damage components.
- Please do not treat the product rudely. Any falling-off, knocking and violate shaking may cause destruction to circuit and components.
- Please do not clean the product with organic solvents or corrodible liquids.
- Please do not dismantle or repair the product by yourself. Contact us when the product malfunctions.
- Please do not modify the product by yourself or use fittings unauthorized by us. Otherwise, the damage caused by that will be on your part and not included in guarantee terms.

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Any questions please feel free to contact Forlinx Technical Service Department..

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Updating Record

Date	Manual Version	CPU Module Version	Base Board Version	Updated
Oct.12, 2016	V1.0	V1.1	20160930	First draft

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Technical Support and Innovation

1. Technical Support

1.1 information about our company's software and hardware
1.2 problems related to our software and hardware manual
1.3 after-sale technical support for OEM and ODM
1.4 requirement of source code and other info which is lost or updated
1.5 failure diagnose and other after-sale service

2. Range of Technical Discussion (non-compulsory)

2.1 modification and comprehension of source code
2.2 how to implant OS
2.3 software and hardware problems occured in self-modifying and programming

3. Accesses to Technical Support

3.1 Tel (non-instant messenger): 0312-3119192
3.2 Email address (non-instant messenger) :
3.2.1. About Linux: linux@forlinx.com
3.2.2. About WinCE: wince@forlinx.com
3.2.3. About Android: android@forlinx.com
3.3 Forum (non-instant): http://bbs.witech.com.cn

4. Timetable for Technical Support

9:00am to 11:30am, 13:30pm to 17:00pm, Monday to Friday

Support will not be available on public holidays. Please send your questions to the email addresses above or Column Technical Support in forum. We'll reply as soon as we are back.

5. Access to Materials

Log in "bbs.witech.com.cn". Click "*materials for development board*" and download what you need.

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Contents

Product Features..... 2
Attentions..... 3
Chapter 1 Overview of Freescale iMX6Ultra Lite..... 9
Chapter 2 i.MX6UL CPU Module Introduction..... 12
2.1 CPU Module Overview..... 12
2.2 CPU Module Features..... 14
2.3 Power Supply Mode..... 14
2.4 Working Environment..... 14
2.5 CPU Module Interface..... 14
2.6 CPU Module Pin Definition..... 15
Chapter 3 i.MX6UL Development Platform Overview..... 22
3.1 Overview of single board computer i.MX6UL..... 22
3.2 Base board resource:..... 23
3.3 i.MX6UL Base Board Introduction..... 24
3.3.1 Base Board Power..... 24
3.3.2 Reset Key..... 24
3.3.3 Boot Configuration..... 24
3.3.4 Debug Port..... 25
3.3.5 SD Card Slot..... 26
3.3.6 RTC..... 26
3.3.7 LED..... 27
3.3.8 Fast Ethernet..... 27
3.3.9 USB Host..... 27
3.3.10 USB OTG..... 28
3.3.11 LCD..... 28
Appendix 1 Hardware Design Guideline..... 29
Appendix 2 Board-to-board connector dimension..... 31

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Chapter 1 Overview of Freescale iMX6Ultra Lite

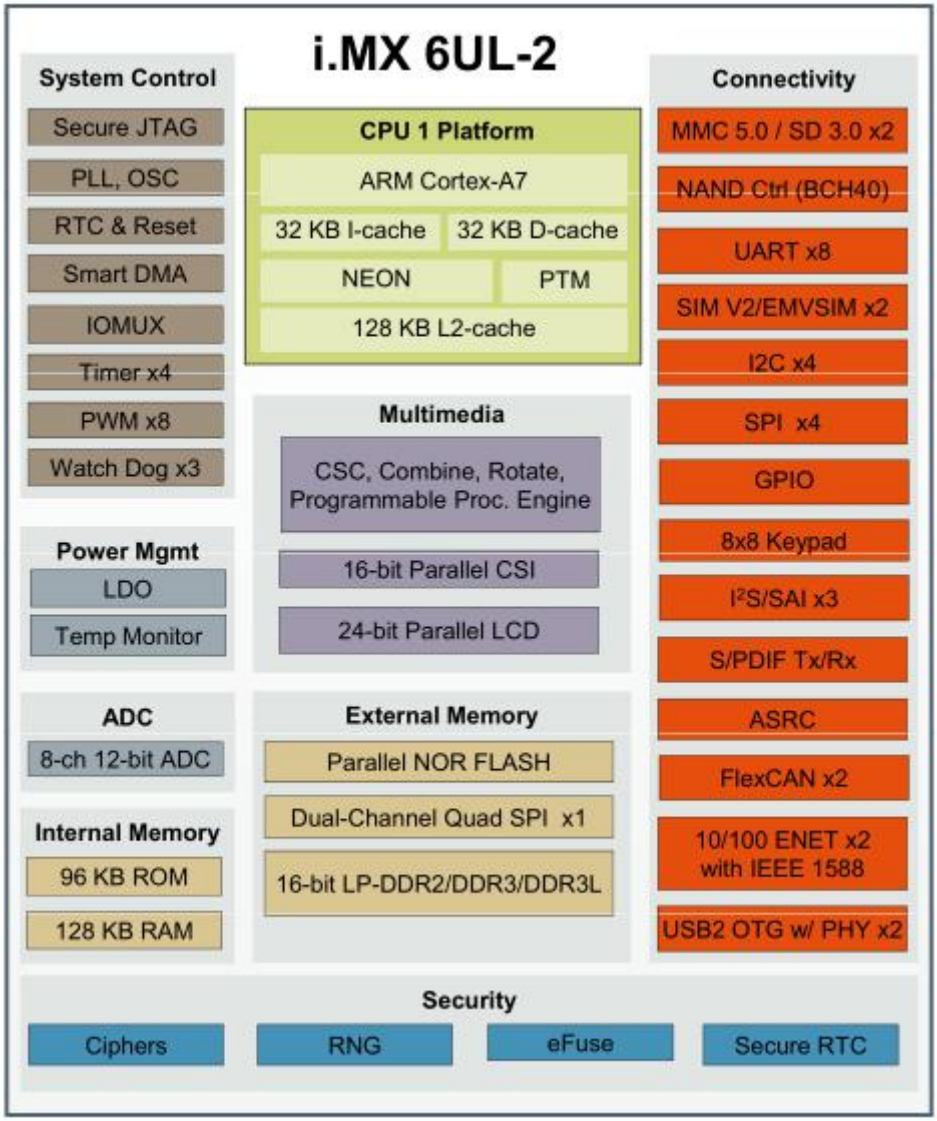
Expanding the i.MX 6 series, the i.MX 6UltraLite is a high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM® Cortex®-A7 core, which operates at speeds up to 528 MHz. The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Each processor in this family provides various memory interfaces, including 16-bit LPDDR2, DDR3, DDR3L, raw and managed NAND flash, NOR flash, eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth™, GPS, displays and camera sensors.

Freescale i.MX6UltraLite

Target Applications

- Automotive telematics
- IoT Gateway
- HMI
- Home energy management systems
- Smart energy concentrators
- Intelligent industrial control systems
- Electronics POS device
- Printer and 2D scanner
- Smart appliances
- Financial payment systems

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i.MX 6ULTRALITE DEVICE OPTIONS

- Red indicates change from column to the left

Feature	MCIMX6G0	MCIMX6G1	MCIMX6G2	MCIMX6G3
Speed	528 MHz	528 MHz	528 MHz	528 MHz
Cache	32 KB-I, 32KB-D	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2	32 KB-I, 32KB-D 128 KB L2
OCRAM	128 KB	128 KB	128 KB	128 KB
DRAM	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L	16-bit LP-DDR2, DDR3/DDR3L
eFuse for Customer	512-bit	1024-bit	1536-bit	2048-bit
NAND (BCH40)	Yes	Yes	Yes	Yes
Parallel NOR/EBI	Yes	Yes	Yes	Yes
Ethernet	10/100 MB x 1	10/100 MB x 1	10/100 MB x 2	10/100 MB x 2
USB with PHY	OTG, HS/FS x 1	OTG, HS/FS x 2	OTG, HS/FS x 2	OTG, HS/FS x 2
CAN	0	1	2	2
Security	Basic	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES with DPA/TDES/SHA/RSA), Secure Boot, Tamper Monitor, PCI4.0 pre-certification, OTF DRAM Encryption
Graphic	None	None	PxP	PxP
CSI	None	None	24-bit Parallel CSI	24-bit Parallel CSI
LCD	None	None	24-bit Parallel LCD	24-bit Parallel LCD
Quad SPI	1	1	1	1
SDIO	2	2	2	2
UART	4	8	8	8
I²C	2	4	4	4
SPI	2	4	4	4
I²S/SAI	1	3	3	3
S/PDIF	1	1	1	1
Timer/PWM	Timer x2, PWM x4	Timer x4, PWM x8	Timer x4, PWM x8	Timer x4, PWM x8
12-bit ADC	1x8ch	1x8ch	2x8ch	2x8ch

The one for Forlinx single board computer OKMX6UL-I and CPU module FETMX6UL-I is MCIMX6G2.

The i.MX 6UltraLite applications processor includes an integrated power management module that reduces the complexity of external power supply and simplifies power sequencing. Each processor in this family provides various memory interfaces, including 16-bit LPDDR2, DDR3, DDR3L, raw and managed NAND flash, NOR flash, eMMC, Quad SPI and a wide range of other interfaces for connecting peripherals such as WLAN, Bluetooth®, GPS, displays and camera sensors. The i.MX 6UltraLite is supported by discrete component power circuitry.

To view more details, please visit Freescale official website

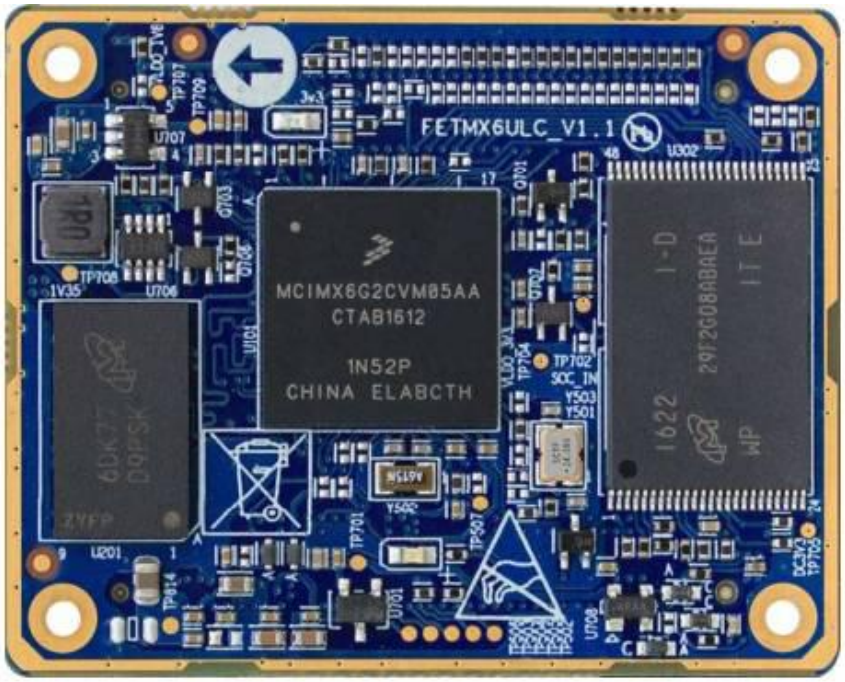
http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors/i.mx6qp/i.mx-6ultralite-processor-low-power-secure-arm-cortex-a7-core:i.MX6UL?uc=true&lang_cd=en

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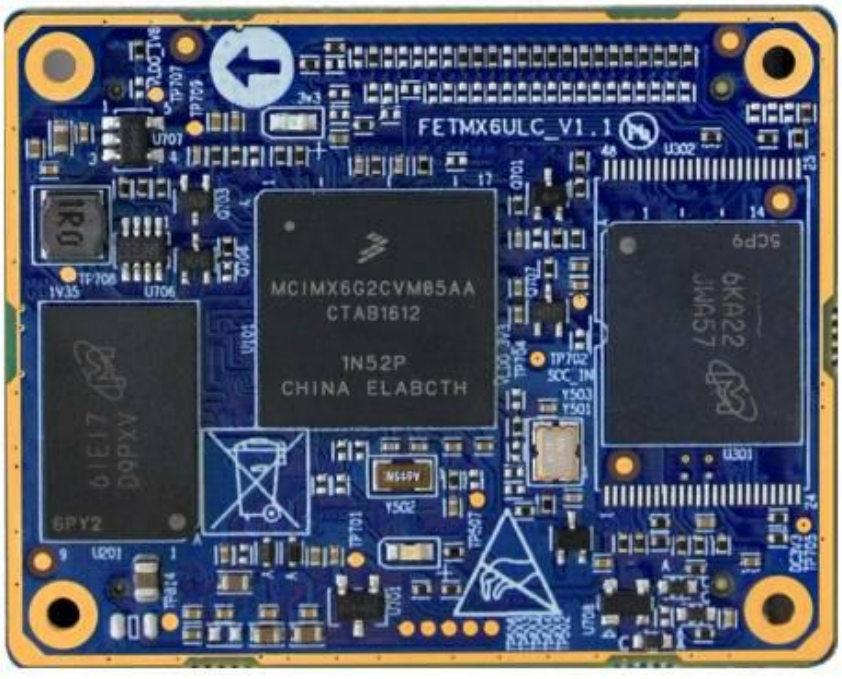
Chapter 2 i.MX6UL CPU Module Introduction

2.1 CPU Module Overview

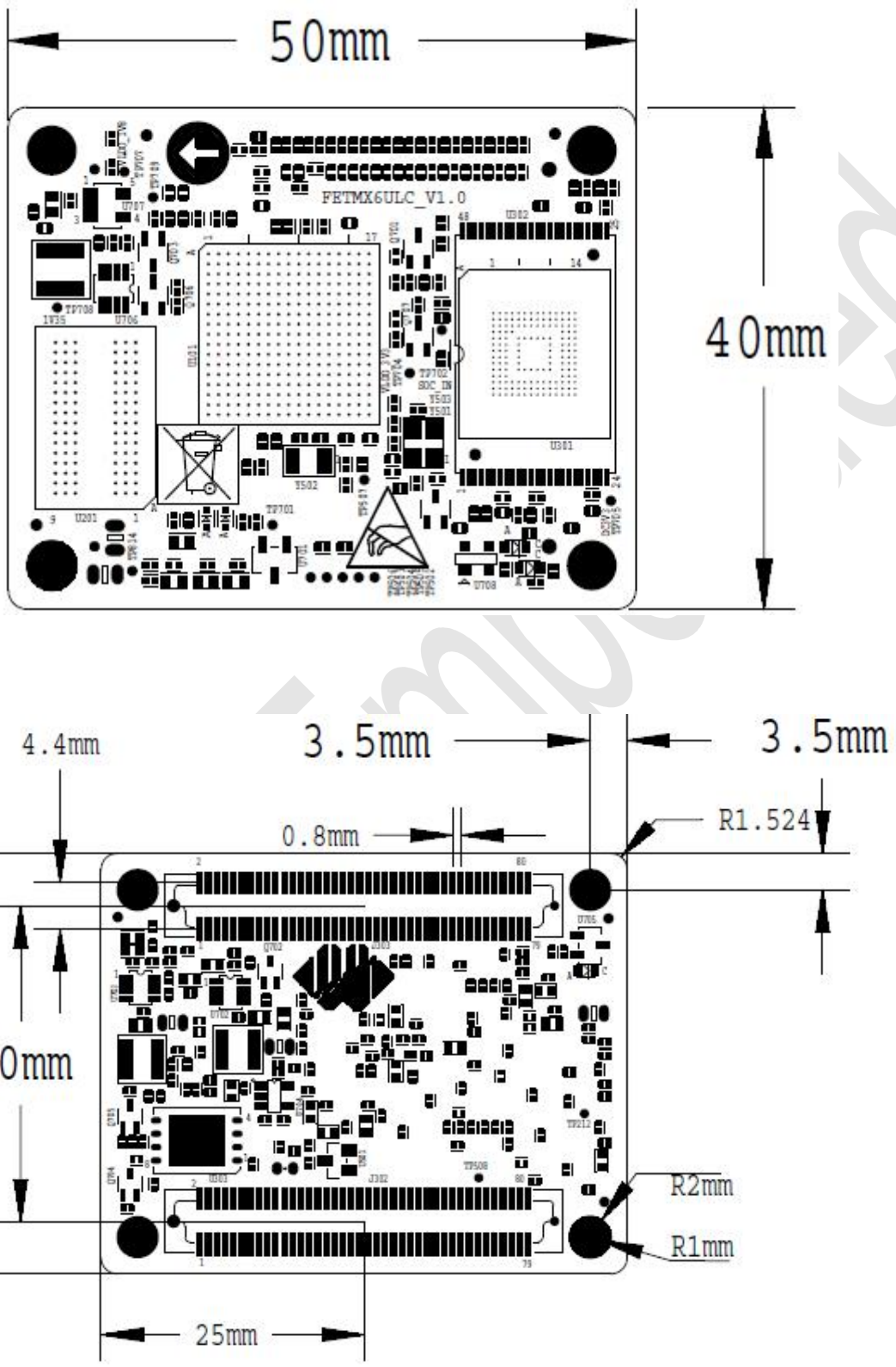
Nand Flash solution



eMMC solution



2.2 FETMX6UL-I CPU Module Dimension



Dimension: 40mm x 50mm, 2x 0.8mm pins, 80pin board-to-board connectors

Craftwork: thickness: 1.1mm, 6-layer ENIG PCB

CPU module connector model: ENG_CD_5177984, carrier board connector model: ENG_CD_5177983, details refer to appendix

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2.2 CPU Module Features

Hardware Item	Model.	CPU Frequency	RAM	Flash
A11	FETMX6UL-C+05512SE8GCA11:A0	528MHz	512MB	8GB
B11	FETMX6UL-C+05512SE4GCB11:A0	528MHz	512MB	4GB
C11	FETMX6UL-C+05256SN256IC11:A0	528MHz	256MB	256MB

2.3 Power Supply Mode

Function	Pin	Value				Spec.
		Minimum	Classic	Maximum	Unit	
Main Power Supply	DC5V	4.5	5	5.5	V	Power adapter: 5V 2A

2.4 Working Environment

Item	Mode	Value				Spec.
		Minimum	Classic	Maximum	Unit	
Working Environment Temp	Working Environment	0	25	+70	℃	Commercial grade
	Storage environment	-40	25	+125	℃	
	Working Environment	-40	25	+85	℃	Industrial grade
	Storage environment	-40	25	+125	℃	
Humidity	Working Environment	10	—	90	%RH	None-condensing
	Storage environment	5	—	95	%RH	

2.5 CPU Module Interface

Function	QTY	Spec.
LCD	1	RGB888, 24-bit, at up to WXGA(1366x 768) (60 Hz)
Camera	1	8-bit parallel interface (DVP), at up to 5-Megapixel
SD/MMC/SDIO	⩽2	At up to UHS-I SDR104 SD and SDIO card with 1-bit or 4-bit transferring standard (up to 104MB/s)
USB	2	USB2.0 (up to 480Mbps), with integrated HS USB Phy

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SAI	≤3	Supports 3x IIS audio at most
SPDIF	1	
UART	≤8	Each up to 5.0 Mbps
eCSPI	≤4	Full duplex enhanced sync. Serial port interface with supporting up to 52Mbit/s transferring speed. It could be configured to be both host/device mode with four chip selection to support multiple devices
IIC	≤4	
Ethernet	≤2	10/100Mbps
PWM	≤8	16-bit
JTAG	Supported	
Keypad Port	Supported	8*8
QSPI	1	
CAN	≤2	CAN 2.0B
ADC	≤10	2x 12-bit ADC, supports up to 10 input channels
ISO07816-3	≤2	
EBI	1	16-bit parallel bus

2.6 CPU Module Pin Definition

CON1 (LEFT)			
No.	**Pin Name**	**Function**	**Note**
1	UART5_RXD	IUART5 receiving	Pinned out by connector P2 on carrier board
2	GND	Ground	
3	UART5_TXD	UAER5 sending	Pinned out by connector P2 on carrier board
4	ENET2_RXER	Ethernet port 2 receiving data valid	Pinned out by connector P2 on carrier board
5	UART4_RXD	UART4 receiving	Pinned out by connector P2 on carrier board
6	ENET2_TX_CLK	Ethernet port 2 sending clock	Pinned out by connector P2 on carrier board
7	UART4_TXD	UART4 sending	Pinned out by connector P2 on carrier board
8	ENET2_TXEN	Ethernet port 2 sending enable	Pinned out by connector P2 on carrier board
9	UART3_CTS	UART3 CTS signal	Pinned out by connector P2 on carrier board
10	ENET2_RXD1	Ethernet port 2 receiving data 1	Pinned out by connector P2 on carrier board
11	UART3_RTS	UART3 RTS signal	Pinned out by connector P2 on

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			carrier board
12	ENET2_RXD0	Ethernet 2 receive data 0	Pinned out by connector P2 on carrier board
13	UART3_RXD	UART3 data receiving	Pinned out by connector P2 on carrier board
14	ENET2_CRS_DV	Ethernet 2 receiving data enable	Pinned out by connector P2 on carrier board
15	UART3_TXD	UART 3 sending	Pinned out by connector P2 on carrier board
16	ENET2_TXD1	Ethernet port 2 sending data 1	Pinned out by connector P2 on carrier board
17	GND		
18	ENET2_TXD0	Ethernet port 2 sending data 0	Pinned out by connector P2 on carrier board
19	UART2_CTS	UART2 CTS signal	Pinned out by connector P2 on carrier board
20	ENET2_MDC	Ethernet to control port RTC output	Connect to Ethernet chipset U2
21	UART2_RTS	UART2 RTS signal	Pinned out by connector P2 on carrier board
22	ENET2_MDIO	Ethernet to control port data	Connect to Ethernet chipset U2
23	UART2_RXD	UART 2 receive	Pinned out by connector P2 on carrier board
24	GND		
25	UART2_TXD	UART 2 sending data	Pinned out by connector P2 on carrier board
26	GPIO_5	USB_OTG2_ID signal	Not pinned out to base board
27	UART1_CTS	UART 1 CTS signal	Pinned out by connector P2 on carrier board
28	GPIO_4	4-wire resistive touching panel X+	Connect to FPC connector
29	UART1_RTS	SDIO1 card detection pin	Connected to SD card connector
30	GPIO_3	4-wire resistive touching panel X-	Connect to FPC connector
31	UART1_RXD	UART1 receiving	Debug port
32	GPIO_2	4-wire resisting touch panel Y+	Connect to base board FPC connector
33	UART1_TXD	UART1 sending	Debug port
34	GPIO_1	4-wire resisting touch panel Y-	Connect to base board FPC connector
35	GND		
36	GPIO-0	USB OTG1 host/device recognization	Connect to base board Micro USB connector
37	JTAG_MOD	JTAG testing mode	Pinned out by P5 on carrier board
38	GPIO-9		Not drawn out on base board
39	JTAG_nTRST	JTAG testing reset	Pinned out by P5 on carrier board

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40	GPIO_8	Backlight adjusting signal	Connect to base board FPC connector
41	JTAG_TCK	JTAG clock testing	Pinned out by P5 on carrier board
42	GND		
43	JTAG_TMS	JTAG testing mode selection	Pinned out by P5 on carrier board
44	SNVS_TAMPER9		Not drawn out on base board
45	JTAG_TDI	JTAG testing data input	Pinned out by P5 on carrier board
46	SNVS_TAMPER8		Not drawn out on carrier bord
47	JTAG_TDO	JTAG testing data output	Pinned out by P5 on carrier board
48	SNVS_TAMPER7		Not drawn out on carrier board
49	GND		
50	SNVS_TAMPER6		Not drawn out on carrier board
51	CLK1_N	RTC out put-	Was not pinned out on base board
52	SNVS_TAMPER5	Ethernet port 1 interruption output	Connect to Ethernet chipset U2
53	CLK1_P	RTC output+	Was not pinned out on base board
54	SNVS_TAMPER4	Ethernet 1 reset	Connect to Ethernet chipset U2
55	GND		
56	SNVS_TAMPER3	Pin for power supply voltage control by CPU on CPU module	Not pinned to base board
57	USB_OTG2_DN	USB host data-	Connected to base board USB-A
58	GND		
59	USB_OTG2_DP	USB host data+	Connected to base board USB-A
60	SNVS_TAMPER2	LCD enable	Connected to FPC connector
61	USB_OTG2_VBUS	USB host power	Connected to 5V
62	SNVS_TAMPER1	Capacitive touch interrupt	Connect to FPC connector on base board
63	GND		
64	SNVS_TAMPER0	3-axis accelerator sense interrupt	Connect to FPC connector on base board
65	nUSB_OTG1_CHD	USB charging control	Not pinned out on base board
66	BOOT_MODE1	BOOT mode selection 1	Connected to DIP switch S2
67	USB_OTG1_DP	USB OTG data+	Connected to Micro USB on base board
68	BOOT_MODE0	BOOT mode selection 0	Connected to DIP switch S2
69	USB_OTG1_DN	USB OTG data-	Connected to Micro USB on base board
70	ONOFF	Power switch	Bit drawn out to carrier board
71	USB_OTG1_VBUS	USB OTG1 power	Connected to Micro USB connector
72	POR_B	i.MX6UL power reset pin	Not drawn out to base board

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73	BAT1	RTC input	Connect to base board 3V RTC
74	MX6_POR_B	CPU module power off reset	Press switch S3 on carrier board to reset CPU module
75	GND		
76	PMIC_ON_REQ	GEN_5V on base board and GEN_3V3	To control GEN_5V and GEN_3V3 output, high level valid
77	VSYS	5V power of the CPU module	
78	PMIC_STBY_REQ		Not pinned out on base board
79	VSYS	5V power of the CPU module	
80	GND		

CON2(RIGHT)

NO.	Pin Name	Description	Remark
1.	LCD_HSYNC	Horizontal sync signal output	Connect to FPC connector on base board
2.	LCD_DATA23	LCD date bit 23	Pinned out by P3 on carrier board
3.	LCD_VSYNC	Filed sync signal output	Connect to FPC connector on base board
4.	LCD_DATA22	LCD data bit 22	Pinned out by P3 on carrier board
5.	LCD_DE	Data enable	Connect to FPC connector on base board
6.	LCD_DATA21	LCD data bit 21	Pinned out by P3 on carrier board
7.	GND		
8.	LCD_DATA20	LCD data bit 20	Pinned out by P3 on carrier board
9.	LCD_PCLK	LCD clock	Connect to FPC connector on base board
10.	LCD_DATA19	LCD data bit 19	Pinned out by P3 on carrier board
11.	LCD_RST	LCD reset	Not pinned out on base board
12.	LCD_DATA18	LCD data bit 18	Pinned out by P3 on carrier board
13.	ENET1_RXER	Ethernet port 1 receive data valid	Connected to Ethernet chipset U2
14.	LCD_DATA17	LCD data bit 17	Pinned out by P3 on carrier board
15.	ENET1_TX_CLK	Ethernet port 1 clock sending	Connected to Ethernet chipset U2
16.	LCD_DATA16	LCD data bit 16	Pinned out by P3 on carrier board
17.	ENET1_TXEN	Ethernet port 1 sending enable	Connected to Ethernet chipset U2
18.	GND		
19.	ENET1_TXD1	Ethernet port 1 send data 1	Connected to Ethernet chipset U2
20.	LCD_DATA15	LCD data bit 15	Connect to FPC connector on base board
21.	ENET1_TXD0	Ethernet port 1 send data 0	Connected to Ethernet chipset U2
22.	LCD_DATA14	LCD data bit 14	Connect to FPC connector on base board
23.	ENET1_CRS_DV	Ethernet port 1 receive data enable	Connected to Ethernet chipset U2
24.	LCD_DATA13	LCD data bit 13	Connect to FPC connector on base board

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25.	ENET1_RXD1	Ethernet port 1 receive data 1	Connected to Ethernet chipset U2
26.	LCD_DATA12	LCD data bit 12	Connect to FPC connector on base board
27.	ENET1_RXD0	Ethernet port 1 receive data 0	Connected to Ethernet chipset U2
28.	LCD_DATA11	LCD data bit 11	Connect to FPC connector on base board
29.	GND		
30.	LCD_DATA10	LCD data bit 10	Connect to FPC connector on base board
31.	NAND_DATA7	NAND data bit 7	Not pinned out to base board
32.	LCD_DATA9	LCD data bit 9	Connect to FPC connector on base board
33.	NAND_DATA6	NAND data bit 6	Not pinned out to base board
34.	LCD_DATA8	LCD data bit 8	Connect to FPC connector on base board
35.	NAND_DATA5	NAND data bit 5	Not pinned out to base board
36.	GND		
37.	NAND_DATA4	Nand data bit 4	This port is for CPU module, it's not pinned out to base board
38.	LCD_DATA7	LCD data bit 7	Connect to FPC connector on base board
39.	NAND_DATA3	Nand data bit 3	This port is for CPU module, it's not pinned out to base board
40.	LCD_DATA6	LCD data bit 6	Connect to FPC connector on base board
41.	NAND_DATA2	NAND data bit 2	This port is for CPU module, it's not pinned out to base board
42.	LCD_DATA5	LCD data bit 5	Connect to FPC connector on base board
43.	NAND_DATA1	Nand data bit 1	This port is for CPU module, it's not pinned out to base board
44.	LCD_DATA4	LCD data bit 4	Connect to FPC connector on base board
45.	NAND_DATA0	Nand data bit 0	This port is for CPU module, it's not pinned out to base board
46.	LCD_DATA3	LCD data bit 3	Connect to FPC connector on base board
47.	NAND_nWE	NAND write signal enable	This port is for CPU module, it's not pinned out to base board
48.	LCD_DATA2	LCD data bit 2	Connect to FPC connector on base board
49.	NAND_nRE	NAND reading signal enable	This port is for CPU module, it's not pinned out to base board

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50.	LCD_DATA1	LCD data bit 1	Connect to FPC connector on base board
51.	CSI_PIXCLK	Pixel clock input of digital camera	Pinned out by P3 on base board
52.	LCD_DATA0	Blue data bit 0(low)	Connect to FPC connector on base board
53.	CSI_HSYNC	horizontal sync signal input of the digital camera	Pinned out by P3 on base board
54.	GND		
55.	CSI_MCLK	Digital camera main clock input	Pinned out by P3 on base board
56.	NAND_DQS	NAND mode selection	This port is for CPU module, it's not pinned out to base board
57.	CSI_VSYNC	Digital camera field sync signal input	Pinned out by P3 on base board
58.	NAND_nWP	NAND read only signal	This port is for CPU module, it's not pinned out to base board
59.	GND		
60.	NAND_ALE	NAND address latch	This port is for CPU module, it's not pinned out to base board
61.	CSI_DAT0	digital camera data 0 input	Pinned out by P3 on base board
62.	NAND_CLE	NAND command latch	This port is for CPU module, it's not pinned out to base board
63.	CSI_DAT1	digital camera data 1 input	Pinned out by P3 on base board
64.	NAND_nCE1	NAND chip select 1	This port is for CPU module, it's not pinned out to base board
65.	CSI_DAT2	digital camera data 2 input	Pinned out by P3 on base board
66.	NAND_nCE0	NAND chip select 0	This port is for CPU module, it's not pinned out to base board
67.	CSI_DAT3	digital camera data 3 input	Pinned out by P3 on base board
68.	NAND_nREADY	NAND busy signal	This port is for CPU module, it's not pinned out to base board
69.	CSI_DAT4	digital camera data 4 input	Pinned out by P3 on base board
70.	SD1_DATA0	SDIO1 data 1	Connected to SD connector on base board
71.	CSI_DAT5	digital camera data 5 input	Pinned out by P3 on base board
72.	SD1_DATA1	SDIO1 data 1	connected to SDIO0 connector on base board
73.	CSI_DAT6	digital camera data 6 input	Pinned out by P3 on base board
74.	SD1_CLK	SDIO1 clock	connected to SDIO0 connector on base board
75.	CSI_DAT7	digital camera data 7 input	Pinned out by P3 on base board
76.	SD1_CMD	SDIO1 command	Connected to SDIO0 connector on base board
77.	GND		
78.	SD1_DATA3	SDIO1 data 3	Connected to SDIO0 connector on

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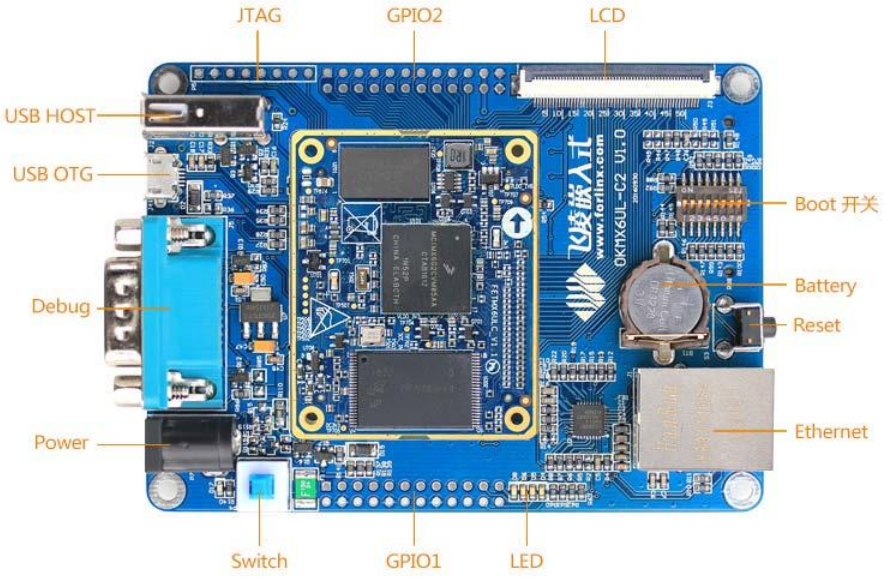
			base board
79.	NVCC_CSI	CPU internal camera power	
80.	SD1_DATA2	SDIO data 2	Connected to SDIO0 connector on base board

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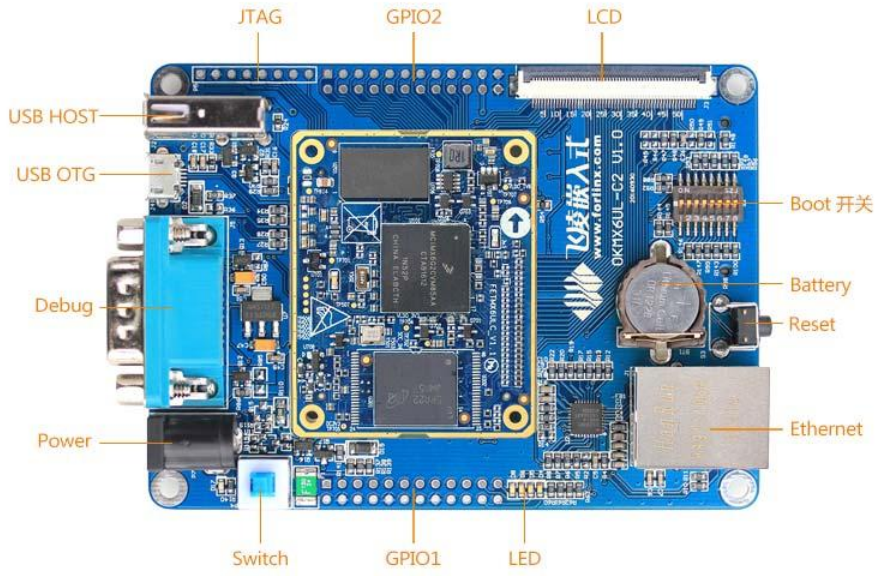
Chapter 3 i.MX6UL Development Platform Overview

3.1 Overview of single board computer i.MX6UL

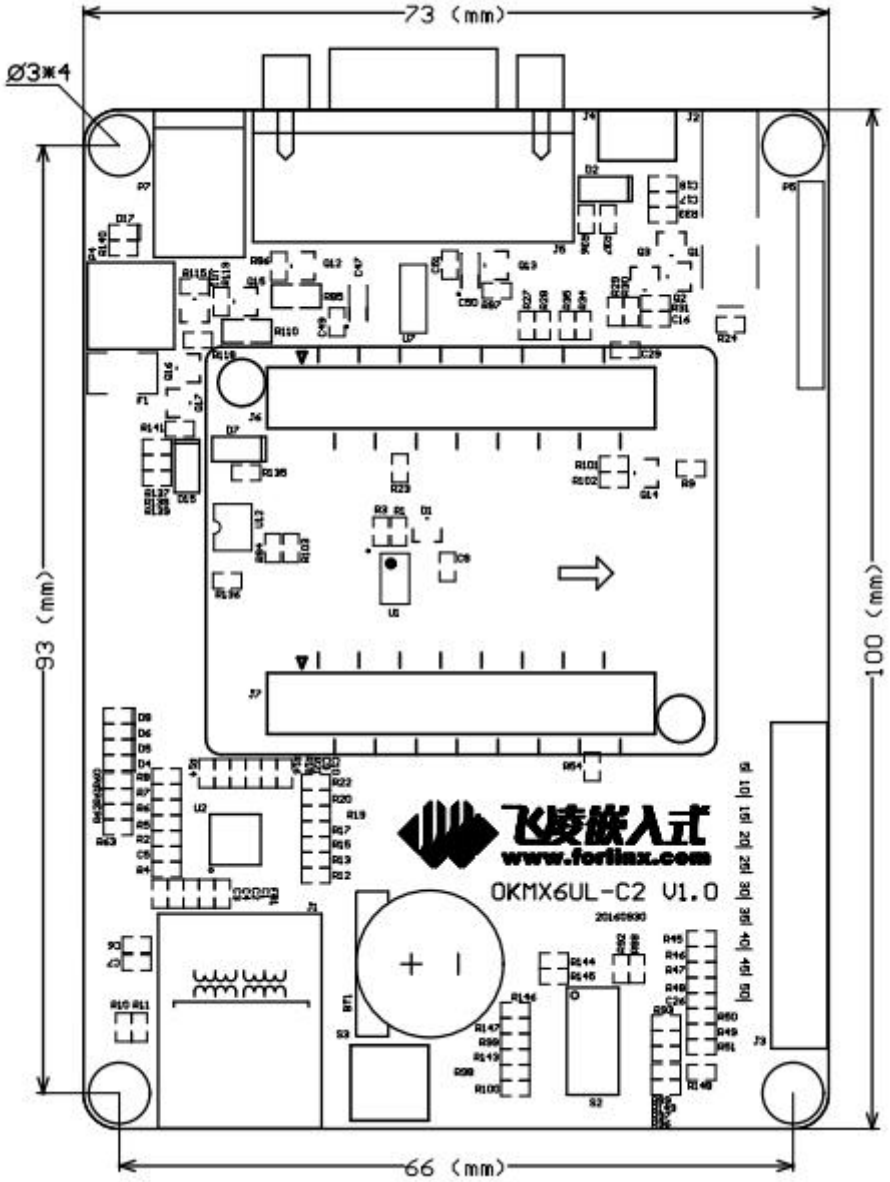
Nand solution



eMMC solution



22



Dimensions: 100mm×73mmrectangle PCB

Mounting hole: space: 93mm x 66mm, pore diameter: 3mm.

Manufacture: thickness of 1.6mm, 2-layer PCB

Power supply: DC5V

3.2 Base board resource:

Item	QTY	Spec.
LCD	1	RGB888, WXGA at up to 1366x 768 (60Hz)
USB Host	1	USB 2.0 (up to 480Mbps)
USB OTG	1	Micro USB 2.0 OTG (up to 480Mbps)
Ethernet	1	10/100Mbps, RJ45

23
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SD card	1	Compatible with SD, SDHC, SDXC (UHS-I)
LED	4	
PWM	1	LCD backlight
ADC	4	For resistive touching
UART	4	Two 5-wire serial port, two 3-wire serial port, all are 3.3V power level, each at up to 5.0 Mbps
UART Debug	1	RS232, DB9 port
JTAG Debug	1	Pinned out by pin connectors

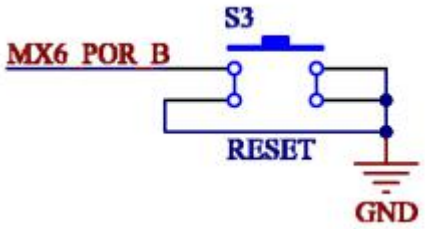
3.3 i.MX6UL Base Board Introduction

3.3.1 Base Board Power

DC5V, on-board over voltage protection, specified power adapter DC 5V 2A

3.3.2 Reset Key

S3 on carrier board, press it to power off CPU module and reset the whole board



3.3.3 Boot Configuration

Different file flashing and booting modes are available for i.MX6UL,. the booting configuration pins are BOOT_MODE0、BOOT_MODE1、LCD_DATA3~LCD_DATA7、LCD_DATA11
BOOT_MODE0, BOOT_MODE1 are pins for BOOT_TYPE selection

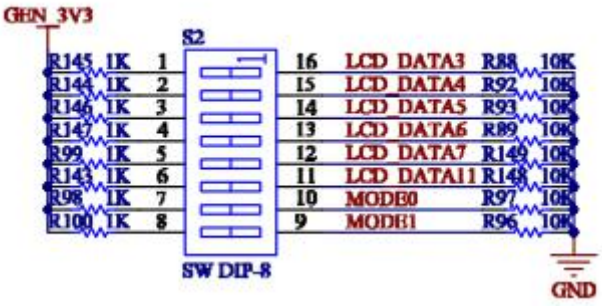
BMODE[1：0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot(Development)
11	Reserved

LCD_DATA3~LCD_DATA7 and LCD_DATA11 are pins for Boot_Device selection

Boot Device	LCD_D7	LCD_D6	LCD_D5	LCD_D4	LCD_D3	LCD_D11
QSPI	0	0	0	1	x	x
WEIM	0	0	0	0	Memory Type: 0-NOR-Flash 1-OneNAND	x
Serial-ROM	0	0	1	1	x	x
SD/eSD	0	1	0	x	x	0-SDHC1 1-SDHC2
MMC/eMMC	0	1	1	x	x	
NAND	1	x	x	x	x	x

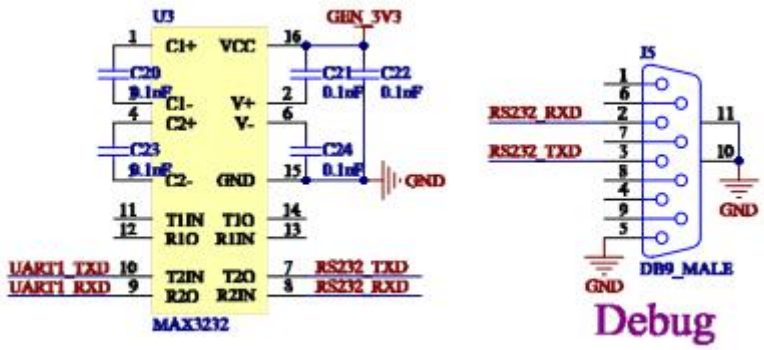
SDHC1 port on base board is for SD card, and SDHC2 interface if for eMMC on CPU module, SW4 is a configuration key for single board computer booting. Below modes are available

1. Flash OS image via SD card: On(up)4, 8
   Off(down)1,2,3, 5, 6, 7
2. Flash OS image via USB OTG: key 8 off, others are all to on,
3. Boot from eMMC: On: 3, 4, 6, 8
   Off: 1, 2, 5, 7
4. Boot from Nand: On: 5, 8
   Off: 1, 2, 3, 4, 6, 7



3.3.4 Debug Port

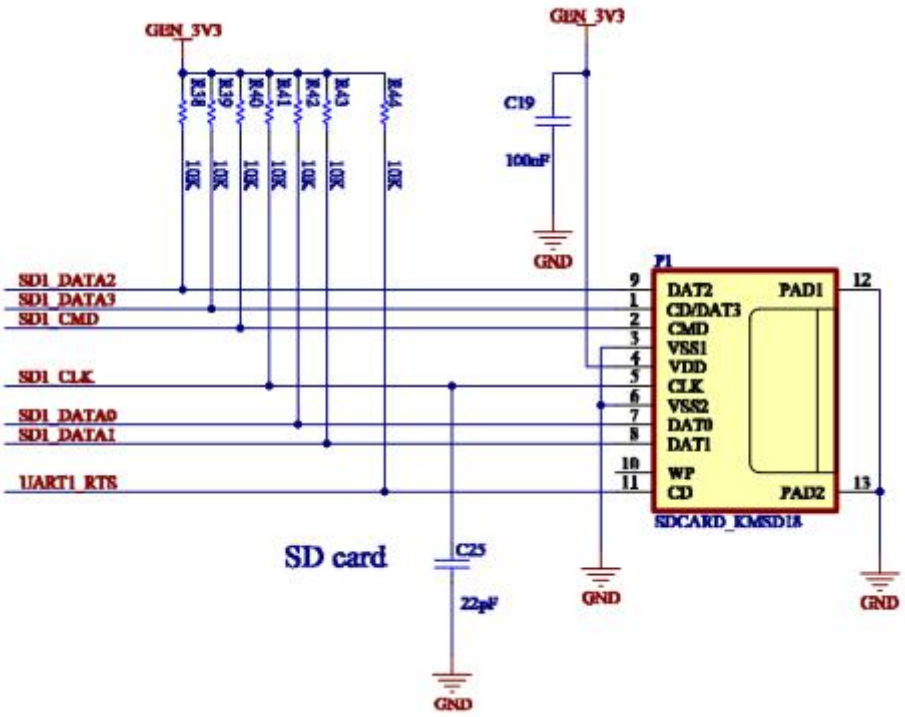
Debug port UART1 is RS232 port connected to PC by a DB9 male connector and it could also be connected to PC via USB to serial port cable



25
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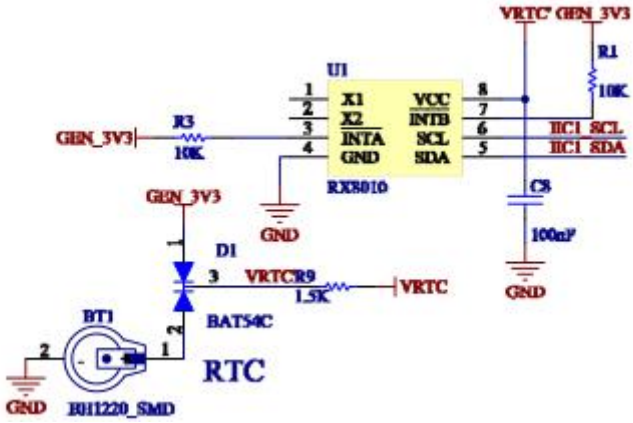
3.3.5 SD Card Slot

P1 is an SD card slot pinned from SDHC1 of the CPU, users could configure the board to be flashed OS by SD card. This port supports SD, SDHC and SDXC(UHS-1) card. When the SDXC card class is UHS-II or above, it will be degraded to UHS-I because from UHS-II begin, new data pins are added.



3.3.6 RTC

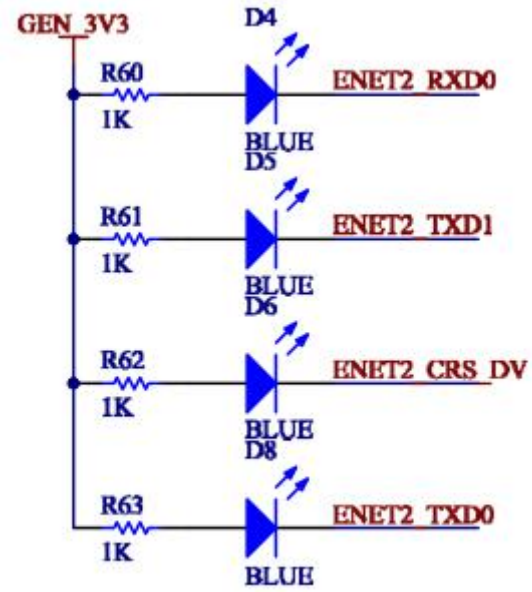
The CPU is with RTC and it also supports external RTC. We selected to use external RTC considering CPU RTC power consumption. The battery model is CR1220.



26
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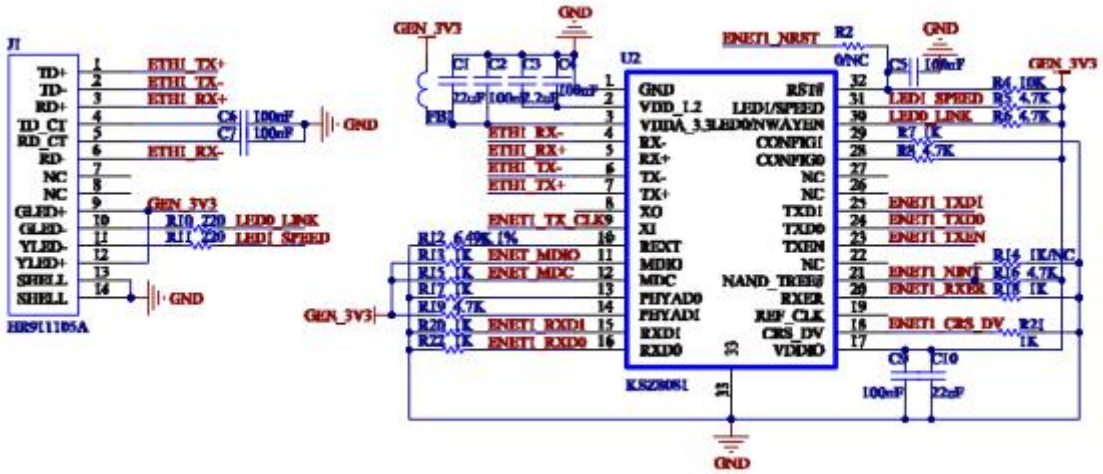
3.3.7 LED

4x LED are available on single board computer i.MX6UL, they are D4, D5, D6 and D8, users should configure the pin(s) to GPIO, when output lower power level, the LED will be lightened, while when output a high power level, the LED will be closed



3.3.8 Fast Ethernet

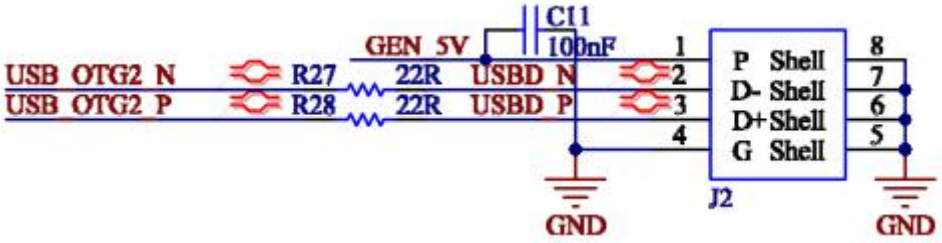
One 100M Ethernet port is available on the carrier board, which is connected to PHY KSZ8081 by RMII. The RJ45 connector model is HR911105A with internal isolation transformer.



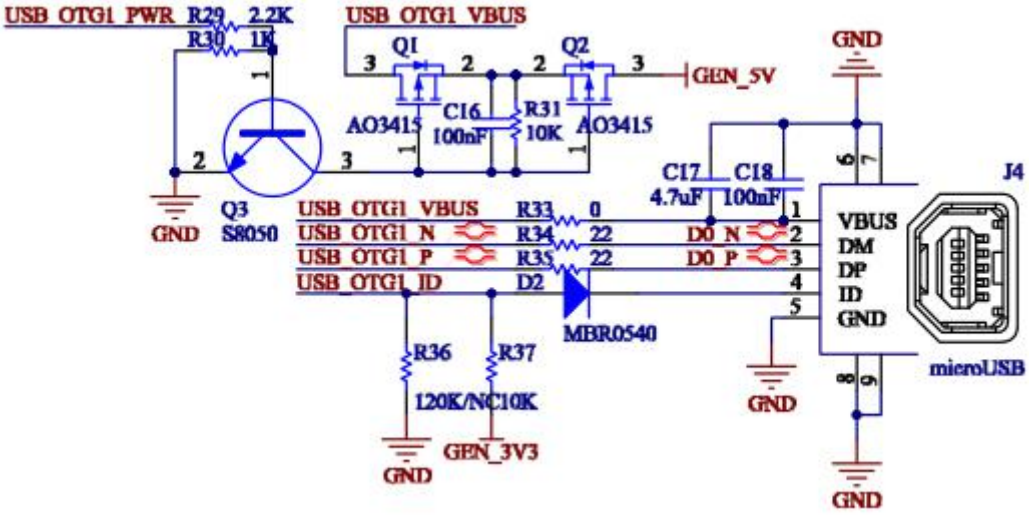
3.3.9 USB Host

USB OTG2 was designed to be USB host 2.0 which is available for mouse, 3G and WIFI device

27



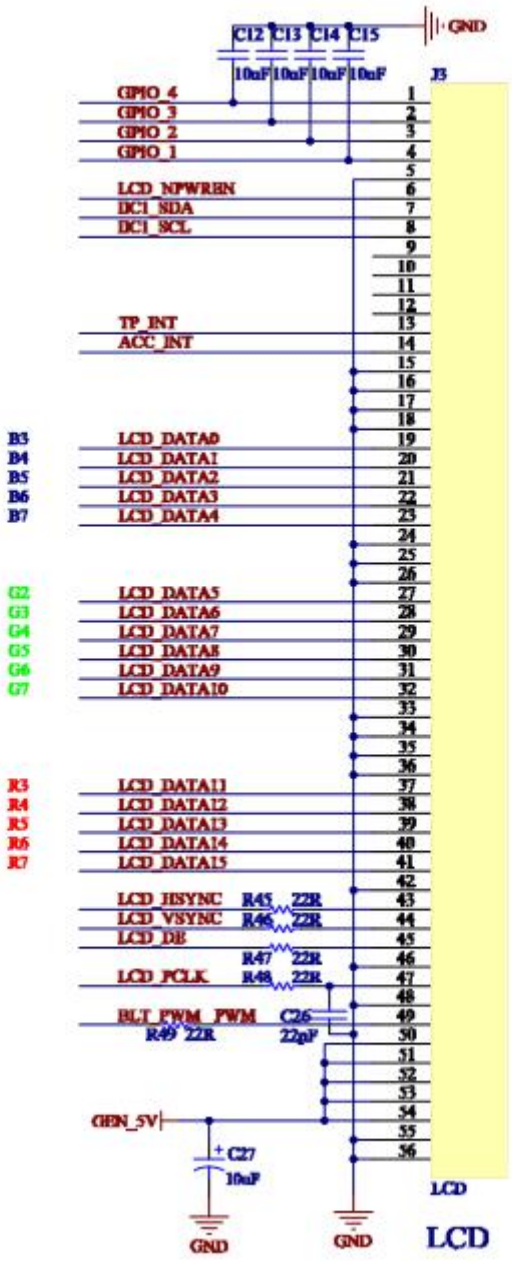
3.3.10 USB OTG



3.3.11 LCD

The board is with a general LCD interface, it's pinned out by a FPC connector(CON27) with 54-pin and 0.5mm pitch, it's used for connection of both resistive LCD and capacitive LCD from Forlinx. This display port is RGB565 16-bit

Forlinx Embedded



Note: to avoid the single board computer booting affected by LCD, we kindly suggest users to add a buffer chip between LCD and CPU, chipset SN74AVC16245 is kindly recommended.

Appendix 1 Hardware Design Guideline

1. boot settings

Users could select different methods to flash OS to the board and boot system by different boot settings. Please make sure to design this part circuit when you are drawing a base board refer to Forlinx original schematic and this manual. If you also need flash OS via SD card and boot from eMMC, you should also need design control

to LCD_DATA11, otherwise, you can also do fix process to power level of LCD_DATA11 accordingly.

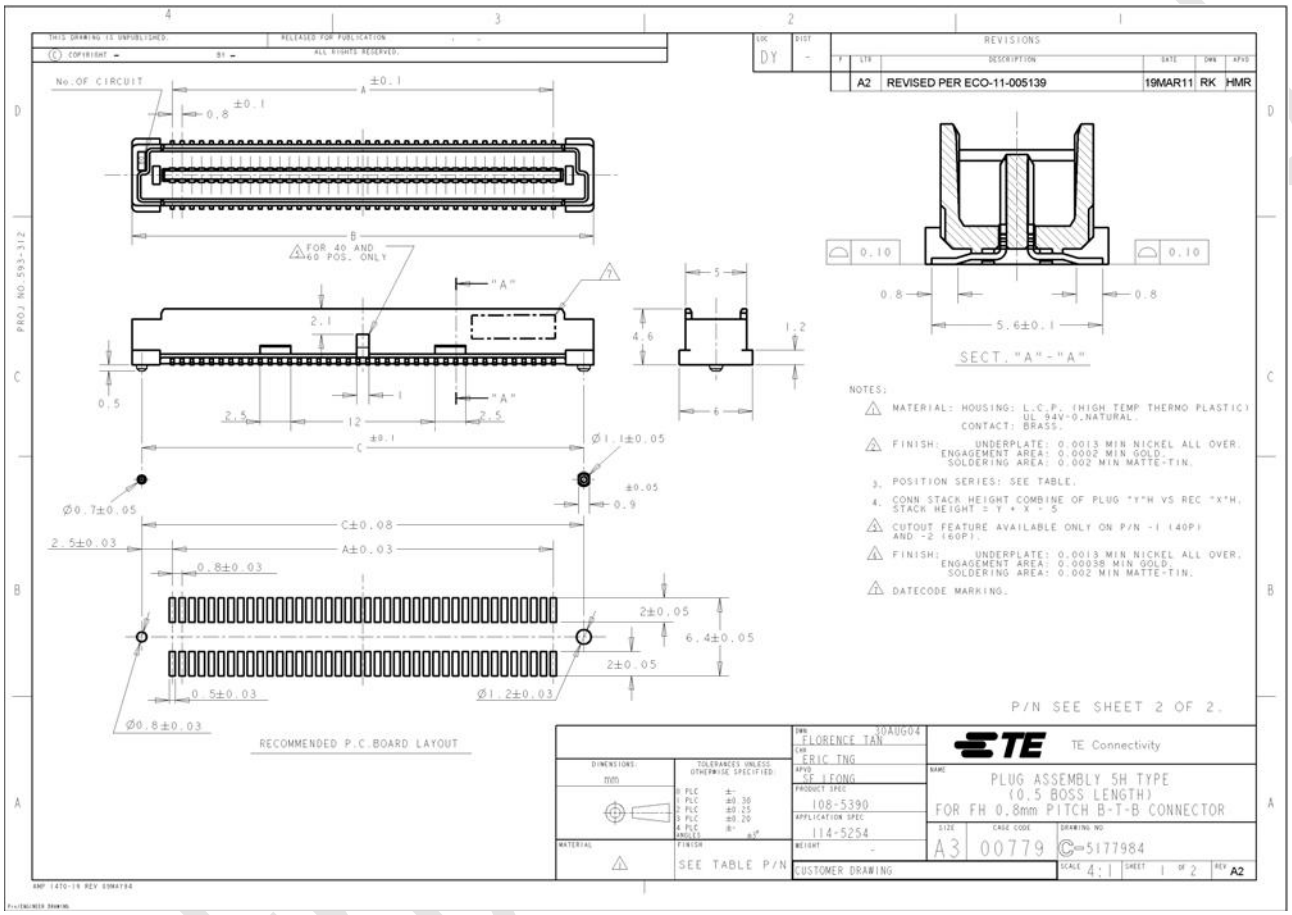
2. PMIC_ON_REQ drive capability issue

Both GEN_5V and GEN_3V3 on base board are all controlled and got from PMIC_ON_REQ, current driving capability of PMIC_ON_REQ is too weak and needs voltage control oriented component, AO3416 was used as N channel field effect transistor, meanwhile, the gate of this filed effect transistor should to be designed with a pull-down resistor, otherwise the transistor could not be powered off.

3. SNVS_TAMPER3 和 GPIO_5 is for CPU module power supplying but not for carrier board power supplying

Forlinx Embedded

Appendix 2 Board-to-board connector dimension



Thank you!