
EDAC Testing Injection of Correctable and Uncorrectable Errors

This application note describes how to test the TSC695 trap mechanism when the EDAC is enabled. A simple EDAC test procedure is described in this application note. To illustrate the procedure, two test cases consisting in single error injection and multiple errors injection are provided.

References

- TSC695 SPARC® 32-bit Space Processor - User Manual
- Application note - "Trap generation under EDAC and parity protection"

Abbreviations

- EDAC: Error Detection And Correction



TSC695

Application Note

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EDAC Testing Overview

The TSC695 processor implements a hardware EDAC for error detection and correction over the 32-bit data bus. Based on a seven bit Hamming code, the EDAC detects any double error on a 40-bit bus and also corrects any single error on a 40-bit data bus (the 40-bit bus includes the 32 data bits, the parity bit over the 32-data bits and the 7-bit checkbit).

For EDAC testing purposes, it is necessary to be able to inject single error and multiple errors to memory. To do such fault injection, the TSC695 processor provides a test control register. With this register, it is possible to force data store to memory with arbitrary checkbit.

Testing Restriction

The TSC695 processor not only integrates an EDAC protection on data bus but also includes parity checking. The data bus parity signal 'DPAR' is used to check and generate an odd parity over the 32-bit data bus.

During a write operation to a memory area protected by the EDAC, the parity and the 7-bit checkbit are automatically calculated over the 32-bit data bus. Then, all 40 bits are stored to memory. Thus, the parity stored to memory is always representative of the data stored.

For EDAC test purpose, the TSC695 processor provides a test control register capable of forcing a store to memory with a user pre-defined checkbit. Regarding parity protection, the TSC695 processor does not implement any test facility.

To do fault injection, only two error sources can be used:

- insertion of error in data field
- insertion of error in checkbit field

Insertion of Error in Data Field

If a single bit flip error is inserted in the 32-bit data, due to automatic parity generation, a write of such a corrupted data to memory generates two errors in memory:

- the flipped bit in data field
- the parity bit flip

A read access to the 'corrupted data' address will always result in a double EDAC error, two errors being detected in the 40-bit word. An uncorrectable error is detected. Trap 0x09 is generated in case of data access. Trap 0x01 is generated in case of instruction fetch.

Error injection in the data can be used to test double error (uncorrectable error) handling.

Insertion of Error in Checkbit Field

If a single bit error is forced in the checkbit through the test control register, the write to the memory will result in a single error:

- one bit flip in checkbit

A read access to the 'corrupted data' address will result in a single EDAC error, one error being detected in the 40-bit word. A correctable error is detected. Trap 0x16 is generated.

Error injection in the test checkbit can be used to test single error (correctable error) handling.

Trap Handlers

In order to identify the origin of an error detected by the EDAC, the TSC695 processor provides three traps. Two synchronous traps represent un-correctable errors (Trap 0x01 and Trap 0x09) while one asynchronous trap represents correctable errors (trap 0x16).

Trap 0x16 is an asynchronous interrupt. The level of this interrupt is 6. To make it possible to generate the corresponding trap, PIL field from the processor state register (PSR) must be set to a value lower than 6. The interrupt mask must also be configured to enable interrupt 6 handling.

Synchronous Traps

Trap 0x01: An uncorrectable error is detected during instruction fetch.

Trap 0x09: An uncorrectable error is detected during data access.

Asynchronous Trap

Trap 0x16: A correctable error is detected during memory access.

Testing Procedure

The testing procedure is based on the use of the test control register (TSTCTR). Setting the 'et' bit from the TSTCTR register allows fault injection for memory test purposes and test of the EDAC function itself. By enabling this EDAC test mode, the bits in the 'cb' field of this register are substituted to the normal checkbits during the following store cycles.

- Step 1** Select the data to be stored to a memory area protected by EDAC and select a test checkbit.
- Step 2** Set the test control register 'et' bit to one to enable EDAC testing.
- Step 3** Write the selected checkbit value to the test checkbit field ('cb') from TSTCTR register.
- Step 4** Store the data to a memory area protected by EDAC.
During the store access, not only the data is stored to memory but also are the data parity and the checkbit that was written in 'cb' field of the TSTCTR register.
- Step 5** Reset the 'et' bit in the test control register 'TSTCTR' to disable fault injection.
- Step 6** Read the data from the memory location chosen for fault injection.
- Step 7** Error detection:
- if a correctable error occurs, trap 0x16 is generated
 - if an uncorrectable error occurs during instruction access, trap 0x01 is generated
 - if an uncorrectable error occurs during data access, trap 0x09 is generated

Correctable Error Trap Handling - Testing

Correctable Error Injection

Single error generation can only be tested through checkbit field error insertion. The following table gives some examples of checkbits/data/parity blocks that could result in a correctable EDAC error.

Table 1. Checkbit Table (Data/Checkbit/Parity)

Data Value	Good Checkbit	False Checkbit (One Error)	Parity
0x0000 0000	0x14	0x04	1
0x0000 0001	0x2C	0x3C	0
0x0000 0002	0x51	0x50	0
...	...	...	...

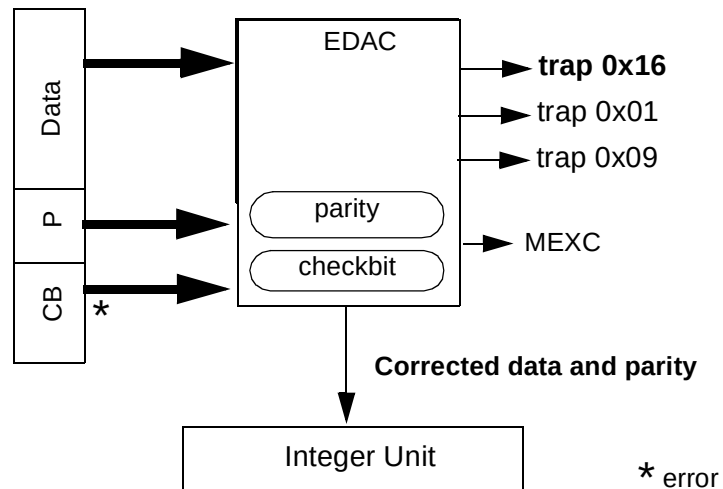
- ex: CB = 0x2C , Data = 0x0000 0001 , Parity =0

Single error insertion consists in the definition of a 'false' checkbit value. This false value simply corresponds to the real EDAC checkbit value for which one bit is flipped.

- ex: CB = 0x2D , Data = 0x0000 0001 , Parity =0

To do the test, refer to the '*testing procedure*' section. When doing the read operation, the EDAC detects that there is one error in the 40-bits word read. A correctable error is detected. Trap 0x16 is generated.

Figure 1. Memory Read With Correctable Error



Correctable Error - Code Sample

!initialise PIL field from PSR

```
set 0x10a0,%l4
mov%l4,%psr
set 0x1f80000,%l0
```

!initialise data address and data value

```
set 0x02020300,%l1
set 0x00000001,%l2
```

! enable EDAC on RAM area

```
set 0x00004000,%l4!enable EDAC on RAM
ld [%l0+0x10],%l7
or %l4,%l7,%l7
st %l7,[%l0+0x10]
```

!unmask IT6: correctable error in memory

```
set 0x00007FBE,%l4
st %l4,[%l0+0x4c]
```

! enable EDAC testing

! insert fault into check bit field:

!good: data = 0x0000 0001 => CB = 0x2C

!error: data = 0x0000 0001 => CB = 0x2D

```
set 0x2002D,%l4
st %l4,[%l0+0xd0]
```

!store data with cb error

```
st %l2,[%l1]
```

!disable EDAC testing

```
st %g0,[%l0+0xd0]
```

!read data and trap generation

```
ld [%l1],%l6
```

Uncorrectable Error Trap Handling - Testing

Uncorrectable Error Injection

The following table gives some examples of checkbits/data/parity blocks that could result in uncorrectable EDAC error.

Table 2. Checkbit Table (Data/Checkbit/Parity)

Data Value	Checkbit	Parity	Data False Value	False Parity
0x0000 0000	0x14	1	0x0000 0200	0
0x0000 0001	0x2C	0	0x0000 0011	1
0x0000 0002	0x51	0	0x0000 1002	1
...	...	...	...	...

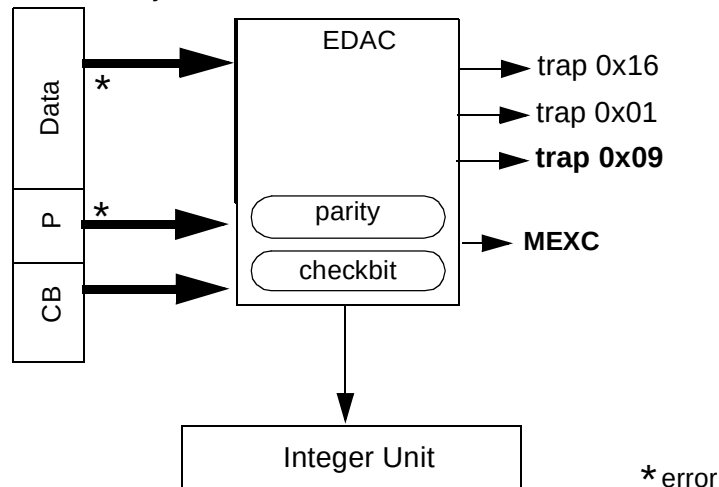
- ex: CB = 0x2C , Data = 0x0000 0001 , Parity =0

Double error insertion consists in the definition of a 'false' data field value. This false value is the real data with one bit flipped. The second error is generated when storing the data (parity generation).

- ex: CB = 0x2C, Data = 0x0000 0011 , Parity =1

To do the test, refer to the '*testing procedure*' section. When doing the read operation, the EDAC detects that there are two errors in the 40-bits word read. An uncorrectable error is detected. Trap 0x09 or trap 0x01 is generated.

Figure 2. Memory Data Read With Uncorrectable Error



Uncorrectable Error - Code Sample

Parity Error + Data Error

```
!initialise data address and data
    set 0x1f80000, %l0
    set 0x02020010,%l1
    set 0x00000003,%l2

! enable EDAC testing
!good: data = 0x0000 0001 => CB = 0x2c
!error: data = 0x0000 0000 => CB = 0x2C
    set 0x2002C,%l4
    st %l4,[%l0+0xd0]

!store data with Cb error
    st %l2,[%l1]

!disable EDAC testing
    st %g0,[%l0+0xd0]

!read data
    ld [%l1],%l6
```

Two Data Errors (No Parity Change)

```
!initialise data address and data
    set 0x1f80000, %l0
    set 0x02020010,%l1
    set 0x00000002,%l2

! enable EDAC testing
    set 0x2002C,%l4
    st %l4,[%l0+0xd0]

!store data with Cb error
    st %l2,[%l1]

!disable EDAC testing
    st %g0,[%l0+0xd0]

!read data
    ld [%l1],%l6
```



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