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155 Mbps UTP#5 Complete PHY Interface

AD6816

FEATURES

Complete ATM Transceiver for 155 Mbps for UTP#5 or Fiber
Meets ATM Forum UNI 3.1 Requirements
Meets SONET/SDH Jitter Requirements
Meets FCC Class B Emissions Requirements
Drives up to 110M Category #5 UTP/FTP
Adjustable Line Driver Output Current
Equalizes up to 110M Category #5 UTP/FTP
Baseline Restoration Function Eliminates Baseline Wander
19.44 MHz Oscillator Circuit
Frequency Synthesizer for 155 MHz Tx Bit Clock
155 Mbps Clock Recovery and Data Retiming
Phase Continuous Switch at Frequency Synthesizer Output
Single Supply Operation: +5 V or –5.2 V
Low Power: 400 mW
10KH ECL Compatible Output
Package: 44-Pin Thin Quad Flatpack

PRODUCT DESCRIPTION

The AD6816 provides a single chip solution for interfacing an ATM User-Network Interface IC to either a Category #5 Unshielded Twisted Pair (UTP) system or a fiber optic system. The IC provides line equalization and baseline restoration, line driver, clock recovery and data retiming, local reference clock oscillator and frequency synthesis functions. Signal multiplexers within the IC allow the user to perform loop-back, bypass the data retiming function and select the frequency reference for the transmit bit clock (independent timing or loop timing).

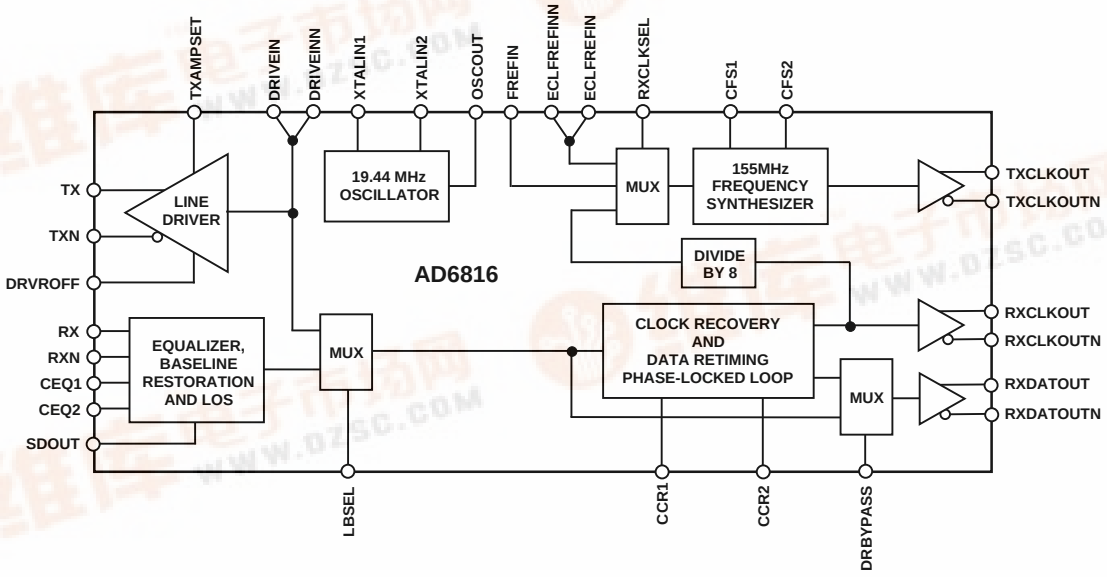
The line equalization and baseline restoration block compensates for up to 110M Category #5 UTP and transformer, respectively. This block has a Signal Detect output, SDOUT, that when low indicates a loss of input signal at RX, RXN. The AD6816 supports application with a fiber optic receiver or transceiver. In this case, the line equalizer block adapts to provide no equalization.

The line driver has a differential ECL input stage providing controlled current output suitable for driving a Category #5 UTP system. A single resistor from the line driver output current control pin to ground controls the output current. The user has the option to disable the line driver output. A signal multiplexer allows the user to loop back the line driver input signal through the clock recovery and data retiming PLL for test purposes.

The clock recovery and data retiming PLL has a factory trimmed VCO center frequency and an integrated frequency control loop that combine to ensure signal acquisition. This eliminates reliance on external components, like a crystal or an SAW filter, to aid frequency acquisition. At frequency lock, the frequency error is zero and the frequency detector has no effect. At this point, the PLL works to ensure that the output phase tracks the input

(Continued on page 4)

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD6816–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = V_{MIN}$ to V_{MAX}, $C_{CR} = 0.1\ \mu F$, $C_{EQ} = 0.1\ \mu F$, $C_{FS} = 0.0047\ \mu F$, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
RECEIVER					
Input Signal Range	Signal Into Up to 110 M UTP #5	0.764		1.06	V p-p
Differential Input Voltage				1.5	Volts
Transitionless Data Run				400	Bit Periods
Equalizer Time Constant	C_{EQ} = 0.1 µF			1	sec
SIGNAL DETECT					
Trip Level	2^{23}–1 PRN, 0 M Cable		98		mV p-p
Release Level	2^{23}–1 PRN Input, 0 M Cable		118		mV p-p
Response Time	30 M Cable, Figure 22. Evaluation Circuit		12.9		µs
SDOUT Output Logic High	Load = +4 mA	3.6			Volts
SDOUT Output Logic Low	Load = –2.2 mA			0.4	Volts
LINE DRIVER	Refer to Figure 2				
Differential Input	Output Current Variation < 1%	0.150		1	V p-p
Common-Mode Input Voltage		2		4	V
Output Current			20		mA
Maximum Current Variation	1.13 kΩ 1% Resistor-to-Ground at TXAMPSET		5.0		%
Common-Mode Current	Percentage of Output Drive Current				%
	50 Ω Collector Loads at TX and TXN, T_A = +25°C		2.5	7	%
Rise and Fall Times	10%–90%, Device Only		2.1		ns
Rise and Fall Times	10%–90%, Transformer Output, Refer to Figure 22		2.7		ns
INPUT CONTROL SIGNALS	Refer to Table I				
Input Logic Low, V_{IL}				0.8	Volts
Input Logic High, V_{IH}		2			Volts
CLOCK RECOVERY PLL					
Output Clock Jitter	2^{23}–1 PRN Input		2.0	3.5	Degrees rms
Static Phase Error	2^{23}–1 PRN Input		4	20	Degrees
Bandwidth	2^{23}–1 PRN Input		100		kHz
Setup Time (t_{SU})	Figure 1	2.4	3.0	3.5	ns
Hold Time (t_H)	Figure 1	2.9	3.4	4.0	ns
OSCILLATOR CIRCUIT	Crystal $R_{SERIES} \le 40\ \Omega$				
Center Frequency	Series Mode Crystal Accuracy ≤ 50 ppm	19.437	19.44	19.442	MHz
Frequency Deviation			±22	±82	ppm
Output Duty Cycle	400 Ω to 2 V Load		43		%
Output Drive High	400 Ω to 2 V Load	3.6			Volts
Output Drive Low	400 Ω to 2 V Load			0.4	Volts
FREQUENCY SYNTHESIZER					
Reference Input Frequency			19.44 or 9.72		MHz
Duty Cycle Tolerance		20		80	%
Bandwidth			200		kHz
Time Constant			800		ns
Output Clock Jitter			1.8	2.8	Degrees rms
ECLFREFIN/N	FREFIN Pin @ Ground				
Common-Mode Input Signal		V_{CC} – 2		V_{CC}	Volts
Differential Input Signal		200			mV
FREF IN Logic Low, V_{IL}	ECLFREF & ECLFREFN Pins @ Ground			0.8	Volts
FREF IN Logic High, V_{IH}		2			Volts
PECL OUTPUT	Pins 10, 11, 13, 14, 17, 18				
Output Logic High, V_{OH}	Referred to V_{CC}	–1.2	–1.0	–0.7	Volts
Output Logic Low, V_{OL}	Referred to V_{CC}	–2.0	–1.8	–1.7	Volts
POWER SUPPLY VOLTAGE	V_{MIN} to V_{MAX}	4.5		5.5	Volts
POWER SUPPLY CURRENT	V_{CC} = 5.0 V, V_{EE} = GND, T_A = +25°C		77	95	mA
OPERATING TEMPERATURE RANGE	T_{MIN} to T_{MAX}	0		70	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . +12 V
Input Voltage (Pin 43 or Pin 44 to V_{CC}) . . . . . V_{CC} + 0.6 V
Maximum Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
ESD Rating (Human Body Model) . . . . . 1500 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

44-Pin Thin Quad Flatpack Package:
θ_{JA} = 50°C/Watt, θ_{JC} = 10°C/Watt

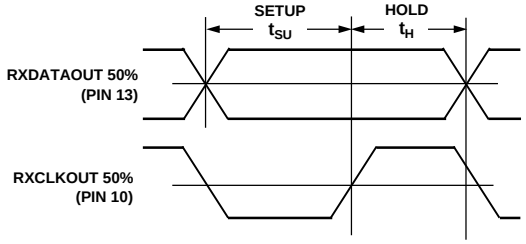


Figure 1. Clock Recovery PLL Setup and Hold Time

PIN CONFIGURATION

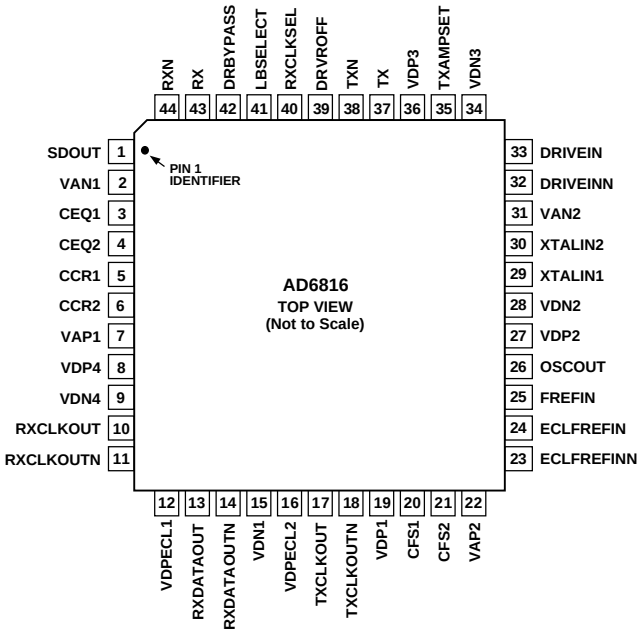


Table I. Control Functions (NC = No Connection)

Function	Input Signal Mnemonic	Description
Disable Line Driver	DRVROFF	Logic 1 Disables Line Driver Output Logic 0 or NC Enables Line Driver Output
Loop-Back	LBSEL	Logic 1 Enables Loop-Back from DRIVEIN/N Logic 0 or NC Disables Loop-Back
Bypass Data Retiming	DRBYPASS	Logic 1 Bypassing Data Retiming Logic 0 or NC Enables Data Retiming
Reference Frequency Select for Frequency Synthesizer	RXCLKSEL	Logic 1 Selects Reference Frequency Derived from Recovered Clock Logic 0 or NC Selects External Frequency Reference

Table II. Configuring the Frequency Synthesizer for Different Oscillator Types

Oscillator Output Type	Apply to Input Pin(s)	Ground Pin(s)
TTL (Single Ended Including On-Chip Oscillator)	FREFIN (Pin 25)	ECLFREFIN/ ECLFREFINN (Pins 24 & 23)
PECL	ECLFREFIN/ ECLFREFINN (Pins 24 & 23)	FREFIN (Pin 25)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6816KST	0°C to +70°C	44-Pin Thin Quad Flatpack	ST-44

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6816 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



(continued from page 1)

phase. The two loops work in harmony with each other, requiring no control signals for enabling or disabling. Shorting the clock recovery and data retiming PLL damping factor capacitor, C_{CR}, brings the recovered clock output signal to the clock recovery VCO center frequency.

The crystal oscillator circuit provides an accurate 19.44 MHz output with a series mode, 19.44 MHz crystal. This circuit requires no capacitive tuning and can provide a 19.44 MHz, ±100 ppm output, capable of driving up to five TTL gates or 50 pF load capacitance.

The frequency synthesizer processes either a 19.44 MHz or a 9.72 MHz input signal at the FREF, ECLFREF/ECLFREFN pins, or the 19.44 MHz byte clock derived from the 155.52 MHz RXCLKOUT & RXCLKOUTN signal. The RXCLKSEL signal determines whether or not the derived byte clock is used by the frequency synthesizer. When the RXCLKSEL signal is high, the frequency synthesizer processes the derived byte clock. When the RXCLKSEL signal is left unconnected, or held low, the frequency synthesizer processes the reference signal at the FREFIN or ECLFREFIN/ECLFREFINN pins (refer to Table II). Having the frequency synthesizer loop process either the derived byte clock or a reference eliminates runt pulses that may occur when switching between two 155.52 MHz bit clocks.

The synthesizer can be configured to accept an external frequency reference in either TTL/CMOS format or in PECL format. This selection is made by sensing the common-mode voltage at Pins 23 and 24. If valid PECL levels are present at Pins 23 and 24, this signal is used as the frequency reference and any signal present at Pin 25 is ignored. If Pins 23 and 24 are connected to ground (VDN1, Pin 15), the TTL/CMOS input (Pin 25) is enabled and used as the frequency reference for the synthesizer.

The AD6816 is packaged in a 44-pin Thin Quad Flatpack (TQFP), having lead frame dimensions 0.55" × 0.55".

PIN DESCRIPTION

Pin No.	Mnemonic	Description
1	SDOUT	Signal Detect Output
2	VAN1	Analog Ground—Clock Recovery and Equalizer
3	CEQ1	Equalizer Loop Filter Capacitor
4	CEQ2	Equalizer Loop Filter Capacitor
5	CCR1	Clock Recovery Loop Damping Capacitor
6	CCR2	Clock Recovery Loop Damping Capacitor
7	VAP1	Analog Supply—Clock Recovery and Equalizer
8	VDP4	Digital Supply—Clock Recovery Logic and Mux
9	VDN4	Digital Ground—Clock Recovery Logic and Mux
10	RXCLKOUT	Differential Recovered Clock Output
11	RXCLKOUTN	Differential Recovered Clock Output
12	VDPECL1	Digital Supply—Clock and Data Output Drivers
13	RXDATAOUT	Differential Recovered Data Output
14	RXDATAOUTN	Differential Recovered Data Output
15	VDN1	Digital Ground—Synthesizer Logic
16	VDPECL2	Digital Supply—Synthesizer Driver
17	TXCLKOUT	Differential Synthesized Clock Output
18	TXCLKOUTN	Differential Synthesized Clock Output
19	VDP1	Digital Supply—Synthesizer Logic
20	CFS1	Synthesizer Loop Filter Capacitor
21	CFS2	Synthesizer Loop Filter Capacitor
22	VAP2	Analog Supply—Synthesizer & Oscillator
23	ECLFREFINN	Differential ECL Input to Synthesizer
24	ECLFREFIN	Differential ECL Input to Synthesizer
25	FREFIN	CMOS/TTL Input to Synthesizer
26	OSCOUT	Crystal Oscillator CMOS/TTL Output
27	VDP2	Digital Supply—Oscillator Output
28	VDN2	Digital Ground—Oscillator Output
29	XTALIN1	Crystal Connection
30	XTALIN2	Crystal Connection
31	VAN2	Analog Ground—Synthesizer and Oscillator
32	DRIVEINN	Line Driver Differential ECL Input
33	DRIVEIN	Line Driver Differential ECL Input
34	VDN3	Digital Ground—Line Driver
35	TXAMPSET	Line Driver Output Current Control
36	VDP3	Digital Supply—Line Driver
37	TX	Line Driver Collector Output
38	TXN	Line Driver Collector Output
39	DRVROFF	Line Driver Disable (CMOS/TTL)
40	RXCLKSEL	Synthesizer Frequency Reference Select
41	LBSELECT	Loop-Back Select
42	DRBYPASS	Data Retiming Bypass
43	RX	Differential Equalizer Input
44	RXN	Differential Equalizer Input

DEFINITION OF TERMS

Maximum, Minimum and Typical Specifications
Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations: if the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guardbanded to account for tester variation to guarantee that no device is shipped outside of data sheet specifications.

Signal Detect: Response Time
Response time is the delay between removal of a dc-coupled input signal (at RX & RXN) and indication of loss of signal (LOS) at SDOUT.

Clock Recovery PLL: Static Phase Error
This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error and IC input and output signals prohibit direct measurement of static phase error.

Data Transition Density, ρ
This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to bit periods. The 2^{23}–1 PRN input data pattern has $\rho = 1/2$.

PLL Jitter
This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms or Unit Intervals (UI).

Output Jitter
This is the jitter on the clock recovery PLL or frequency synthesizer PLL output clock, in degrees rms, due to a specific pattern or some pseudo random input data sequence (PRN sequence).

Jitter Transfer
The clock recovery PLL and frequency synthesizer PLL both exhibit a low-pass filter response to jitter applied to their respective inputs.

Bandwidth
This describes the frequency at which the clock recovery PLL or frequency synthesizer PLL attenuate sinusoidal input jitter by 3 dB.

Frequency Synthesizer PLL: Duty Cycle Tolerance
The frequency synthesizer PLL exhibits a duty cycle tolerance that is measured by applying an input signal (nominal input frequency) with a known duty cycle imbalance, and then measuring the output frequency and jitter.

Time Constant
The Frequency Synthesizer PLL time constant (800 ns = 1/bandwidth) determines the output frequency drift after switching the reference frequency input. The time constant works to smooth the output frequency response to change in reference input guaranteeing no runt pulses at the output.

Crystal Oscillator
The AD6816 integrated oscillator circuit is specified to provide a 19.44 MHz output frequency with ±100 ppm frequency accuracy using a 19.44 MHz ±50 ppm series mode crystal with series resistance less than 40 Ω.

A series mode crystal oscillator is used instead of the more common parallel mode circuit. The primary advantage of the series mode oscillator is that shunt capacitance has no effect since the crystal presents a low impedance at resonance. All the accuracy inherent in the crystal can be achieved by the series mode circuit. In contrast, the parallel mode circuit requires a trimmer capacitor shunt to the crystal to compensate stray capacitances. In addition, these stray and trim capacitances must be stable over temperature for high accuracy. Crystal vendors easily supply either type of crystal. It is necessary to specify that a series mode crystal is needed.

Oscillator Circuit: Duty Cycle
Duty cycle is calculated as (100 × on time)/period, where on time equals the time the clock signal is greater than the midpoint between its "0" level and its "1" level.

Line Driver Differential Input (Refer to Figure 2)
The line driver is specified to provide output current variation less than 1% with a 3 V input common-mode signal and a differential input signal between 150 mV and 1 V p-p.

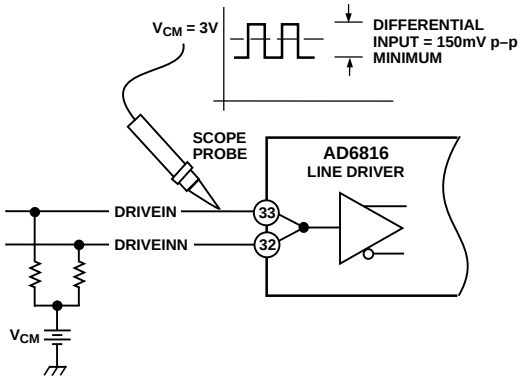


Figure 2. Line Driver Differential Input (Single-Ended Measurement Shown)

AD6816–Typical Characteristic Curves

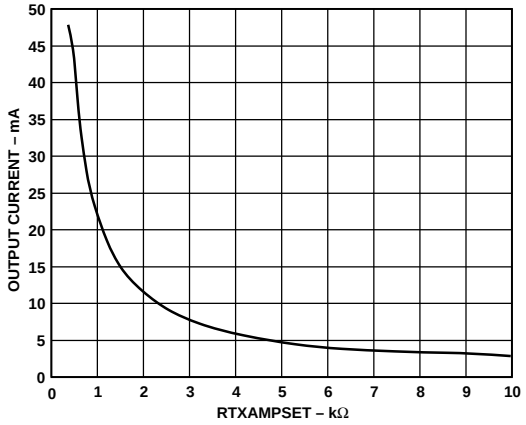


Figure 3. Line Driver Output Current vs. $R_{TXAMPSET}$

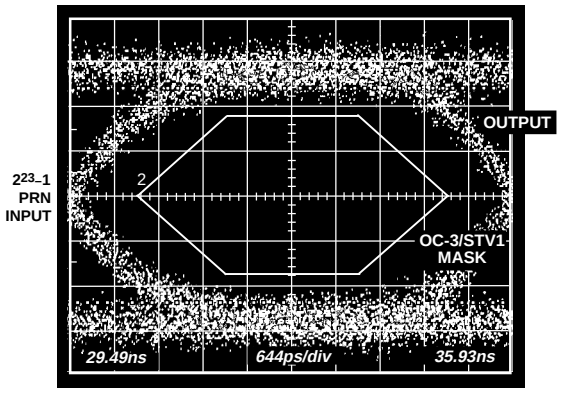


Figure 6. Line Driver Eye Diagram (Measurement at XFMR Output)

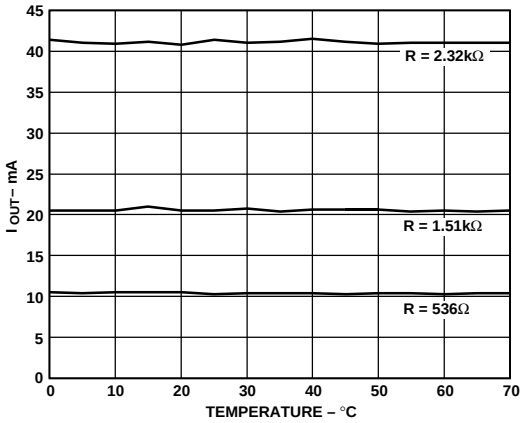


Figure 4. Line Driver Output Current vs. Temperature

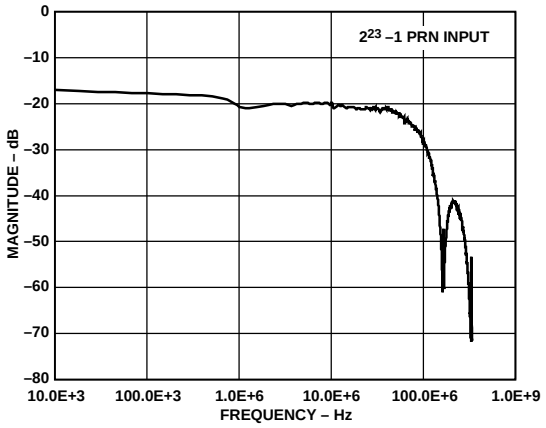


Figure 7. Line Driver Output Frequency Spectrum (Measurement at XFMR Output)

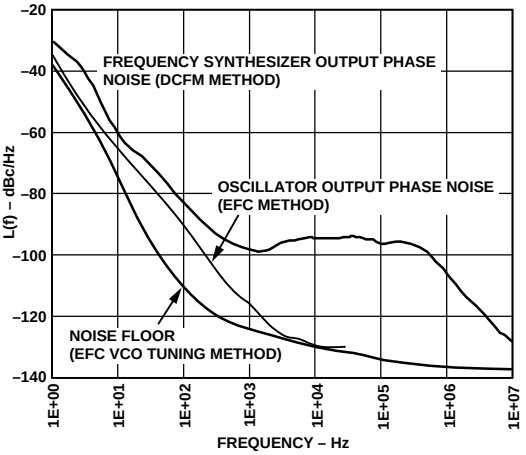


Figure 5. Oscillator Circuit and Frequency Synthesizer Phase Noise

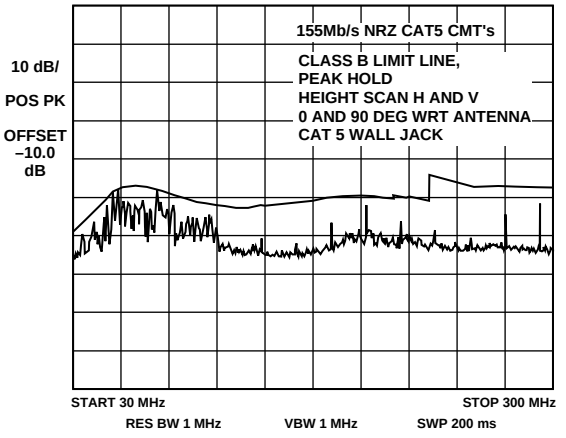


Figure 8. UTP #5 Emissions & FCC Class B Limit Line

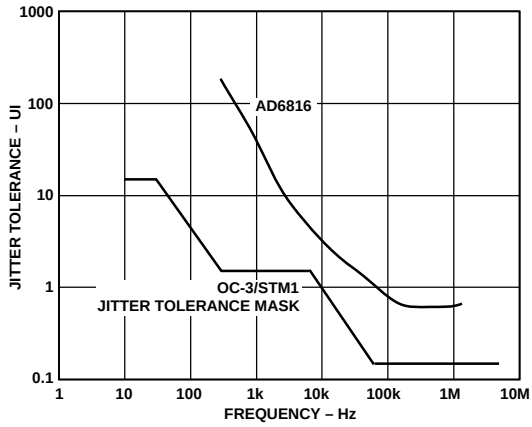


Figure 9. Clock Recovery PLL Jitter Tolerance

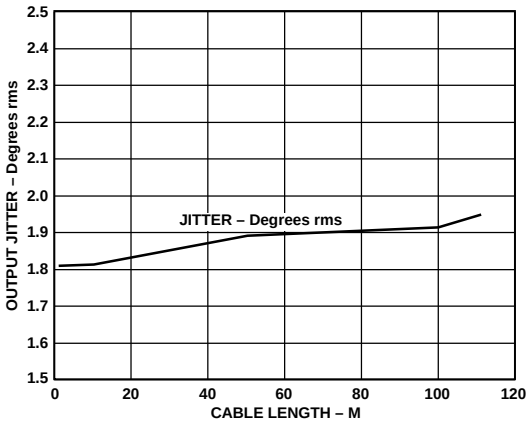


Figure 12. Receive Channel Output Jitter vs. Cable Length (Measured at RXCLKOUT/N)

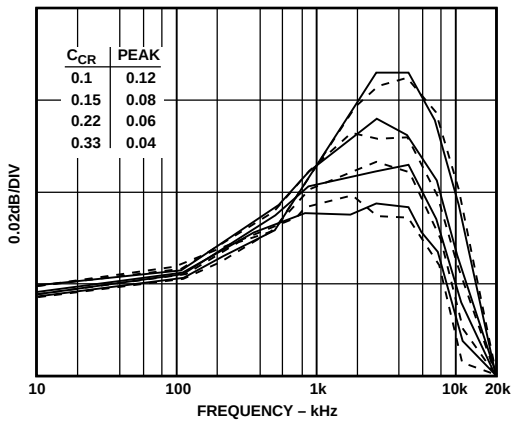


Figure 10. Clock Recovery Jitter Transfer vs. C_{CR}

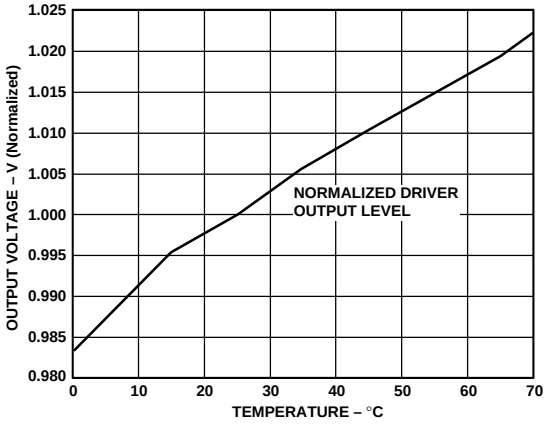


Figure 13. Driver Output Level vs. Temperature (Normalized to 1 V @ +25°C)

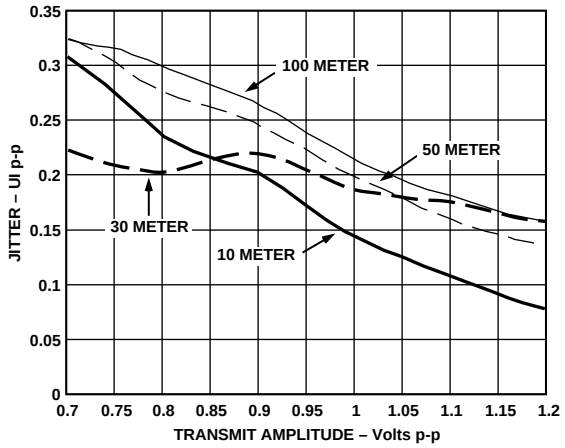


Figure 11. Equalize Jitter vs. Transmit Amplitude

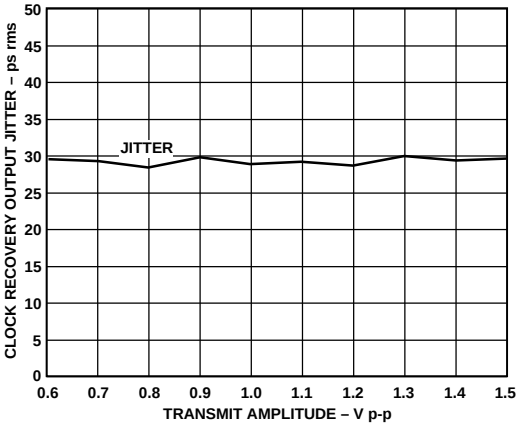
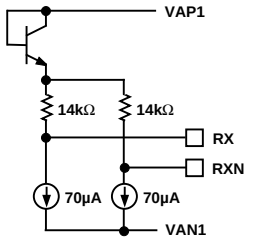
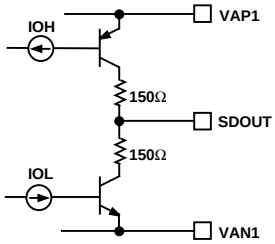


Figure 14. Receive Channel Output Jitter vs. Transmit Amplitude (2E7-1 PRN Data Input into 100 M UTP#5 Cable)

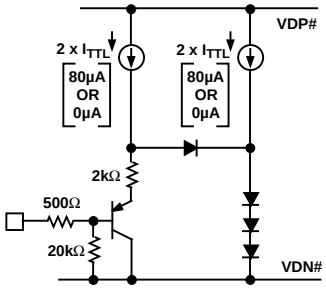
Receiver Differential Input Stage



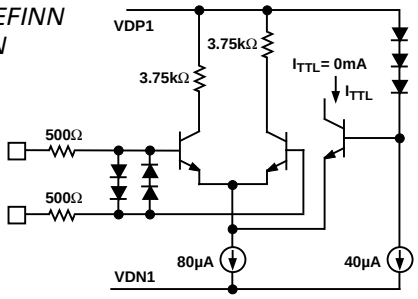
Receiver Signal Detect Output (SDOUT)



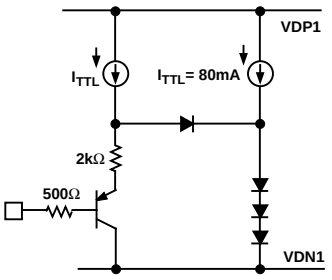
Control Signal Input (LBSEL, DRBYPASS, TXSALVESEL,DRVROFF)



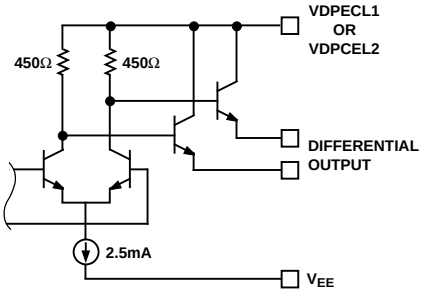
Frequency Synthesizer ECLFREFIN/ECLFREFINN PECL Input (FREFIN @ V_{EE})



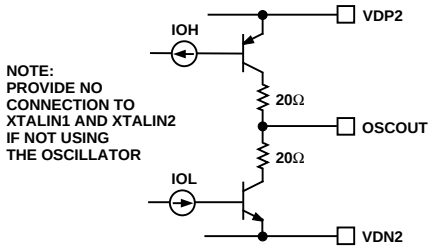
Frequency Synthesizer FREFIN TTL/CMOS Input (ECLFREFIN & ECLFREFINN @ V_{EE})



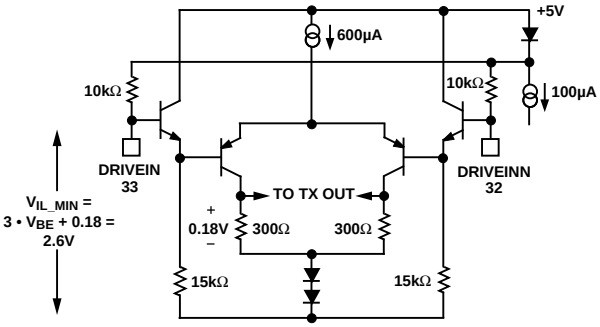
Frequency Synthesizer PLL and Clock Recovery PLL Differential Output Stage TXCLKOUT/TXCLKOUTN, RXCLKOUT/RXCLKOUTN, RXDATAOUT/RXDATAOUTN



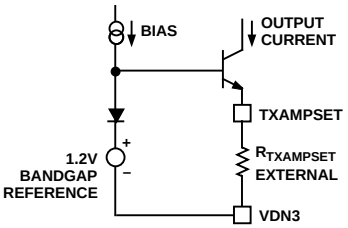
Oscillator Circuit OSC OUT



Line Driver DRIVEIN/DRIVEINN



Line Driver TXAMPSET Output Current Control



Line Driver TX/TXN Output

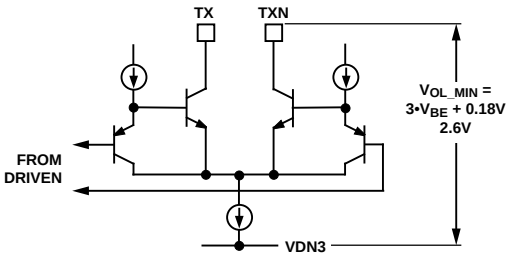


Figure 15. Simplified Schematics

THEORY OF OPERATION

Line Driver

The line driver accepts differential input data between 100 mV and 1.0 V peak (ac coupled or ECL common mode), and transmits the 155 Mbps NRZ data signal through a transformer and up to 110 M of Category #5 Unshielded Twisted Pair cable (UTP#5) per ATM Forum UNI 3.1 requirements. The user sets output current, I_{OUT}, between 4 mA and 40 mA (cable removed and 100 Ω resistor across transformer) with a single external resistor. A 1.0 V p-p output signal is obtained with an I_{OUT} of 20 mA, corresponding to an $R_{TXAMPSET}$ = 1114 Ω. Generally, I_{OUT} = 22.3 / $R_{TXAMPSET}$.

The line driver does not share any power supplies or biases with other blocks of the AD6816. This, and techniques used to stabilize the effective beta of transistors during switching, keeps output common mode current to < 3%.

Crystal Oscillator

The oscillator circuit works with a 19.44 MHz ±50 ppm series mode crystal to provide a TTL level 19.44 MHz ±100 ppm clock output without needing adjustment. Start-up is guaranteed for crystals with series mode resistance ≤ 40 Ω. Typical start-up time for a crystal with series mode resistance is 2 ms. Power in the crystal is limited to 1 μW rms.

Synthesizer Phase-Locked Loop

The synthesizer PLL provides a 155 MHz PECL output clock from a 19.44 MHz or 9.72 MHz reference frequency. The synthesizer PLL automatically selects ×8 or ×16 synthesis, based on the frequency present at FREFIN(N) pins. A signal multiplexer at the synthesizer PLL input allows the user to select a 19.44 MHz reference frequency derived from the 155.52 MHz recovered clock (loop timing application) or an independent reference frequency. The device can be configured to support a PECL/TTL/CMOS-level reference frequency.

The synthesizer PLL gives phase continuous switching between independent and loop timing. The 200 kHz time constant of the PLL smooths the clock output response due to an instantaneous change in frequency at its input (as in the case of a switch between loop timing and independent timing). This guarantees no runt clock pulses due to switching timing references.

Receiver (Equalizer, Baseline Restoration and Loss of Signal Detect Circuits)

The Receiver processes an NRZ data stream from a transformer and up to 110 M of Category #5 Unshielded Twisted Pair cable (UTP#5)**.** The receiver (Figure 16) consists of an adaptive equalizer, a baseline restore loop and a loss of signal (LOS) detector. The adaptive equalizer compensates for intersymbol interference and distortion caused by the cable. The baseline restore loop corrects for base line wander due to the transformer. The LOS detector indicates a cable break.

The incoming data chooses either the high pass path, shown as E(s), the straight path or some combination of both. The strength of each path is determined by the control variable, *x*.

The loop works by comparing the amplitude of the equalizer output to the expected value. If the amplitude is too small, the signal is underequalized and the control variable *x* is decreased to choose more of the high pass path. The signal is equalized when the output amplitude equals the reference value. The time constant of the loop is slow enough so that the equalization remains constant if the signal amplitude decreases due to the absence of transitions.

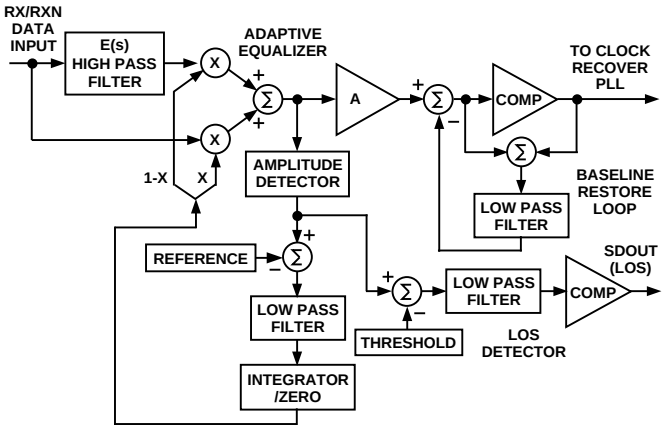


Figure 16. Receiver (Equalizer, Baseline Restoration, Signal Level Detect) Block Diagram

The baseline restore loop also compensates for the baseline wander caused by the transformer (ac coupling) used to terminate the cable. This loop adjusts the slice level of the data signal for lengthy transitionless data runs to ensure that no bit errors are made upon new transitions. This loop also compensates for a dc offset that could be created by the transformer processing non- 50% duty cycle, repetitive data patterns (baseline wander). The circuit works by subtracting the comparator input signal from the output signal. The error signal output of the subtracter is added to offset the incoming signal and to keep the average value equal to the average output. If the equalizer output goes to zero, this loop will servo the comparator input to the last logic level.

The LOS detector monitors the output amplitude of the equalizer and trips when it falls below a predetermined threshold. The low-pass filter is slow enough that the detector will not trip for less than 800 missing edges.

Clock Recovery Phase-Locked Loop

The phase-locked loop recovers clock and retimes data from NRZ data. The architecture uses a frequency detector to aid initial frequency acquisition; refer to Figure 17 for a block diagram. Note that the frequency detector is always in the circuit. When the PLL is locked, the frequency error is zero and the frequency detector has no further effect. Since the frequency detector is always in the circuit, no control functions are needed to initiate acquisition or change mode after acquisition.

The frequency detector delivers pulses of current to the charge pump to either raise or lower the frequency of the VCO. During the frequency acquisition process the frequency detector output is a series of pulses of width equal to the period of the VCO. These pulses occur on the cycle slips between the data frequency and the VCO frequency. With a maximum density data pattern (1010. . .), every cycle slip will produce a pulse at the frequency detector output. With random data, however, not every cycle slip produces a pulse. The density of pulses at the frequency detector output increases with the density of data transitions. The probability that a cycle slip will produce a pulse increases as the frequency error approaches zero. After the frequency error has been reduced to zero, the frequency detector output will have no further pulses. At this point the PLL begins the process of phase acquisition, with a settling time of roughly 2000 bit periods.

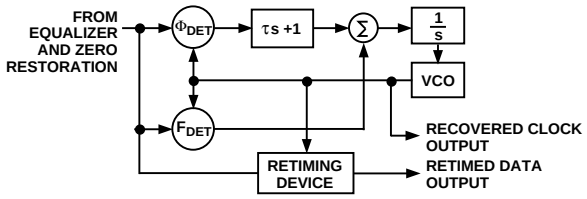


Figure 17. PLL Block Diagram

Jitter caused by variations of density of data transitions (pattern jitter) is virtually eliminated by use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCO phase to increase to above the average run rate set by the data frequency. The jitter created by a 2^7-1 pseudo random code is 1/2 degree; this is small compared to random jitter.

The jitter bandwidth for the PLL is 0.07% of the center frequency. This figure is chosen so that sinusoidal input jitter at 110 kHz will be attenuated by 3 dB.

The damping ratio of the PLL is user programmable with a single external capacitor. At 155 MHz, a damping ratio of 5 is obtained with a 0.15 µF capacitor. More generally, the damping ratio scales as $(f_{DATA} \times C_D)^{1/2}$.

A lower damping ratio allows a faster frequency acquisition; generally the acquisition time scales directly with the capacitor value. However, at damping ratios approaching one, the acquisition time no longer scales directly with capacitor value. The acquisition time has two components: frequency acquisition and phase acquisition. The frequency acquisition always scales with capacitance, but the phase acquisition is set by the loop bandwidth of the PLL and is independent of the damping ratio. Thus, the 0.07% fractional loop bandwidth sets a minimum acquisition time of 2000 bit periods. Note the acquisition time for a damping factor of one 15,000 bit periods. This comprises 13,000 bit periods for frequency acquisition and 2,000 bit periods for phase acquisition. Compare this to the 400,000 bit periods acquisition time for a damping ratio of 5; this consists entirely of frequency acquisition, and the 2,000 bit periods of phase acquisition is negligible.

While a lower damping ratio affords faster acquisition, it also allows more peaking in the jitter transfer response (jitter peaking). For example, with a damping ratio of 10 the jitter peaking is 0.02 dB, but with a damping ratio of 1, the peaking is 2 dB.

APPLICATIONS

Application with Fiber Optic Receivers/Transceivers

The AD6816 receiver (adaptive equalizer and baseline restore loop) can be configured to receive a signal from a fiber optic receiver or transceiver that provides full PECL or ECL outputs. By properly adjusting the common mode and amplitude level, the AD6816 receiver will be essentially transparent to the (P)ECL inputs. The common-mode input voltage should be between 1.5 V and 1.9 V referred to V_{CC}. The differential input amplitude should be between 0.7 V and 1.1 V. The common-mode issue can be addressed simply by ac coupling. The amplitude of the (P)ECL signal should be attenuated by two to meet the above requirement.

Figure 18 provides a simple solution that satisfies the above requirements as well as providing proper 50 Ω terminations for transmission lines when needed. The circuit also allows a convenient way to double pad a PC board for either fiber or copper cable applications.

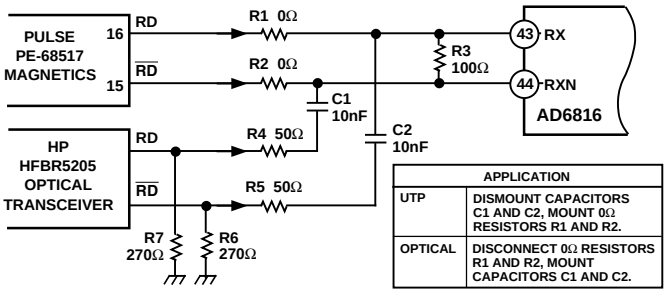


Figure 18. Fiber Optic Receiver PECL/ECL Output Interface to AD6816 Receiver Schematic

Generation of 19.44 MHz TTL-Level Byte Clock from 155.52 MHz Recovered Clock

Some applications require that a local master clock at 19.44 MHz be generated from the 155.52 MHz recovered clock. Figure 19 shows a circuit schematic for such an application. The circuit uses one ECL (PECL) IC to divide the recovered 155 MHz clock by eight, and one ECL/TTL converter IC to deliver the 19.44 MHz TTL output.

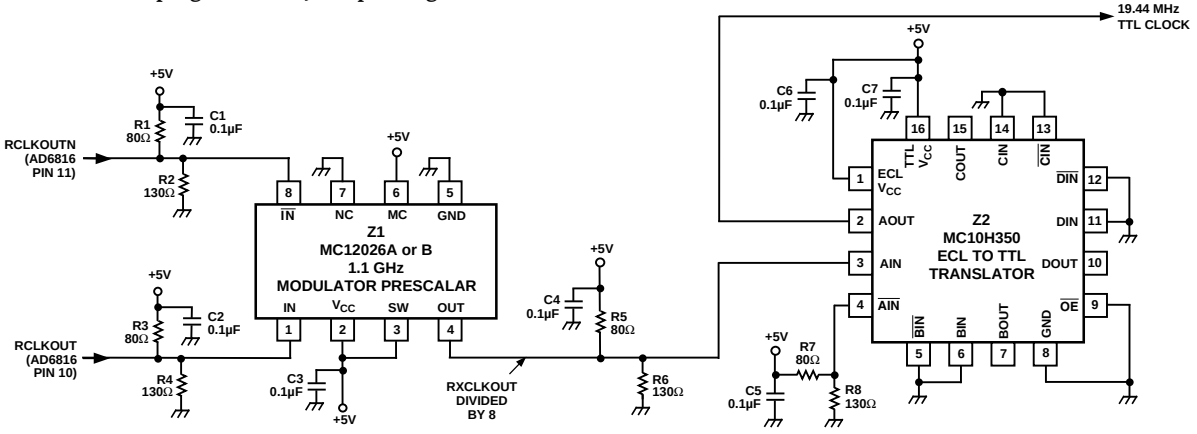


Figure 19. Generation of 19.44 MHz TTL-Level Byte Clock from 155.52 MHz Recovered Clock-Circuit Schematic

PECL Output Compatibility with ATM User–Network Interface IC Inputs

The PECL outputs (RXCLKOUT/N, RXDATAOUT/N) are more than adequate for driving UNI IC PECL inputs. A focus on PECL output specifications and on UNI IC PECL input dc characteristics, given below, demonstrates this.

The PECL output levels, specified in single-ended terms over 0°C to +70°C (V_{OH} and V_{OL}), should not be taken at face value. Since the output signals that V_{OH} and V_{OL} refer to are differentially processed (typical UNI IC "self-biased" PECL Inputs require ac coupling), the differential voltage swing between V_{OH} and V_{OL} determine compatibility. Simply combining the $V_{OH\ MIN}$ specification with the $V_{OL\ MAX}$ specification, however, confuses a compatibility analysis since both V_{OH} and V_{OL} track with temperature. This means $V_{OH\ MIN}$ and $V_{OL\ MAX}$ do not occur simultaneously, but at opposite temperature extremes (refer to Figure 20). Note that the differential voltage swing (V_{OH}–V_{OL}) remains $\geq$ 0.93 V over temperature.

Test results of identical PECL outputs over temperature reveal that minimum differential voltage swings at –40°C and at +85°C equal 0.72 V and 0.81 V, respectively (with 6σ confidence).

Typical UNI ICs have $V_{IH\ MIN}$ and $V_{IL\ MAX}$ dc specifications that require differential drive ($V_{IH\ MIN}$–$V_{IL\ MAX}$) $\geq$ 0.4 V. One UNI IC has $V_{IH\ MIN}$ and $V_{IL\ MAX}$ specifications that require differential drive $\geq$ 0.6 V. The AD6816 PECL outputs have the differential swing (0.72 V minimum) to drive these UNI ICs comfortably, and with adequate margin.

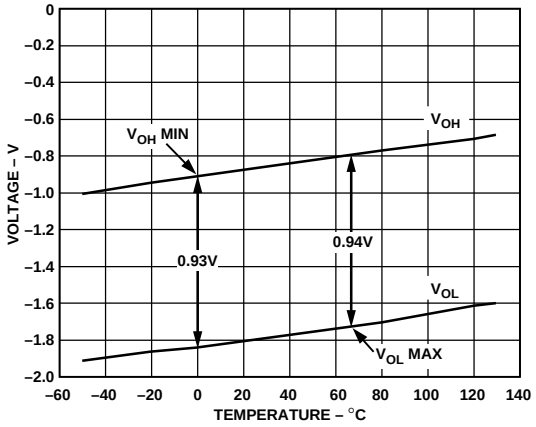


Figure 20. PECL Output Levels–Simulation Graph

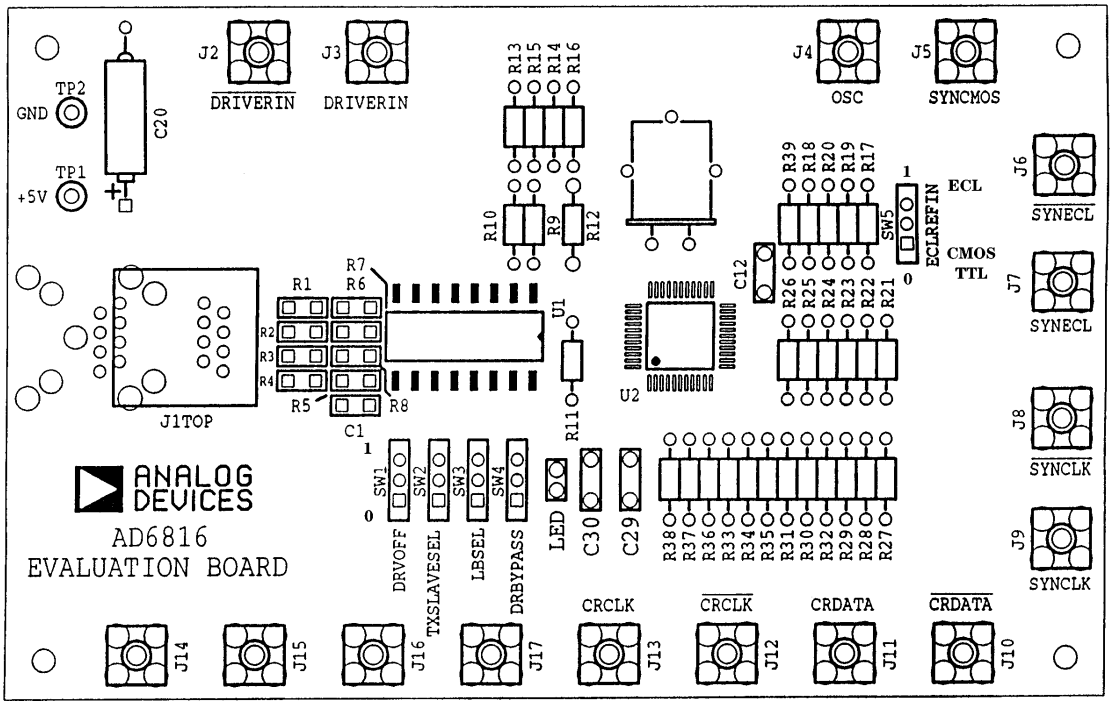


Figure 21. Evaluation/Test Circuit Assembly Drawing

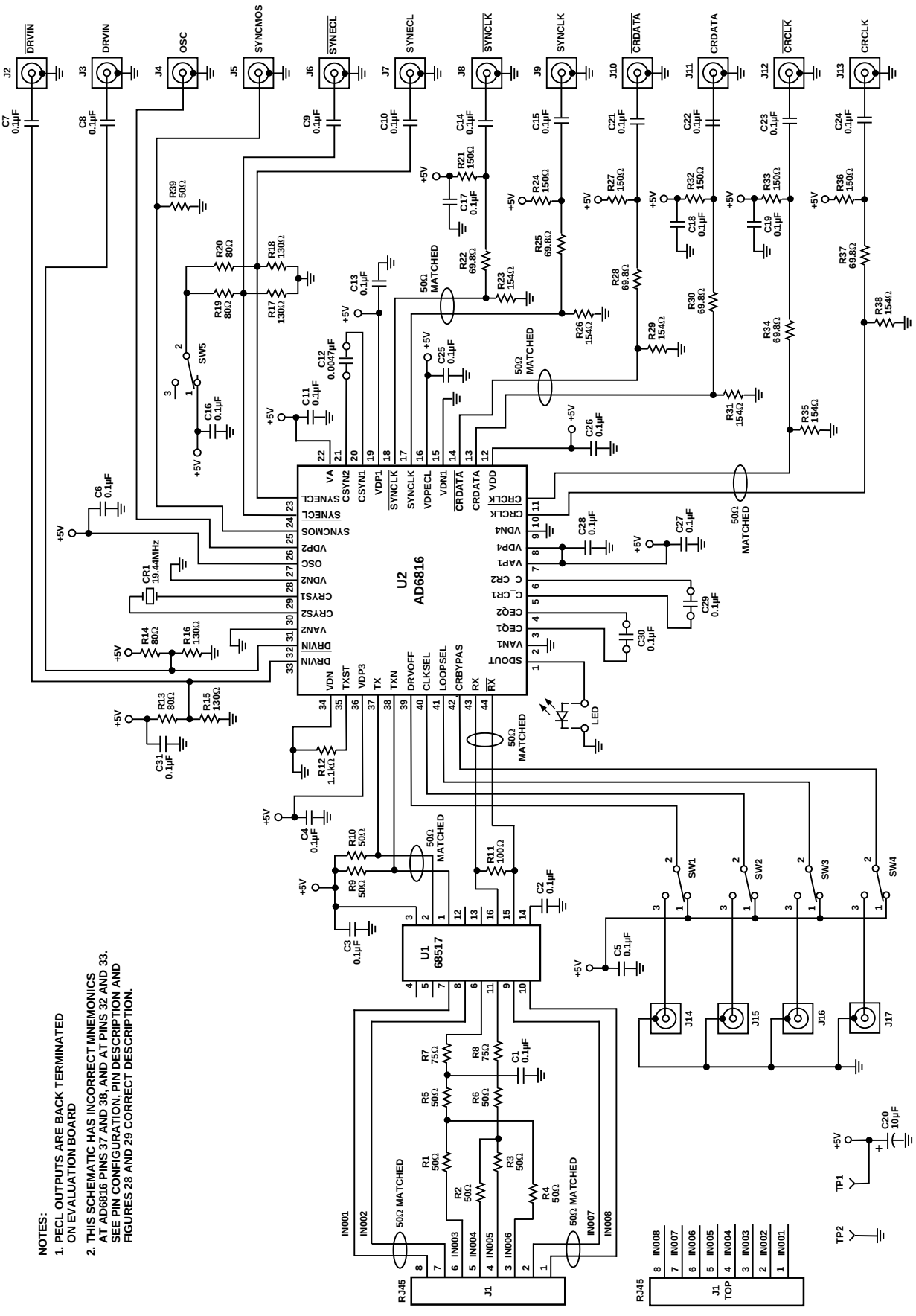


Figure 22. Evaluation/Test Circuit Schematic

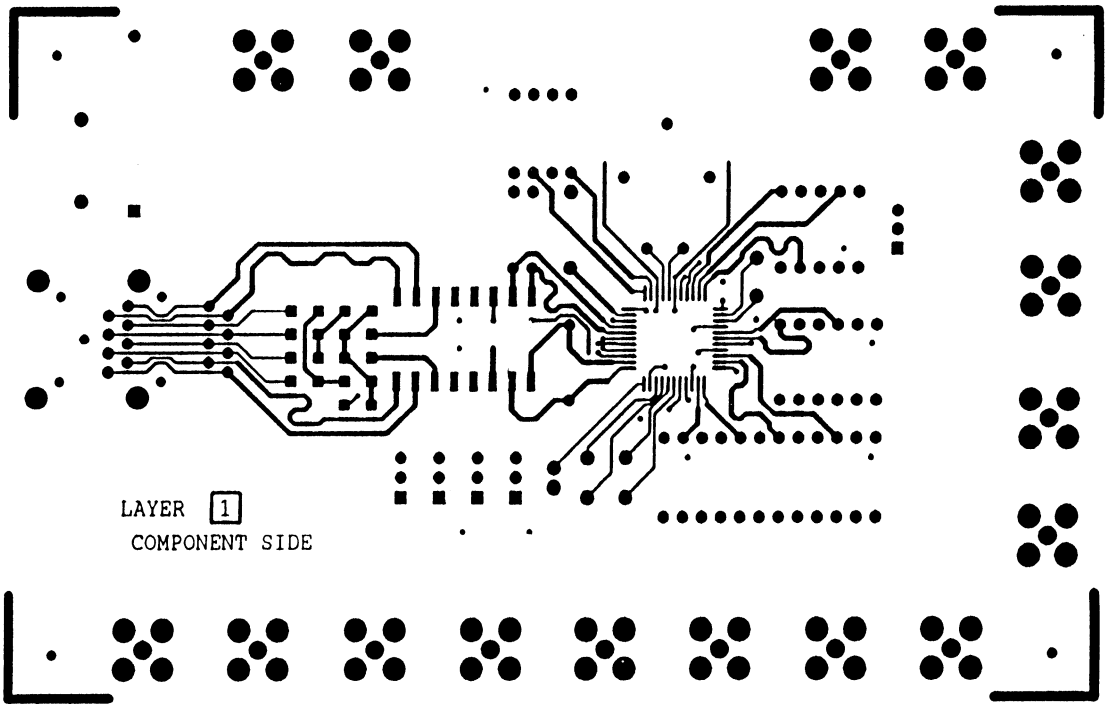


Figure 23. Evaluation/Test Circuit PCB Layer 1 Signal Traces

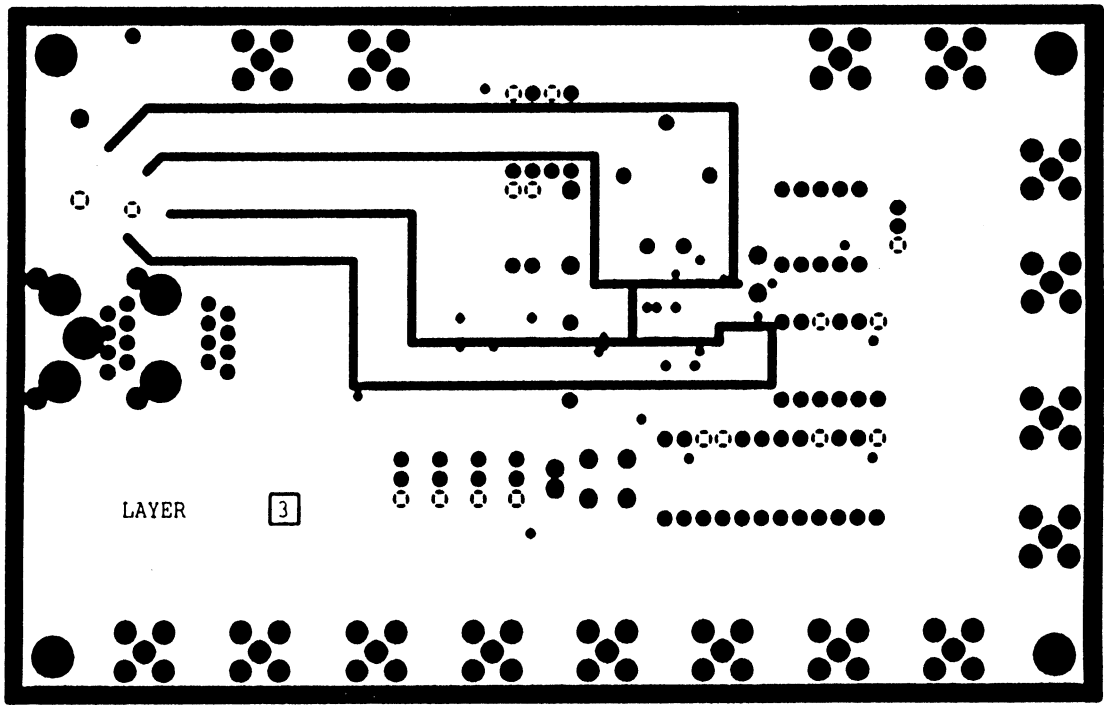
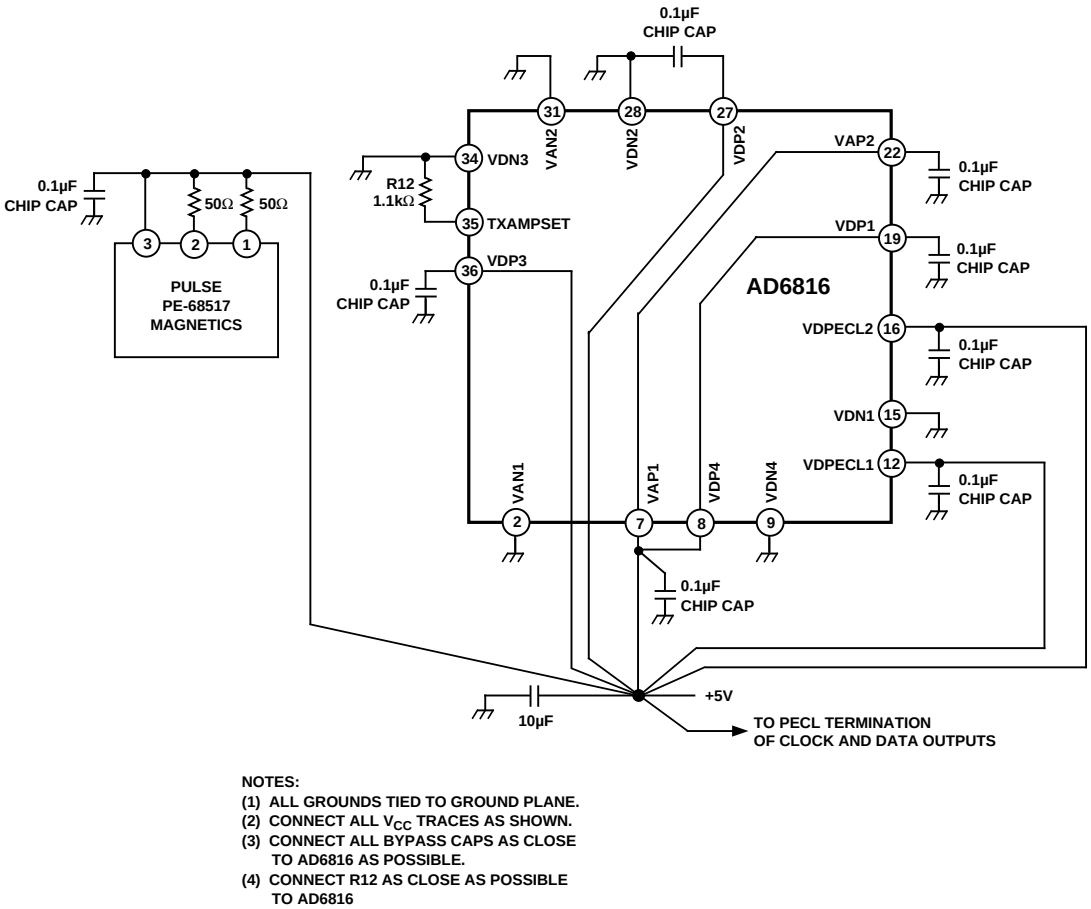


Figure 24. Evaluation/Test Circuit PCB Layer Three Power Plane



NOTES:
(1) ALL GROUNDS TIED TO GROUND PLANE.
(2) CONNECT ALL V_{CC} TRACES AS SHOWN.
(3) CONNECT ALL BYPASS CAPS AS CLOSE TO AD6816 AS POSSIBLE.
(4) CONNECT R12 AS CLOSE AS POSSIBLE TO AD6816

Figure 25. Power and Ground Recommendations

Using the AD6816 to Interface ATM to Optical and Electrical Media: Examples

Example 1: ATM UNI PHY Layer(s) Using AD6816 & IgT WAC-013 (or IgT WAC-413)

The following system implementation examples show how to implement a 155 Mbps ATM User Network Interface (UNI) to Category #5 Unshielded Twisted Pair cable (UTP#5) using the AD6816 and either the IgT WAC-013 ATM UNI Processor (single channel) or the IgT WAC-413 Quad ATM UNI Processor (four channels). Contact Integrated Telecom Technology (IgT), Gaithersburg, MD, US, (301)990-9890, for information on the WAC-013 or WAC-413 devices beyond that provided below.

Figures 26 and 27 show generic block diagrams of the single channel and four channel ATM PHY interface circuit. The ATM PHY interface circuit is made up of a Physical Medium Dependent (PMD) block and a Transmission Convergence (TC) block. The PMD interface block provides the digital baseband communication between ATM user devices and ATM network equipment. The TC block interfaces with the PHY layer aspects that are independent of the transmission medium characteristics.

The PMD blocks for these applications use the AD6816 which provides the UTP#5 line interface (Tx: Line Driver, Rx: Equalizer & Baseline Restoration) and provides an interface to the TC Layer (Tx: 155 MHz Transmit Clock, Rx: 155 MHz Recovered Clock and 155 Mbps Retimed Data).

The TC block for these applications use the IgT WAC-013 (single channel) or the IgT WAC-413 (four channel). These devices process and generate ATM cells over SONET/ SDH frames.

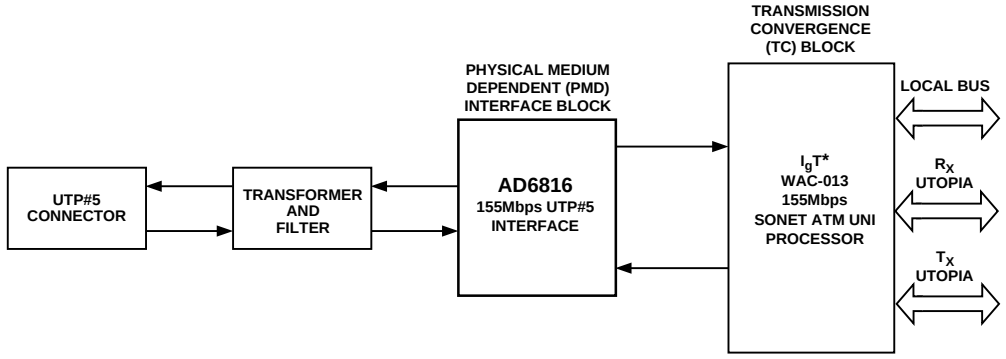


Figure 26. Single Channel ATM PHY Block Diagram (AD6816 with IgT WAC-013)

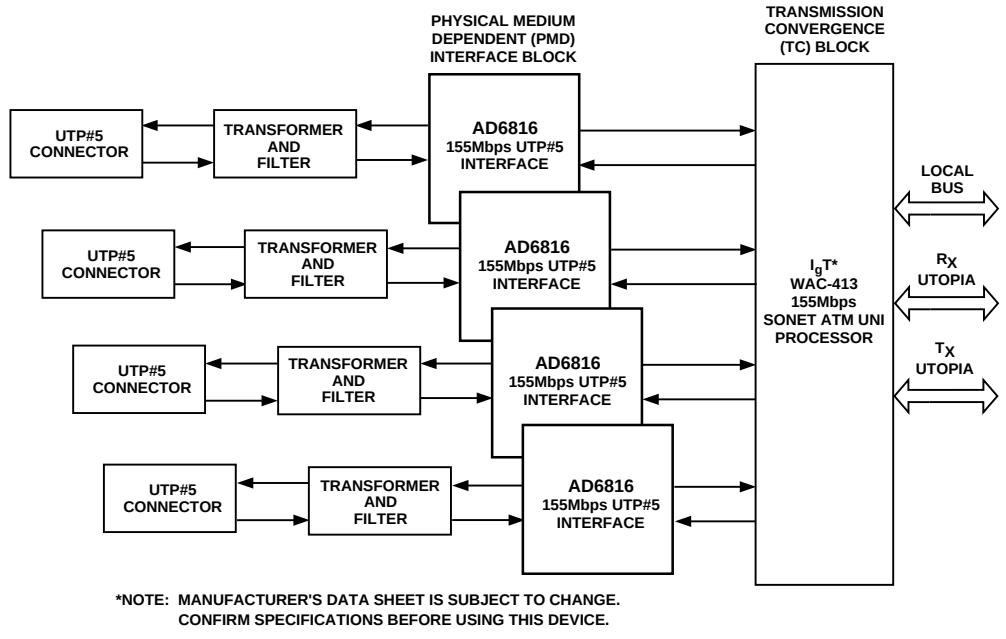


Figure 27. Four Channel ATM PHY Block Diagram (AD6816 with IgT WAC-413)

Single Channel ATM UNI PHY

Figure 28 shows a more detailed block diagram of the single channel application. The AD6816 provides the WAC-013 with a 155 MHz Tx clock at PECL levels. The WAC-013 processes 155 Mbps Tx data directly from this 155 MHz clock. The WAC-013 generates 155 Mbps differential NRZ data at CMOS levels. These differential data output signals data are PECL-level translated using the 3-resistor network (refer to Figure 25). The AD6816 processes the NRZ data through its line driver. The line driver output data is processed through an external low-pass filter and transformer before entering the RJ45 connector.

In the receive section, the NRZ data enters the RJ45 connector and passes through an isolation transformer and band-limiting filter. The adaptive equalizer in the AD6816 compensates for the amplitude and phase distortion incurred from up to 110M UTP#5. The AD6816 baseline restoration loop compensates for the dc wander that the transformer introduces to its input data. Once the signal has been equalized and had its dc level restored, the AD6816 recovers clock and retimes data. The AD6816 differential recovered clock signal and retimed differential data are fed directly to the WAC-013.

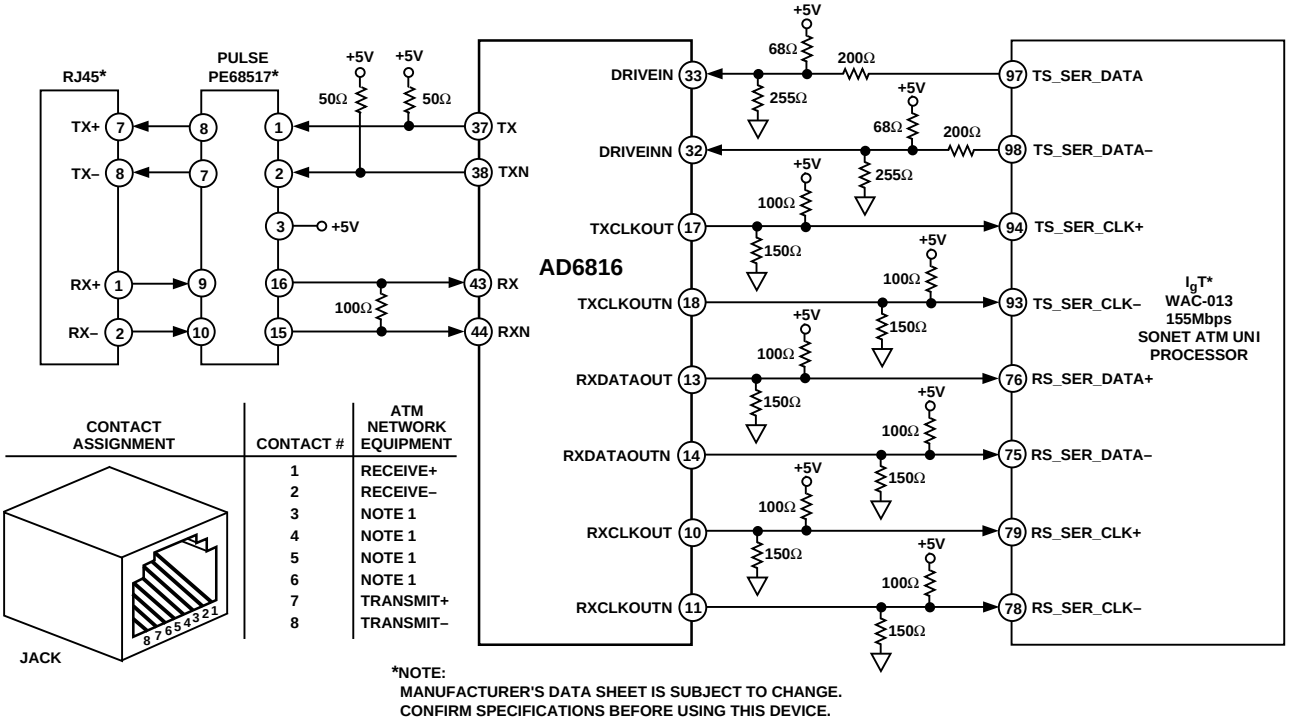


Figure 28. UTP#5 Application with IgT WAC-013

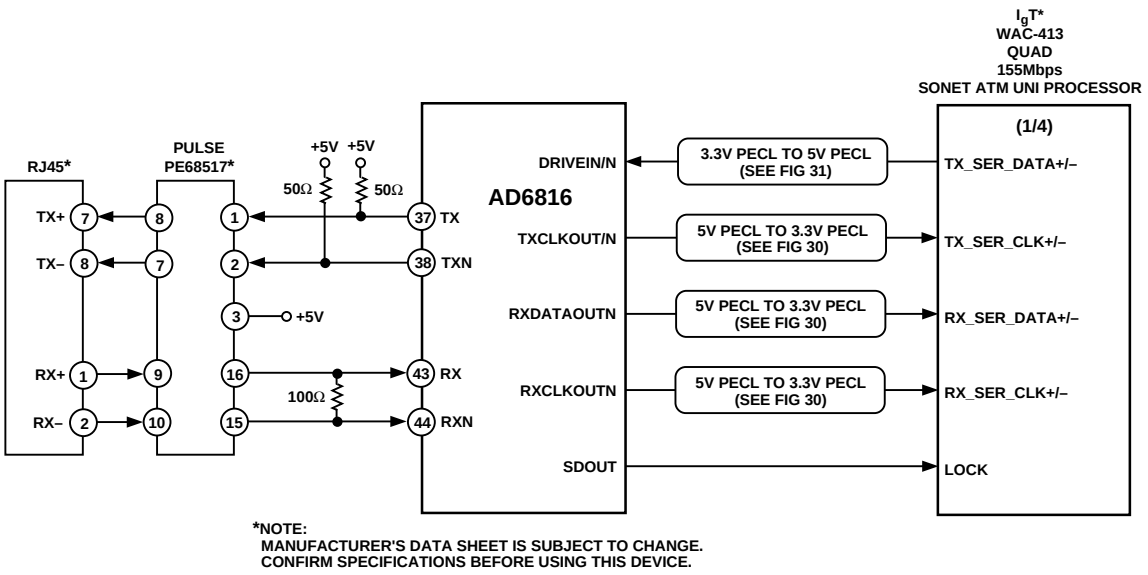


Figure 29. UTP#5 Application with IgT WAC-413

Four-Channel ATM UNI PHY

Figure 29 shows a block diagram of the AD6816 and one channel of the IgT WAC-413 Quad ATM UNI Processor. The AD6816 provides the WAC-413 with a 155 MHz Tx clock at 5 V PECL levels. The 5 V PECL levels are level-shifted using a 3-resistor network (Figure 30) to drive the WAC-413 TX_SER_CLK ± inputs. The WAC-413 processes 155 Mbps data directly from this 155 MHz clock. The WAC-413 generates 155 Mbps differential NRZ data at 3.3 V PECL levels. The 3.3 V PECL signals are level-shifted to 5 V PECL using a 3-resistor network (Figure 31) to drive the AD6816 line driver. The AD6816 processes the NRZ data through its line driver. The line driver output data is processed through an external low-pass filter and transformer before entering the RJ45 connector.

In the receive section, the NRZ data enters the RJ45 connector and passes through an isolation transformer and band-limiting filter. The adaptive equalizer in the AD6816 compensates for the amplitude and phase distortion incurred from up to 110M UTP#5. The AD6816 baseline restoration loop compensates for the dc wander that the transformer introduces to its input data. Once the signal has been equalized and had its dc level restored, the AD6816 recovers clock and retimes data. The AD6816 produces a 5 V PECL differential recovered clock signal and a 5 V PECL retimed differential data signal that get level shifted using a three resistor network (Figure 30) to drive the WAC-413 RX_SER_CLK± and RX_SER_DATA± inputs, respectively.

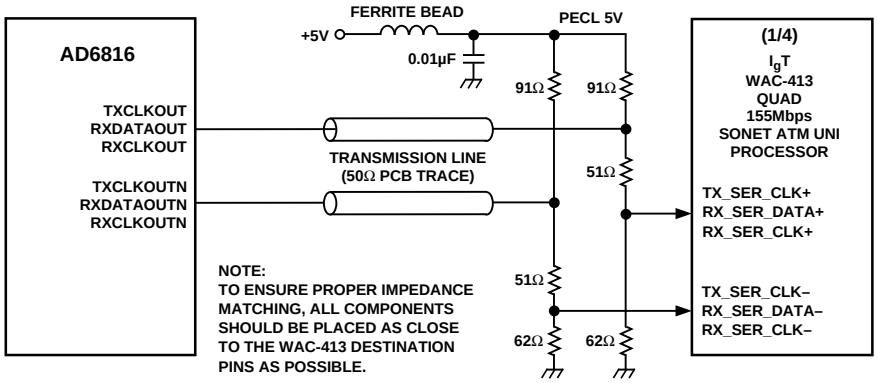


Figure 30. AD6816 5 V PECL to WAC-413 3.3 V PECL Resistor Network

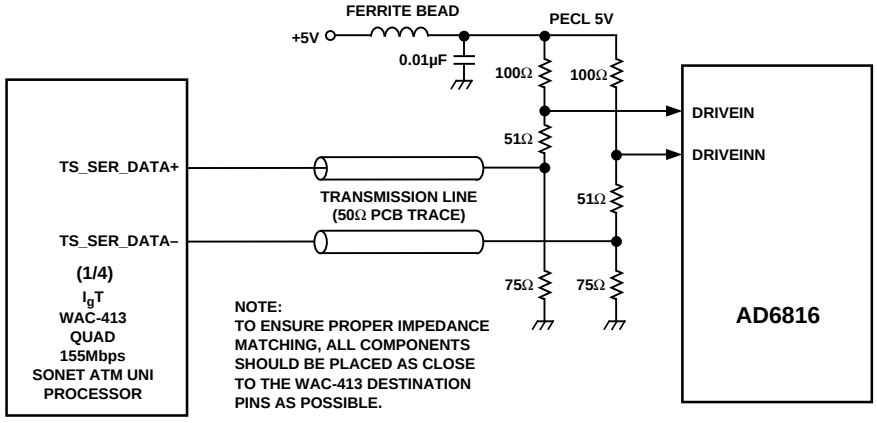


Figure 31. WAC-413 3.3 V PECL to AD6816 5 V PECL Resistor Network

5 V PECL to 3.3 V PECL Interface Analysis
The following three equations must be satisfied for this interface (in the following example: R_H = Resistor connected to PECL 5 V, R_M = Resistor connected between termination line and destination pin, and R_L = Resistor connected to ground):

1. Termination Impedance must match trace impedance:

   $Termination\ impedance = (R_H \times (R_M + R_L))/(R_H + R_M + R_L) = 50\ \Omega.$

2. Resistors need to provide the correct voltage levels:

   $(V_{SOURCE} - V_{TERM_DESTINATION})/R_M = V_{TERM_DESTINATION})/R_L,$

   where V_{SOURCE} = 3.67 V (PECL 5 V midpoint) and $V_{TERM_DESTINATION}$ = 2.0 V PECL 3.3 V midpoint).

3. Desired driver current of 25 mA:

   $I_{DRIVE} = [(4 - V_{DEST_HIGH})/R_M] - [(5–4)/R_H],$

   where $V_{DEST_HIGH} = (4 \times R_L)/(R_M + R_L)$ and I_{DRIVE} = 0.025.

The midpoints are used to ensure that the waveforms are centered at the critical levels. The waveform is attenuated at the destination because of the voltage divider. Rounding the resistor values to the nearest standard 5% resistors results in the circuit of Figure 30. A 3.2 V to 4.0 V input swing into this circuit creates an output swing between 1.8 V and 2.2 V.

3.3 V PECL to 5 V PECL Interface Analysis
The common-mode rejection area of the AD6816 line driver input requires the input signal voltage swing to be above 2.6 V. This is lower than standard PECL and helps simplify the termination resistor network (less driver current is required). In the following example: R_H = Resistor connected to PECL 5 V, R_M = Resistor connected between termination line and destination pin, and R_L = Resistor connected to ground). The following three equations need to be satisfied for this interface:

1. The voltage swings need to be centered at the correct voltage levels:

   $(5 - V_{MID_DESTINATION})/R_H = (V_{MID_DESTINATION} - V_{MID_SOURCE})/R_M,$

   where $V_{MID_DESTINATION}$ = 3.0 V and V_{MID_SOURCE} = 2.0 V.

2. Termination Impedance must match trace impedance:

   $Termination\ impedance = (R_L \times (R_M + R_H))/(R_H + R_M + R_L) = 50\ \Omega.$

3. The voltage for the driver should be within 5% of 1.7 V for the proper swing:

   $V_{SOURCE} = (5 \times R_L)/(R_H + R_M + R_L),$

   where V_{SOURCE} = 1.7 V.

Using these equations, and rounding the resistor values to the nearest standard 5% resistors, results in the circuit of Figure 31. This circuit will result in a source voltage swing between 1.66 V and 2.4 V and a destination voltage swing between 2.79 V and 3.28 V. This exceeds the minimum required voltage swing, with plenty of margin.

4. Also, the current required by the driver must be less than 17 mA:

   $I_{DRIVE} = (2.4/R_L) - [(5 - V_{TERM_DESTINATION_HIGH})/R_H$

In this case, the current of the driver is 15 mA.

Example 2: 155 Mbps NIC (Fiber or UTP#5) Using AD6816 & Siemens* ATM Chip Set
The following circuit implementation example shows how to implement a 155 Mbps ATM Network Interface Card (NIC) to Fiber Optics or to Category #5 Unshielded Twisted Pair cable (UTP#5) using the AD6816 with the Siemens PXB 4240 Synchronous Digital Hierarchy Transceiver IC (SDHT) and the PXB 4110 Segmentation and Reassembly Element IC (SARE). Contact Siemens Semiconductor, Dusseldorf, Germany, (49) 203 74201 45 for information on the NIC implementation or PXB 4240/PXB 4110 chipset beyond the information provided below.

AD6816 Interface to Fiber or to UTP#5
The NIC is designed to interface to either Fiber (via a 1 × 9 Fiber Optic Transceiver) or to UTP#5 (via transformer assembly and RJ45 connector). The unused interface is disconnected by jumpers.

AD6816 Interface to Siemens SDHT
The AD6816 delivers both recovered clock (associated with the receive data) and transmit clock to the SDHT. The AD6816 recovers the receive clock from the data coming in via the fiber or the UTP#5 and generates the local clock from a 19.44 MHz quartz. The AD6816 provides the ability to create the local 155 MHz clock (system clock) from either the 19.44 MHz crystal, an 19.44 MHz PECL- or TTL-level signal, or the 155 MHz recovered clock.

The AD6816 high speed signal inputs and outputs operate at PECL levels. The Siemens SDHT is a 3.3 V CMOS device that uses IEEE LVDS levels (Low Voltage Differential Signal) for its high speed signal inputs and outputs. Refer to the paragraphs below and to Figures 33 and 34 for the description of the interface between the AD6816 and the Siemens SDHT IC.

SDHT/SARE/PCI Bus Interfaces
Interfacing to the PCI bus does not require any external components. Nor do the two UTOPIA interfaces between SARE and SDHT. SARE is master and drives the ATMCLK. The connection of the SDHT to the SARE's Local Bus Interface needs a piece of glue logic to adapt bus cycles.

*All trademarks are properties of their respective holders.

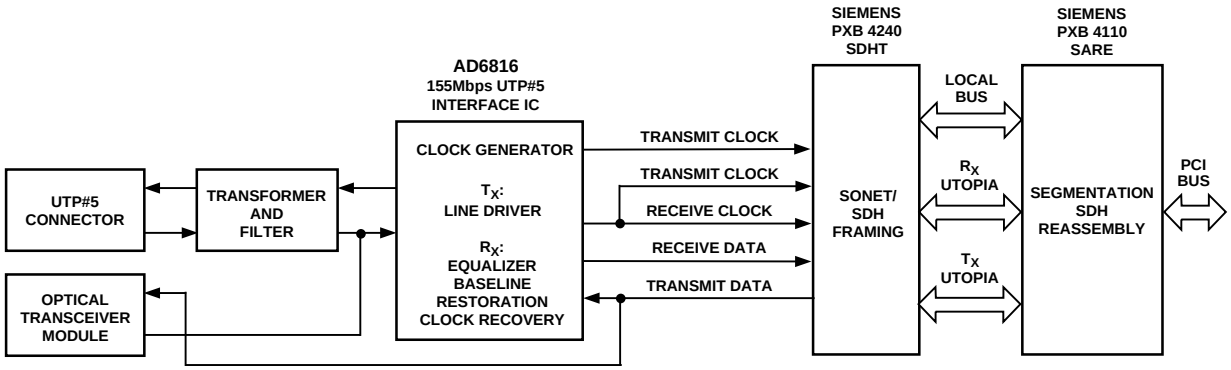
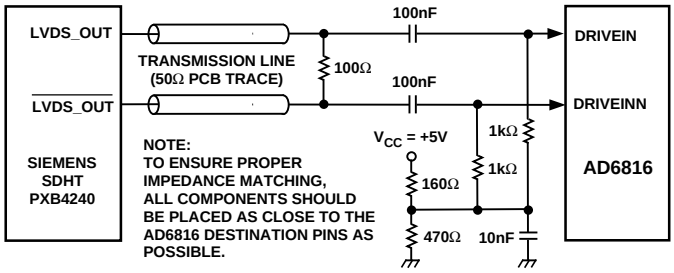


Figure 32. NIC Block Diagram: AD6816 with Siemens ATM Chipset

LVDS to PECL Conversion

LVDS levels from the Siemens SDHT can be shifted to PECL levels to the AD6816 using capacitive coupling (Figure 33). This scheme assumes the LVDS output drives the "long" portion of the transmission line. The passive shifting and termination network is located as close to the PECL input as possible.

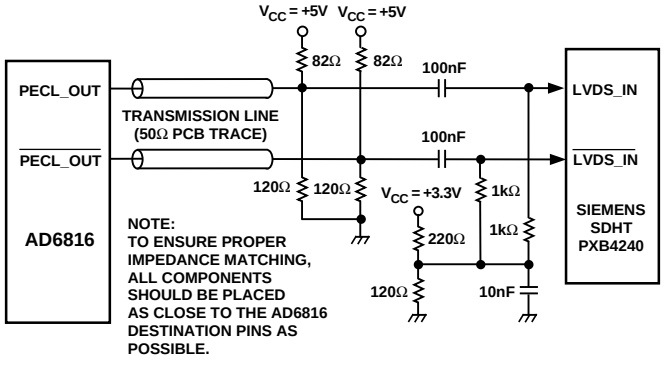


BRIEF ANALYSIS:
1. TERMINATION IS DONE BY THE 100Ω RESISTOR BETWEEN THE DIFFERENTIAL LINES.
2. THE 100nF CAPACITORS PROVIDE AC COUPLING TO THE SDHT OUTPUT.
3. THE RESISTOR DIVIDER GENERATES THE NEW OFFSET VOLTAGE (VBB, IN CENTER BETWEEN PECL VIH VIL) OF APPROXIMATELY 3.7V.
4. THE TWO 1kΩ RESISTORS ARE USED FOR DECOUPLING THE TWO SIGNALS.
5. PECL COMMON-MODE VOLTAGE EXTERNALLY SUPPLIED. COMPONENTS ARE NOT REQUIRED.

Figure 33. LVDS to PECL Conversion

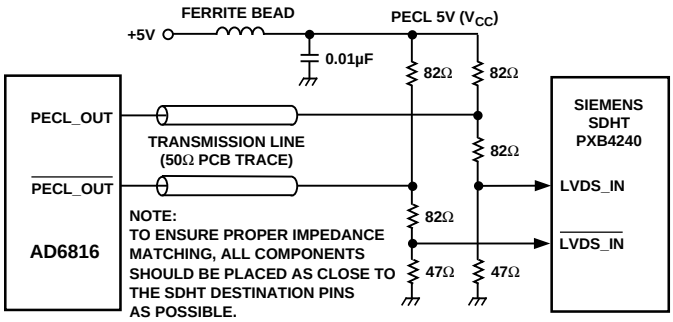
PECL to LVDS Conversion

PECL levels from the AD6816 can be shifted to LVDS levels to the Siemens SDHT using either ac coupling or dc coupling (Figures 34a and 34b). These schemes assume that the PECL output drives the "long" portion of the transmission line. The passive shifting and termination network is located as close to the LVDS input as possible.



BRIEF ANALYSIS:
1. TERMINATION IS DONE BY A PARALLEL THEVENIN SCHEME.
2. THE 100nF CAPACITORS PROVIDE AC COUPLING.
3. THE RESISTOR DIVIDER NETWORK FIXES NEW OFFSET VOLTAGE AT 1.2V.

a.



BRIEF ANALYSIS:
1. SHIFTING NETWORK BASED ON THEVENIN SCHEME WITH LOWER RESISTOR REPLACED BY DIVIDER.
2. COMMON MODE VOLTAGE TRANSFORMED FROM 3.7V DOWN TO 1.4V.
3. DIFFERENTIAL VOLTAGE SWING ATTENUATED FROM 600mV MINIMUM (PECL) TO 220mV MINIMUM FOR LVDS.

b.

Figure 34. PECL to LVDS Conversion

AD6816 Evaluation PCB Test Results Over UTP#5 Cable and L120 Cable (Foil Twisted Pair)

The AD6816 Evaluation PCB supports error free (< 1×10^{-11} BER) transmission over up to 110M UTP#5 cable or L120 cable. Figures 35, 36, 37 below show the different configurations tested. Table III provides the test results. Note that to properly terminate the L120 cable (120 Ω impedance line), the following resistor changes were made to the PCB: R9 = 60 Ω, R10 = 60 Ω, R11 = 120 Ω.

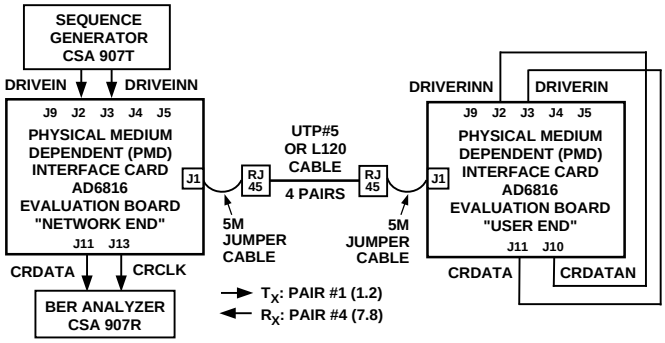


Figure 35. Configuration Test Block Diagram: Loop-Back

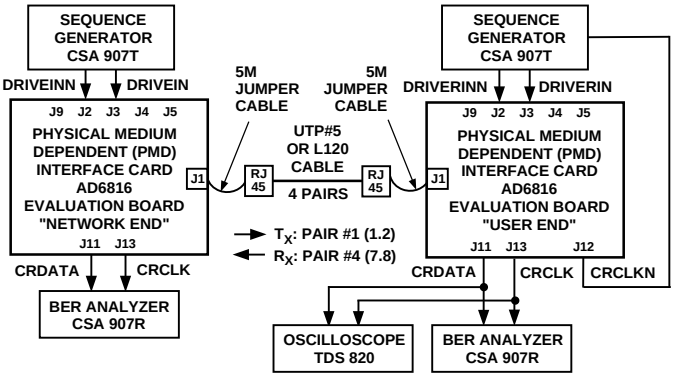


Figure 36. Configuration Test Block Diagram: Loop-Back with Work Station—End Transmitting Data

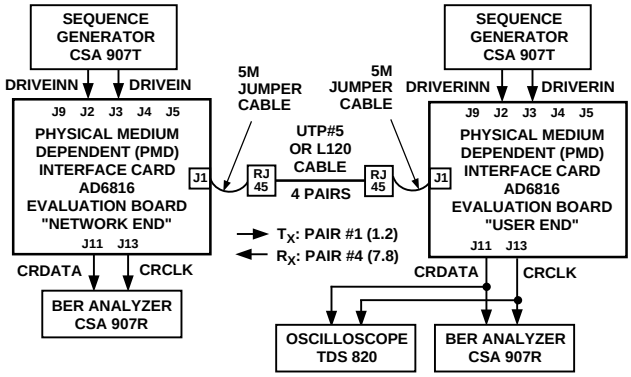


Figure 37. Configuration Test Block Diagram: Dual Simplex

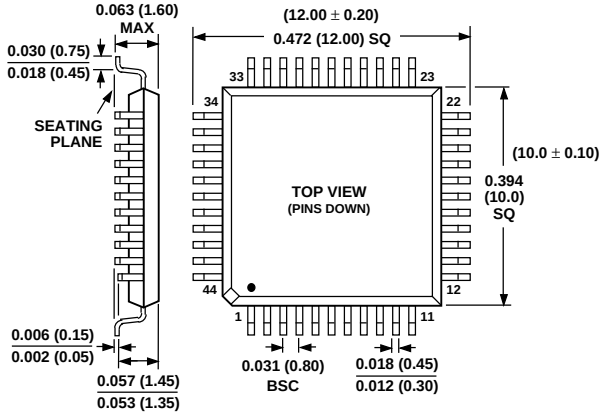
Table III. BER vs. UTP#5 & L120 Cable Length

Configuration	Path(s) Tested	UTP#5 (100 Ω) 100 M	UTP#5 (100 Ω) 145 M	UTP#5 (100 Ω) 150 M	L120 (120 Ω) 100 M	L120 (120 Ω) 175 M	L120 (120 Ω) 190M
Loop-Back (Figure 32)	Tx & Rx	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	7.50E-06
Loop-Back with WS Data (Figure 33)	Tx	< 1.00E-11	< 1.00E-11	6.70E-08	< 1.00E-11	< 1.00E-11	1.00E-07
	Rx	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	1.00E-10
Dual Simplex (Figure 34)	Tx	< 1.00E-11	< 1.00E-11	8.10E-08	< 1.00E-11	< 1.00E-11	2.80E-06
	Rx	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	< 1.00E-11	7.00E-10

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Pin Thin Quad Flatpack Package (ST-44)



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