

System Reset Monolithic IC PST575

Outline

This IC functions in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted. This ultra-low current consumption low reset type system reset IC has a built-in delay time generating circuit that can set the time by an external capacitor and resistor. It is ideal for use in multi-CPU systems because a fast-rising output waveform can be obtained.

Features

1. Ultra-low current consumption
2. Low operating limit voltage
3. Output current high for ON
4. Hysteresis voltage provided in detection voltage
5. Delay time can set over a wide range using external capacitor and resistor.
6. 10 ranks of detection voltage

$I_{CCH}=7.5\mu A$ typ. $I_{CCL}=400\mu A$ typ.
 0.65V typ.
 30mA typ.
 50mV typ.

10 μS ~10S

PST575	C : 4.5V typ.	H : 3.1V typ.
	D : 4.2V typ.	I : 2.9V typ.
	E : 3.9V typ.	J : 2.7V typ.
	F : 3.6V typ.	K : 2.5V typ.
	G : 3.3V typ.	L : 2.3V typ.

Package

MMP-4A (PST575□M)

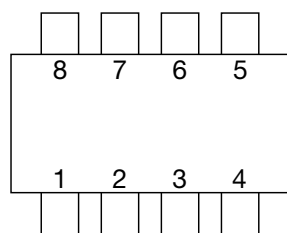
DIP-8A (PST575□)

*□ contains detection voltage rank

Applications

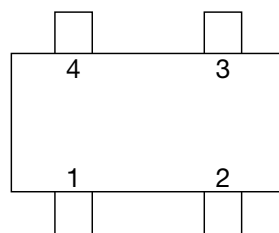
1. Reset circuits in microcomputers, CPUs and MPUs (especially multi-CPU sets)
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.

Pin Assignment



DIP-8A

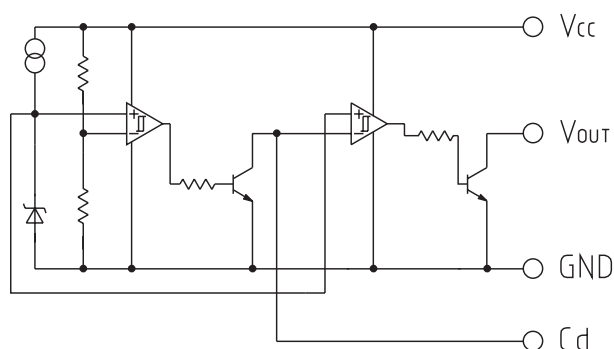
3	GND
4	Cd
5	V _{OUT}
7	V _{CC}



MMP-4A

1	V _{CC}
2	V _{OUT}
3	Cd
4	GND

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Allowable loss	P _d	200 (MMP-3A) 300 (TO-92A)	mW

Electrical Characteristics (Ta=25°C) (Except where noted otherwise, resistance unit is Ω)

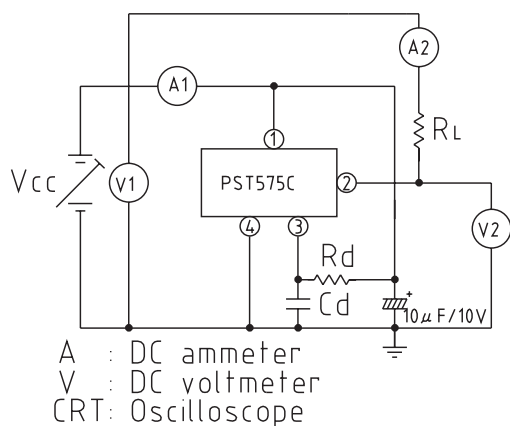
Item	Symbol	Measuring circuit	Measurement conditions	Min.	Typ.	Max.	Units
Detection voltage	V _s	1	R _L =470 V _{OL} ≤ 0.4V V _{CC} =H→L	PST575C	4.3	4.5	4.7
				PST575D	4.0	4.2	4.4
				PST575E	3.7	3.9	4.1
				PST575F	3.4	3.6	3.8
				PST575G	3.1	3.3	3.5
				PST575H	2.9	3.1	3.3
				PST575I	2.75	2.90	3.05
				PST575J	2.55	2.70	2.85
				PST575K	2.35	2.50	2.65
				PST575L	2.15	2.30	2.45
Hysteresis voltage	ΔV _s	1	R _L =470, V _{CC} =L→H→L	25	50	100	mV
Detection voltage temperature coefficient	V _s /ΔT	1	R _L =470, Ta=-20°C~+75°C		±0.01		%/°C
Low-level output voltage	V _{OL}	1	V _{CC} =V _s min.-0.05V, R _L =470		0.1	0.4	V
Output leakage current	I _{OH}	1	V _{CC} =7.5V			±0.1	μA
Circuit current while on	I _{CC} L	1	V _{CC} =V _s min.-0.05V, R _L =∞		400	650	μA
Circuit current while off	I _{CC} H	1	V _{CC} =V _s typ./0.85V, R _L =∞		7.5	12.0	μA
"H" transport delay time	tp _{LH}	2	R _d =100k, C _d =0.01μF *1	0.75	1.25	1.75	mS
"L" transport delay time	tp _{HL}	2	R _d =100k, C _d =0.01μF *1		6	20	μS
Operating power supply voltage	V _{op} L	1	R _L =4.7kΩ, V _{OL} ≤ 0.4V		0.65	0.85	V
Output current while on I	I _{OL} I	1	V _{CC} =V _s min.-0.05V, R _L =0	8	30		mA
Output current while on II	I _{OL} II	1	Ta=-20°C~+75°C, R _L =0 *2	5			mA
Threshold voltage for delay time setting comparator (CO2)	V _{tsh}	1	V _{CC} =5.0V, R _d =100k, C _d =0.01μF R _L =4.7k, C _L =100pF	3.5	3.7	3.9	V

*1 : tp_{LH} : V_{CC}= (V_s typ.-0.4V) → (V_s typ.+0.4V), tp_{HL} : V_{CC}= (V_s typ.+0.4V) → (V_s typ.-0.4V), C_L=100pF

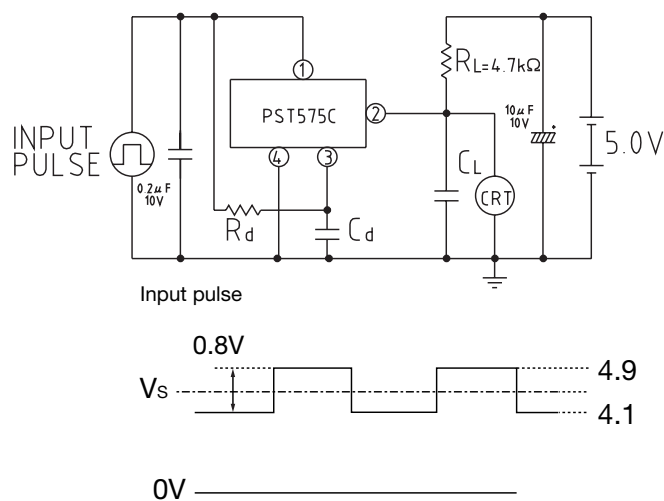
*2: V_{CC}=V_s min.-0.15V

Measuring Circuit (Example: PST575C)

[1]



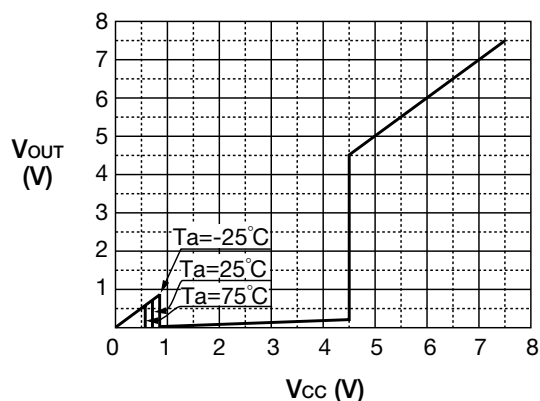
[2]



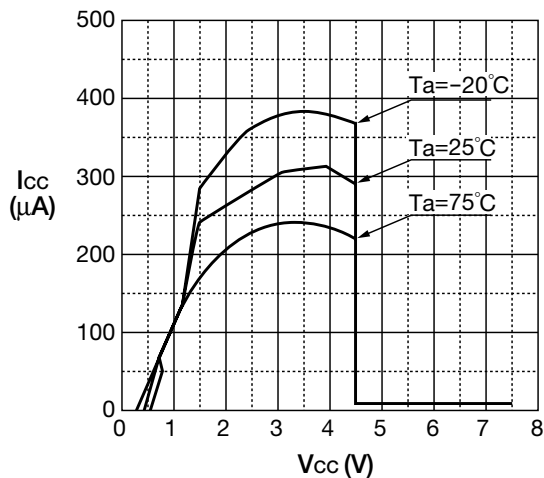
Note: Input model is an example for PST575C (MMP-4P).

Characteristics (Example: PST575C)

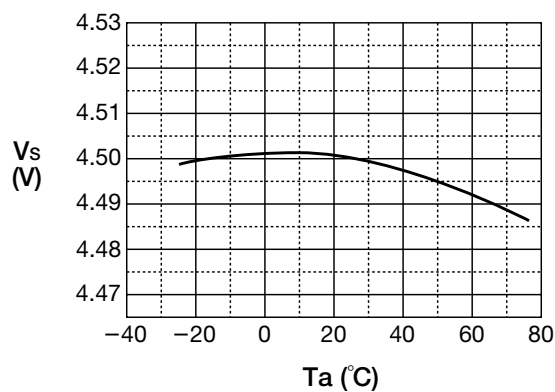
Vcc vs. VOUT



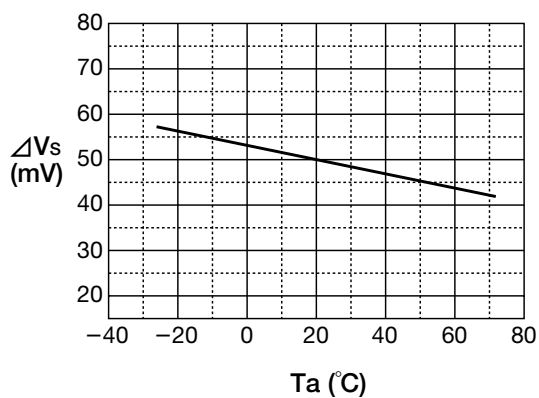
Vcc vs. Icc



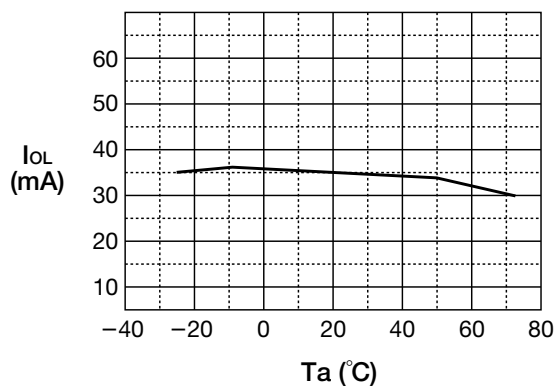
Vs vs. Ta



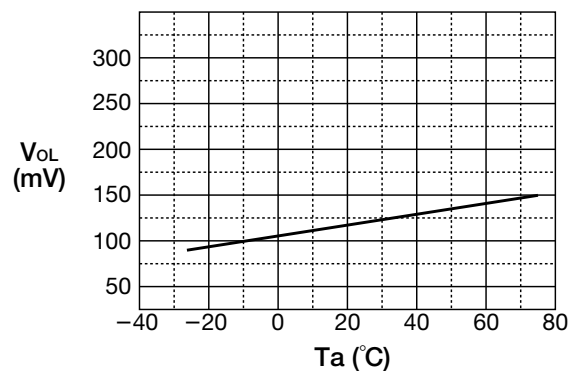
ΔVs vs. Ta



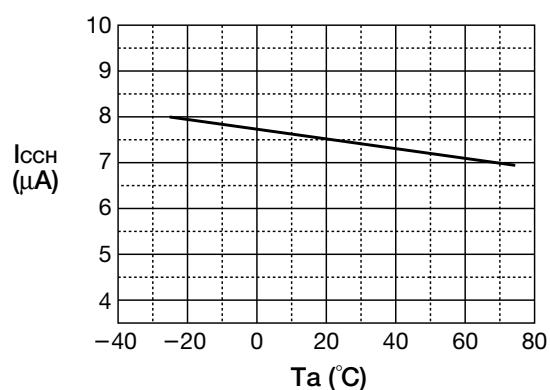
■ I_{OL} vs. T_a



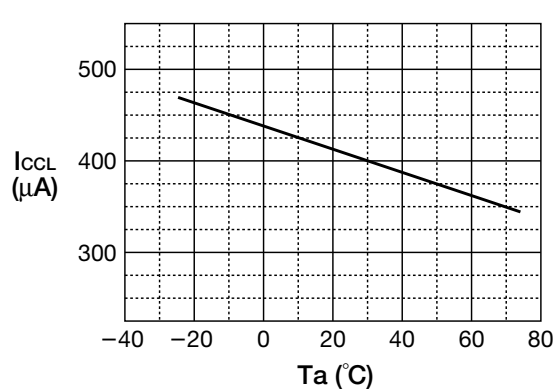
■ V_{OL} vs. T_a



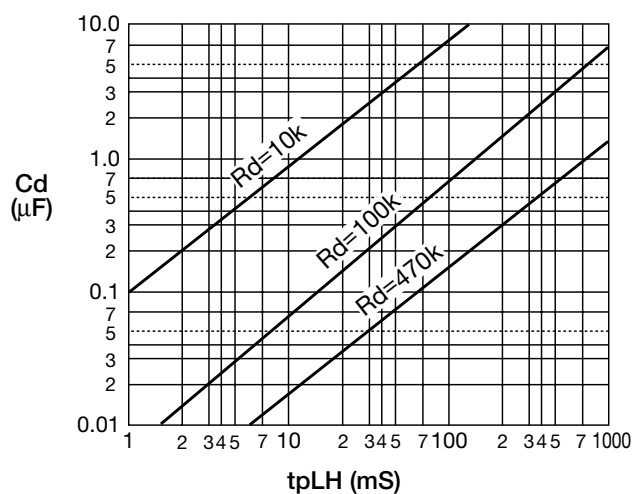
■ I_{CCH} vs. T_a



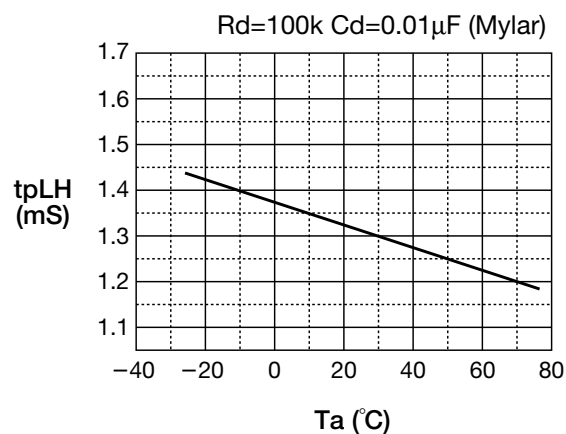
■ I_{CCL} vs. T_a



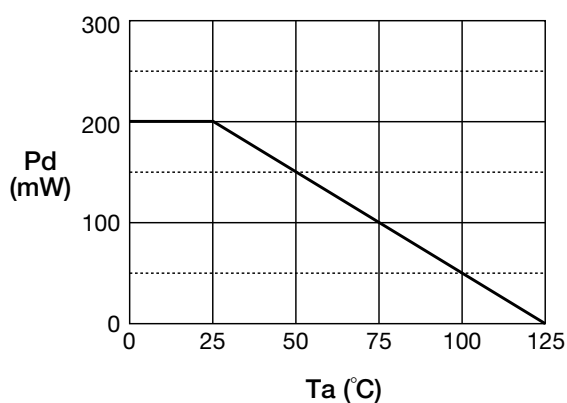
■ C_d (R_d) vs. t_{pLH}



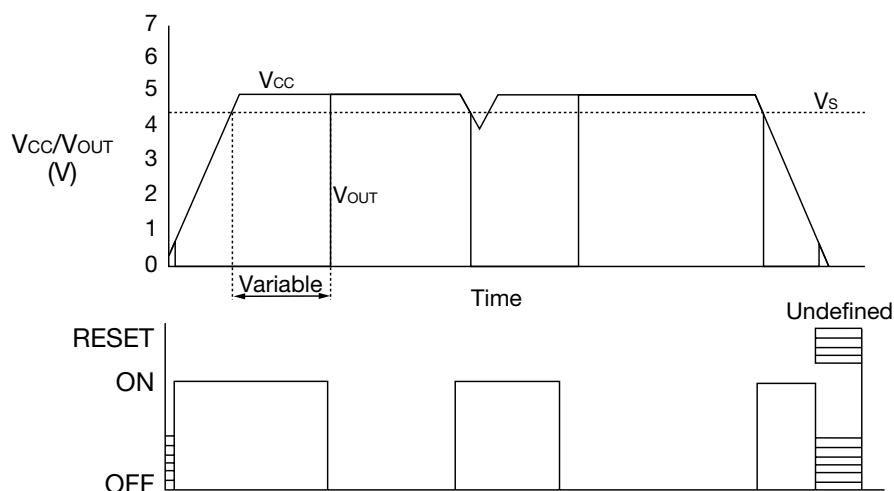
■ t_{pLH} vs. T_a



■ P_d vs. T_a

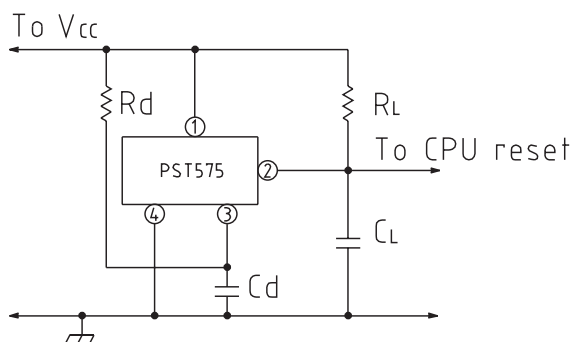


Timing Chart



Application Circuits (Pin numbers are for an example of MMP-4P.)

1. Normal hard reset



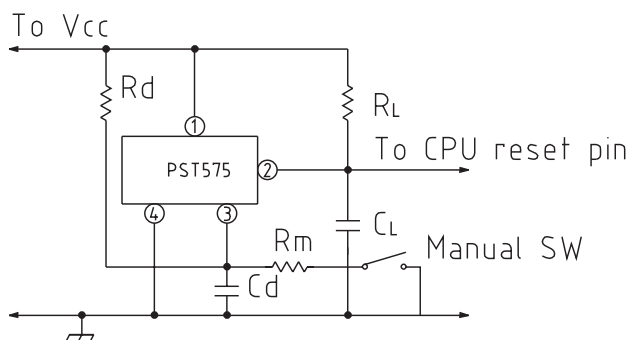
Delay time (t_{PLH})

$$\approx 1.3C_d \times R_d + 0.007 \text{ (mS)}$$

C_d : μF R_d : $\text{k}\Omega$

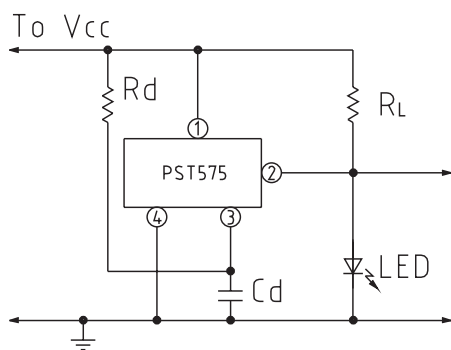
Note: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

2. Manual reset added



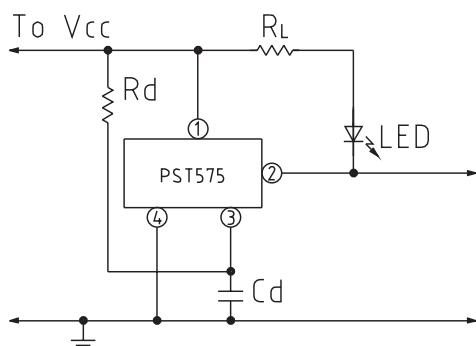
Note: Use R_L , C_L and R_m to prevent manual switch chattering. Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

3. Battery checker (LED ON for high voltage)



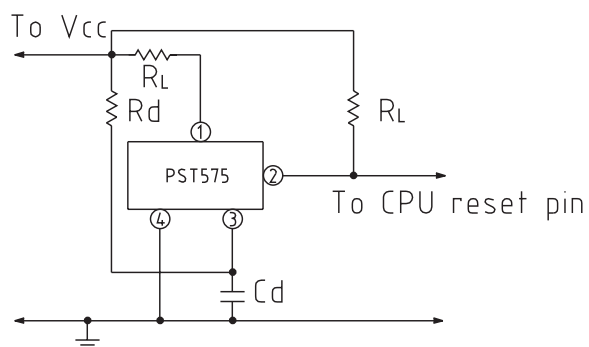
Note: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

4. Battery checker (LED ON for low voltage)



Note: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

5. Hysteresis voltage UP method



When increasing hysteresis voltage for stable system operation, determine R_H as follows and connect externally.

However, I_{CCH} is $-5000\text{PPM}/^{\circ}\text{C}$, so perform temperature compensation at R_H when using over a wide temperature range.

Hysteresis voltage UP amount (ΔV_{sup}) is

$$\Delta V_{sup} \approx R_H \times I_{CCL}$$

Total hysteresis voltage (ΔV_{stotal}) is

$$\Delta V_{stotal} \approx V_s + \Delta V_{sup}$$

(Operation will be destabilized is R_H is raised too much.)

Note: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.