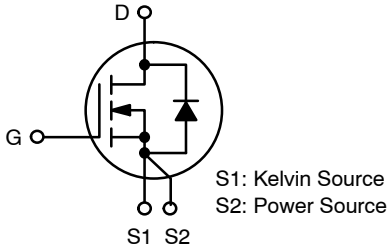
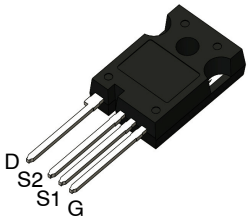
Silicon Carbide (SiC) MOSFET – EliteSiC, 160 mohm, 1200 V, M1, TO-247-4L

NTH4L160N120SC1

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
1200 V	224 mΩ @ 20 V	17.3 A



N−CHANNEL MOSFET



TO−247−4LD
CASE 340CJ

Features

- Typ. $R_{DS(on)}$ = 160 mΩ
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 34 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 49.5 pF)
- 100% Avalanche Tested
- T_J = 175°C
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

- UPS
- DC-DC Converter
- Boost Inverter

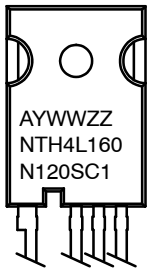
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	1200	V
Gate−to−Source Voltage			V_{GS}	−15/+25	V
Recommended Operation Values of Gate−to−Source Voltage		T_C < 175°C	V_{GSop}	−5/+20	V
Continuous Drain Current (Note 2)	Steady State	T_C = 25°C	I_D	17.3	A
Power Dissipation (Note 2)			P_D	111	W
Continuous Drain Current (Notes 1, 2)	Steady State	T_C = 100°C	I_D	12.3	A
Power Dissipation (Notes 1, 2)			P_D	55.5	W
Pulsed Drain Current (Note 3)	T_A = 25°C		I_{DM}	69	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	11	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 16 A, L = 5 mH) (Note 4)			E_{AS}	128	mJ
Maximum Lead Temperature for Soldering (1/8″ from case for 5 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JA is constant value to follow guide table of LV/HV discrete final datasheet generation .
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. E_{AS} of 128 mJ is based on starting T_J = 25°C; L = 5 mH, I_{AS} = 16 A, V_{DD} = 120 V, V_{GS} = 18 V.

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability
NTH4L160N120SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTH4L160N120SC1	TO−247−4LD	30 Units / Tube

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Table 1. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	1.35	°C/W
Junction−to−Ambient − Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		1200	−	−	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, referenced to 25°C		−	0.6	−	V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	T_J = 25°C	−	−	100	μA
			T_J = 175°C	−	−	1	mA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +25/−15 V, V_{DS} = 0 V		−	−	±1	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 2.5 mA		1.8	3.1	4.3	V
Recommended Gate Voltage	V_{GOP}			−5	−	+20	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 12 A, T_J = 25°C		−	160	224	mΩ
		V_{GS} = 20 V, I_D = 12 A, T_J = 175°C		−	271	377	
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 12 A		−	3.2	−	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V		−	665	−	pF
Output Capacitance	C_{OSS}			−	49.5	−	
Reverse Transfer Capacitance	C_{RSS}			−	4.3	−	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/20 V, V_{DS} = 600 V, I_D = 16 A		−	34	−	nC
Threshold Gate Charge	$Q_{G(TH)}$			−	6	−	
Gate−to−Source Charge	Q_{GS}			−	12.5	−	
Gate−to−Drain Charge	Q_{GD}			−	9.6	−	
Gate−Resistance	R_G	f = 1 MHz		−	1.4	−	Ω
SWITCHING CHARACTERISTICS, VGS = 10 V							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5/20 V,V_{DS} = 800 V, I_D = 16 A, R_G = 6 Ω Inductive load		−	11	20	ns
Rise Time	t_r			−	10	20	
Turn−Off Delay Time	$t_{d(OFF)}$			−	14	25	
Fall Time	t_f			−	7	14	
Turn−On Switching Loss	E_{ON}			−	104	−	μJ
Turn−Off Switching Loss	E_{OFF}			−	32	−	
Total Switching Loss	E_{tot}			−	136	−	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Continuous Drain−Source Diode Forward Current	I_{SD}	V_{GS} = −5 V, T_J = 25°C		−	−	11	A
Pulsed Drain−Source Diode Forward Current (Note 3)	I_{SDM}			−	−	69	
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 6 A, T_J = 25°C		−	4	−	V
Reverse Recovery Time	t_{RR}	V_{GS} = −5/20 V, I_{SD} = 16 A, dI_S/dt = 1000 A/μs		−	15	−	ns
Reverse Recovery Charge	Q_{RR}			−	47	−	nC

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Energy	E_{REC}	V_{GS} = −5/20 V, I_{SD} = 16 A, dI_S/dt = 1000 A/μs	–	3.9	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	6.6	–	A
Charge Time	Ta		–	7.0	–	ns
Discharge Time	Tb		–	7.4	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

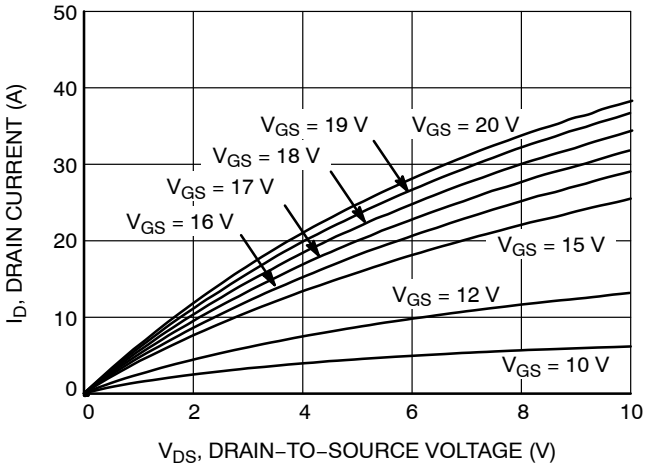


Figure 1. On Characteristics

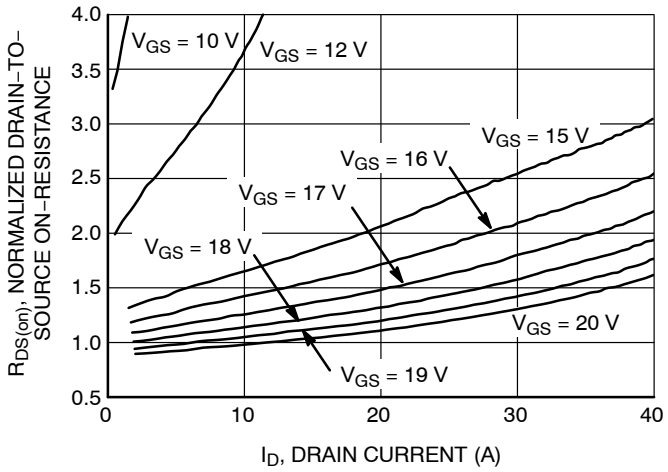


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

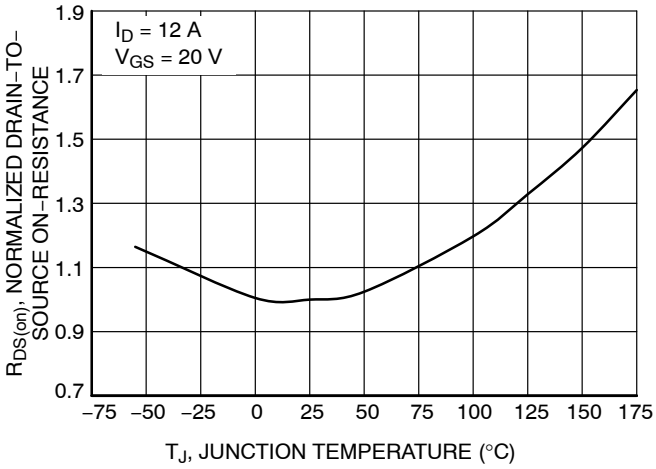


Figure 3. On−Resistance Variation with Temperature

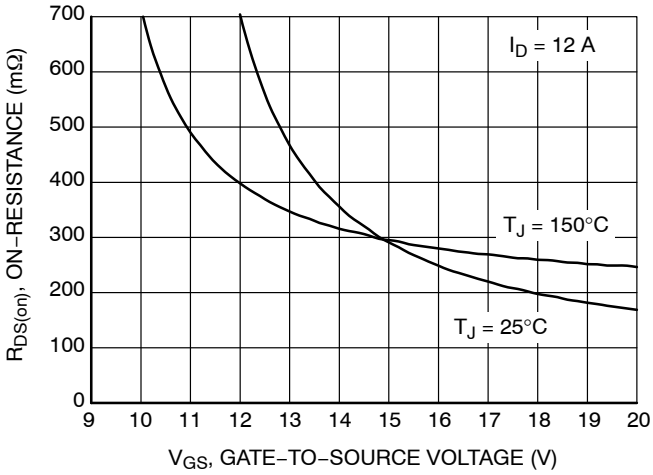


Figure 4. On−Resistance vs. Gate−to−Source Voltage

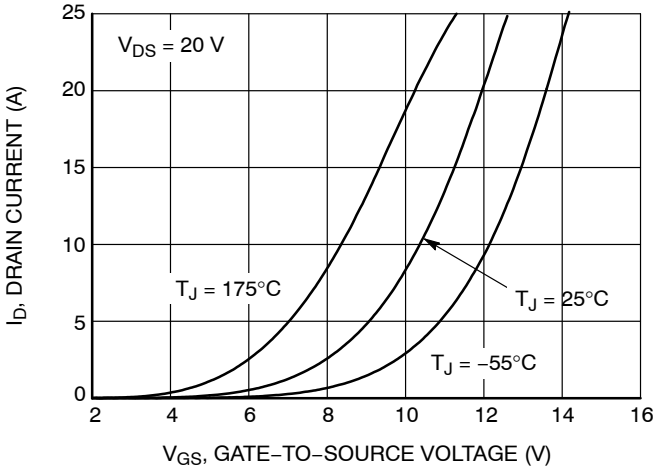


Figure 5. Transfer Characteristics

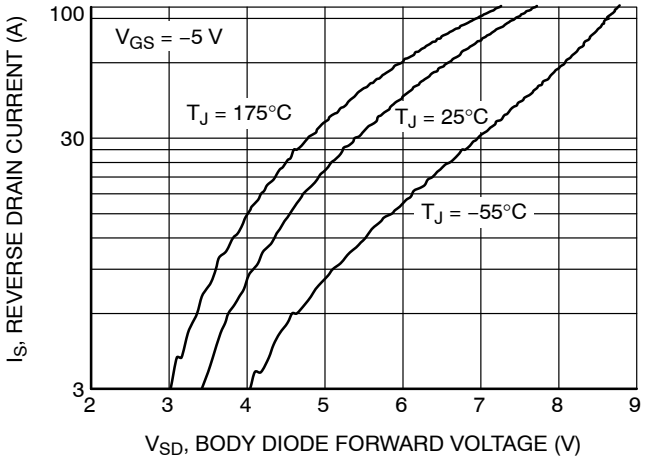


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (CONTINUED)

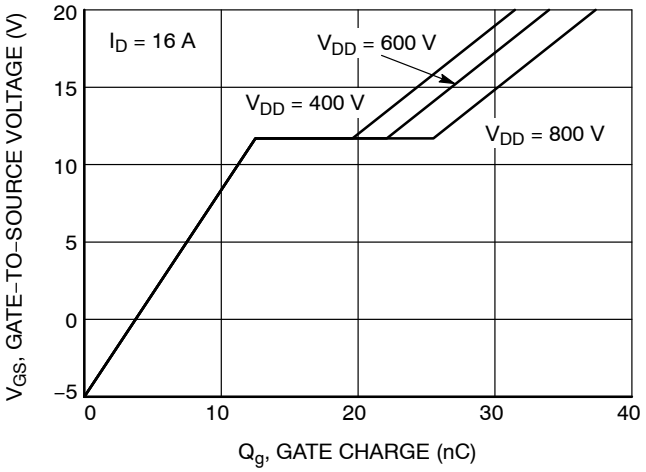


Figure 7. Gate−to−Source Voltage vs. Total Charge

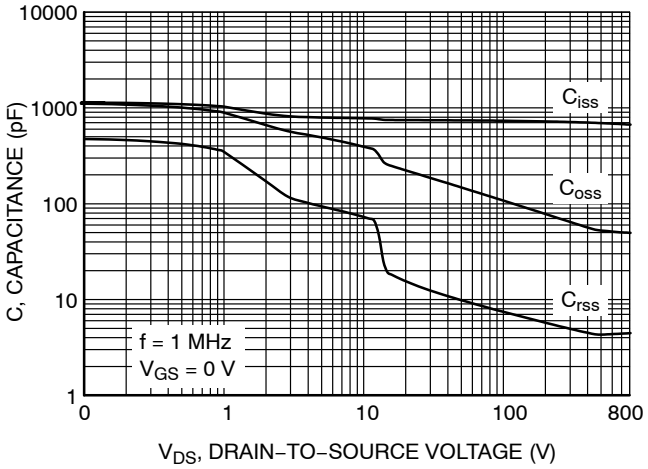


Figure 8. Capacitance vs. Drain−to−Source Voltage

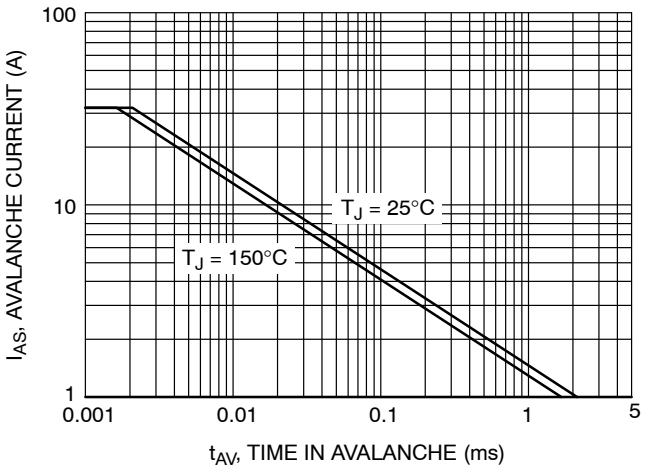


Figure 9. Unclamped Inductive Switching Capability

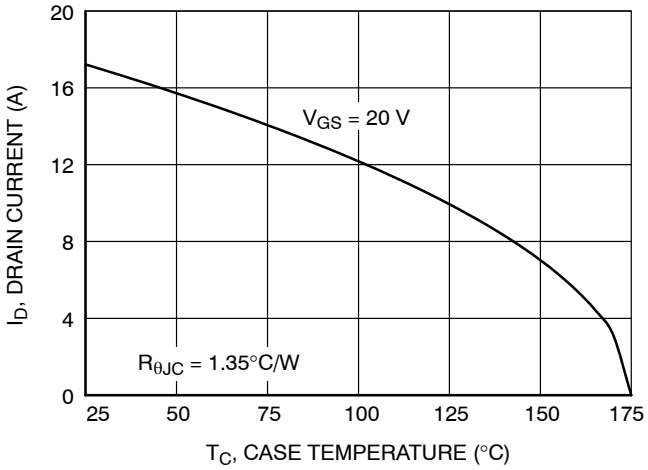


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

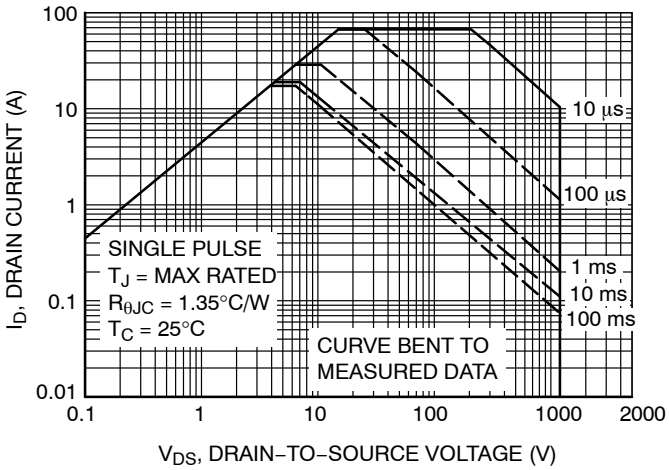


Figure 11. Maximum Rated Forward Biased Safe Operating Area

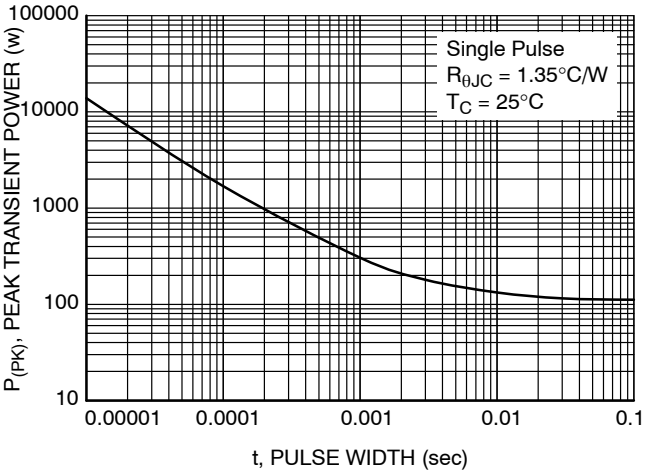


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

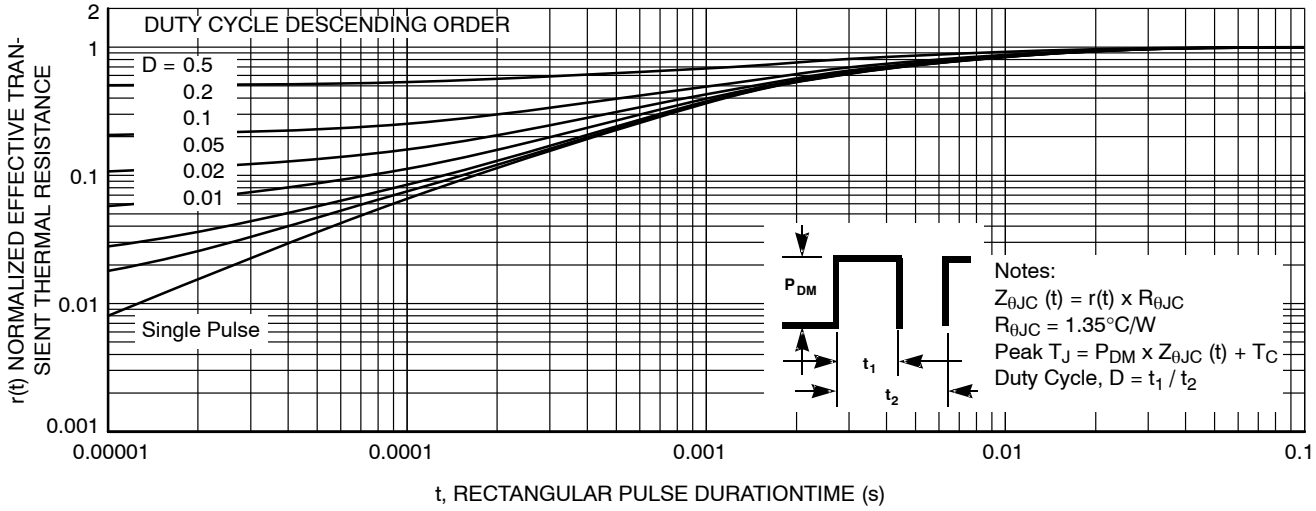


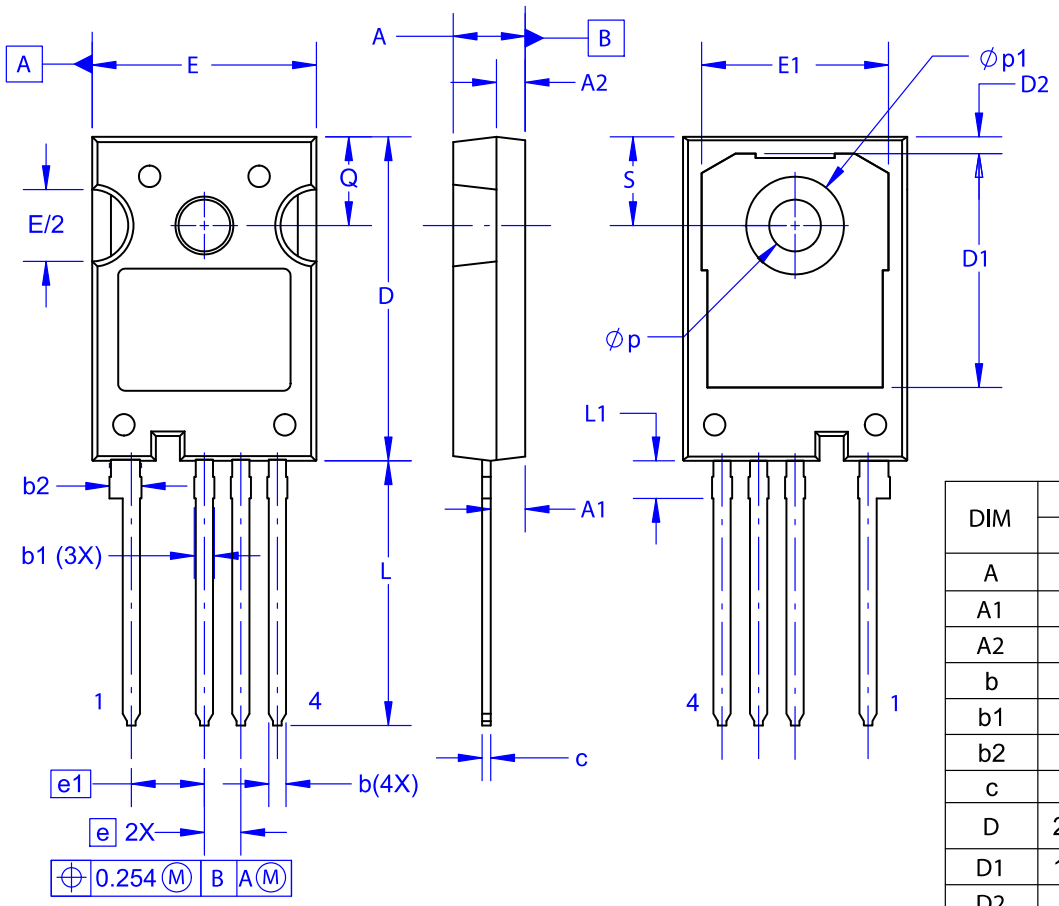
Figure 13. Junction−to−Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−4LD
CASE 340CJ
ISSUE A

DATE 16 SEP 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
c	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
e	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
p	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

NOTES:

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B. DIMENSIONS ARE EXCLUSIVE OF BURRS,MOLD FLASH,AND TIE BAR EXTRUSIONS.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
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