LMX2531 High-Performance Frequency Synthesizer System With Integrated VCO

1 Features

- Multiple Frequency Options Available
  - See *Device Information* Table
  - Frequencies From: 553 MHz to 3132 MHz
- PLL Features
  - Fractional-N Delta-Sigma Modulator Order Programmable up to Fourth Order
  - FastLock/Cycle Slip Reduction with Timeout Counter
  - Partially Integrated, Adjustable Loop Filter
  - Very Low Phase Noise and Spurs
- VCO Features
  - Integrated Tank Inductor
  - Low Phase Noise
- Other Features
  - 2.8-V to 3.2-V Operation
  - Low Operating Current
  - Low Power-Down Current
  - 1.8-V MICROWIRE Support
  - 36-Pin 6-mm × 6-mm × 0.8-mm WQFN Package

2 Applications

- Cellular Base Stations
- Wireless LANs
- Broadband Wireless Access
- Satellite Communications
- Wireless Radios
- Automotive
- CATV Equipment
- Instrumentation and Test Equipment
- RFID Readers
- Data Converter Clocking

3 Description

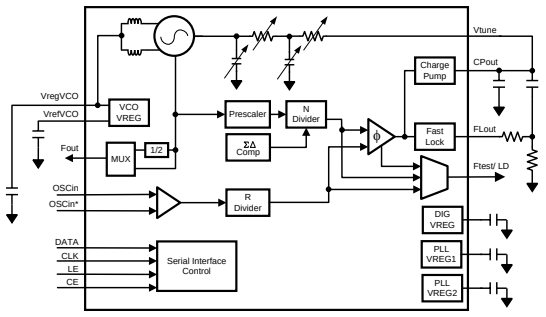
The LMX2531 is a low-power, high-performance frequency synthesizer system which includes a fully integrated delta-sigma PLL and VCO with fully integrated tank circuit. The third and fourth poles are also integrated and adjustable. Ultra-low noise and high-precision LDOs are integrated for the PLL and VCO, which yield higher supply-noise immunity and more consistent performance. When combined with a high-quality reference oscillator, the LMX2531 device generates very stable, low-noise local-oscillator signals for up and down conversion in wireless communication devices. The LMX2531 device is a monolithic integrated circuit, fabricated in an advanced BiCMOS process. Several different versions of this product accommodate different frequency bands.

Device Information(1)

PART	LOW BAND	HIGH BAND
LMX2531LQ1146E	553 — 592 MHz	1106 — 1184 MHz
LMX2531LQ1226E	592 — 634 MHz	1184 — 1268 MHz
LMX2531LQ1312E	634 — 680 MHz	1268 — 1360 MHz
LMX2531LQ1415E	680 — 735 MHz	1360 — 1470 MHz
LMX2531LQ1500E	749.5 — 755 MHz	1499 — 1510 MHz
LMX2531LQ1515E	725 — 790 MHz	1450 — 1580 MHz
LMX2531LQ1570E	765 — 818 MHz	1530 — 1636 MHz
LMX2531LQ1650E	795 — 850 MHz	1590 — 1700 MHz
LMX2531LQ1700E	831 — 885 MHz	1662 — 1770 MHz
LMX2531LQ1742	880 — 933 MHz	1760 — 1866 MHz
LMX2531LQ1778E	863 — 920 MHz	1726 — 1840 MHz
LMX2531LQ1910E	917 — 1014 MHz	1834 — 2028 MHz
LMX2531LQ2080E	952 — 1137 MHz	1904 — 2274 MHz
LMX2531LQ2265E	1089 — 1200 MHz	2178 — 2400 MHz
LMX2531LQ2570E	1168 — 1395 MHz	2336 — 2790 MHz
LMX2531LQ2820E	1355 — 1462 MHz	2710 — 2925 MHz
LMX2531LQ3010E	1455 — 1566 MHz	2910 — 3132 MHz

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Simplified Schematic ... 1
5 Revision History ... 2
6 Pin Configuration and Functions ... 3
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 6
7.6 MICROWIRE Timing Requirements ... 13
7.7 Typical Performance Characteristics ... 14
8 Detailed Description ... 15
8.1 Overview ... 15
8.2 Functional Block Diagram ... 15
8.3 Feature Description ... 15
8.4 Device Functional Modes ... 20
8.5 Programming ... 20
8.6 Register Maps ... 21
9 Application and Implementation ... 33
9.1 Application Information ... 33
9.2 Typical Application ... 33
9.3 Do's and Don'ts ... 35
10 Power Supply Recommendations ... 35
11 Layout ... 35
11.1 Layout Guidelines ... 35
11.2 Layout Example ... 36
12 Device and Documentation Support ... 37
12.1 Device Support ... 37
12.2 Trademarks ... 37
12.3 Electrostatic Discharge Caution ... 37
12.4 Glossary ... 37
13 Mechanical, Packaging, and Orderable Information ... 37

5 Revision History

Changes from Revision R (April 2013) to Revision S — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

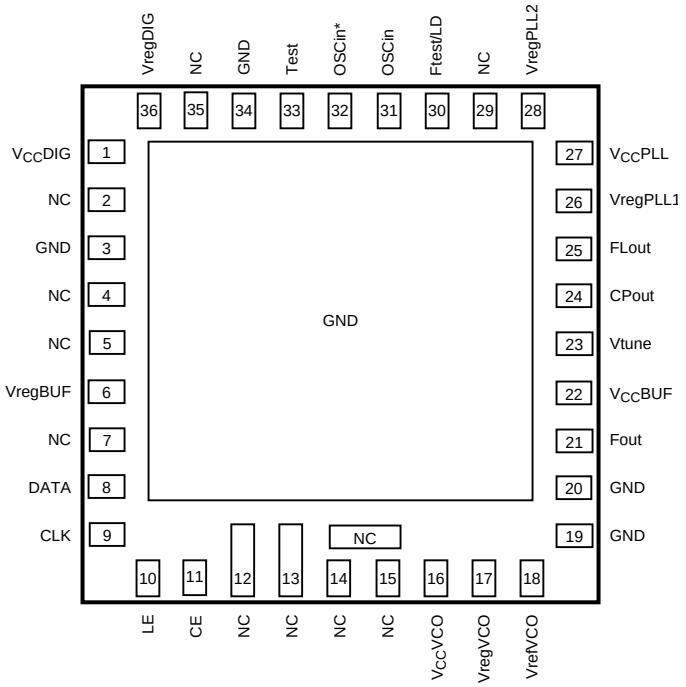
Changes from Revision Q (February 2013) to Revision R — **Page**

- Changed layout of National Data Sheet to TI format ... 32

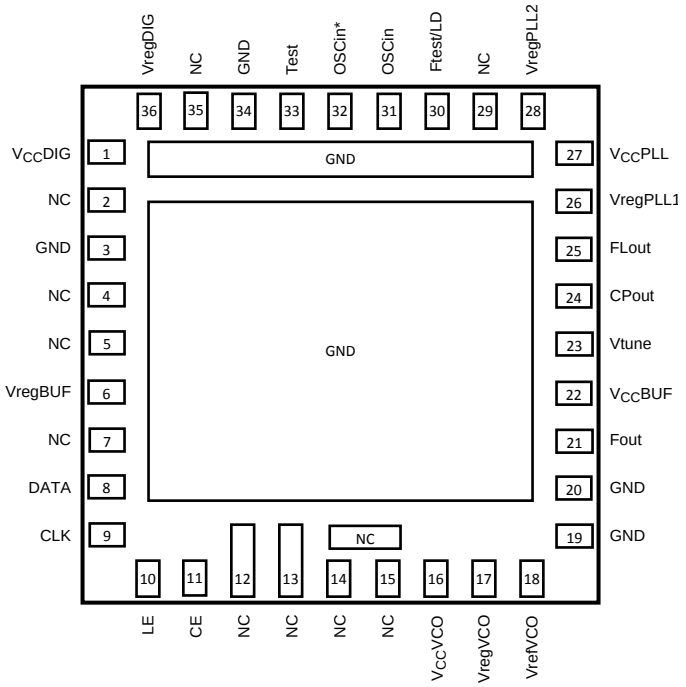
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6 Pin Configuration and Functions

NJH0036D Package
36-Pin WQFN, D Version, (LMX2531LQ1146E/1226E/1312E/1415E/1515E/2820E/3010E)
Top View



NJG0036A Package
36-Pin WQFN, A Version, (All Other Versions)
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CE	11	Input	Chip Enable Input. High impedance CMOS input. This pin must not exceed 2.75 V. When CE is brought high the LMX2531 is powered up corresponding to the internal power control bits. Although the part can be programmed when powered down, it is still necessary to reprogram the R0 register to get the part to re-lock.
CLK	9	Input	MICROWIRE clock input. High impedance CMOS input. This pin must not exceed 2.75 V. Data is clocked into the shift register on the rising edge.
CPout	24	Output	Charge pump output for PLL. For connection to Vtune through an external passive loop filter.
DATA	8	Input	MICROWIRE serial data input. High impedance CMOS input. This pin must not exceed 2.75 V. Data is clocked in MSB first. The last bits clocked in form the control or register select bits.
FLout	25	Output	An open drain NMOS output which is used for FastLock or a general purpose output.
Fout	21	Output	Buffered RF Output for the VCO.
Ftest/LD	30	Output	Multiplexed CMOS output. Typically used to monitor PLL lock condition.
GND	3	—	Ground
GND	19	—	Ground for the VCO circuitry.
GND	20	—	Ground for the VCO Output Buffer circuitry.
GND	34	—	Ground
LE	10	Input	MICROWIRE Latch Enable input. High impedance CMOS input. This pin must not exceed 2.75 V. Data stored in the shift register is loaded into the selected latch register when LE goes HIGH.
NC	2, 4, 5, 7, 12, 13, 29, 35	—	No Connect.
NC	14, 15	—	No Connect. Do NOT ground. This also includes the pad above these pins.
OSCin	31	Input	Oscillator input.
OSCin*	32	Input	Oscillator complimentary input. When a single ended source is used, then a bypass capacitor should be placed as close as possible to this pin and be connected to ground.
Test	33	Output	This pin is for test purposes and should be grounded for normal operation.
VccBUF	22	—	Power Supply for the VCO Buffer circuitry. Input may range from 2.8 — 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
VccDIG	1	—	Power Supply for digital LDO circuitry. Input may range from 2.8 — 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
VccPLL	27	—	Power Supply for the PLL. Input may range from 2.8 — 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
VccVCO	16	—	Power Supply for VCO regulator circuitry. Input may range from 2.8 — 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
VrefVCO	18	—	Internal reference voltage for VCO LDO. Not intended to drive an external load. Connect to ground with a capacitor.
VregBUF	6	—	Internally regulated voltage for the VCO buffer circuitry. Connect to ground with a capacitor.
VregDIG	36	—	Internally regulated voltage for LDO digital circuitry.
VregPLL1	26	—	Internally regulated voltage for PLL charge pump. Not intended to drive an external load. Connect to ground with a capacitor.
VregPLL2	28	—	Internally regulated voltage for RF digital circuitry. Not intended to drive an external load. Connect to ground with a capacitor.
VregVCO	17	—	Internally regulated voltage for VCO circuitry. Not intended to drive an external load. Connect to ground with a capacitor and some series resistance.
Vtune	23	Input	Tuning voltage input for the VCO. For connection to the CPout pin through an external passive loop filter.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
V_{CC} (VccDIG, VccVCO, VccBUF, VccPLL)	Power Supply Voltage	–0.3	3.5	V
All other pins (Except Ground)	Power Supply Voltage	–0.3	3.0	V
T_L	Lead Temperature (solder 4 sec.)		260	°C
T_J	Junction Temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power Supply Voltage (VccDig, VccVCO, VccBUF)	2.8	3.0	3.2	V
V_i	Serial Interface and Power Control Voltage	0		2.75	V
T_A	Ambient Temperature (1)	–40		85	°C

(1) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R0 register was last programmed, and still have the part stay in lock. The action of programming the R0 register, even to the same value, activates a frequency calibration routine. This implies that the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R0 register to ensure that it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of $–40°C \le T_A \le 85°C$ without violating specifications.

7.4 Thermal Information

THERMAL METRIC (1)		LMX2531 NJH0036D 36 PINS	LMX2531 NJG0036A 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.5	35.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.1	9.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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7.5 Electrical Characteristics

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I_{CC}	Power Supply Current Power Supply Current	Divider Disabled	LMX2531LQ2265E/ 2570E		38	44	mA
			LMX2531LQ2820E/ 3010E		38	46	
			All Other Options		34	41	
		Divider Enabled	LMX2531LQ2265E/ 2570E		41	49	
			LMX2531LQ2820E/ 3010E		44	52	
			All Other Options		37	46	
$I_{CC}PD$	Power Down Current	CE = 0 V, Part Initialized			7		µA
OSCILLATOR							
$I_{IH}OSC$	Oscillator Input High Current	V_{IH} = 2.75 V				100	µA
$I_{IL}OSC$	Oscillator Input Low Current	V_{IL} = 0		–100			µA
f_{OSCin}	Frequency Range	See (1)		5		80	MHz
v_{OSCin}	Oscillator Sensitivity			0.5		2.0	Vpp
PLL							
f_{PD}	Phase Detector Frequency					32	MHz
I_{CPout}	Charge Pump Output Current Magnitude	ICP = 0			90		µA
		ICP = 1			180		µA
		ICP = 3			360		µA
		ICP = 15			1440		µA
$I_{CPout}TRI$	CP TRI-STATE Current	0.4 V < V_{CPout} < 2.0 V			2	10	nA
$I_{CPout}MM$	Charge Pump Sink vs Source Mismatch	V_{CPout} = 1.2 V, T_A = 25°C			2%	8%	
$I_{CPout}V$	Charge Pump Current vs CP Voltage Variation	0.4 V < V_{CPout} < 2.0 V, T_A = 25°C			4%		
$I_{CPout}T$	CP Current vs Temperature Variation	V_{CPout} = 1.2 V			8%		
LN(f)	Normalized PLL 1/f Noise $LN_{PLL_flicker}$(10 kHz) See (2)	ICP = 1X Charge Pump Gain			–94		dBc/Hz
		ICP = 16X Charge Pump Gain			–104		
	Normalized PLL Noise Floor LN_{PLL_flat} See (3)	ICP = 1X Charge Pump Gain			–202		dBc/Hz
		ICP = 16X Charge Pump Gain			–212		

(1) There are program bits that need to be set based on the OSCin frequency. Refer to the following sections: *XTLSEL[2:0] -- OSCin Select*, *XTLDIV[1:0] -- Division Ratio for the OSCin Frequency*, *XTLMAN[11:0] -- Manual OSCin Mode*, *XTLMAN2 -- Manual Crystal Mode Second Adjustment*, and *LOCKMODE -- Frequency Calibration Mode*. Not all bit settings can be used for all frequency choices of OSCin. For instance, automatic modes described in *XTLSEL[2:0] -- OSCin Select* do not work below 8 MHz.

(2) One of the specifications for modeling PLL in-band phase noise is the PLL 1/f noise normalized to 1 GHz carrier frequency and 10 kHz offset, $L_{PLL_flicker}$(10 kHz). From this normalized index of PLL 1/f noise, the PLL 1/f noise can be calculated for any carrier and offset frequency as: $LN_{PLL_flicker}(f) = L_{PLL_flicker}(10\ kHz) - 10 \times \log(10\ kHz / f) + 20 \times \log(F_{out} / 1\ GHz)$. Flicker noise can dominate at low offsets from the carrier and has a 10 dB/decade slope and improves with higher charge pump currents and at higher offset frequencies . To accurately measure $L_{PLL_flicker}$(10 kHz) it is important to use a high phase detector frequency and a clean reference to make it such that this measurement is on the 10 dB/decade slope close to the carrier. $L_{PLL_flicker}(f)$ can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL_flicker}(f)$ and L_{PLL_flat}. In other words, $L_{PLL}(f) = 10 \times \log(10^{(LN_{PLL_flat}/10)} + 10^{(LN_{PLL_flicker}(f)/10)})$

(3) A specification used for modeling PLL in-band phase noise floor is the Normalized PLL noise floor, LN_{PLL_flat}, and is defined as: $LN_{PLL_flat} = L(f) - 20 \times \log(N) - 10 \times \log(f_{PD})$. L_{PLL_flat} is the single side band phase noise in a 1 Hz Bandwidth and f_{PD} is the phase detector frequency of the synthesizer. L_{PLL_flat} contributes to the total noise, L(f). To measure L_{PLL_flat} the offset frequency must be chosen sufficiently smaller then the loop bandwidth of the PLL, and yet large enough to avoid a substantial noise contribution from the reference and PLL flicker noise. L_{PLL_flat} can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL_flicker}(f)$ and L_{PLL_flat}. In other words, $L_{PLL}(f) = 10 \times \log(10^{(LN_{PLL_flat}/10)} + 10^{(LN_{PLL_flicker}(f)/10)})$

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCO FREQUENCIES						
f_{Fout}	Operating Frequency Range (All options have a frequency divider, this applies before the divider. The frequency after the divider is half of what is shown)	LMX2531LQ1146E	1106		1184	MHz
		LMX2531LQ1226E	1184		1268	
		LMX2531LQ1312E	1268		1360	
		LMX2531LQ1415E	1360		1470	
		LMX2531LQ1500E	1499		1510	
		LMX2531LQ1515E	1450		1580	
		LMX2531LQ1570E	1530		1636	
		LMX2531LQ1650E	1590		1700	
		LMX2531LQ1700E	1662		1770	
		LMX2531LQ1742	1760		1866	
		LMX2531LQ1778E	1726		1840	
		LMX2531LQ1910E	1834		2028	
		LMX2531LQ2080E	1904		2274	
		LMX2531LQ2265E	2178		2400	
		LMX2531LQ2570E	2336		2790	
		LMX2531LQ2820E	2710		2925	
		LMX2531LQ3010E	2910		3132	
OTHER VCO SPECIFICATIONS						
ΔT_{CL}	Maximum Allowable Temperature Drift for Continuous Lock See (4)	LMX2531LQ1742	65			°C
		LMX2531LQ1500E/1570E/1650E/ 1146E/1226/1312E/1415E/1515E	90			
		LMX2531LQ1700E/1778E/1910E/ 2080E/2265E/2570E/2820E/3010E	125			

(4) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R0 register was last programmed, and still have the part stay in lock. The action of programming the R0 register, even to the same value, activates a frequency calibration routine. This implies that the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R0 register to ensure that it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of –40°C ≤T_A≤ 85°C without violating specifications.

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
p_{Fout}	Output Power to a 50-Ω Load (Applies across entire tuning range.)	Divider Disabled	LMX2531LQ1146E	1	4.0	7	dBm
			LMX2531LQ1226E	1	3.5	7	
			LMX2531LQ1312E	1	3.5	7	
			LMX2531LQ1415E	0	3.0	6	
			LMX2531LQ1500E	1	3.5	7.0	
			LMX2531LQ1515E	–1	2.5	5	
			LMX2531LQ1570E	2	4.5	8	
			LMX2531LQ1650E	2	4.5	8	
			LMX2531LQ1700E	1	3.5	7	
			LMX2531LQ1742	1	3.5	7	
			LMX2531LQ1778E	1	3.5	7	
			LMX2531LQ1910E	1	3.5	7	
			LMX2531LQ2080E	1	3.5	7	
			LMX2531LQ2265E	1	3.5	7	
			LMX2531LQ2570E	0	3.0	6	
			LMX2531LQ2820E	–0.5	2.5	5.5	
			LMX2531LQ3010E	–1.5	1.5	4.5	
		Divider Enabled	LMX2531LQ1146E	–1	2.0	5	dBm
			LMX2531LQ1226E	–1	2.0	5	
			LMX2531LQ1312E	–1	1.5	4	
			LMX2531LQ1415E	–2	0.5	3	
			LMX2531LQ1500E	1	3.0	6.0	
			LMX2531LQ1515E	–2	0.5	3	
			LMX2531LQ1570E	1	3.0	6	
			LMX2531LQ1650E	1	3.0	6	
			LMX2531LQ1700E	1	3.0	6	
			LMX2531LQ1742	1	3.0	6	
			LMX2531LQ1778E	1	3.0	6	
			LMX2531LQ1910E	1	3.0	6	
			LMX2531LQ2080E	0	2.5	5	
			LMX2531LQ2265E	0	2.5	5	
			LMX2531LQ2570E	–1	1.5	4	
			LMX2531LQ2820E	–2.5	0	2.5	
			LMX2531LQ3010E	–3	–0.5	2	

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
K_{Vtune}	Fine Tuning Sensitivity (When a range is displayed in the typical column, indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range.)	LMX2531LQ1146E				2.5 — 5.5		MHz/V
		LMX2531LQ1226E				3 — 6		
		LMX2531LQ1312E				3 — 6		
		LMX2531LQ1415E				3.5 — 6.5		
		LMX2531LQ1500E				4 — 7		
		LMX2531LQ1515E				4 — 7		
		LMX2531LQ1570E				4 — 7		
		LMX2531LQ1650E				4 — 7		
		LMX2531LQ1700E				6 — 10		
		LMX2531LQ1742				4 — 7		
		LMX2531LQ1778E				6 — 10		
		LMX2531LQ1910E				8 — 14		
		LMX2531LQ2080E				9 — 20		
		LMX2531LQ2265E				10 — 16		
		LMX2531LQ2570E				10 — 23		
		LMX2531LQ2820E				12 — 28		
		LMX2531LQ3010E				13 — 29		
HS_{Fout}	Harmonic Suppression (Applies Across Entire Tuning Range)	Second Harmonic 50 Ω Load	Divider Disabled	LMX2531LQ1146E /1226E/1312E /1415E/1515E		–35	–25	dBc
				LMX2531LQ2820E /3010E		–40		
				All Other Options		–30	–25	
			Divider Enabled	LMX2531LQ1146E /1226E/1312E /1415E/1515E		–30	–20	
				LMX2531LQ2820E /3010E		–30	–15	
				All Other Options		–20	–15	
		Third Harmonic 50 Ω Load	Divider Disabled	LMX2531LQ1146E /1226E/1312E		–35	–30	
				LMX2531LQ2820E /3010E		–50		
				All Other Options		–40	–35	
			Divider Enabled	LMX2531LQ1146E /1226E/1312E /1570E/1650E		–20	–15	
				LMX2531LQ2820E /3010E		–40	–20	
				All Other Options		–25	–20	
$PUSH_{Fout}$	Frequency Pushing	Creg = 0.1 µF, V_{DD} ± 100 mV, Open Loop				300		kHz/V
$PULL_{Fout}$	Frequency Pulling	VSWR = 2:1, Open Loop					±600	kHz
Z_{Fout}	Output Impedance					50		Ω

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO PHASE NOISE (5)							
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1146E)	f_{Fout} = 1146 MHz DIV2 = 0	10-kHz Offset		–96		dBc/Hz
			100-kHz Offset		–121		
			1-MHz Offset		–142		
			5-MHz Offset		–156		
		f_{Fout} = 573 MHz DIV2 = 1	10-kHz Offset		–101		
			100-kHz Offset		–126		
			1-MHz Offset		–147		
			5-MHz Offset		–156		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1226E)	f_{Fout} = 1226 MHz DIV2 = 0	10-kHz Offset		–95		dBc/Hz
			100-kHz Offset		–121		
			1-MHz Offset		–142		
			5-MHz Offset		–155		
		f_{Fout} = 613 MHz DIV2 = 1	10-kHz Offset		–101		
			100-kHz Offset		–126		
			1-MHz Offset		–147		
			5-MHz Offset		–155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1312E)	f_{Fout} = 1314 MHz DIV2 = 0	10-kHz Offset		–95		dBc/Hz
			100-kHz Offset		–121		
			1-MHz Offset		–140		
			5-MHz Offset		–154		
		f_{Fout} = 657 MHz DIV2 = 1	10-kHz Offset		–101		
			100-kHz Offset		–126		
			1-MHz Offset		–146		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1415E)	f_{Fout} = 1415 MHz DIV2 = 0	10-kHz Offset		–95		dBc/Hz
			100-kHz Offset		–121		
			1-MHz Offset		–141		
			5-MHz Offset		–154		
		f_{Fout} = 707.5 MHz DIV2 = 1	10-kHz Offset		–100		
			100-kHz Offset		–126		
			1-MHz Offset		–146		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1500E)	f_{Fout} = 1500 MHz DIV2 = 1	10-kHz Offset		–97		dBc/Hz
			100-KHz Offset		–120		
			1-MHz Offset		–142		
			5-MHz Offset		–155		
		f_{Fout} = 750 MHz DIV2 = 1	10-kHz Offset		–103		
			100-kHz Offset		–126		
			1-MHz Offset		–131		
			5-MHz Offset		–155		

(5) The VCO phase noise is measured assuming that the loop bandwidth is sufficiently narrow that the VCO noise dominates. The maximum limits apply only at center frequency and over temperature, assuming that the part is reloaded at each test frequency. Over frequency, the phase noise can vary 1 to 2 dB, with the worst case performance typically occurring at the highest frequency. Over temperature, the phase noise typically varies 1 to 2 dB, assuming the part is reloaded.

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1515E)	f_{Fout} = 1515 MHz DIV2 = 0	10-kHz Offset		–96		dBc/Hz
			100-kHz Offset		–122		
			1-MHz Offset		–142		
			5-MHz Offset		–153		
		f_{Fout} = 757.5 MHz DIV2 = 1	10-kHz Offset		–99		
			100-kHz Offset		–125		
			1-MHz Offset		–145		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1570E)	f_{Fout} = 1583 MHz DIV2 = 0	10-kHz Offset		–93		dBc/Hz
			100-kHz Offset		–118		
			1-MHz Offset		–140		
			5-MHz Offset		–154		
		f_{Fout} = 791.5 MHz DIV2 = 1	10-kHz Offset		–99		
			100-kHz Offset		–122		
			1-MHz Offset		–144		
			5-MHz Offset		–155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1650E)	f_{Fout} = 1645 MHz DIV2 = 0	10-kHz Offset		–93		dBc/Hz
			100-kHz Offset		–118		
			1-MHz Offset		–140		
			5-MHz Offset		–154		
		f_{Fout} = 822.5 MHz DIV2 = 1	10-kHz Offset		–99		
			100-kHz Offset		–122		
			1-MHz Offset		–144		
			5-MHz Offset		–155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1700E)	f_{Fout} = 1716 MHz DIV2 = 0	10-kHz Offset		–92		dBc/Hz
			100-kHz Offset		–117		
			1-MHz Offset		–139		
			5-MHz Offset		–153		
		f_{Fout} = 858 MHz DIV2 = 1	10-kHz Offset		–98		
			100-kHz Offset		–122		
			1-MHz Offset		–144		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1742)	f_{Fout}= 1813 MHz DIV2 = 0	10-kHz Offset		–92		dBc/Hz
			100-kHz Offset		–117		
			1-MHz Offset		–140		
			5-MHz Offset		–152		
		f_{Fout} = 906.5 MHz DIV2 = 1	10-kHz Offset		–99		
			100-kHz Offset		–122		
			1-MHz Offset		–143		
			5-MHz Offset		–152		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1778E)	f_{Fout} = 1783 MHz DIV2 = 0	10-kHz Offset		–92		dBc/Hz
			100-kHz Offset		–117		
			1-MHz Offset		–139		
			5-MHz Offset		–152		
		f_{Fout} = 891.5 MHz DIV2 = 1	10-kHz Offset		–97		
			100-kHz Offset		–122		
			1-MHz Offset		–144		
			5-MHz Offset		–154		

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1910E)	f_{Fout} = 1931 MHz DIV2 = 0	10-kHz Offset		–89		dBc/Hz
			100-kHz Offset		–115		
			1-MHz Offset		–138		
			5-MHz Offset		–151		
		f_{Fout} = 965.5 MHz DIV2 = 1	10-kHz Offset		–95		
			100-kHz Offset		–121		
			1-MHz Offset		–143		
			5-MHz Offset		–155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2080E)	f_{Fout} = 2089 MHz DIV2 = 0	10-kHz Offset		–87		dBc/Hz
			100-kHz Offset		–113		
			1-MHz Offset		–136		
			5-MHz Offset		–150		
		f_{Fout} = 1044.5 MHz DIV2 = 1	10-kHz Offset		–93		
			100-kHz Offset		–119		
			1-MHz Offset		–142		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2265E)	f_{Fout} = 2264 MHz DIV2 = 0	10-kHz Offset		–88		dBc/Hz
			100-kHz Offset		–113		
			1-MHz Offset		–136		
			5-MHz Offset		–150		
		f_{Fout} = 1132 MHz DIV2 = 1	10-kHz Offset		–94		
			100-kHz Offset		–118		
			1-MHz Offset		–141		
			5-MHz Offset		–154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2570E)	f_{Fout} = 2563 MHz DIV2 = 0	10-kHz Offset		–86		dBc/Hz
			100-kHz Offset		–112		
			1-MHz Offset		–135		
			5-MHz Offset		–149		
		f_{Fout} = 1281.5 MHz DIV2 = 1	10-kHz Offset		–91		
			100-kHz Offset		–117		
			1-MHz Offset		–139		
			5-MHz Offset		–152		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2820E)	f_{Fout} = 2818 MHz DIV2 = 0	10-kHz Offset		–84		dBc/Hz
			100-kHz Offset		–111		
			1-MHz Offset		–133		
			5-MHz Offset		–148		
		f_{Fout} = 1409 MHz DIV2 = 1	10-kHz Offset		–90		
			100-kHz Offset		–117		
			1-MHz Offset		–138		
			5-MHz Offset		–150		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ3010E)	f_{Fout} = 3021 MHz DIV2 = 0	10-kHz Offset		–83		dBc/Hz
			100-kHz Offset		–110		
			1-MHz Offset		–132		
			5-MHz Offset		–147		
		f_{Fout} = 1510.5 MHz DIV2 = 1	10-kHz Offset		–88		
			100-kHz Offset		–116		
			1-MHz Offset		–137		
			5-MHz Offset		–148		

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Electrical Characteristics (continued)

(V_{CC} = 3.0 V, –40°C ≤ T_A ≤ 85 °C; except as specified.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INTERFACE (DATA, CLK, LE, CE, Ftest/LD, FLout)						
V_{IH}	High-Level Input Voltage		1.6		2.75	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = 1.75	–3.0		3.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V	–3.0		3.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = 500 µA	2.0	2.65		V
V_{OL}	Low-Level Output Voltage	I_{OL} = –500 µA		0.0	0.4	V

7.6 MICROWIRE Timing Requirements

See Figure 2 and *Serial Data Timing Requirements*.

		MIN	NOM	MAX	UNIT
t_{CS}	Data to Clock Set-Up Time	25			ns
t_{CH}	Data to Clock Hold Time	20			ns
t_{CWH}	Clock Pulse Width High	25			ns
t_{CWL}	Clock Pulse Width Low	25			ns
t_{ES}	Clock to Enable Set-Up Time	25			ns
t_{CES}	Enable to Clock Set-Up Time	25			ns
t_{EWH}	Enable Pulse Width High	25			ns

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7.7 Typical Performance Characteristics

See Table 1.

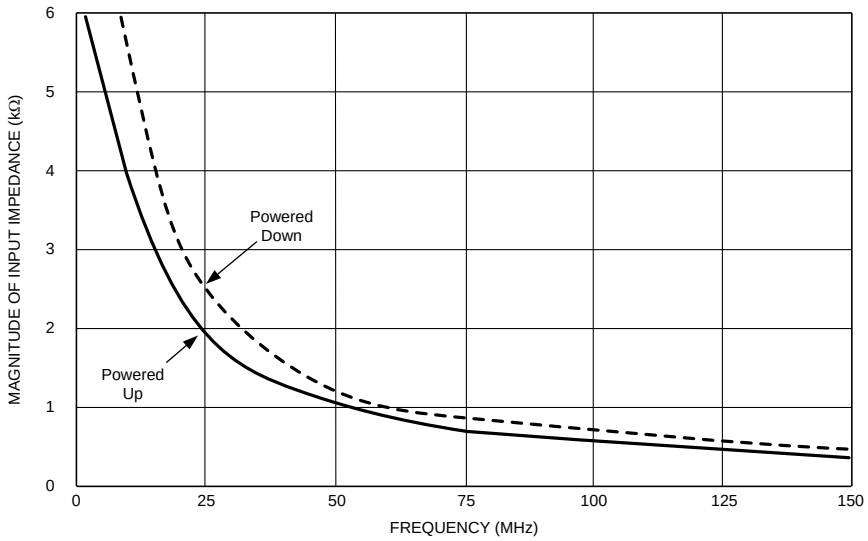


Figure 1. OSCin Input Impedance

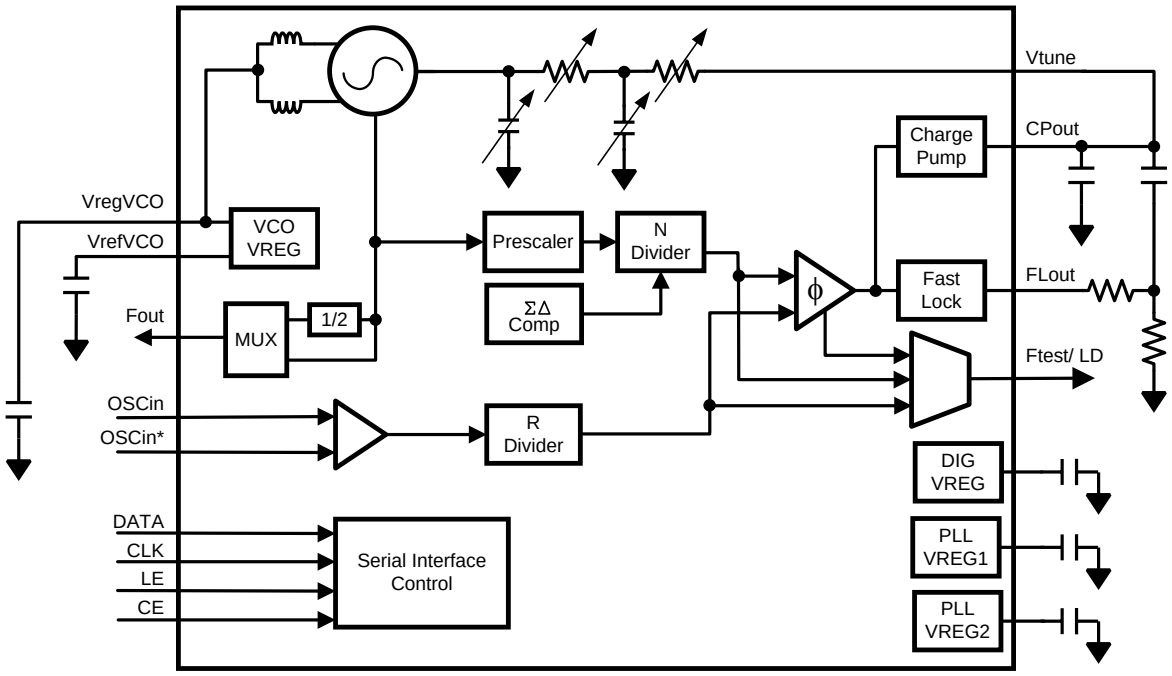
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8 Detailed Description

8.1 Overview

The LMX2531 is a low-power, high-performance frequency synthesizer system which includes the PLL, VCO, and partially integrated loop filter. *Feature Description* gives a discussion of the various blocks of this device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reference Oscillator Input

Because the VCO frequency calibration algorithm is based on clocks from the OSCin pin, there are certain bits that need to be set depending on the OSCin frequency. XTLSEL (R6[22:20]) and XTLDIV (R7[9:8]) are both need to be set based on the OSCin frequency, f_{OSCin}. For some options and for low OSCin frequencies, the XTLMAN (R7[21:10]) and XTLMAN2 (R8[4]) words need to be set to the correct value.

Table 1. OSCin Input Impedance (See Figure 1)

FREQUENCY (MHz)	POWERED UP (kΩ)			POWERED DOWN (kΩ)		
	REAL	IMAGINARY	MAGNITUDE	REAL	IMAGINARY	MAGNITUDE
1	4.98	–2.70	5.66	6.77	–8.14	10.59
5	3.44	–3.04	4.63	5.73	–6.72	9.03
10	1.42	–2.67	3.02	1.72	–5.24	5.51
20	0.52	–1.63	1.71	0.53	–2.94	2.98
30	0.29	–1.22	1.25	0.26	–2.12	2.14
40	0.18	–0.92	0.94	0.17	–1.58	1.59
50	0.13	–0.74	0.75	0.14	–1.24	1.25
60	0.10	–0.63	0.64	0.10	–1.06	1.06
70	0.09	–0.56	0.56	0.09	–0.95	0.95
80	0.07	–0.50	0.50	0.08	–0.86	0.87
90	0.07	–0.46	0.46	0.07	–0.80	0.80

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Feature Description (continued)

Table 1. OSCin Input Impedance (See Figure 1) (continued)

FREQUENCY (MHz)	POWERED UP (kΩ)			POWERED DOWN (kΩ)		
	REAL	IMAGINARY	MAGNITUDE	REAL	IMAGINARY	MAGNITUDE
100	0.06	–0.41	0.42	0.07	–0.72	0.72
110	0.06	–0.37	0.38	0.07	–0.65	0.65
120	0.05	–0.34	0.34	0.06	–0.59	0.59
130	0.05	–0.32	0.32	0.06	–0.55	0.55
140	0.04	–0.29	0.30	0.05	–0.50	0.50
150	0.04	–0.27	0.28	0.05	–0.47	0.47

8.3.2 R Divider

The R divider divides the OSCin frequency down to the phase detector frequency. The R divider value, R, is restricted to the values of 1, 2, 4, 8, 16, and 32. If R is greater than 8, then this also puts restrictions on the fractional denominator, FDEN, than can be used. This is discussed in greater depth in later sections.

8.3.3 Phase Detector and Charge Pump

The phase detector compares the outputs of the R and N dividers and puts out a correction current corresponding to the phase error. The phase detector frequency, f_{PD}, can be calculated as shown in Equation 1.

$$f_{PD} = f_{OSCin} / R \quad (1)$$

Choosing R = 1 yields the highest possible phase detector frequency and is optimum for phase noise, although there are restrictions on the maximum phase detector frequency which could force the R value to be larger. The far out PLL noise improves 3 dB for every doubling of the phase detector frequency, but at lower offsets, this effect is much less due to the PLL 1 / f noise. Aside from getting the best PLL phase noise, higher phase detector frequencies also make it easier to filter the noise that the delta-sigma modulator produces, which peaks at an offset frequency of f_{PD} / 2 from the carrier. The LMX2531 also has 16 levels of charge pump currents and a highly flexible fractional modulus. Increasing the charge pump current improves the phase noise about 3 dB per doubling of the charge pump current, although there are small diminishing returns as the charge pump current increases.

From a loop filter design and PLL phase noise perspective, one might think to always design with the highest possible phase detector frequency and charge pump current. However, if one considers the worst case fractional spurs that occur at an output frequency equal to 1 channel spacing away from a multiple of the f_{OSCin}, then this gives reason to reconsider. If the phase detector frequency or charge pump currents are too high, then these spurs could be degraded, and the loop filter may not be able to filter these spurs as well as theoretically predicted. For optimal spur performance, a phase detector frequency around 2.5 MHz and a charge pump current of 1X are recommended.

8.3.4 N Divider and Fractional Circuitry

The N divider in the LMX2531 includes fractional compensation and can achieve any fractional denominator between 1 and 4,194,303. The integer portion, $N_{Integer}$, is the whole part of the N divider value and the fractional portion, $N_{Fractional}$, is the remaining fraction. So in general, the total N divider value, N, is determined by Equation 2.

$$N = N_{Integer} + N_{Fractional} \quad (2)$$

For example, if the phase detector frequency (f_{PD}) was 10 MHz and the VCO frequency (f_{VCO}) was 1736.1 MHz, then N would be 173.61. This would imply that $N_{Integer}$ is 173 and $N_{Fractional}$ is 61/100. $N_{Integer}$ has some minimum value restrictions that are arise due to the architecture of this divider. The first restrictions arise because the N divider value is actually formed by a quadruple modulus 16/17/20/21 prescaler, which creates minimum divide values. $N_{Integer}$ is further restricted because the LMX2531 due to the fractional engine of the N divider.

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The fractional word, $N_{Fractional}$, is a fraction formed with the NUM and DEN words. In the example used here with the fraction of 61/100, NUM = 61 and DEN = 100. The fractional denominator value, DEN, can be set from 2 to 4,194,303. The case of DEN = 0 makes no sense, because this would cause an infinite N value; the case of 1 makes no sense either (but could be done), because integer mode should be used in these applications. All other values in this range, like 10, 32, 42, 734, or 4,000,000 are all valid. Once the fractional denominator, DEN, is determined, the fractional numerator, NUM, is intended to be varied from 0 to DEN-1.

In general, the fractional denominator, DEN, can be calculated by dividing the phase detector frequency by the greatest common divisor (GCD) of the channel spacing (f_{CH}) and the phase detector frequency. If the channel spacing is not obvious, then it can be calculated as the greatest common divisor of all the desired VCO frequencies.

$$FDEN = k \times f_{PD} / GCD (f_{PD} , f_{CH}) \quad k = 1, 2, 3 .. \tag{3}$$

For example, consider the case of a 10 MHz phase detector frequency and a 200 kHz channel spacing at the VCO output. The greatest common divisor of 10 MHz and 200 kHz is just 200 kHz. If one takes 10 MHz divided by 200 kHz, the result is 50. So a fractional denominator of 50, or any multiple of 50 would work in this example. Now consider a case with a 10 MHz phase detector frequency and a 30 kHz channel spacing. The greatest common divisor of 10 MHz and 30 kHz is 10 kHz. The fractional denominator therefore must be a multiple 1000, because this is 10 MHz divided by 10 kHz. For a final example, consider an application with a fixed output frequency of 2110.8 MHz and a OSCin frequency of 19.68 MHz. If the phase detector frequency is chosen to be 19.68 MHz, then the channel spacing can be calculated as the greatest common multiple of 19.68 MHz and 2110.8 MHz, which is 240 kHz. The fractional denominator is therefore a multiple of 41, which is 19.68 MHz / 240 kHz. Refer to *AN-1865 Frequency Synthesis and Planning for PLL Architectures* (SNAA061) for more details on frequency planning.

To achieve a fractional N value, an integer N divider is modulated between different values. This gives rise to three main degrees of freedom with the LMX2531 delta-sigma engine including the modulator order, dithering, and the way that the fractional portion is expressed. The first degree of freedom is the modulator order, which gives the user the ability to optimize for a particular application. The modulator order can be selected as zero (integer mode), two, three, or four. One simple technique to better understand the impact of the delta-sigma fractional engine on noise and spurs is to tune the VCO to an integer channel and observe the impact of changing the modulator order from integer mode to a higher order. The higher the fractional modulator order is, the lower the spurs theoretically are. However, this is not always the case, and the higher order fractional modulator can sometimes give rise to additional spurious tones, but this is dependent on the application. The second degree of freedom with the LMX2531 delta-sigma engine is dithering. Dithering is often effective in reducing these additional spurious tones, but can add phase noise in some situations. The third degree of freedom is the way that the fraction is expressed. For example, 1/10 can be expressed as 100000/1000000. Expressing the fraction in higher order terms sometimes improves the performance, particularly when dithering is used. In conclusion, there are some guidelines to getting the optimum choice of settings, but these optimum settings are application specific. Refer to *AN-1879 Fractional N Frequency Synthesis* (SNAA062) for a much more detailed discussion on fractional PLLs and fractional spurs.

8.3.5 Partially Integrated Loop Filter

The LMX2531 integrates the third pole (formed by R3 and C3) and fourth pole (formed by R4 and C4) of the loop filter. The values for C3, C4, R3, and R4 can also be programmed independently through the MICROWIRE interface and also R3 and R4 can be changed during FastLock, for minimum lock time. The larger the values of these components, the stronger the attenuation of the internal loop filter. The maximum attenuation can be achieved by setting R3 = R4 = 40 kΩ and C3 = C4 = 100 pF while the minimum attenuation is achieved by disabling the loop filter by setting EN_LPFLTR (R6[15]) to zero. Note that when the internal loop filter is disabled, there is still a small amount of input capacitance on front of the VCO on the order of 200 pF.

Because that the internal loop filter is on-chip, it is more effective at reducing certain spurs than the external loop filter. The higher order poles formed by the integrated loop filter are also helpful for attenuating noise due to the delta-sigma modulator. This noise produced by the delta-sigma modulator is outside the loop bandwidth and dependent on the modulator order. Although setting the filtering for maximum attenuation gives the best filtering, it puts increased restrictions on how wide the loop bandwidth of the system can be, which corresponds to the case where the shunt loop filter capacitor, C1, is zero. Increasing the charge pump current and/or the phase detector frequency increases the maximum attainable loop bandwidth when designing with the integrated filter. It

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is recommended to set the internal loop filter as high as possible without restricting the loop bandwidth of the system more than desired. If some setting between the minimum and maximum value is desired, it is preferable to reduce the resistor values before reducing the capacitor values because this will reduce the thermal noise contribution of the loop filter resistors. For design tools and more information on partially integrated loop filters, go to the Clock Design Tool on www.ti.com.

8.3.6 Low Noise, Fully Integrated VCO

The LMX2531 includes a fully integrated VCO, including the inductors. For optimum phase noise performance, this VCO has frequency and phase noise calibration algorithms. The frequency calibration algorithm is necessary because the VCO internally divides up the frequency range into several bands, to achieve a lower tuning gain, and therefore better phase noise performance. The frequency calibration routine is activated any time that the R0 register is programmed. There are several bits including LOCKMODE and XTLSEL that need to be set properly for this calibration to be performed in a reliable fashion. If the temperature shifts considerably and the R0 register is not programmed, then it cannot drift more than the maximum allowable drift for continuous lock, ΔT_{CL}, or else the VCO is not ensured to stay in lock. The phase noise calibration algorithm is necessary to achieve the lowest possible phase noise. Each version of the LMX2531, the VCO_ACI_SEL bit (R6[19:16]) needs to be set to the correct value to ensure the best possible phase noise.

The gain of the VCO can change considerably over frequency. It is lowest at the minimum frequency and highest at the maximum frequency. This range is specified in *Electrical Characteristics* of the data sheet. When designing the loop filter, the following method is recommended to determine what VCO gain to design to. First, take the geometric mean of the minimum and maximum frequencies that are to be used. Then use a linear approximation to extrapolate the VCO gain. Suppose the application requires the LMX2531LQ2080E PLL to tune from 2100 to 2150 MHz. The geometric mean of these frequencies is sqrt (2100 × 2150) MHz = 2125 MHz. The VCO gain is specified as 9 MHz/V at 1904 MHz and 20 MHz/V at 2274 MHz. Over this range of 370 MHz, the VCO gain changes 11 MHz/V. Therefore, at 2125 MHz, the VCO gain would be approximately 9 + (2125 – 1904) × 11 / 370 = 15.6 MHz/V. Although the VCO gain can change from part to part, this variation is small compared to how much the VCO gain can change over frequency.

The VCO frequency is related to the other frequencies and divider values as shown in Equation 4.

$$f_{VCO} = f_{PD} \times N = f_{OSCin} \times N / R \quad (4)$$

8.3.7 Programmable VCO Divider

All options of the LMX2531 offer the option of dividing the VCO output by two to get half of the VCO frequency at the Fout pin. The channel spacing at the Fout pin is also divided by two as well. Because this divide by two is outside feedback path between the VCO and the PLL, enabling does require one to change the N divider, R divider, or loop filter values. When this divider is enabled, there will be some far-out phase noise contribution to the VCO noise. Note that the R0 register should be reprogrammed the first time after the DIV2 bit is enabled or disabled for optimal phase noise performance. The frequency at the Fout pin is related to the VCO frequency and divider value, D, as shown in Equation 5.

$$f_{Fout} = f_{VCO} / D \quad (5)$$

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8.3.8 Serial Data Timing Requirements

See *MICROWIRE Timing Requirements*.

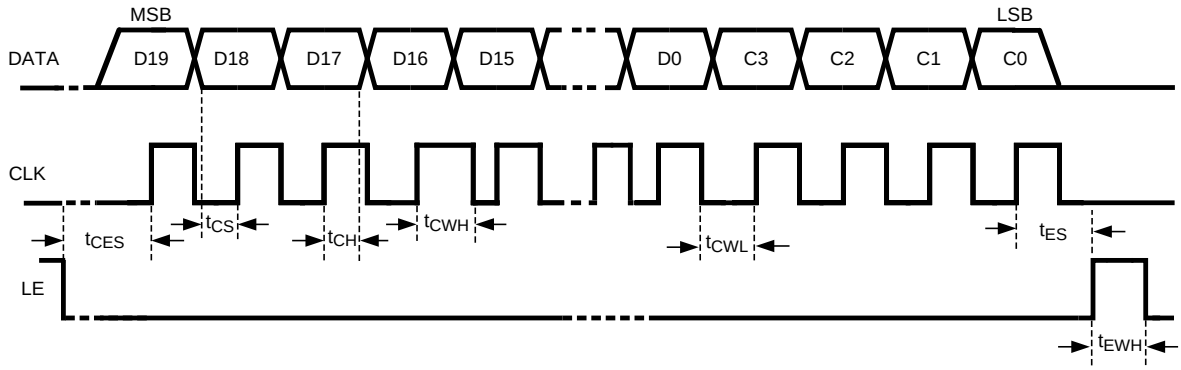


Figure 2. Serial Data Timing Diagram

The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter. There are several other considerations as well:

- A slew rate of at least 30 V/µs is recommended for the CLK, DATA, and LE signals.
- After the programming is complete, the CLK, DATA, and LE signals should be returned to a low state.
- It is recommended to put a small delay between the falling edge of the last CLK pulse and the rising edge of the LE pulse for optimal noise immunity and the most reliable programming.
- Although it is strongly recommended to keep LE low after programming, LE can be kept high if bit R5[23] is changed to 0 (from its default value of 1). If this bit is changed, then the operation of the part is not ensured because it is not tested under these conditions.
- If the CLK and DATA lines are toggled while the in VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.
- If the part is not programmed, the values of the registers in this part have to be assumed to be random. Therefore, the current consumption and spurs generated by this part can be random. If this is an issue, the CE pin can be held low for more consistent behavior.

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8.4 Device Functional Modes

The LMX2531 operates mainly in the active mode. The other two modes are reset and powerdown modes. The powerdown mode can be achieved by taking the CE pin to 0 V. The reset mode is achieved if the REG_RST bit is set to 1.

8.5 Programming

The LMX2531 is programmed using 11 24-bit registers used to control the LMX2531 operation. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 register bits, CTRL[3:0] form the address field, which is used to decode the internal register address. The remaining 20 bits form the data field DATA[19:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank. Although there are actually 14 registers in this part, only a portion of them should be programmed, because the state of the other hidden registers (R13, R11, and R10) are set during the initialization sequence. Although it is possible to program these hidden registers, as well as a lot of bits that are defined to either 1 or 0, the user should not experiment with these hidden registers and bits, because the parts are not tested under these conditions and doing so will most likely degrade performance.

Table 2. Register Location Truth Table

C3	C2	C1	C0	Data Address
1	1	0	0	R12
1	0	0	1	R9
1	0	0	0	R8
0	1	1	1	R7
0	1	1	0	R6
0	1	0	1	R5
0	1	0	0	R4
0	0	1	1	R3
0	0	1	0	R2
0	0	0	1	R1
0	0	0	0	R0

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8.6 Register Maps

8.6.1 General Programming Information

Table 3. Programming Register Structure

DATA[19:0]																				CONTROL[3:0]			
MSB																							LSB
D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C3	C2	C1	C0

8.6.1.1 Initialization Sequence

The initial loading sequence from a cold start is described in Table 4. The registers must be programmed in order shown. There must be a minimum of 10 ms between the time when R5 is last loaded and R1 is loaded to ensure time for the LDOs to power up properly.

Table 4. Initialization Sequence

REG.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R5 INIT1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5 INIT2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1
R12	Program R12 as shown in the complete register map.																				1	1	0	0
R9	Program R9 as shown in the complete register map.																				1	0	0	1
R8	See individual section for Register R8 programming information. Programming of this register is necessary under specific circumstances.																				1	0	0	0
R7	See individual section for Register R7 programming information.																				0	1	1	1
R6	See individual section for Register R6 programming information.																				0	1	1	0
R4	See individual section for Register R4 programming information. Register R4 only needs to be programmed if FastLock is used.																				0	1	0	0
R3	See individual section for Register R3 programming information.																				0	0	1	1
R2	See individual section for Register R2 programming information.																				0	0	1	0
R1	See individual section for Register R1 programming information.																				0	0	0	1
R0	See individual section for Register R0 programming information.																				0	0	0	0

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8.6.1.2 Complete Register Content Map

Table 5 shows all the programmable bits for the LMX2531. No programming order or initialization sequence is implied by Table 5, only the location of the programming information.

Table 5. Complete Register Content Map

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R0	N [7:0]								NUM [11:0]												0	0	0	0
R1	0	0	1	ICP [3:0]				N [10:8]			NUM [21:12]										0	0	0	1
R2	0	1	DEN [11:0]												R [5:0]						0	0	1	0
R3	DIV2	FDM	DITHER [1:0]		ORDER [1:0]		FoLD [3:0]				DEN [21:12]										0	0	1	1
R4	0	0	ICPFL [3:0]				TOC [13:0]														0	1	0	0
R5	1	0	0	0	0	REG_RST	0	0	0	0	0	0	0	EN_DIG LDO	EN_PLL LDO2	EN_PLL LDO1	EN_VCO LD	EN_OSC	EN_VCO	EN_PLL	0	1	0	1
R6	0	XTLSEL [2:0]			VCO_ACI_SEL [3:0]			EN_LPF LTR	R4_ADJ [1:0]		R4_ADJ_FL [1:0]		R3_ADJ [1:0]		R3_ADJ_FL [1:0]		C3_4_ADJ [2:0]				0	1	1	0
R7	0	0	XTLMAN [11:0]												XTLDIV [1:0]		0	0	0	0	0	1	1	1
R8	0	0	0	0	0	0	1	LOCK MODE		0	0	0	0	0	0	0	0	0	0	XTLMAN2	1	0	0	0
R9	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1
R12	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0

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8.6.1.3 Register R0

The action of programming the R0 register activates a frequency calibration routine for the VCO. This calibration is necessary to get the VCO to center the tuning voltage for optimal performance. If the temperature drifts considerably, then the PLL should stay in lock, provided that the temperature drift specification is not violated.

8.6.1.3.1 NUM[10:0] and NUM[21:12] -- Fractional Numerator

The NUM word is split between the R0 register and R1 register. The Numerator bits determine the fractional numerator for the delta-sigma PLL. This value can go from 0 to 4095 when the FDM bit (R3[22]) is 0 (the other bits in this register are ignored), or 0 to 4194303 when the FDM bit is 1.

Table 6. Fractional Numerator

FRACTIONAL NUMERATOR	NUM[21:12]										NUM[11:0]											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
409503	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note that there are restrictions on the fractional numerator value depending on the R divider value if it is 16 or 32.

8.6.1.3.2 N[7:0] and N[10:8]

The N counter is 11 bits. 8 of these bits are located in the R0 register, and the remaining 3 (MSB bits) are located in the R1 register. The LMX2531 consists of an A, B, and C counter, which work in conjunction with the 16/17/20/21 prescaler to form the final N counter value.

Table 7. N Divider Value

	N[10:8]			N[7:0]						
N Value	C							B	A	
<48	Values less than 48 are prohibited.									
48 - 51	Possible ONLY with ORDER = 1 (Reset Modulator)									
52-54	Values of 52 - 54 are prohibited.									
55	0	0	0	0	0	1	1	0	1	1	1
...											
2039	1	1	1	1	1	1	1	0	1	1	1

8.6.1.4 Register R1

8.6.1.4.1 NUM[21:12]

These are the MSB bits in for the fractional numerator that already have been described.

8.6.1.4.2 N[10:8] -- 3 MSB Bits for the N Counter

These are the 2 MSB bits for the N counter, which were discussed in *Register R0*.

8.6.1.4.3 ICP[3:0] -- Charge Pump Current

This bit programs the charge pump current in from 90 µA to 1440 µA in 90 µA steps. In general, higher charge pump currents yield better phase noise for the PLL, but also can cause higher spurs.

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Table 8. Charge Pump Current

ICP	CHARGE PUMP STATE	TYPICAL CHARGE PUMP CURRENT at 3 VOLTS (µA)
0	1X	90
1	2X	180
2	3X	270
3	4X	360
4	5X	450
5	6X	540
6	7X	630
7	8X	720
8	9X	810
9	10X	900
10	11X	990
11	12X	1080
12	13X	1170
13	14X	1260
14	15X	1350
15	16X	1440

8.6.1.5 Register R2

8.6.1.5.1 R[5:0] -- R Counter Value

These bits determine the phase detector frequency. The OSCin frequency is divided by this R counter value. Note that only the values of 1, 2, 4, 8, 16, and 32 are allowed.

Table 9. R Divider Value

R VALUE	FRACTIONAL DENOMINATOR RESTRICTIONS	R[5:0]					
0,3,5-7, 9-15,17-31, 33-63	n/a	These values are illegal.					
1	none	0	0	0	0	0	1
2	none	0	0	0	0	1	0
4	none	0	0	0	1	0	0
8	none	0	0	1	0	0	0
16	Must be divisible by 2	0	1	0	0	0	0
32	Must be divisible by 4	1	0	0	0	0	0

The R counter value can put some restrictions on the fractional denominator. In the case that it is 16, the fractional denominator must be divisible by 2, which is equivalent to saying that the LSB of the fractional denominator word is zero. In the case that the R counter is 32, the two LSB bits of the fractional denominator word must also be zero, which is equivalent to saying that the fractional denominator must be divisible by 4. Because the fractional denominator can be very large, this should cause no issues. For instance, if one wanted to achieve a fractional word of 1/65, and the R counter value was 16, the fractional word could be changed to 4/260, and the same resolution could be achieved.

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8.6.1.5.2 DEN[21:12] and DEN[11:0]-- Fractional Denominator

These bits determine the fractional denominator. Note that the MSB bits for this word are in register R3. If the FDM bit is set to 0, DEN[21:12] are ignored. The fractional denominator should only be set to zero if the fractional circuitry is being disabled by setting ORDER = 1. A value of one never makes sense to use. All other values could reasonably be used in fractional mode.

Table 10. Fractional Denominator

FRACTIONAL DENOMINATOR	DEN[21:12]										DEN[11:0]											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4095	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.6.1.6 Register R3

8.6.1.6.1 DEN[21:12] -- Extension for the Fractional Denominator

These are the MSB bits of the DEN word, which have already been discussed.

8.6.1.6.2 FoLD[3:0] -- Multiplexed Output for Ftest/LD Pin

The FoLD[3:0] word is used to program the output of the Ftest/LD pin. This pin can be used for a general purpose I/O pin, a lock detect pin, and for diagnostic purposes. When programmed to the digital lock detect state, the output of the Ftest/LD pin will be high when the part is in lock, and low otherwise. Lock is determined by comparing the input phases to the phase detector. The analog lock detect modes put out a high signal with very fast negative pulses, that correspond to when the charge pump comes on. This output can be low pass filtered with an RC filter to determine the lock detect state. If the open drain state is used, a additional pullup resistor is required. For diagnostic purposes, the options that allow one to view the output of the R counter or the N counter can be very useful. Be aware that the output voltage level of the Ftest/LD is not equal to the supply voltage of the part, but rather is given by V_{OH} and V_{OL} in *Electrical Characteristics*.

Table 11. Ftest/LD Pin Functions

FoLD	OUTPUT TYPE	FUNCTION
0	High Impedance	Disabled
1	Push-Pull	Logical High State
2	Push-Pull	Logical Low State
3	Push-Pull	Digital Lock Detect
4	N/A	Reserved
5	Push-Pull	N Counter Output Divided by 2
6	Open-Drain	Analog Lock Detect
7	Push-Pull	Analog Lock Detect
8	N/A	Reserved
9	N/A	Reserved
10	N/A	Reserved
11	N/A	Reserved
12	N/A	Reserved
13	N/A	Reserved
14	Push-Pull	R Counter Output
15	N/A	Reserved

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8.6.1.6.3 ORDER -- Order of Delta-Sigma Modulator

This bit determines the order of the delta-sigma modulator in the PLL. In general, higher order fractional modulators tend to reduce the primary fractional spurs that occur at increments of the channel spacing, but can also create spurs that are at a fraction of the channel spacing, if there is not sufficient filtering. The optimal choice of modulator order is very application specific, however, a third order modulator is a good starting point if not sure what to try first.

Table 12. Delta-Sigma Modulator

ORDER	DELTA-SIGMA MODULATOR ORDER
0	Fourth
1	Reset Modulator (Integer Mode - all fractions are ignored)
2	Second
3	Third

8.6.1.6.4 DITHER -- Dithering

Dithering is useful in reducing fractional spurs, especially those that occur at a fraction of the channel spacing. The only exception is when the fractional numerator is zero. In this case, dithering usually is not a benefit. Dithering also can sometimes increase the PLL phase noise by a fraction of a dB. In general, if dithering is disabled, phase noise may be slightly better inside the loop bandwidth of the system, but spurs are likely to be worse too.

Table 13. Fractional Dithering

DITHER	DITHERING MODE
0	Weak Dithering
1	Reserved
2	Strong Dithering
3	Dithering Disabled

8.6.1.6.5 FDM -- Fractional Denominator Mode

When this bit is set to 1, the 10 MSB bits for the fractional numerator and denominator are considered. This allows the fractional denominator to range from 1 to 4,194,303. If this bit is set to zero, only the 12 LSB bits of the fractional numerator and denominator are considered, and this allows a fractional denominator from 1 to 4095. When this bit is disabled, the current consumption is about 0.5 mA lower.

8.6.1.6.6 DIV2

When this bit is enabled, the output of the VCO is divided by 2. Enabling this bit does have some impact on harmonic content and output power.

Table 14. VCO Output Divider

DIV2	VCO OUTPUT FREQUENCY
0	Not Divided by 2
1	Divided by 2

8.6.1.7 Register R4

8.6.1.7.1 TOC[13:0] -- Time-Out Counter for FastLock

When the value of this word is 3 or less, then FastLock is disabled, and this pin can only be used for general purpose I/O. When this value is 4 or greater, the time-out counter is engaged for the amount of phase detector cycles shown in Table 15.

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Table 15. FastLock Timeout Counter

TOC VALUE	FLout PIN STATE	TIMEOUT COUNT
0	High Impedance	0
1	Low	Always Enabled
2	Low	0
3	High	0
4	Low	4 × 2 Phase Detector
.	.	.
16383	Low	16383 × 2 Phase Detector

When this count is active, the FLout pin is grounded, the FastLock current is engaged, and the resistors R3 and R4 are also potentially changed. The table below summarizes the bits that control various values in and out of FastLock differences.

Table 16. FastLock Filter Values

FastLock STATE	FLout	CHARGE PUMP CURRENT	R3	R4
Steady State	High Impedance	ICP	R3_ADJ	R4_ADJ
Fastlock	Grounded	ICPFL	R3_ADJ_FL	R4_ADJ_FL

8.6.1.7.2 ICPFL[3:0] -- Charge Pump Current for Fastlock

When FastLock is enabled, this is the charge pump current that is used for faster lock time.

Table 17. FastLock Charge Pump Current

ICPFL	Fastlock CHARGE PUMP STATE	TYPICAL Fastlock CHARGE PUMP CURRENT at 3 VOLTS (µA)
0	1X	90
1	2X	180
2	3X	270
3	4X	360
4	5X	450
5	6X	540
6	7X	630
7	8X	720
8	9X	810
9	10X	900
10	11X	990
11	12X	1080
12	13X	1170
13	14X	1260
14	15X	1350
15	16X	1440

8.6.1.8 Register R5

8.6.1.8.1 EN_PLL -- Enable Bit for PLL

When this bit is set to 1 (default), the PLL is powered up, otherwise, it is powered down.

8.6.1.8.2 EN_VCO -- Enable Bit for the VCO

When this bit is set to 1 (default), the VCO is powered up, otherwise, it is powered down.

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8.6.1.8.3 EN_OSC -- Enable Bit for the Oscillator Inverter

When this bit is set to 1 (default), the reference oscillator is powered up, otherwise it is powered down.

8.6.1.8.4 EN_VCOLDO -- Enable Bit for the VCO LDO

When this bit is set to 1 (default), the VCO LDO is powered up, otherwise it is powered down.

8.6.1.8.5 EN_PLLLDO1 -- Enable Bit for the PLL LDO 1

When this bit is set to 1 (default), the PLL LDO 1 is powered up, otherwise it is powered down.

8.6.1.8.6 EN_PLLLDO2 -- Enable Bit for the PLL LDO 2

When this bit is set to 1 (default), the PLL LDO 2 is powered up, otherwise it is powered down.

8.6.1.8.7 EN_DIGLDO -- Enable Bit for the digital LDO

When this bit is set to 1 (default), the Digital LDO is powered up, otherwise it is powered down.

8.6.1.8.8 REG_RST -- Resets All Registers to Default Settings

This bit needs to be programmed three times to initialize the part. When this bit is set to one, all registers are set to default mode, and the part is powered down. The second time the R5 register is programmed with REG_RST = 0, the register reset is released and the default states are still in the registers. However, because the default states for the blocks and LDOs is powered off, it is therefore necessary to program R5 a third time so that all the LDOs and blocks can be programmed to a power up state. When this bit is set to 1, all registers are set to the default modes, but part is powered down. For normal operation, this bit is set to 0. Once this initialization is done, it is not necessary to do this again unless power is removed from the device.

8.6.1.9 Register R6

8.6.1.9.1 C3_C4_ADJ[2:0] -- Value FOR C3 and C4 In The Internal Loop Filter

Table 18. Internal Loop Filter Capacitors

C3_C4_ADJ	C3 (pF)	C4 (pF)
0	50	50
1	50	100
2	50	150
3	100	50
4	150	50
5	100	100
6	50	150
7	50	150

8.6.1.9.2 R3_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R3 During Fastlock

Table 19. Internal Loop Filter Resistor R3 During Fastlock

R3_ADJ_FL Value	R3 RESISTOR DURING Fastlock (kΩ)
0	10
1	20
2	30
3	40

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8.6.1.9.3 R3_ADJ[1:0] -- Value for Internal Loop Filter Resistor R3

Table 20. Internal Loop Filter Resistor R3

R3_ADJ	R3 VALUE (kΩ)
0	10
1	20
2	30
3	40

8.6.1.9.4 R4_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R4 During Fastlock

Table 21. Internal Loop Filter Resistor R4 During FastLock

R4_ADJ_FL	R4 VALUE DURING Fast Lock (kΩ)
0	10
1	20
2	30
3	40

8.6.1.9.5 R4_ADJ[1:0] -- Value for Internal Loop Filter Resistor R4

Table 22. Internal Loop Filter Resistor R4

R4_ADJ	R4 VALUE (kΩ)
0	10
1	20
2	30
3	40

8.6.1.9.6 EN_LPFLTR-- Enable for Partially Integrated Internal Loop Filter

The Enable Loop Filter bit is used to enable or disable the third and fourth pole on-chip loop filters.

Table 23. Enable Bit for Internal Loop Filter

EN_LPFLTR	3rd and 4th POLES of LOOP FILTER
0	disabled (R3 = R4 = 0 Ω and C3 + C4 = 200 pF)
1	enabled

8.6.1.9.7 VCO_ACI_SEL

This bit is used to optimize the VCO phase noise. The recommended values are what are used for all testing purposes, and this bit should be set as instructed in the following table.

Table 24. VCO ACI Selection

PART	VCO_ACI_SEL
All Other Options	8
LMX2531LQ2265E LMX2531LQ2570E LMX2531LQ2820E LMX2531LQ3010E	6

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8.6.1.9.8 XTLSEL[2:0] -- OSCin Select

The XTLSEL bit is used to select between manual oscin mode and one of the automatic modes. The user may choose manual oscin mode (XTLSEL = 4) and program the XTLMAN (R7[21:10]) and XTLMAN2 (R7[4]) bits for a specific OSCin frequency, or one of the automatic modes (XTLSEL = 0, 1, 2, 3). For the LMX2531LQ2080E/2570E options or when the OSCin frequency is less than 8 MHz, manual oscin mode must always be selected. The automatic modes can be used for the other frequency options. When using one of the automatic modes, XTLSEL should be set based on the OSCin frequency.

Table 25. OSCin Frequency Select

XTLSEL	MODE	OSCin FREQUENCY
0	**Automatic Modes** Programming of XTLMAN (R7[21:10]) not required. Programming of XTLMAN2 (R7[4]) not required.	8 — 25 MHz
1		25 — 50 MHz
2		50 — 70 MHz
3		70 — 80 MHz
4	**Manual OSCin Mode** Must use this for LMX2531LQ2080E/2570E/2820E/3010E Must use this if f_{OSCin} < 8 MHz Programming of XTLMAN (R7[21:10]) required. Programming of XTLMAN2 (R7[4]) may be required.	5 — 80 MHz
5, 6, 7	Reserved	

8.6.1.10 Register R7

8.6.1.10.1 XTLDIV[1:0] -- Division Ratio for the OSCin Frequency

The frequency provided to the VCO frequency calibration circuitry is based on the OSCin frequency divided down by a factor, determined by the XTLDIV word. Note that this division ratio is independent of the R counter value or the phase detector frequency. The necessary division ratio depends on the OSCin frequency and is shown in Table 26.

Table 26. OSCin Division Ratio

XTLDIV	OSCin DIVISION RATIO	OSCin RANGE
0	Reserved	Reserved
1	Divide by 2	< 20 MHz
2	Divide by 4	20 — 40 MHz
3	Divide by 8	> 40 MHz

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8.6.1.10.2 XTLMAN[11:0] -- Manual OSCin Mode

XTLMAN must be programmed if word XTLSEL (*XTLSEL[2:0] -- OSCin Select*) is set to manual OSCin mode. In the table below, the proper value for XTLMAN is shown based on some common OSCin frequencies (f_{OSCin}) and various LMX2531 options. For any OSCin frequency XTLMAN can be calculated as 16 × f_{OSCin} / Kbit. f_{OSCin} is expressed in MHz and Kbit values for the LMX2531 frequency options can be found in Table 28.

Table 27. XTLMAN Values for Common OSCin Frequencies

DEVICE	f_{OSCin}					
	5 MHz	10 MHz	20 MHz	30.72 MHz	61.44 MHz	76.8 MHz
LMX2531LQ1146E	53	107	213	327	655	819
LMX2531LQ1226E	53	107	213	327	655	819
LMX2531LQ1312E	47	94	188	289	578	722
LMX2531LQ1415E	47	94	188	289	578	722
LMX2531LQ1500E	40	80	160	246	492	614
LMX1531LQ1515E	40	80	160	246	492	614
LMX2531LQ1570E	38	76	152	234	468	585
LMX2531LQ1650E	38	76	152	234	468	585
LMX2531LQ1700E	35	70	139	214	427	534
LMX2531LQ1742	32	64	128	197	393	492
LMX2531LQ1778E	31	62	123	189	378	473
LMX2531LQ1910E	27	53	107	164	328	410
LMX2531LQ2265E	20	40	80	123	246	307
LMX2531LQ2080E	18	36	71	109	218	273
LMX2531LQ2570E	13	27	53	82	164	205
LMX2531LQ2820E	11	23	46	70	140	178
LMX2531LQ3010E	10	20	40	61	123	154

Table 28. Kbit Values for Various LMX2531 Options

DEVICE	Kbit
LMX2531LQ1146E	1.5
LMX2531LQ1226E	1.5
LMX2531LQ1312E	1.7
LMX2531LQ1415E	1.7
LMX2531LQ1500E	2
LMX2531LQ1515E	2
LMX2531LQ1570E	2.1
LMX2531LQ1650E	2.1
LMX2531LQ1700E	2.3
LMX25311742	2.5
LMX2531LQ1778E	2.6
LMX2531LQ1910E	3
LMX2531LQ2265E	4
LMX2531LQ2080E	4.5
LMX2531LQ2570E	6
LMX2531LQ2820E	7
LMX2531LQ3010E	8

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8.6.1.11 Register R8

8.6.1.11.1 XTLMAN2 -- Manual Crystal Mode Second Adjustment

This bit also adjusts the calibration timing for lock time. In the case that manual mode for XTLSEL is selected and the OSCin frequency is greater than 40 MHz, this bit should be enabled, otherwise it should be 0.

8.6.1.11.2 LOCKMODE -- Frequency Calibration Mode

This bit controls the method for which the VCO frequency calibration is done. The two valid modes are linear mode and mixed mode. Linear mode works by searching through the VCO frequency bands in a consecutive manner. Mixed mode works by initially using a divide and conquer approach and then using a linear approach. For small frequency changes, linear mode is faster and for large frequency changes, mixed mode is faster. Linear mode can always be used, but there are restrictions for when Mixed Mode can be used.

Table 29. Lockmode Settings

LOCKMODE	DESCRIPTION	CONDITIONS on OPTIONS	CONDITIONS on OSCin FREQUENCY
0	Reserved	Never use this mode	
1	Linear Mode	Works over all options and all valid OSCin Frequencies	
2	Mixed Mode	All but the following options LMX2531LQ1146E/1226E/1312E/1415E/1515E	$f_{OSCin} \geq 8$ MHz
3	Reserved	Never use this mode	

8.6.1.12 Register R9

All the bits in this register should be programmed as shown in *Complete Register Content Map*.

8.6.1.13 Register R12

Even though this register does not have user-selectable bits, it still needs to be programmed. This register should be loaded as shown in *Complete Register Content Map*.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMX2531 can be used in a broad class of applications. In general, they tend to fall in the categories where the output frequency is a nicely related input frequency and those that require fractional mode. The following schematic generally applies to most applications.

9.2 Typical Application

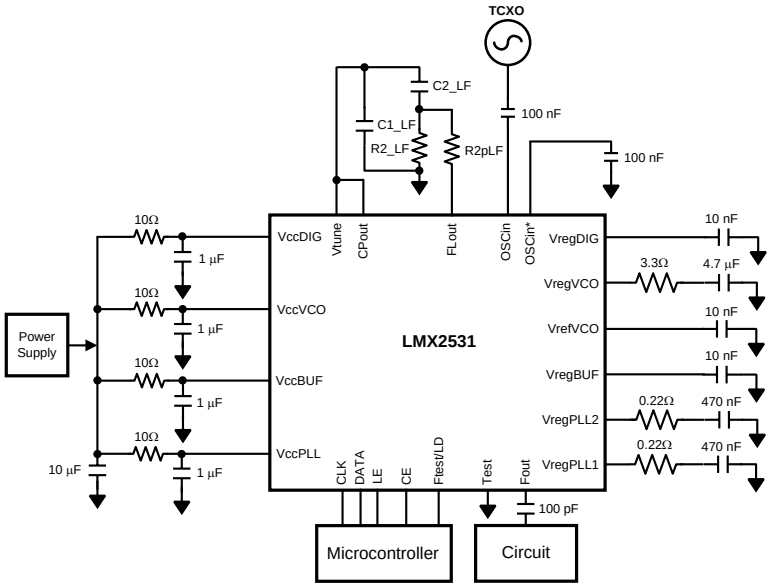


Table 30. Typical Connection Diagram

PIN(S)	APPLICATION INFORMATION
Vcc, Vreg, and Vref Pins	Consult the power supply recommendations for these pins.
CLK DATA LE	Because the maximum voltage on these pins is less than the minimum Vcc voltage, level shifting may be required if the output voltage of the microcontroller is too high. This can be accomplished with a resistive divider.
CE	As with the CLK, DATA, and LE pins, level shifting may be required if the output voltage of the microcontroller is too high. A resistive divider or a series diode are two ways to accomplish this. The diode has the advantage that no current flows through it when the chip is powered down.
Ftest/LD	It is an option to use the lock detect information from this pin.
Fout	This is the high frequency output. This needs to be AC coupled, and matching may also be required. The value of the DC blocking capacitor may be changed, depending on the output frequency.
CPout Vtune	In most cases, it is sufficient to short these together, although there always the option of adding additional poles. C1_LF, C2_LF, and R2_LF are used in conjunction with the internal loop filter to make a fourth order loop filter.
R2pLF	This is the fastlock resistor, which can be useful in many cases, because the spurs are often better with low charge pump currents, and the internal loop filter can be adjusted during fastlock.
OSCin	This is the reference oscillator input pin. It needs to be AC coupled.
OSCin*	If the device is being driven single-ended, this pin needs to be shunted to ground with a capacitor.

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Typical Application (continued)

9.2.1 Design Requirements

Consider generating 1500-MHz fixed frequency from a fixed 10-MHz input frequency. This is the situation similar that was used for the LMX2531LQ1500E evaluation board.

For this design example, use the parameters listed in Table 31 as the user-input parameters.

Table 31. Design Procedure

PARAMETER	VALUE	REASON FOR CHOOSING
Fout	1500 MHz	This value was given.
Fosc	10 MHz	This value was given.
Fpd	10 MHz	This maximized for the best phase noise performance. This is an integer PLL design, so it makes sense to maximize this. If Fpd 10 MHz it was a fractional design, then sometimes lowering this frequency can improve fractional spurs.
Loop Bandwidth	11.5 kHz	This is wider for better jitter, but it is also restricted by the internal loop filter
Phase Margin	76.8 deg	Choosing a high phase margin is good for better jitter.
Kpd	16x	Higher charge pump gains are better for better PLL phase noise
C3_LF	50 pF	In general, the internal loop filter restricts how wide the loop bandwidth can be. Although a wider loop bandwidth could be obtained by switching out the internal loop filter altogether, it is nice to have some internal poles to filter some unwanted spurs. So this is the minimum setting for the internal loop filter.
C4_LF	50 pF	
R3_LF	10 kΩ	
R4_LF	10 kΩ	
C1_LF	Open	The internal loop filter restricts the loop bandwidth. By making C1_LF=open, this maximizes the achievable bandwidth for a particular setup condition.
C2_LF	82 nF	These can be calculated with the Clock Architect.
R2_LF	1.5 kΩ	These can be calculated with the Clock Architect.
ORDER	"Reset Modulator"	The device should be set to integer mode.
DITHER	"Disabled"	Dithering does not help in integer mode.
XTLMAN	80	This is a setting for the LMX2531LQ1500E for a 10 MHz input.

9.2.2 Detailed Design Procedure

Use the WEBENCH® Clock Architect to calculate the values of C2_LF and R2_LF.

Set the device to integer mode and DITHER to disabled.

9.2.3 Application Curves

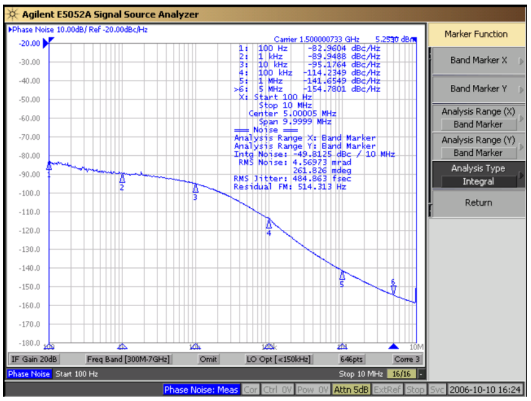


Figure 3. Closed Loop Phase Noise

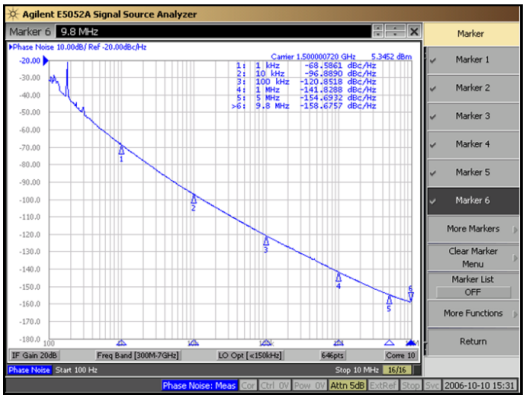


Figure 4. Open Loop VCO Noise

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9.3 Do's and Don'ts

Category	Do	Don't	Why
Loop Filter Design	For integer Designs: Maximize charge pump current and phase detector frequency.	For Fractional Designs: Blindly maximize charge pump current and phase detector frequency.	Maximizing the charge pump current and phase detector frequency give the best PLL phase noise and also allow a wider bandwidth with the internal filter engaged. However, increasing these also increase the integer boundary spur. So for a fractional design, these need to be balanced against fractional spurs.
Partially Integrated Loop Filter	Be aware that engaging this can restrict the loop filter bandwidth. Use TI simulation tools to see how wide the bandwidth can be.	Design for the widest possible bandwidth with the integrated filter engaged and be surprised when the bandwidth is smaller.	Enabling the internal loop filter poles provides useful filtering, but also restricts how wide the loop bandwidth can be.
"No Connect" and DAP Pins	Ground the DAP Pin	Ground the "No Connect" Pins where the pin description says "Do Not Ground".	The DAP is grounded and used. However, if the terminal description says "Do not ground" this is for a reason. Some of these pins are for the VCO tank circuit. There are other no connect pins that are true no connect, but there is no advantage to grounding them. Note that the pad labeled "NC" above pins 14 and 15 should NOT be grounded.

10 Power Supply Recommendations

The device is designed to operate within a recommended supply voltage range of 2.8 V to 3.2 V. Do not exceed the values listed in the *Absolute Maximum Ratings* table. If the supply is not available, ensure that the CLK, DATA, LE, and CE pins are held low. A power-on reset (POR) feature is not available for this device.

11 Layout

11.1 Layout Guidelines

For the layout of the LMX2531, perhaps the most important factor is to be aware of the package footprint. The asymmetrical land pattern can cause issues if not correctly done.

11.1.1 Typical Connection Diagram

11.1.1.1 VccDIG, VccVCO, VccBUF, and VccPLL

These pins are inputs to voltage regulators. Because the LMX2531 contains internal regulators, the power supply noise rejection is very good and capacitors at this pin are not critical. An RC filter can be used to reduce supply noise, but if the capacitor is too large and is placed too close to these pins, they can sometimes cause phase noise degradation in the 100 — 300 kHz offset range. Recommended values are from open to 1 µF. The 10 Ω series resistors serve to filter power supply noise and isolate these pins from large capacitances.

11.1.1.2 VregDIG

A bypass capacitor of 10 nF is recommended.

11.1.1.3 VrefVCO

If the VrefVCO capacitor is changed, it is recommended to keep this capacitor between 1/100 and 1/1000 of the value of the VregVCO capacitor.

11.1.1.4 VregVCO

Because this pin is the output of a regulator, there are stability concerns if there is not sufficient series resistance. For ceramic capacitors, the ESR (Equivalent Series Resistance) is too low, and it is recommended that a series resistance of 1 — 3.3 Ω is necessary. If there is insufficient ESR, then there may be degradation in the phase noise, especially in the 100 — 300 kHz offset. Recommended values are from 1 µF to 10 µF.

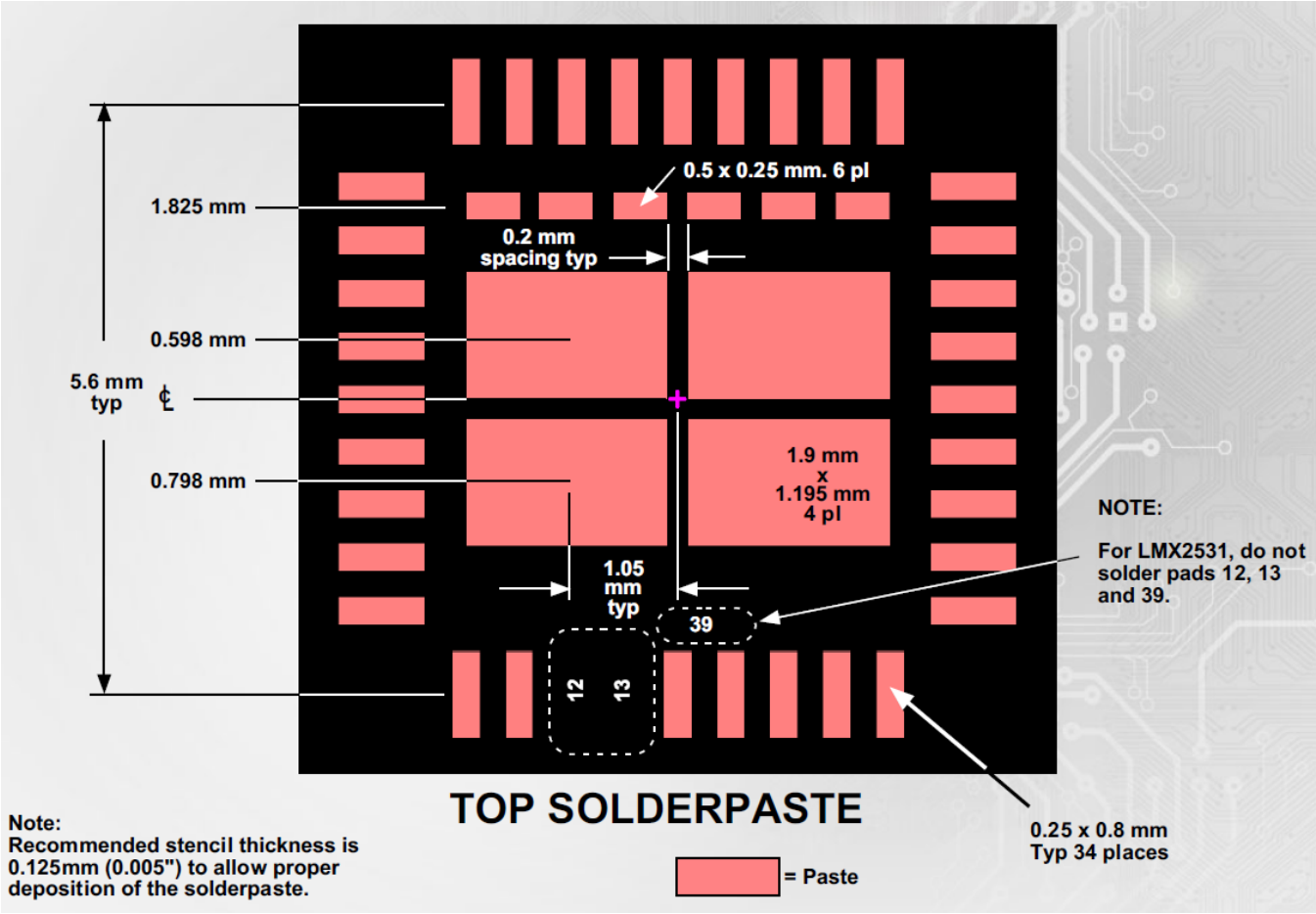
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Layout Guidelines (continued)

11.1.1.5 VregPLL1VregPLL2

The choice of the capacitor value at this pin involves a trade-off between integer spurs and phase noise in the 100 — 300 kHz offset range. Using a series resistor of about 220 mΩ in series with a capacitance that has an impedance of about 150 mΩ at the phase detector frequency seems to give an optimal trade-off. For instance, if the phase detector frequency is 2.5 MHz, then make this series capacitor 470 nF. If the phase detector frequency is 10 MHz, make this capacitance about 100 nF.

11.2 Layout Example



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12 Device and Documentation Support

12.1 Device Support

For the Clock Architect tool, go to http://www.ti.com/lsds/ti/analog/webench/clock-architect.page

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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