

Nintendo Entertainment System

Now you’re playing with power!



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Agenda

1. What is video gaming?
2. History
3. Console Specifications
4. CPU (2A03)
5. Picture Processing Unit (PPU)
6. Cartridges
7. Memory Management
8. Conclusion



What is video gaming?

- Popular pastime of today's youth, and other's not so youthful
- Video gamers
  - Excited about gaming
  - Want to see continual progress
- Market
  - Several competing companies
  - Satisfy gamer's needs
  - Nintendo, Sony, Microsoft, etc.
  - Strategy is different based on company
- Nintendo
  - Hardware is traditionally less expensive
  - Cost is generally lower per console unit with higher market longevity



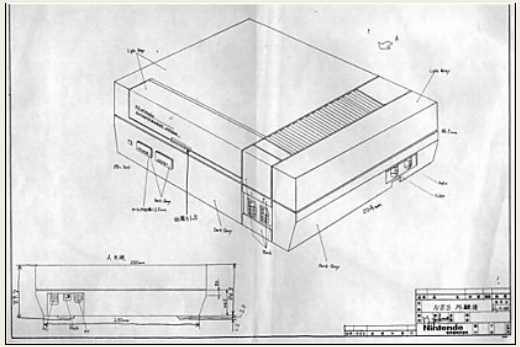
History



- Nintendo released the FAMICOM (FAMily COMputer) in Japan in 1984 [2]
- Despite the video game crash in the US, Nintendo released the N.E.S. in 1986.
  - $250 version came with R.O.B., Gyromite, Super Mario Bros, 2 controllers, Duck Hunt, and a light gun
  - $200 version came with Super Mario Bros, and 2 controllers.
- Nintendo designed the N.E.S. to look like a VCR instead of a Video Game System due to the crash.

History

- 1993: Nintendo released the N.E.S. 2
- 1995: Nintendo discontinued the N.E.S.
- The N.E.S. sold 62 million systems and over 500 million games
    - One of the most popular game systems of all time.



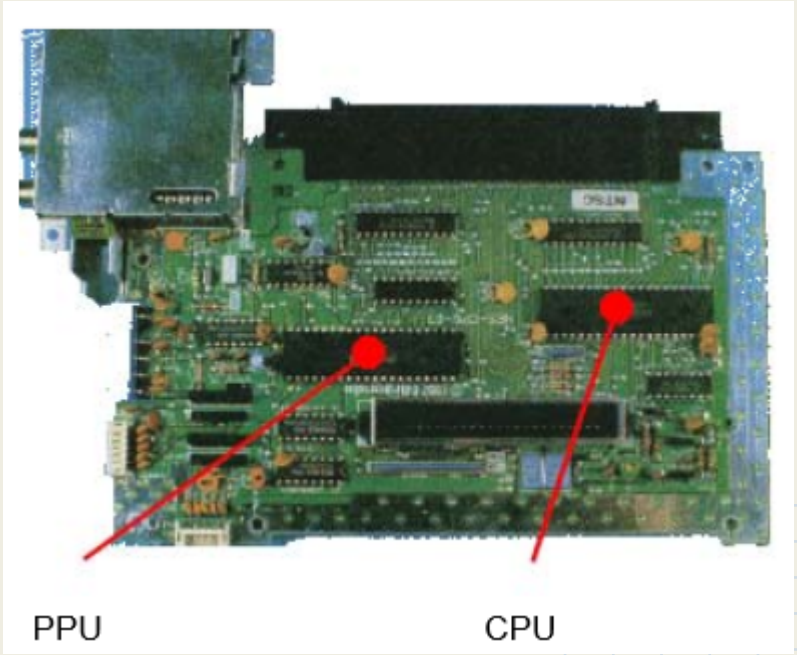
NES External Design



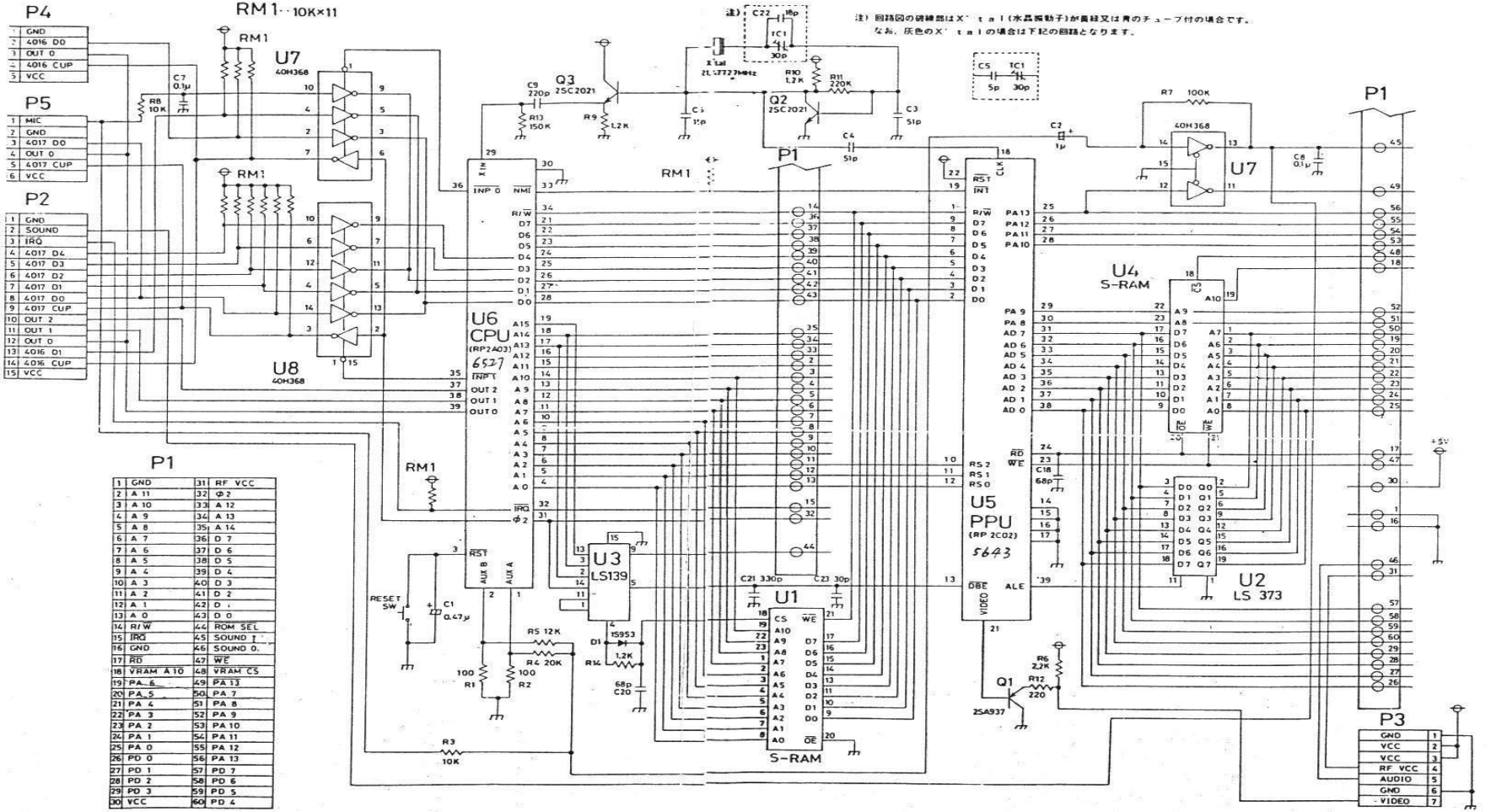
NES 2 - 1993 Release

Console Specifications

- 8-bit CPU
- 1.79 MHz
- PPU
- 64 Value Color Palette
- System Memory - 2KB
- VRAM - 2KB
- Program ROM - 32+ KB
- Character ROM - 8+ KB
- Sprite RAM - 256 Bytes
- Temporary Sprite RAM - 24 bytes
- Color palette RAM - 32 bytes [4]



CPU基板回路図

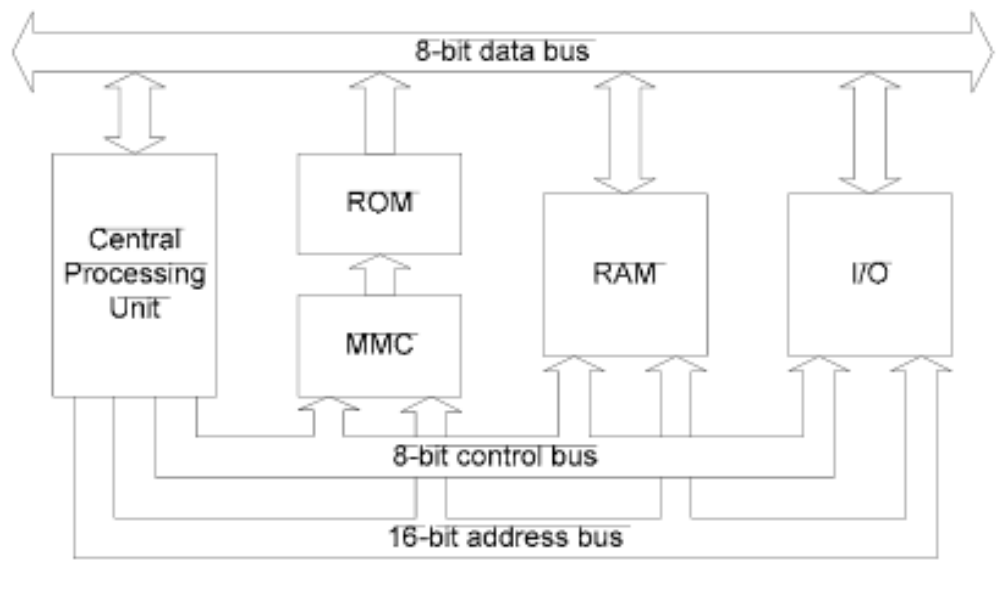

P4
1 GND
2 4016 D0
3 OUT 0
4 4016 CUP
5 VCC
P5
1 MIC
2 GND
3 4017 D0
4 OUT 0
5 4017 CUP
6 VCC
P2
1 GND
2 SOUND
3 IRQ
4 4017 D4
5 4017 D3
6 4017 D2
7 4017 D1
8 4017 D0
9 4017 CUP
10 OUT 2
11 OUT 1
12 OUT 0
13 4016 D1
14 4016 CUP
15 VCC
RM1 ‥ 10K×11
U7 40H368
U8 40H368
C7 0.1μ
R8 10K
Q3 2SC2021
Q2 2SC2021
C9 220p
R13 150K
R9 L2K
R10 L2K
R11 220K
C3 51p
C4 51p
C2 1μ
R7 100K
C8 0.1μ
注) 回路図の破線部はX'tal(水晶振動子)が黄緑又は青のチューブ付の場合です。
なお、灰色のX'talの場合は下記の回路となります。
C5 5p
TC1 30p
U6 CPU (RP2A03) 6527
U5 PPU (RP 2C02) 5643
U4 S-RAM
U1 S-RAM
U3 LS139
U2 LS 373
RESET SW
C1 0.47μ
R5 12K
R4 20K
R1 100
R2 100
R3 10K
D1 1S953
R14 1.2K
C20 68p
C18 68p
C21 33p
C23 30p
Q1 2SA937
R6 2.2K
R12 220
P1
1 GND
2 A 11
3 A 10
4 A 9
5 A 8
6 A 7
7 A 6
8 A 5
9 A 4
10 A 3
11 A 2
12 A 1
13 A 0
14 R/W
15 IRQ
16 GND
17 RD
18 VRAM A10
19 PA 6
20 PA 5
21 PA 4
22 PA 3
23 PA 2
24 PA 1
25 PA 0
26 PD 0
27 PD 1
28 PD 2
29 PD 3
30 VCC
31 RF VCC
32 Φ2
33 A 12
34 A 13
35 A 14
36 D 7
37 D 6
38 D 5
39 D 4
40 D 3
41 D 2
42 D 1
43 D 0
44 ROM SEL
45 SOUND I
46 SOUND O
47 WE
48 VRAM CS
49 PA 13
50 PA 7
51 PA 8
52 PA 9
53 PA 10
54 PA 11
55 PA 12
56 PA 13
57 PD 7
58 PD 6
59 PD 5
60 PD 4
P3
GND 1
VCC 2
VCC 3
RF VCC 4
AUDIO 5
GND 6
VIDEO 7
NOTE 指定なき抵抗コンデンサは0.01μF使用

CPU - 2A03

Overview [2 ,p.9]:

- Ricoh - 2A03
- NMOS
- Little Endian
- 8-bit data bus
- MMC
- 8-bit control
- 16-bit address



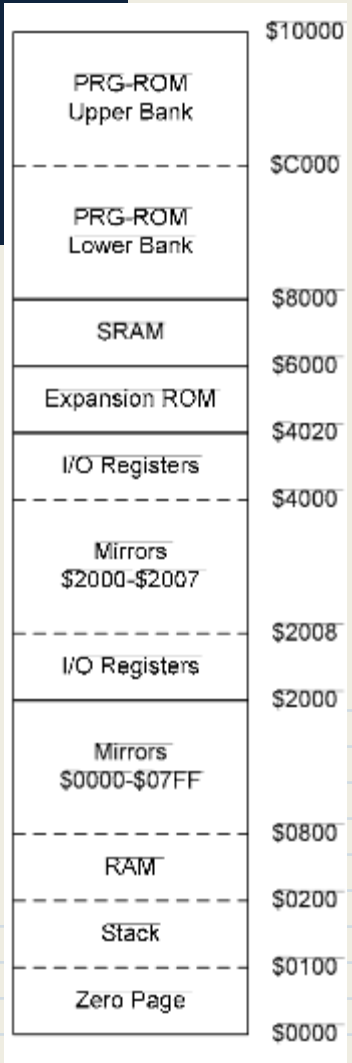


Processor Diagram

CPU - 2A03

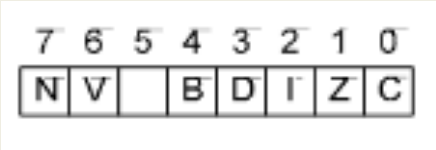
Memory Access [2 ,pp. 9,10]:

- ROM
  - Read-only
  - Accessed via MMC
- MMC
  - Controller for ROM access
  - Allows for bank swapping
- RAM
  - Mirroring
  - Zero Page
  - PRG-ROM
- Address Bus
  - 16-bit
  - Set address
  - Support for 64KB
    - $0000-$FFFF
- Control Bus
  - Read or Write?
  - Screen Mirroring
  - Disk IRQs
- I/O
  - PPU and control



CPU - 2A03 - Registers

- Registers [2, pp. 11-13]
  - 16 - bit Program Counter (PC)
    - Games could only be 64 Kb
  - 8 - bit Stack Pointer (SP)
  - 8 - bit Accumulator (A)
  - 8 - bit Index Register X (X)
  - 8 - bit Index Register Y (Y)



- 8 - bit Processor Status
  - N - is number negative
  - V - overflow
  - B - set if the BRK instruction occurs
  - D - Used to switch into BCD mode
  - I - Disable interrupts
  - Z - Zero
  - C - Carry

CPU - 2A03 - ISA

- Instruction Set Architecture [8]
  - Load/Store operations
    - LDA, LDX, LDY, STA, STX, STY, etc.
  - Register Transfer Operations
    - TAX, TAY, TSX, TXA, TXY, etc.
  - Stack Operations
    - PHA, PLA, etc.
  - Arithmetic Operations
    - ADC, AND, etc.
  - Increments / Decrements
    - INX, INY, DEX, DEY, etc.
- Shifts
  - ASL, LSR
- Jumps/calls
  - JMP, JSR
- Branches
  - BNE, BEQ
- Status Register Operations
  - CLC, CLI, SEC, SEI

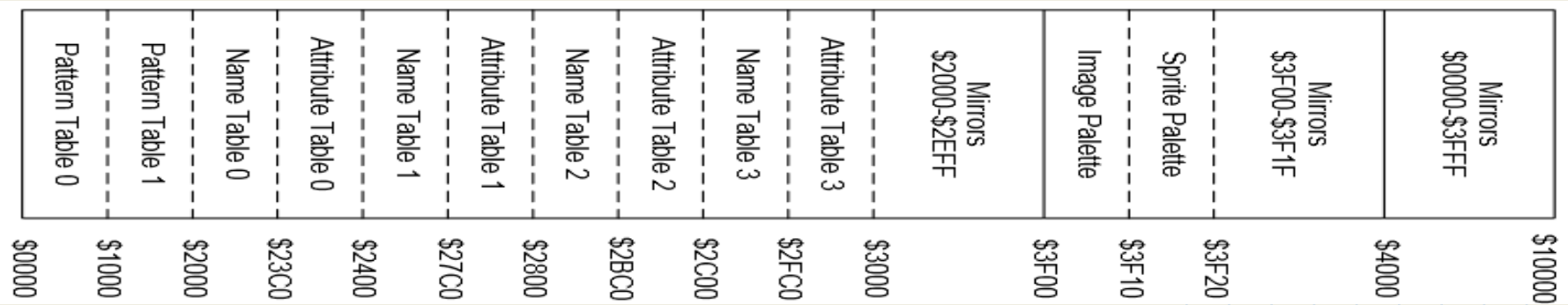
Picture Processing Unit (PPU)

- The CPU by itself was not enough power [3]
- The Picture Processing unit could:
  - Generate Colors
  - Move characters on the Screen
  - Display 52 colors
    - 24 allowed on the screen at the same time
    - Other video game units only had 6-8 colors.

Picture Processing Unit (PPU)

Memory Map [2, p. 17]

- Pattern Tables
- Name Tables
- Palettes
- Mirrors



Picture Processing Unit (PPU)

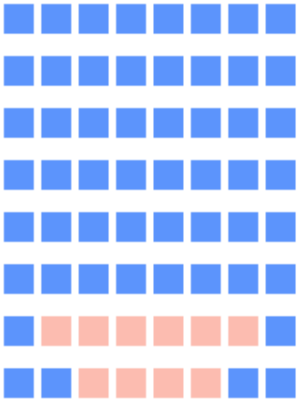
Pattern Tables [3]

- The sprites and background images are saved in here
- Sprites are 8X8 pixel titles
  - Titles are 16 bytes (128 bits)
  - Each byte (bits) is a row in the sprite
  - The sprites have 2 layers
    - First 8 bytes are the first layer
    - Second 8 bytes are the second layer
  - Each sprite can have 4 possible colors

```
001CD0: 96 96 96 F6 46 C6 0E FE 6F 6F 6F 0F BF 3F FF FF
001CE0: 00 00 00 00 00 00 7E 3C 3C 7E 7E FF FF FF 42 00
001CF0: 3C 42 99 A1 A1 99 42 3C 00 00 00 00 00 00 00 00
```



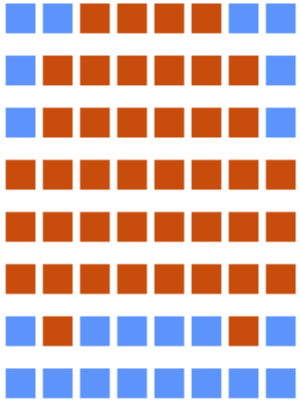
$00 = 00000000
$00 = 00000000
$00 = 00000000
$00 = 00000000
$00 = 00000000
$00 = 00000000
$7E = 01111110
$3C = 00111100



Layer 1



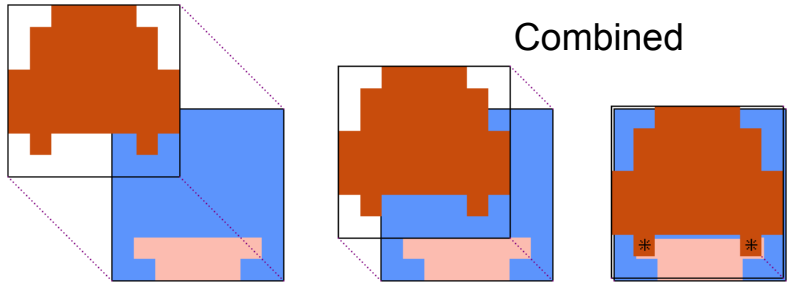
$3C = 00111100
$7E = 01111110
$7E = 01111110
$FF = 11111111
$FF = 11111111
$FF = 11111111
$42 = 01000010
$00 = 00000000



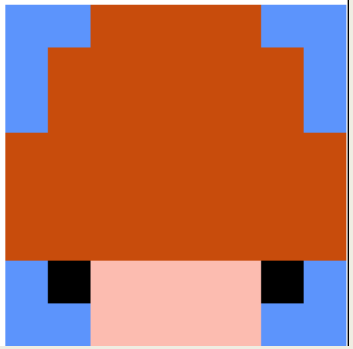
Layer 2



Combined



00111100 00000000 00222200
01111110 00000000 02222220
01111110 00000000 02222220
11111111 00000000 22222222
11111111 00000000 22222222
11111111 00000000 22222222
01000010 01111110 03111130
00000000 00111100 00111100
"Layer 2" + "Layer 1" = Final Palette Assnmt



Layer 2	Layer 1	Overall	Palette Assignment
0	0	00	Color 0
0	1	01	Color 1
1	0	10	Color 2
1	1	11	Color 3

Images from Badder Hacks

Picture Processing Unit (PPU)

Name Tables [3]

- Backgrounds are stored here
- PPU supports 4 name tables
- NES RAM can only support 2
  - Other 2 tables are mirrored
- Each table has 30, 32-byte strings of data
  - tiles assigned left-to-right, top-to-bottom
- Remaining 64 bytes are for background palette assignments

Picture Processing Unit (PPU)

- Scrolling with nametables [3]

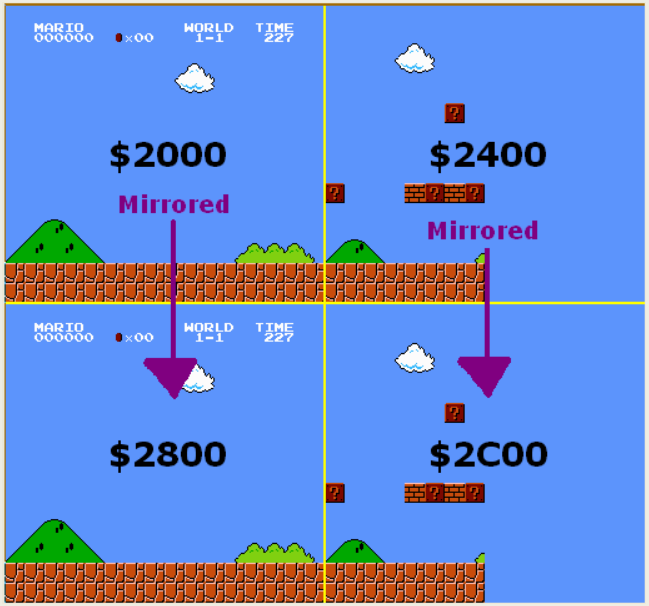


Image from Badder Hacks

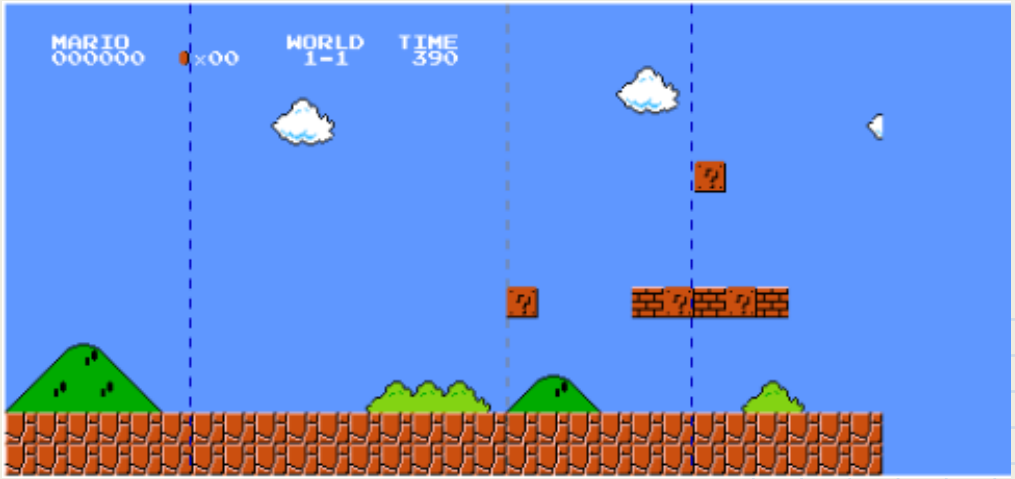


Image from NES System Documentation

Picture Processing Unit (PPU)

Palettes [3]

- Consists of four colors chosen from NES' internal index
- Tiles are colored by assigning them a palette
- Background tiles can be assigned to any of four palettes
- Sprite tiles can be assigned to any of a separate set of four palettes



Layer 2	Layer 1	Overall	Palette Assignment
0	0	00	Color 0
0	1	01	Color 1
1	0	10	Color 2
1	1	11	Color 3

Image from NES System Documentation

Cartridges

- Unlike previous systems, Nintendo released a cartridge standard.
- The FAMICOM cartridge
  - Smaller than the N.E.S. Cartridge
  - 60 pin connection
- The N.E.S. Cartridge
  - Bigger than the FAMICOM's
  - 72 - pin connection
  - Mostly empty space
  - Had a "Lock out system."
- The N.E.S. had enough memory for early games
  - Some games needed more
  - Cartridges could have their own ROM.



Images from NES System Documentation



Memory Management

- Game Specific MMC [6]
  - Nintendo made 9
  - Konami made 4
  - Namco
  - Sunsoft
- Supplement On-Board MMC
  - More complexity → Increasing demand
  - Swappable memory



Nintendo MMC3



Konami VRC4

Memory Management

- How Memory Mapping works [6]:
  - The N.E.S. used bank switching
  - MMC monitors memory writes for specific address (or range)
  - When the system needs access to data on a ROM bank and the data is not in PRG-ROM yet, software indicates the need to switch banks.
  - The selected memory is loaded into the bank in PRG-ROM from the cartridge.

- The use of memory mappers helped the N.E.S. to survive technological limitations and extend the life of their product

Conclusion



- The NES uses the 6502 Microprocessor
- The NES has its own custom PPU
- The NES can swap memory between it and the cartridge
- The NES was one of the most popular Video Game Systems
- The Super NES was the NES's replacement (1990 Japan, 1991 US).
- Nintendo continues to follow practices regarding selling their consoles that started with the NES today.

THANK YOU!

Any Questions, Comments, Queries, or Threats?

References

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