Experiment 5 MOS Device Characterization

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1.0 Objective

In this experiment, you will find the device parameters for an n-channel MOSFET. From the parameters, you will reproduce its *I-V* characteristics and compare them to SPICE. The characteristics will be compared to the SPICE level 1 model. We will also compare your data with data from the HP 4155 parameter analyzer. The key concepts you should learn in this lab are:

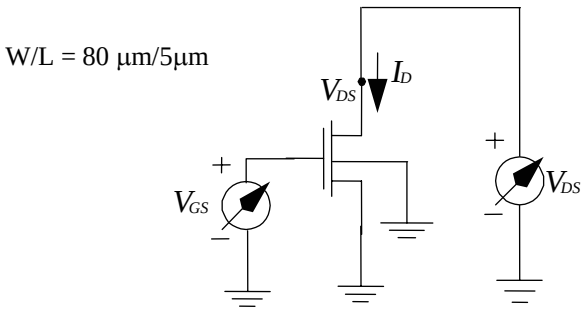
- determining which region of operation the MOSFET is in depending on the values of V_{GS} and V_{DS},
- application of correct equations for I_D depending on the region of operation,
- compare the operation of "long channel" and "short channel" transistors,
- extraction of basic SPICE parameters from experimental measurements

2.0 Prelab

1. Review: H & S Chapter 4.1 - 4.3, 4.5-4.6.

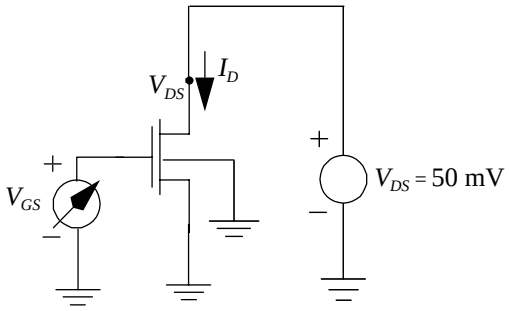
2. Prepare a SPICE deck for the circuit in Figure 1. Let V_{DS} range from 0 – 3 V in 0.05 V increments and let V_{GS} range from 0 – 3 V in 0.5 V increments. Print a plot of I_D vs. V_{DS} with V_{GS} as a parameter. Using this plot, explain how one would obtain the parameters V_{TOn}, $K_n = \mu_n C_{ox}$ and λ_n. Use the following SPICE parameters for getting started (note SPICE uses K_p for K_n.):
    - $V_{TOn} = .4$ V
    - $K_p = 100\ \mu A/V^2$
    - $\lambda_n = 0.05\ V^{-1}$

Figure 1 Circuit for SPICE simulation as described above



3. Prepare a SPICE deck for the circuit in Figure 2. Print a plot of I_D vs. V_{GS}. Let V_{GS} range from 0 to 3 V in 0.05 V increments and let V_{DS}= 50mV. Using this plot, explain how one would obtain the parameters V_{TO}, $k_n = \mu_n C_{ox}$ and λ_n . Use the same SPICE parameters as procedure 2.

Figure 2 Circuit for SPICE simulation as described above



3.0 Procedure

1. Use the *FET* $I_D - V_{DS}$ program in the HP 4155 to obtain the I-V characteristic for the MOS transistor; press the [**CHAN]** key to enter the **CHANNEL DEFINITION** screen. Select the *FET* $I_D - V_{DS}$ program using softkeys.

2. Place chip Subchip A into the test fixture and connect the SMUs according to how they are configured in the **CHANNEL DEFINITION** screen. Make sure that Pin 1 on the chip is aligned with Pin 1 on the test fixture. Pins for the NMOS transistor are as follows: (drain = PIN 19 gate = PIN 24 source = PIN 2 substrate = PIN 1)[1]. This transistor is a "long channel" transistor with W/L of 80μm/5 μm.

   Figure 3 shows how SMUs are connected to the pins of the chip. Figure 4 shows how the SMUs are being used in the experiment. To correctly set up the SMUs, connect the appropriate SMU to the corresponding variable pin socket.

1. Since we are using 24-pin chips on a 28-pin test fixture, pins 1-12 on the lab chip map to pins 1-12 on the test fixture, but pins 13-24 map to pins 17-28 on the test fixture

Figure 3 HP 4155 Test Fixture showing SMU1 being connected to pint 2 of a 28-pin chip.

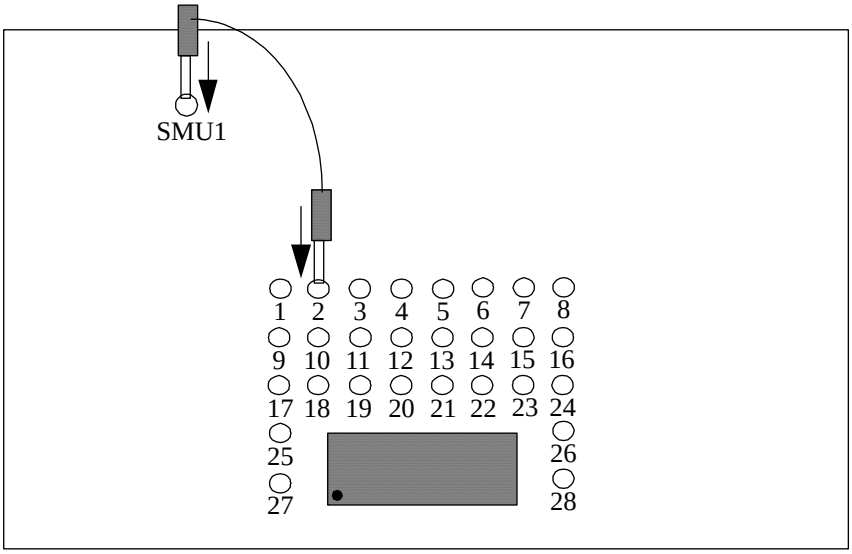
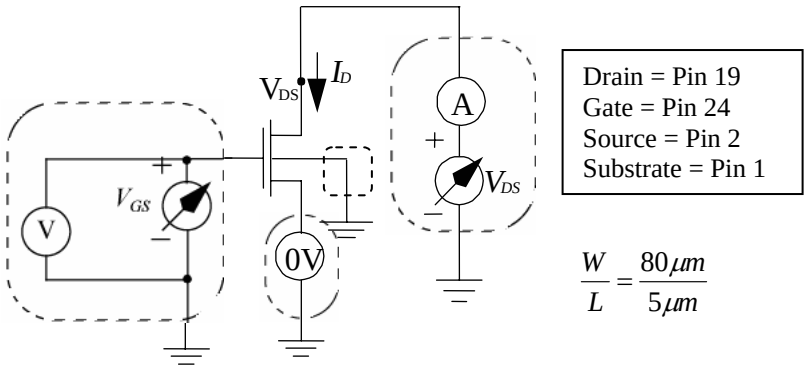


Figure 4 Circuit to gather data for I_D vs. V_{DS} plot. Note the SMU connections in dashed boxes.



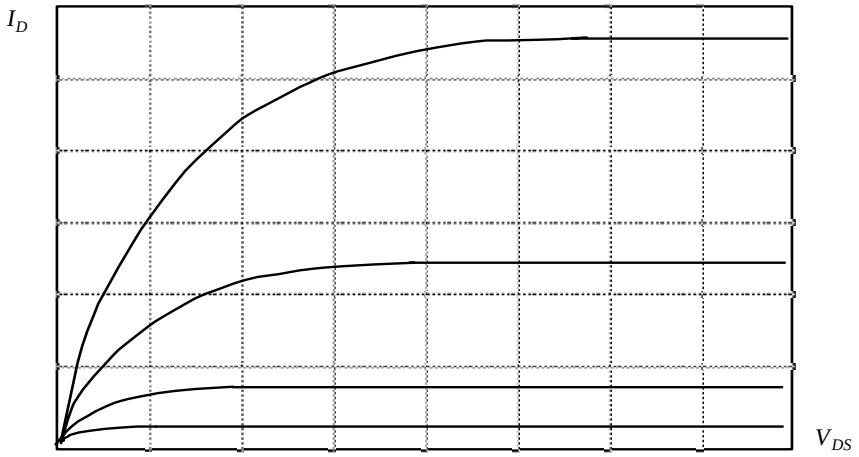
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3. Go to the **MEASURE/SOURCE SETUP** page using the **[NEXT]** or **[PREV]** key and note what voltages/currents are constant and what voltages/currents are variables. Change the parameters to the appropriate values to perform the analysis (i.e., step the V_{GS} from 0 to 3 V in 0.5 V increments and sweep V_{DS} from 0 to 3 V in 0.05 V increments). Set the **COMPLIANCE** for the V_{DS} and V_{GS} to 10 mA and 1 mA, respectively. For a voltage variable, the **COMPLIANCE** is the maximum amount of current that can flow through that node. What would happen if the **COMPLIANCE** for V_{DS} was lowered? What about V_{GS}? Why?

4. Continue to the **DISPLAY SETUP PAGE** and make sure the x-axis is set to display V_{DS} and the y-axis is set to display I_D. Set the appropriate bounds for these axes.

5. Go to the **GRAPHICS** page and hit the **[SINGLE]** key. This will perform the measurements and plot the resulting data. Hit the **SCALING→AUTO SCALE** softkeys to optimize the display of the results. The display screen should look something like Figure 5.

Figure 5 Sample I_D vs. V_{DS} characteristic of NMOS.



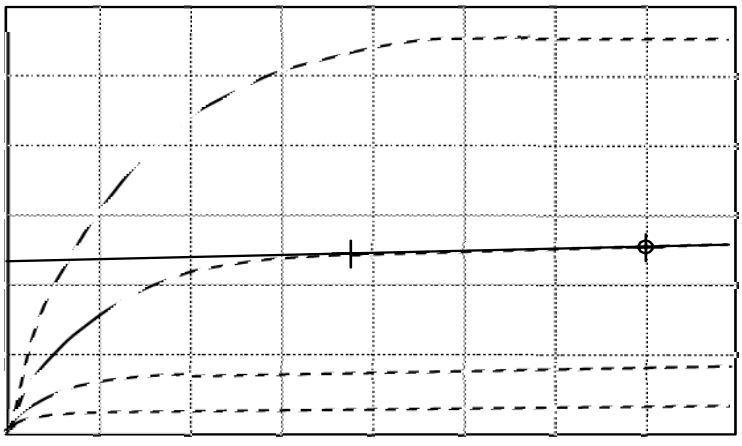
3.1 Finding λ_n

1. From the screen with the above plot, hit the **MARKER/CURSOR** softkey and **MARKER ON** softkey. You will notice a small green **o** marker.

2. Hit the softkey **MARKER SKIP** three times until you reach the third curve from the top (V_{GS}= 2 V). You can move the marker using the cylindrical knob. Notice that as you move the marker along the V_{DS} axis, the corresponding I_D value is displayed on the CRT. Move the marker to V_{DS} = 2 V. What is the region of operation of the MOSFET? Write the equation for the drain current I_D in this region of operation.

3. Fit a line between V_{DS} = 1.5V and V_{DS} = 2.5V. If you have forgotten how to fit a line, consult the instructions in Lab 4. Use the slope of the line to find λ_n.

Figure 6 Sample I_D vs. V_{DS} characteristic of NMOS showing a best fit line to find λ_n.



Best Fit Line and λ_n Data

V_{DS} (V)	I_D (A)

Best Fit Line Slope	
Best Fit Line Y-Intercept	
Calculated λ_n	

4. Obtain a plot of your data by using the **PRINT** function of your HP 4155 parameter analyzer. Additional instructions on printing can be found in the lab manual.

3.2 Finding V_{Ton} and K_n in the Triode Region.

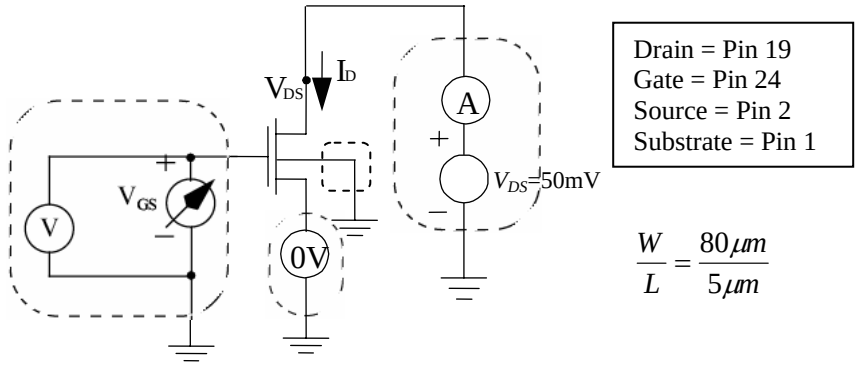
1. Now use the FET $V_{GS} - I_D$ program in the HP 4155. You may select this with the softkeys after pressing the **[CHAN]** key.

2. Connect the SMUs according to how they are configured in the **CHANNEL DEFINITION** screen. Refer to the circuit in Figure 7 for reference on how to connect the pins to the correct SMUs. Note that V_{DS} = 50 mV and that the MOSFET will be in the triode region for $V_{GS} > V_{Ton}$ + 50 mV. Write the equation for drain current I_D that corresponds to this region of operation.

3. Once again, observe the setup in the **MEASURE/SOURCE SETUP** page. The V_{GS} voltage should now be set to sweep from 0 to 3 V in 0.05 V increments and V_{DS}= 50 mV. Set the **COMPLIANCE** for V_{DS} and V_{GS} like before.

4. Make sure the **DISPLAY SETUP** is set to view only V_{GS} vs. I_D and the bounds for the axis are appropriate.

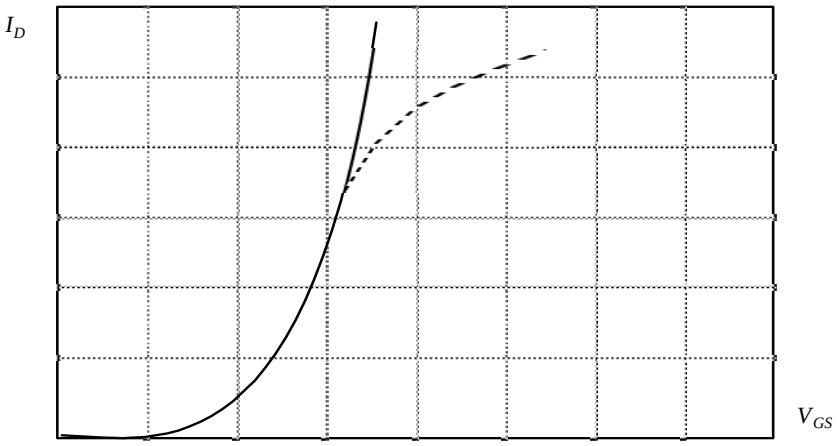
Figure 7 Circuit to gather data for I_D vs. V_{GS} plot. Note SMUs in dashed boxes.



5. Go to the **GRAPHICS** page, hit the **[SINGLE]** key again and hit **SCALING→AUTO SCALE** to rescale the curve if necessary. Observe the curve, paying special attention to the shape of the graph, the max current and the turn on voltage. The curve should look similar to the one shown in Figure 8.

6. From the plot, find a best fit line and use the line to estimate values for V_{Ton} and K_n. Use data points near low I_D since the transistor diverges from ideal behavior for high I_D. Use the W/L values from the prelab for the calculations. Obtain a hardcopy of the plot. Label the different regions of operation on the plot.

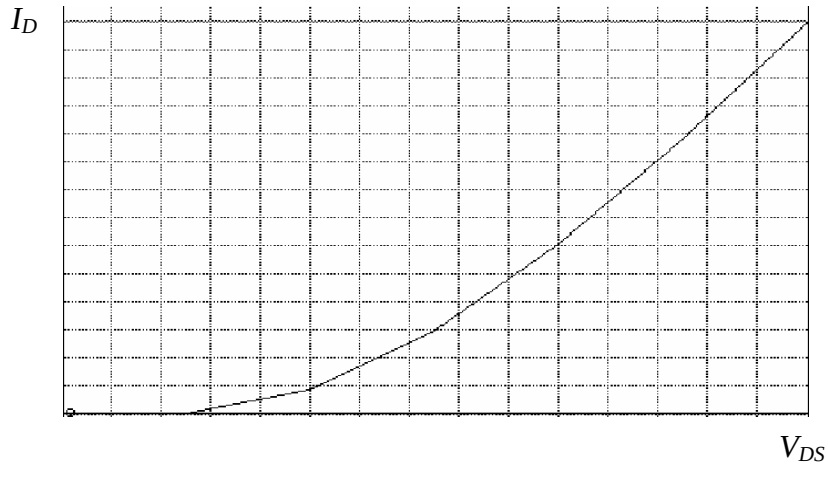
Figure 8 Sample V_{GS} vs. I_D curve for NMOS transistor in triode region.



Best Fit Line Slope	
Best Fit Line x-Intercept	
Calculated V_{Ton}	
Calculated K_n	

7. Now, return to the **MEASURE/SOURCE SETUP** and set V_{DS}= 3 V. Note that now, $V_{GS} < V_{TOn} + 3V$ and the transistor is in saturation. Plot the curve and obtain a hard copy of the plot. It should look like Figure 9.

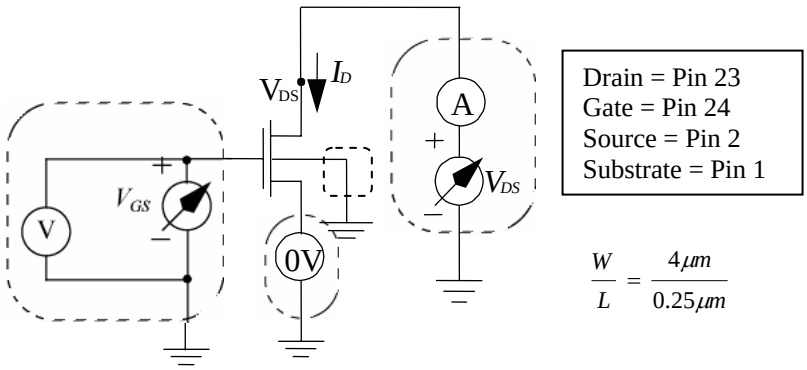
Figure 9 Sample V_{GS} vs. I_D curve for NMOS transistor in saturation region.



3.3 Short-Channel NMOS Transistor

1. We will now obtain the same $V_{DS} - I_D$ and $V_{GS} - I_D$ plots for a "short channel" transistor (W/L= 4μm/0.25 μm). Start the FET $V_{DS} - I_D$ program again from the channel menu again using the **[CHAN]** key. Connect the appropriate SMUs according to the test setup and the circuit in Figure 10. Note that the pins for the drain, gate, source and substrate are different than before.

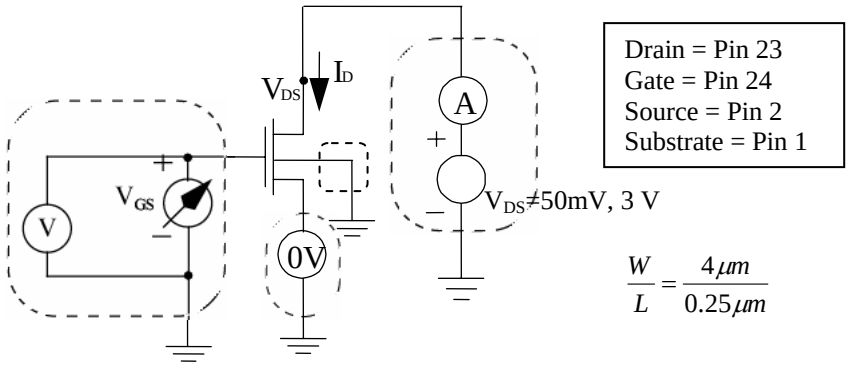
Figure 10 Circuit to gather data for $V_{DS} - I_D$ plot for short channel transistor.



2. Set up the variables as in **3.1** (sweeping V_{DS} from 0 to 3 V in 0.05 V increments and V_{GS} from 0 to 3 V in 0.5 V increments). Plot the graph with the **SINGLE** key and **AUTO SCALE** if necessary. Obtain a hard copy of the plot

3. Now, return to the **CHANNEL DEFINITION** window with the **[CHAN]** key and select the FET $V_{GS} - I_D$ test. Set up the SMUs like before according to the test setup and the circuit in Figure 11. Note the different V_{DS} value and different pins for the drain, gate, source and substrate.

Figure 11 Circuit to gather data for V_{GS} vs. I_D plot for short channel transistor



4. Set up the sweep measurements as in **3.2** (sweeping V_{GS} from 0 to 3 V in 0.1 V increments). Plot the graph with the **SINGLE** key and autoscale if

necessary. Do this for both V_{DS}= 50 mV and V_{DS}= 3 V. Obtain a hard copy of the graphs.

3.4 Further Analysis

1. Look at the graphs you obtained for the "long channel" transistor. Does the transistor behave as expected in each region of operation? (i.e. quadratic in saturation?) If the transistor does not behave ideally, can you explain why?

2. Look at the graphs you obtained for the "short channel" transistor. How do they differ from those of the "long channel?" Pay particular attention to the shape of the plot (i.e. Does I_D seem to be linear? Quadratic?). Compare the two.

3. Using the I_D plots and your knowledge of device physics, formulate an explanation for the changes in current between the long channel and short channel transistors.

3.5 Comparison with SPICE

1. Fill in the values of V_{Ton}, k_n and λ_n in the datasheet in the appendix. You will need to refer to them in future labs.

2. The values you extracted in this lab will be used in SPICE to model the NMOS. Using the SPICE decks you constructed for the prelab, replace the old values of V_{Ton}, k_n and λ_n, with those that you just found. (Note k_n is defined as k_p in SPICE.)

3. Obtain plots of V_{DS} vs. I_D and V_{GS} vs. I_D plots for the "long channel" transistor as you did in the prelab. Compare the experimental plots with the plots you generated in SPICE. How do the currents differ?

4. On page 9 of the "Interlinear Becomes Chip Set for Undergraduate Laboratories in Microelectronic Devices and Circuits," two Level 1 SPICE models are given for the NMOS transistor in this technology, an "analog" model and a "digital" model. Compare plots of these models with the experimental measurements. Note that the Level 1 SPICE model is not adequate for accurate modeling of devices with channel lengths shorter than around 2 μm.

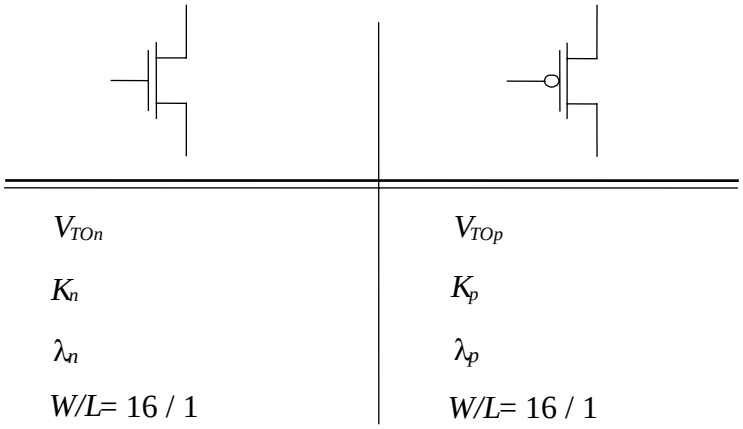
4.0 Optional Experiments

4.1 PMOS Characterization

1. Using the programs **PVT** and **PIDVD**, change the settings in the **CHANNEL DEFINITION** and **SOURCE SETUP** page to perform the experiments for the "long channel" PMOS3 transistor (W/L = 16μm/1μm) and the "short channel" PMOS1 transistor (W/L = 4μm/0.25μm).

5.0 Appendix

5.1 Datasheet



Data Sheet for NMOS3 and PMOS3

5.2 A Note on Layout and MOSFET Geometry

Consider the following NMOS transistor in Figure 11:

Figure 12 Long channel MOSFET

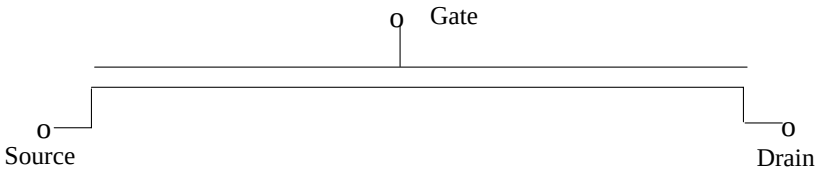
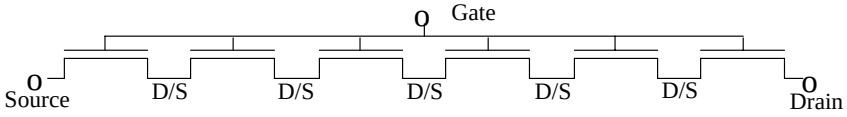
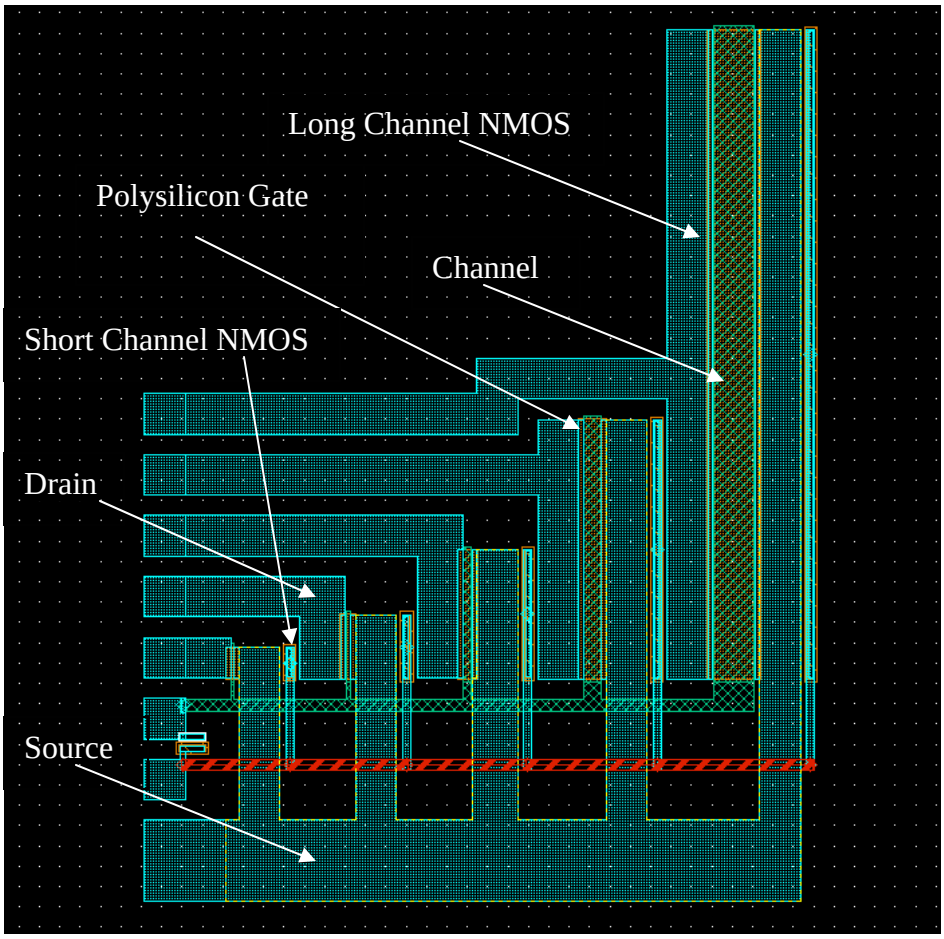


Figure 13 Equivalent MOSFET consisting of short channel transistors



It is possible to make a “long channel” device using a series of short channel devices. The effective channel length is the sum of the channel lengths. For the 0.25µm process on which these chips were built, transistors of varying sizes were constructed. Figure 13 show the layout of the NMOS transistors.

Figure 14 Layout of a series of NMOS transistors.



The layout of the PMOS transistors is similar in structure.

Figure 15 NMOS transistor schematic

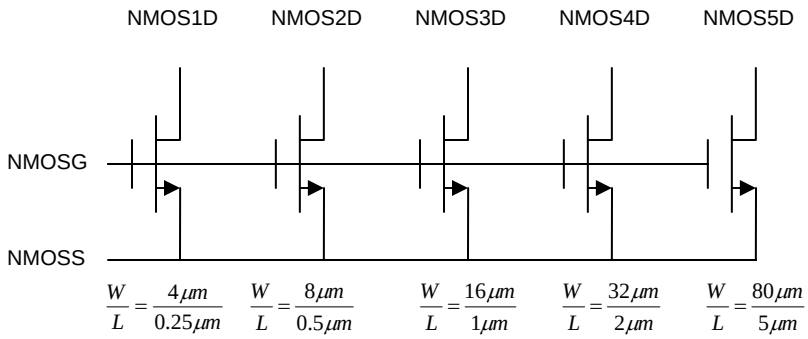


Figure 16 PMOS transistor schematic

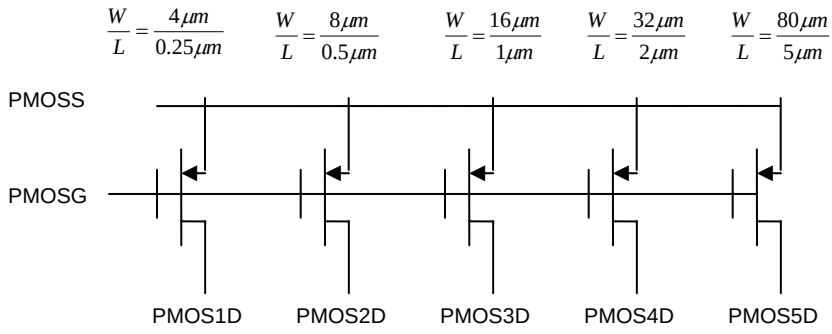


Figure 17 Lab Chip Pin Layout

