ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT_PRBS20C
PRBS7/15 Generator Featuring Jitter Insertion, Selectable Sync, Output Amplitude Control and USB Control

- Broadband operation from 20*Mbps* – 22.0*Gbps*
- Fast rise and fall times
- Two PRBS data outputs with output amplitude control
- Up to 155*ps* delay variation on each output
- Built-in Programmable Clock Generator
- External high-speed clock input capability (AC-coupled on board)
- Differential high-speed clock output
- 50% duty cycle for sync output on all divide ratios
- USB Software GUI Control Interface via USB 2.0
- Single positive 5*V* supply

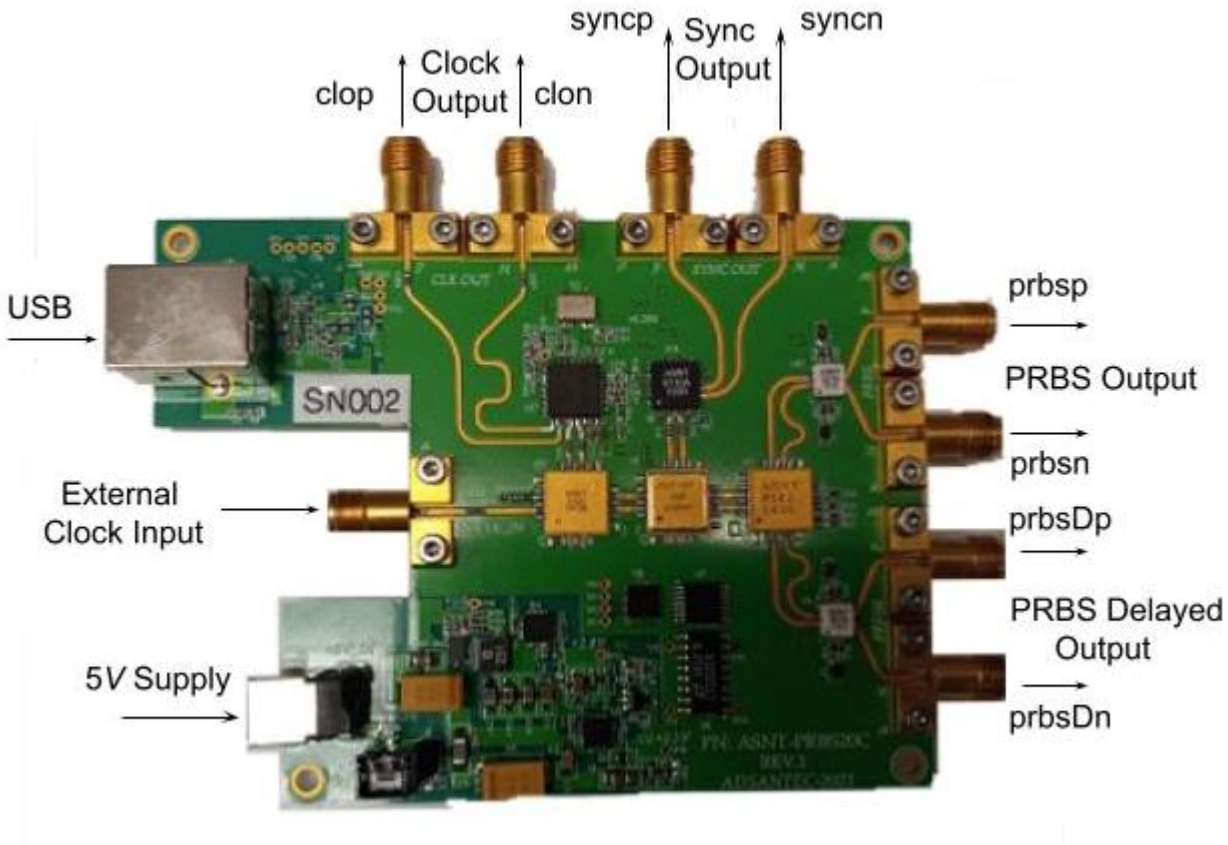

Fig. 1 ASNT_PRBS20C board

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505
Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

DESCRIPTION

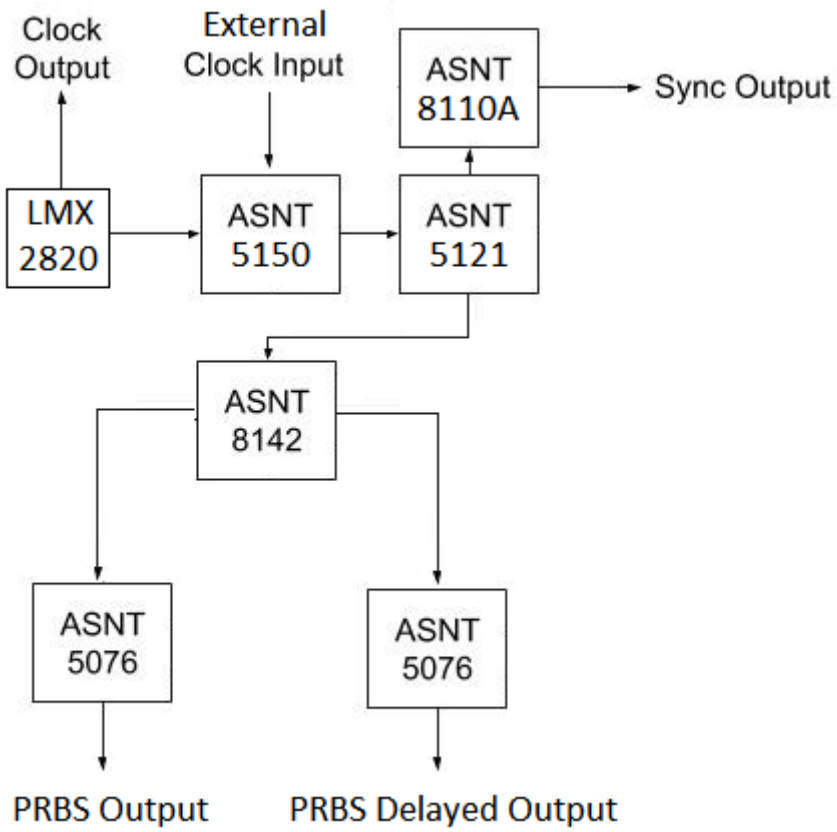

Fig. 2 PCB Block Diagram

The ASNT_PRBS20C is a broadband 2^7-1, or 2^{15}-1 PRBS generator intended for test, and prototyping of microwave communication applications. The board features a programmable clock synthesizer up to 22GHz, while also supporting an external clock input. The PRBS data amplitude is adjustable from 50mV to 1.2*V* single-ended peak to peak, and its phase is adjustable up to 155*ps* for both differential outputs. A single-ended clock from 10*MHz* to 22*GHz* with an amplitude as low as 50*mV* peak to peak may be applied to the high-speed clock input. An independent differential clock output from the internal programmable clock generator is provided. A programmable differential Sync Output provides a divided copy of the input clock with a division ratio from 1 to 256. The Sync Output is mainly used to trigger a high-speed oscilloscope. The system is capable of triggering an eye diagram for PRBS7/PRBS15, or for a PRBS7 pattern with divide ratios 127 or 254. The USB 2.0 port allows the board to connect to any compatible PC for a simplified software-based operation.

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

OPERATION

1. Measure 50*Ohms* on all SMA connectors referenced to VCC.
2. Connect the power supply (provided) to the board, and connect to any PC via an USB cable.
3. Install the included software on the connected PC following the software installation dialog box as shown in **Fig. 3**.

(This step will not need to be repeated unless switching PC's).

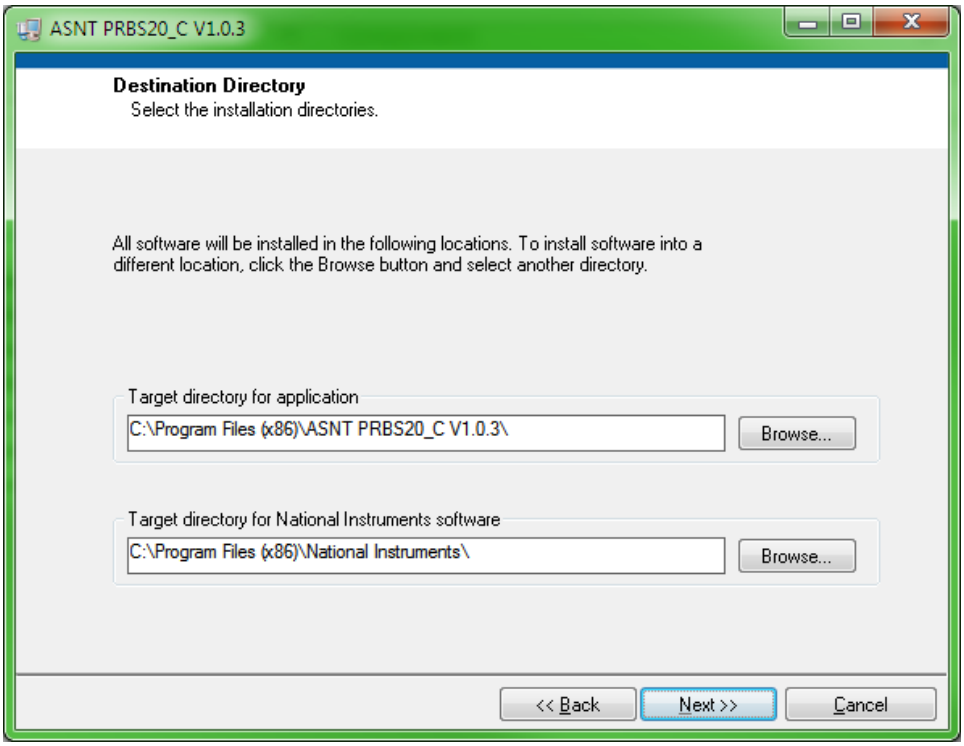

Fig. 3 Software Installation Dialog

4. After the installation is complete, initiate the GUI software and confirm its connection by ensuring that the USB Connection Indicator light is green as it's depicted in **Fig. 4**.
5. The Clock Input Control can be used to select the use of either on-board synthesized, or externally generated clock when desired. If using an external input clock signal, a DC block is not required due to on-board integrated AC coupling.
6. Set the frequency as desired either via the software GUI, or through manipulation of the external clock signal.

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

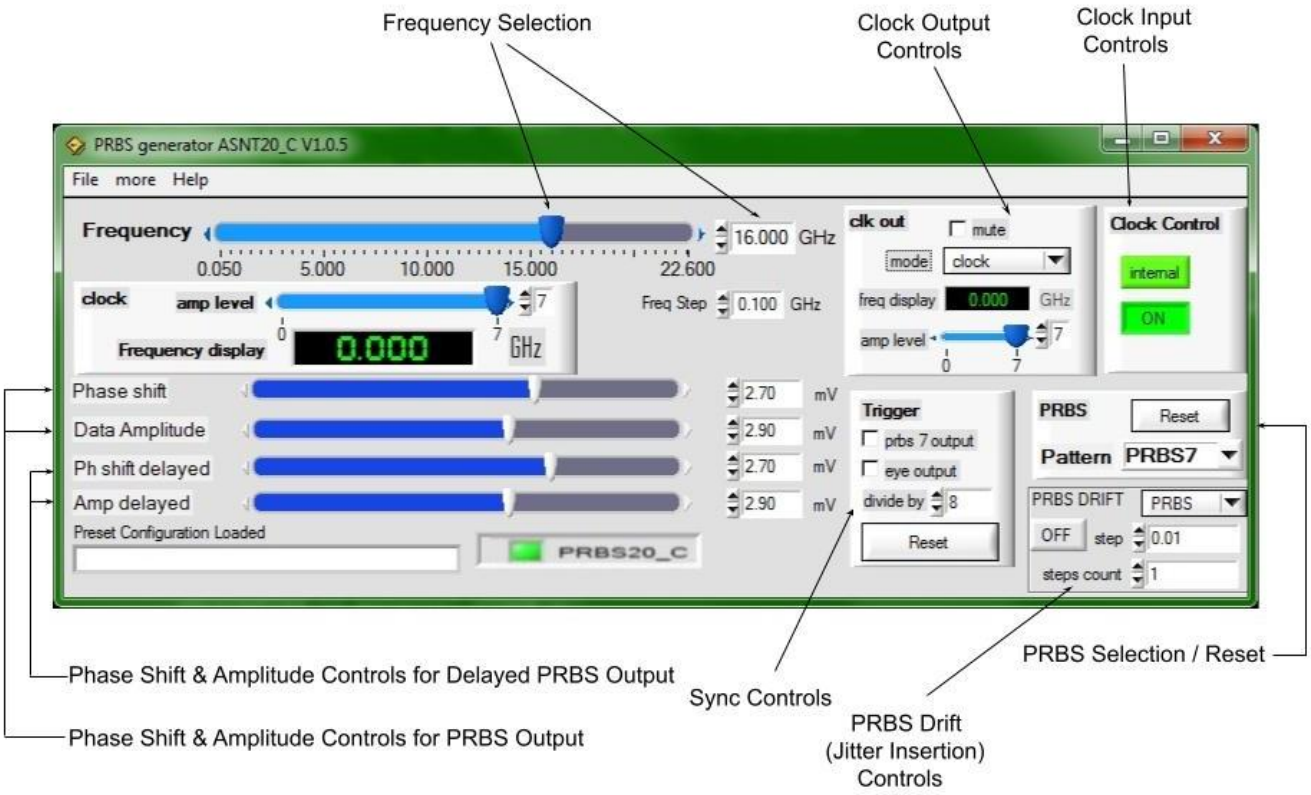

Fig. 4 Software GUI

7. The PRBS Selection/Reset Control can be used to select the desired output pattern (PRBS7/PRBS15), and to provide a PRBS reset when necessary (The board is equipped with automatic reset).

8. The Clock Output Control can be used to enable/disable the clock output from the built-in frequency synthesizer used for data generation. The amplitude of the output clock can also be controlled from here. Using the "**mode**" drop down window, the controls will allow for a divided clock output when desired. Note that these clock outputs are also AC coupled on-board.

9. The Sync Controls (Trigger) can be used to manipulate the division ratio used for the sync signal output; when viewing PRBS7 data this can be easily configured to view either an eye diagram, or an output data pattern. It can also be used to set a manual division ratio when desired.

10. The Amplitude Controls (Data Amplitude and Amp delayed) can be used to adjust the amplitude of both the PRBS Output, and the Delayed PRBS Output. The Phase Shift (Phase Shift and Ph shift delayed) controls can also be used to adjust the phase of each data output by up to 155*ps*.

11. The PRBS Drift (Jitter Insertion) Controls can be used to inject jitter into the output signal if desired. The Step Value and Step Count can both be used to create jitter in different ways, or be used in combination, with higher values corresponding with greater inserted jitter.

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505
Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee		0		*V*	External ground
vcc		5.0		*V*	Provided
I_{VCC}	1.7	2.2	2.6	*A*	
Power		13		*W*	
Operating Temperature	-25	50	85	*°C*	
External Clock Input					
Frequency	0.02		22	*GHz*	
Single-Ended Swing	50	400	1000	mV_{PP}	
Clock Output (clop/clon)					
Frequency	0.02		22	*GHz*	
Single-Ended Swing	50		1000	mV_{PP}	
High-level output voltage		2.4		*V*	
Low-level output voltage			0.4	*V*	
Duty Cycle	45	50	55	%	For Clock Signal
Sync Output (Trigger) (syncp/syncn)					
Frequency	0.01		22	*GHz*	Programmable Divider
Single-Ended Swing	500	600	1000	mV_{PP}	
Rise/Fall Times	15	17	19	*ps*	20%-80%
Duty Cycle	45%	50%	55%		
PRBS Output (prbsp/prbsn)					
Single-Ended Voltage Level	50	500	1200	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	
Duty Cycle	45	50	55	%	
PRBS Delayed Output (prbsDp/prbsDn)					
Single-Ended Voltage Level	50	500	1200	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	
Duty Cycle	45%	50%	55%		

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

BOARD DIMENSIONS DIAGRAM

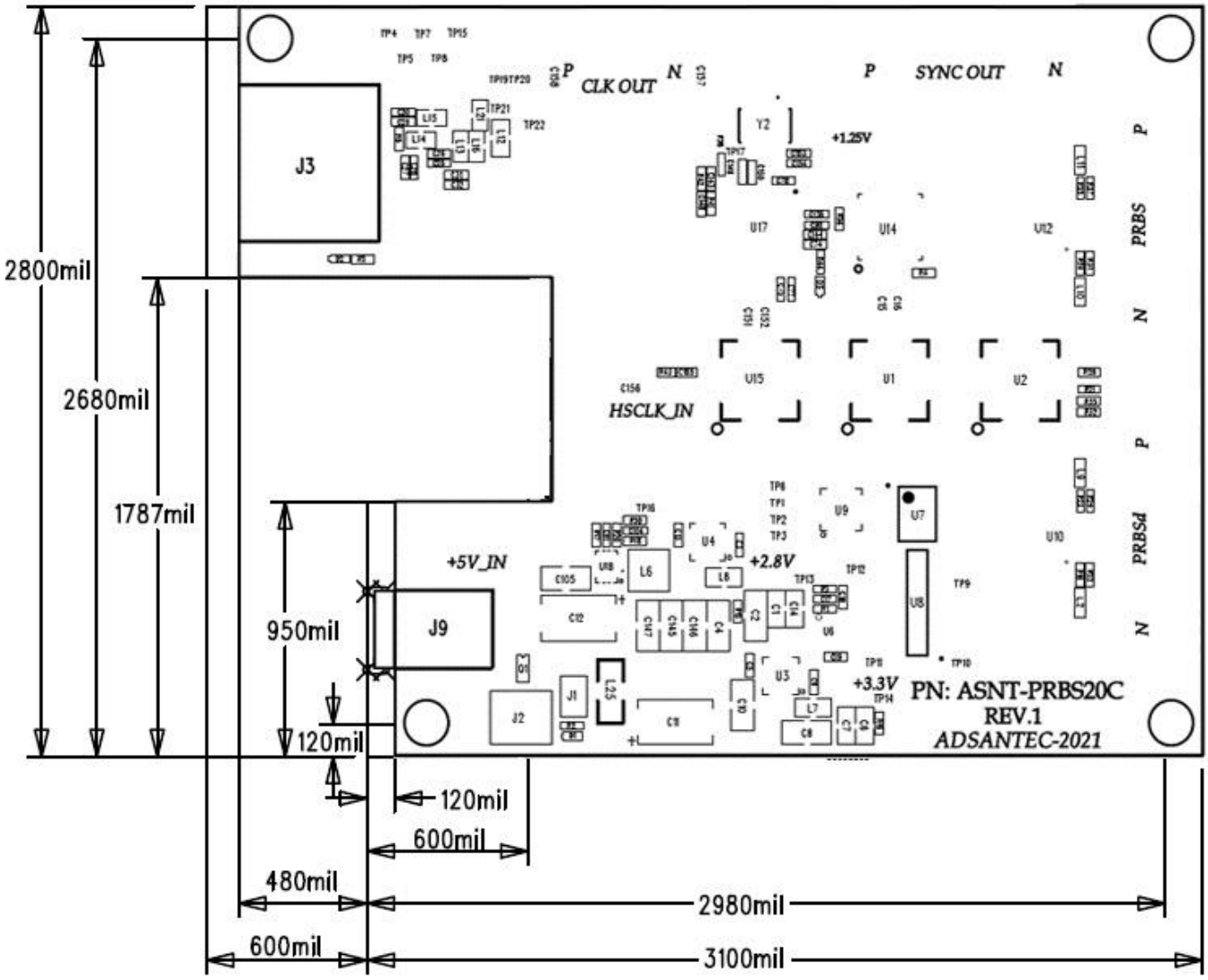

Fig. 5 Board Dimensions Diagram

REVISION HISTORY

Revision	Date	Changes
1.1.2	05-2023	Added Board Dimensions Section Added Fig. 5 Board Dimensions Diagram
1.0.2	03-2022	Standard Release Added Fig. 3 & Fig. 4 Added Control Descriptions
0.1.3	02-2022	Updated Fig. 1
0.1.2	01-2022	Preliminary Release