

D2006TX

VHF Narrow Band FM

(27~300MHz)

Transmitter V1.1



Contents

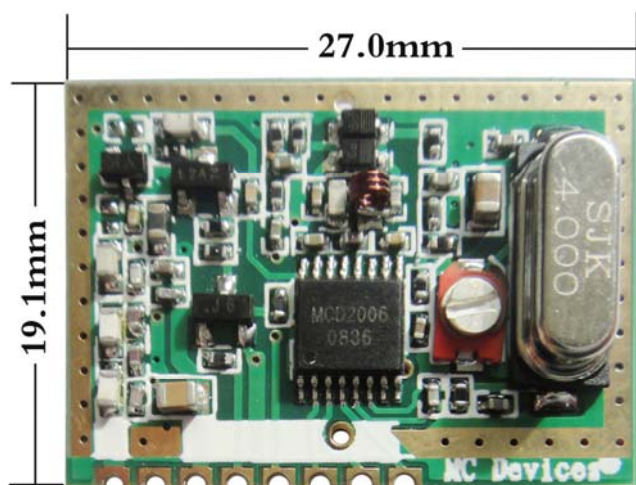
1 Description	2
2 Basic Module Parameters	3
3 Guide to Module	6
4. Reference Frequency and VCO Frequency Configuration Examples	9

Version	Date	Remarks
V1.0	Nov 10, 2010	The first version
V1.1	Dec 10, 2010	Updated parameters required by amateur radio customer.

1 Description

The D2006TX module is used for VHF wireless transmission market. The module consists of PLL, VCO, FM modulation, AMP, LPF and other circuits, suitable for 27~300MHz wireless audio or digital transmission products. Users could adjust D2006TX frequency according to their requirements. Frequency band is about 5% of frequency, that is 1.5~15MHz. Users need to design audio circuit for D2006TX. Based on frequency response feature of audio circuit, wide band or narrow band transmission products could be made with D2006TX.

D2006TX output power is 12dBm, with channel spacing controlled by external MCU. For narrow band, reference frequency is advised to be set as 5KHz for channel step 5KHz. For wide band, reference frequency is advised to be set as 25KHz for channel step 25KHz. A typical application is tracking transmitter in amateur radio market. The transmitter works at 2 narrow band FM frequency points in Europe and North America: 144.390MHz and 144.800MHz.



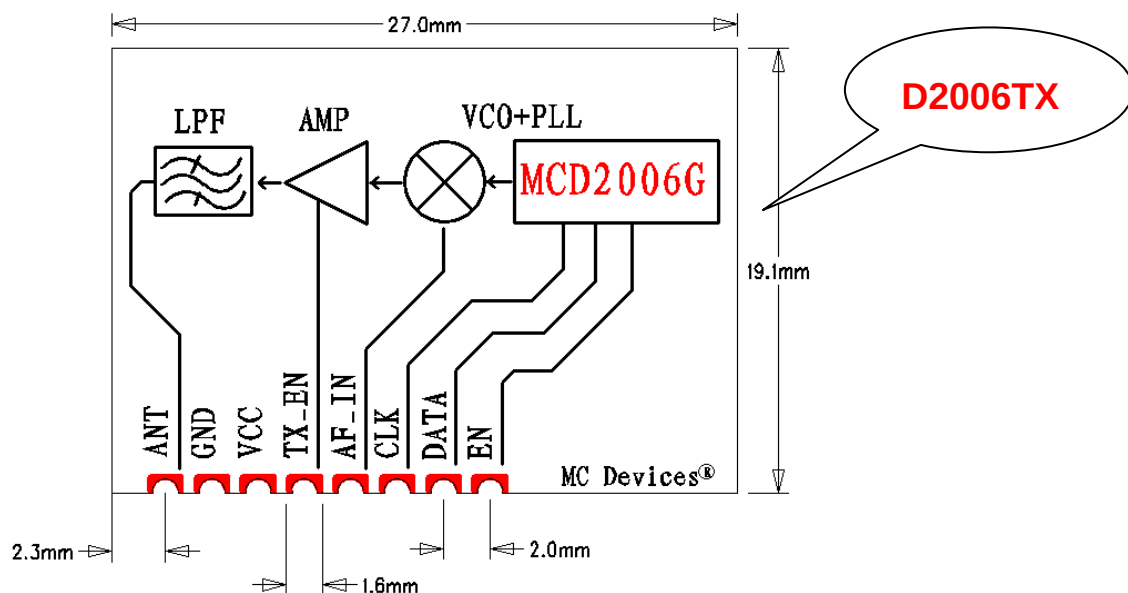
Front



Back

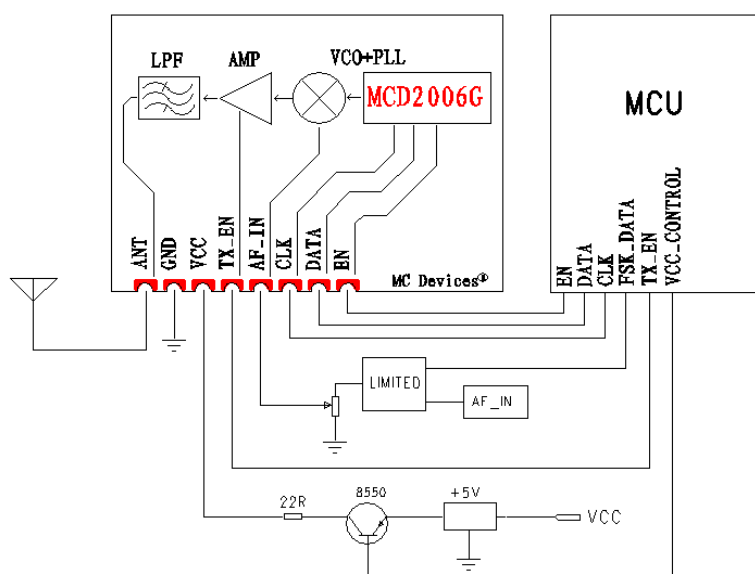
2 Basic Module Parameters

2.1 Pin position and size



Notes: The highest part of D2006TX is 5.5mm.

2.2 Wiring mode



2.3 Pin description

Pin No.	I/O	Description
EN	I	EN is input enable port. When EN is at high level, data in shift register would be loaded in latch distinguished by group identification code.
DATA	I	DATA is input port of MCU serial data. The lowest bit is input first, and the last two bits are group identification code.
CLK	I	CLK is clock input port of serial data. On the rising edge of clock, data is input to shift register of serial interface.
AF_IN	I	Modulation input port. Frequency is within 50Hz-20KHz, modulation sensitivity: at input 1KHz, 100mV, modulation frequency deviation is 4.5 ± 0.5 KHz.
TX_EN	I	Transmitting power enable control port. At high level, amplifier is on, and ANT output rating power is 12 ± 1 dBm. At low level, amplifier is off, PLL is at work, and ANT output power decrease into about 35dBm.
VCC	I	Power supply input port (2.7V-4.5V)。
GND	-	Ground port
ANT	O	Antenna output port

2.4 Recommended operating voltage and electrical property

Recommended operating voltage

Parameter		No.	Value			Unit
			The minimum value	typical value	The maximum value	
Operating voltage	D2006 TX	VDD	2.7	4.0	4.5	V

Electrical property

parameter	Test condition	Value			Unit
		The minimum value	typical value	The maximum value	
General property					
Operating frequency	Band is 5% of frequency	27		300	MHz
Crystal frequency			4		MHz
D2006TX					
1. RF property					
Output impedance			50		ohm
Current	VDD=4.0V		45		mA
Output power (50ohmload)	145MHz	11	12	13	dBm
Phase noise	50Hz loop band,10KHz frequency deviation		-100		dBc/Hz
2. Audio property					
Input impedance(audio input)		600K			ohm
Transmitting frequency response	±3dB	50		20K	Hz
Modulation degree	1KHz, 100mV input range		4.5		KHz
Ratio of signal to noise	1KHz, 4.5K modulation degree		39		dB
Modulation distortion	1KHZ@±4.5KHz frequency deviation	1.0	1.5	2.0	%

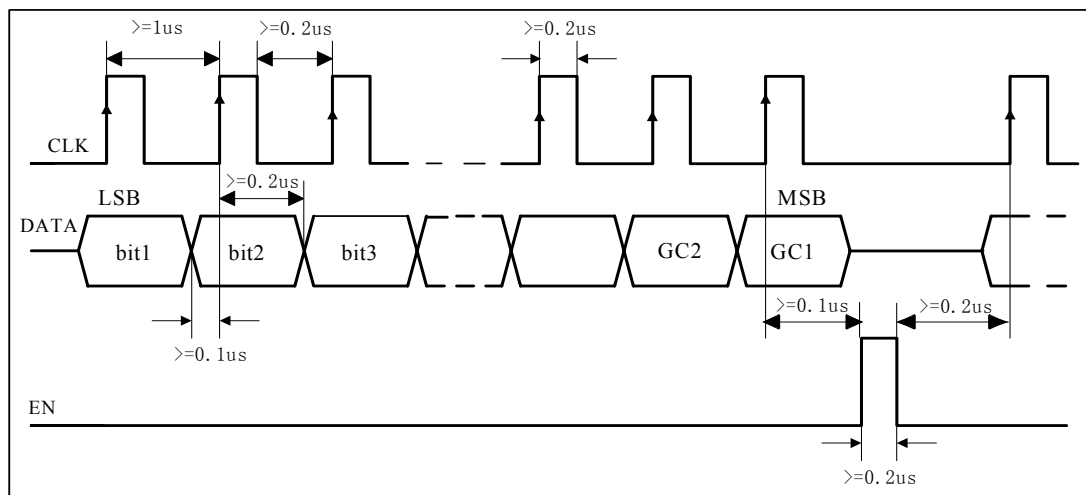
3 Guide to Module

3.1 Frequency setting

D2006TX is based on IC MCD2006G, and frequency setting is to control MCD2006G. Port CLK, DATA and EN are serial data input port. Binary serial data is input from DATA port, and converted into parallel data through serial-parallel port. And then distinguished by group identification code, it is input into reference frequency-dividing counter or channel frequency-dividing counter.

On rising edge of CLK signal, each data is read into internal shift register. Configuraion data to be read first is LSB (the lowest bit), and the last two bits (group identification code) are used to decode internal register address. On rising edge of EN signal, the data in shift register is loaded in latch distinguished by group identification code.

Timing of signal CLK, DATA and EN is as follows:



Notes: (1) LSB is input into shift register first.

(2) When powered on, reference frequency divider is configured first, channel frequency divider is configured then.

Group identification code distribution:

Group identification code		Controlled counter
GC1 (MSB)	GC2 (LSB)	
0	0	Control register (for function test only)
1	0	channel frequency divider
1	1	reference frequency divider

3.2 Configuration of programmable counter

3.2.1 Reference frequency-dividing counter R

Reference frequency-dividing counter provides reference frequency for PLL, including one 2-frequency divider and one 10-bit programmable frequency divider. The frequency range of 10-bit frequency divider is 3~1023. Together with stable 2-frequency divider, the total frequency range of reference divider is 6~2046.

LSB				Configuration word							MSB	
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	GC2=1	GC1=1	

Frequency-dividing number of programmable 10-bit counter:

Frequency-dividing number (R)	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

$$R = R1 \times 2^0 + R2 \times 2^1 + \dots + R10 \times 2^9 \quad (R \geq 3)$$

Total frequency range: 6~2046

3.2.2 Channel frequency-dividing counter N

This programmable frequency divider consists of one 4-bit SWALLOW counter and one 12-bit PULSE counter.

Guide to D2006TX VHF Narrow Band Transmitter V1.1

Together with 16/17 prescaler, the frequency dividing range is 48~65535.

LSB

Configuration word

MSB

N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	GC2=0	GC1=1
----	----	----	----	----	----	----	----	----	-----	-----	-----	-----	-----	-----	-----	-------	-------

|----swallow counter---|-----pulse counter-----|group identification code-

Frequency-dividing number of Swallow counter (A)

Frequency-dividing number (A)	N4	N3	N2	N1
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

$$A = N1 \times 2^0 + N2 \times 2^1 + \dots + N4 \times 2^3$$

Frequency-dividing range: 0~15

Frequency-dividing number of Pulse counter (B)

Frequency-dividing number (B)	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

$$B = N5 \times 2^0 + N6 \times 2^1 + \dots + N16 \times 2^{11}$$

Frequency-dividing range: 3~4095 (B≥A)

Total frequency-dividing number of N counter:

$$N = 16 \times B + A \quad (B \geq A)$$

Frequency-dividing range: 48~65535

4. Reference Frequency and VCO Frequency Configuration Example

Example 1: getting 5KHz reference frequency from 4MHz crystal

- Total frequency-dividing number $2R = 4\text{MHz} \div 5\text{KHz} = 800$
- Programmalbe frequency-dividing number $R = 800 \div 2 = 400$
- Binary system (10 bit) $R = 0110010000$
- Group identification code of reference frequency divider "11"
- Configuration word (12 bit) "110110010000"

LSB (input to register first) → MSB

0	0	0	0	1	0	0	1	1	0	1	1
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Example 2: integrating 40.665MHz VCO frequency from 5KHz reference frequency

- Reference frequency 5KHz (please refer to Example 1)
- Total frequency-dividing number $16*B + A = 40.665\text{MHz} \div 5\text{KHz} = 8133$
- frequency-dividing number of Pulse counter (rounded to integer) $B = \text{Int}(8133 \div 16) = 508$
- binary system(12-bit) $B = 000111111100$
- frequency-dividing number of Swallow counter $A = 8133 - 16*508 = 5$
- binary system (4bit) $A = 0101$
- group identification code of N counter "10"
- configuration word(18bit) "100001111111000101"

LSB (input to register first) → MSB

1	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	1
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