Evaluation Board Manual

DESCRIPTION

SiP32419EVB and SiP32429EVB are a load switch that integrates multiple control features that simplify the design and increase the reliability of the circuitry connected to the switch. The SiP32419EVB and SiP32429EVB are a 56 mΩ switch designed to operate in the 6 V to 28 V range. An internally generated gate drive voltage ensures good R_{ON} linearity over the input voltage operating range.

The SiP32419EVB and SiP32429EVB have a slew rate control circuit that controls the switch turn-on time to the value set by an external capacitor.

After soft start, an over-current protection circuit (OCP) continuously monitors the current through the load switch, and controls the switch impedance to limit the current to the level programmed by an external resistor. If the over-current condition persists for more than 7 ms, the switch shuts off automatically. The SiP32419EVB and SiP32429EVB have an over temperature protection circuit (OTP) which will shut the switch off if the junction temperature exceeds about 145 °C. The OTP circuit will release the switch when the temperature has decreased by about 20 °C of hysteresis.

When the device is at OCP fault condition for over 8 ms the power switch will turn off, and the FLG pin will be pulled low. In case of OT fault condition, the power switch will be off immediately. The FLG pin will be pulled low. For the SiP32429EVB, the fault flag will release 150 ms after the fault condition is cleared, and the switch will turn on at the programmed slew rate. For the SiP32419EVB, the switch will remain off and the fault flag will remain on. The power switch can be reset by toggling EN or input power recycle if over temperature fault is removed.

This device features a low voltage control logic interface which can be controlled without the need for level shifting.

These devices also include a power good flag. The SiP32419EVB and SiP32429EVB are available in a space efficient DFN10 3 mm x 3 mm package.

SiP32419EVB, SiP32429EVB EVALUATION BOARD

SiP32419EVB and SiP32429EVB demo board is designed to evaluate the over current protection and programmable soft star function of the device.

POWER INPUT AND OUTPUT TERMINALS

These power header terminals are designed for easily hood up to the power supply and the load for the evaluation (see fig. 1). The input voltage range for this evaluation is from 6 V to 24 V.

CONNECTION AND SIGNAL TEST POINTS

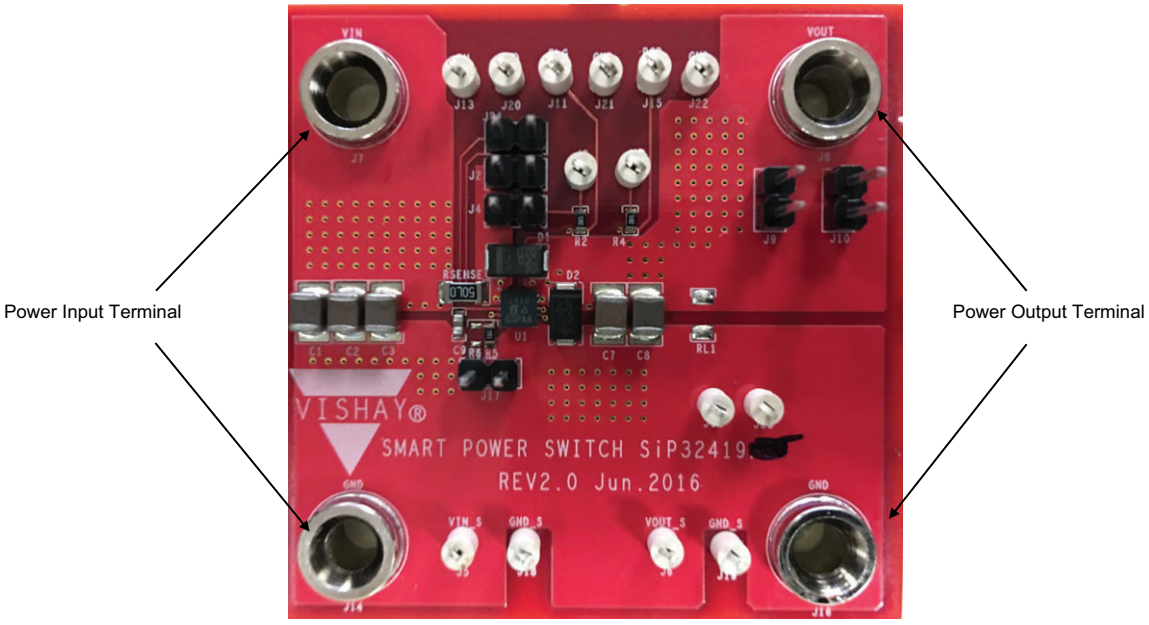


Fig. 1 - SiP32419EVB, SiP32429EVB Evaluation Board Rev. 2.0

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INPUT CAPACITOR AND OUTPUT CAPACITOR

The input capacitors (C1 to C6) and output capacitors (C7, C8) are mounted close to the device to ensure stable voltage right before and after the SiP32419EVB and SiP32429EVB load switch (see fig. 2). The capacitances of these capacitors are 10 µF. The voltage rating for input and output capacitor is 50 V. SiP32419EVB and SiP32429EVB devices can operate normally up to 28 V. It is importance to use the 35 V or higher rated capacitor for the input and output capacitors.

ENABLE TERMINAL

The header J6 is directly connected to the EN pin for the enable function of the device (see fig. 2). The voltage rating of EN pin is 6 V. To have the design margin, never apply voltage higher than 5 V to this enable pin. The enable threshold voltage is 1.5 V and the disable threshold voltage is 0.4 V or lower.

FAULT FLAG AND POWER GOOD FLAG

SiP32419EVB and SiP32429EVB devices have the fault flag and power good flag to indicate the operation status of the device. The header J11 is connected to fault flag of the device. The header J15 is connected power good of the device (see fig. 2). Both flags are open drain pin of the device. An external bias voltage is required to header J1 and J3 to ensure proper operation of these flag. This external bias voltage can be provided by the input voltage by shorting jumpers J2 and J4 because the voltage rating of the power good and fault flag are 28 V maximum.

OVER CURRENT LIMIT SETTING

One of the key features of the SiP32419 and SiP32429 is to provide over current limit protection. Current limit setting resistor R_{SET} can be calculated by the following formula to set the current of the device:

$$I_{LIM} = \frac{1.24\ V \times 5000}{R_{SET}}$$

Where:
R_{SET} is R5 on the board.
I_{LIM} is the target current limit setting.

PROGRAMMABLE SOFT POWER UP

Soft power up is another feature of SiP32419EVB and SiP32429EVB devices. The soft power time is not only the function of I_{SS} and C_{SS} but it also is the function load current and current limiting setting.

The soft power time can be calculated by the following formula:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{SS}}{C_{SS}} \times \frac{R_{OUT} \times 5000}{R_{SET}}$$

Where:
Δt is the soft power up time
ΔV_{OUT} is the output voltage power up range
I_{SS} is the built-in current to charge up C_{SS}. The value is 5 µA
C_{SS} is the soft power setting capacitor shown as C9 on the board
R_{SET} is the current limit resistor, which is C5 on the board
R_{OUT} is the output resistor

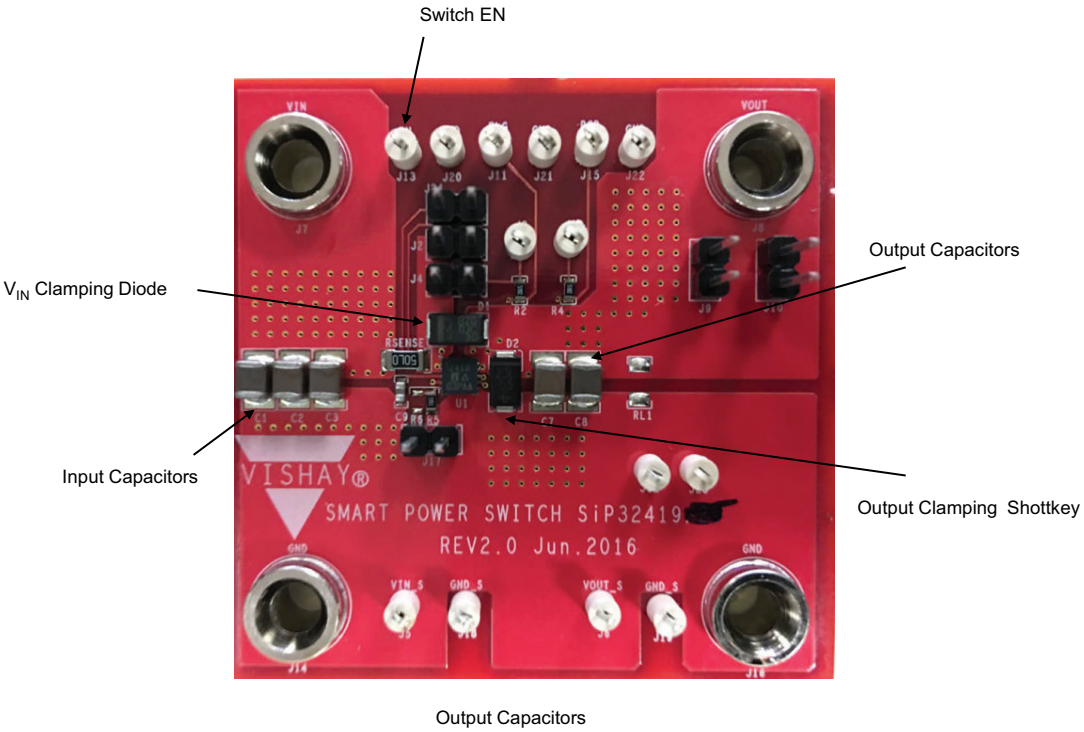


Fig. 2 - SiP32419EVB, SiP32429EVB Evaluation Board Rev. 2.0

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SiP32419EVB, SiP32429EVB EVALUATION BOARD SCHEMATIC

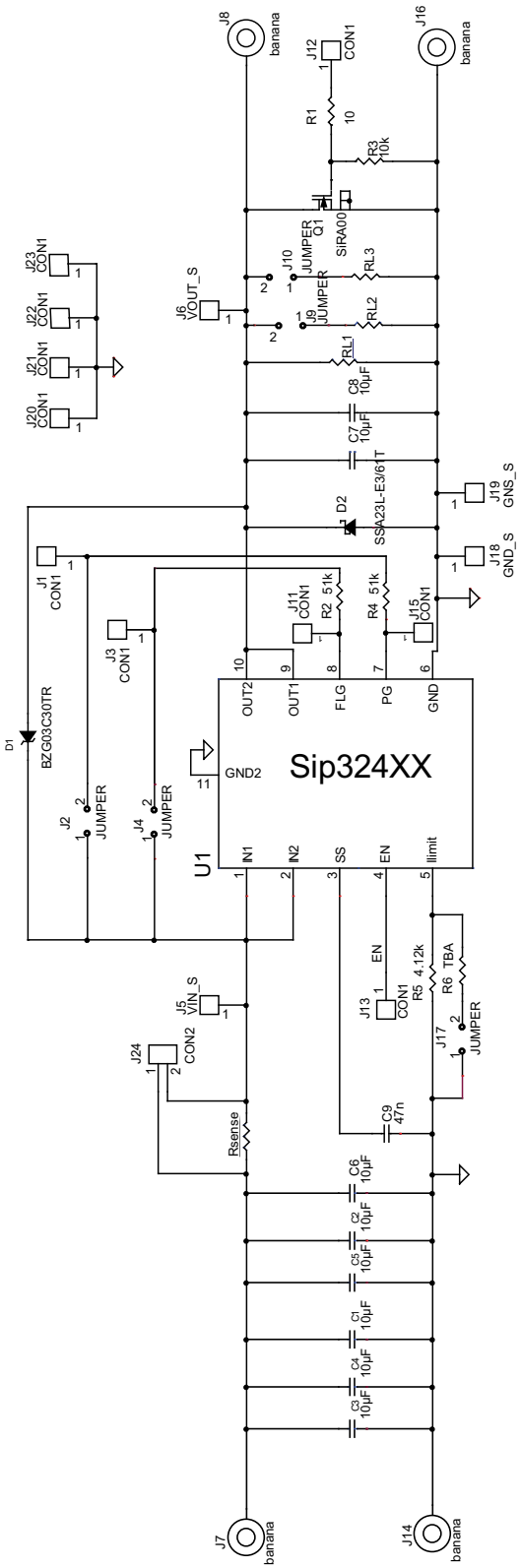


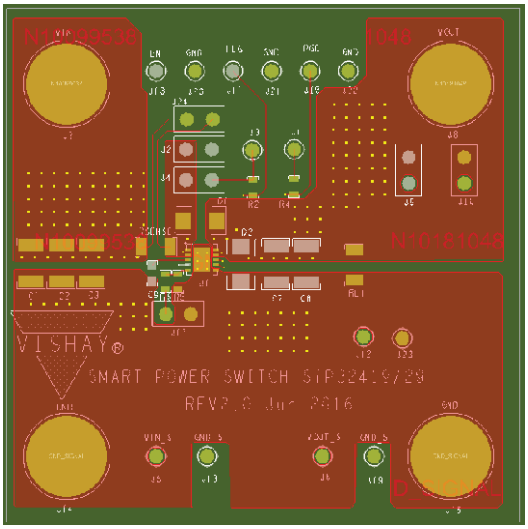
Fig. 3 - SiP32419EVB, SiP32429EVB Evaluation Board Schematic

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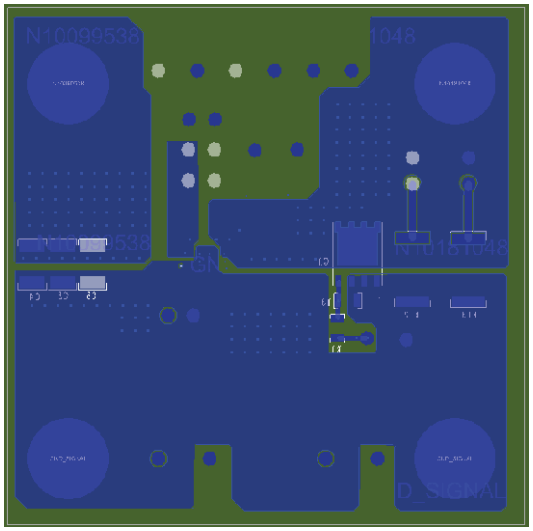
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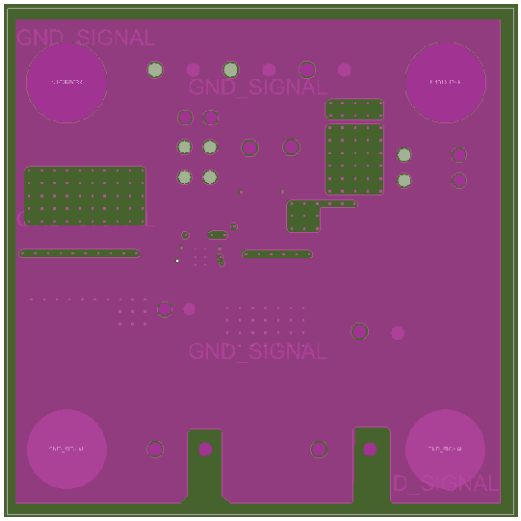
EVALUATION BOARD LAYOUT



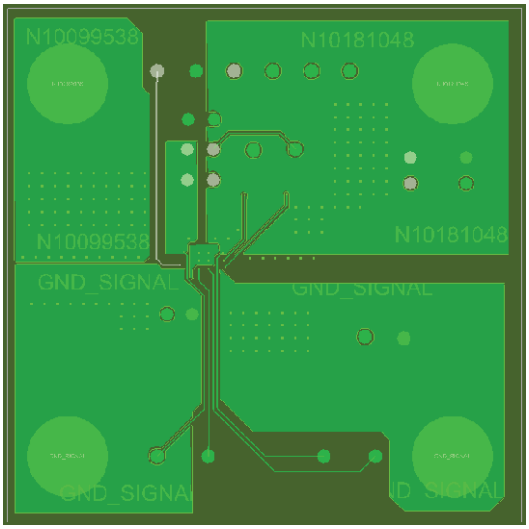
Top Layer



Bottom Layer



Inner 1



Inner 2

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BILL OF MATERIAL						
DESIGNATOR	**QTY**	**VALUE**	**DESCRIPTION**	**PACKAGE**	**MANUFACTURER PART NUMBER**	**MANUFACTURER**
C1, C2, C3, C4, C5, C6, C7, C8	8	10 µF	CAP CER 10 µF 35 V X7R 1210	1210	GRM32ER7YA106KA12L	Murata
C9	1	47 nF	CAP CER 0.047 µF 35 V X7R 0603	0603	GMJ107BB7473KAHT	Taiyo Yuden
D1	1	-	DIODE ZENER 30 V 1.25 W DO214AC	DO214AC	BZG03C30TR	Vishay
D2	1	-	DIODE SCHOTTKY 30 V 2 A DO214AC	DO214AC	SSA23L-E3/61T	Vishay
R1	1	10	RES SMD 10 Ω 1% 1/8 W 0805	0805	CRCW080510R0FKEA	Vishay
R2, R4	2	51 kΩ	RES SMD 51 kΩ 1% 1/10 W 0603	0603	CRCW060351K0FKEA	Vishay
R3	1	10 kΩ	RES SMD 10 kΩ 1% 1/8 W 0805	0805	CRCW080510K0FKEA	Vishay
R5	1	4.12 kΩ (1)	RES SMD 4.12 kΩ 0.1% 1/10 W 0603	0603	TNPW06034K12BEEA	Vishay
R6	-	-	“Do Not Populate”	0603	-	-
RL1	-	-	“Do Not Populate”	1206	-	-
RL2, RL3	-	-	“Do Not Populate”	2515	-	-
RSENNSE	1	50 mΩ	RES SMD 0.05 Ω 1% 1/2 W 1206	1206	RCWE120650L0FNEA	Vishay
Q1	1	SiRA00	MOSFET N-CH 30 V 100 A PPAK SO-8	PPAK SO-8	SIRA00DP-T1-GE3	Vishay
U1	1	SiP32419 SiP32429	IC LOAD SW LVL SHIFT 10DFN	TDFN10	SIP32429DN-T1-GE4	Vishay
J1, J3, J5, J6, J11, J12, J13, J15, J18, J19, J20, J21, J22, J23	14	-	TEST POINT PC MINI 0.040"D WHITE	TP30	5002	Keystone Electronics
J2, J4, J9, J10, J17, J24	6	Jumper	SIL VERTICAL PC TAIL PIN HEADER	SIP2	M20-9990246	xx
J7, J8, J14, J16	4	-	JACK NON-INSULATED 0.218"	Banana	575-4	Keystone Electronics

Note

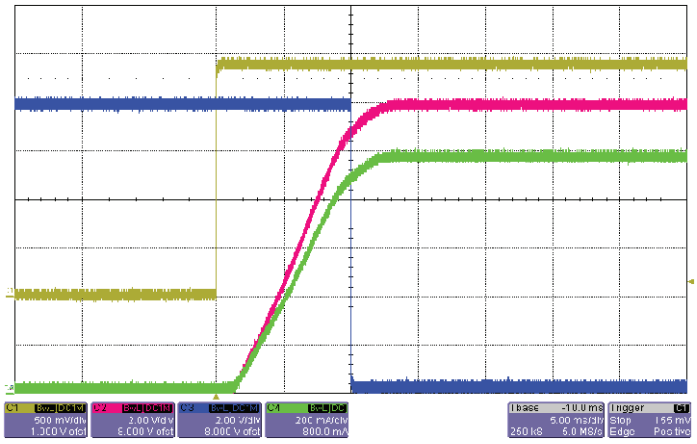
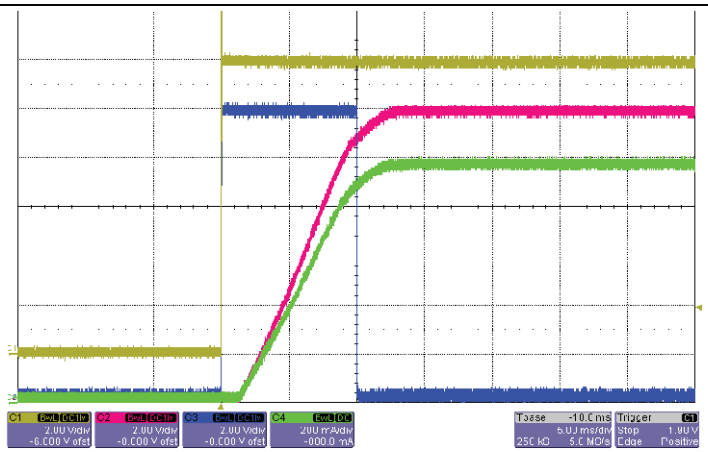
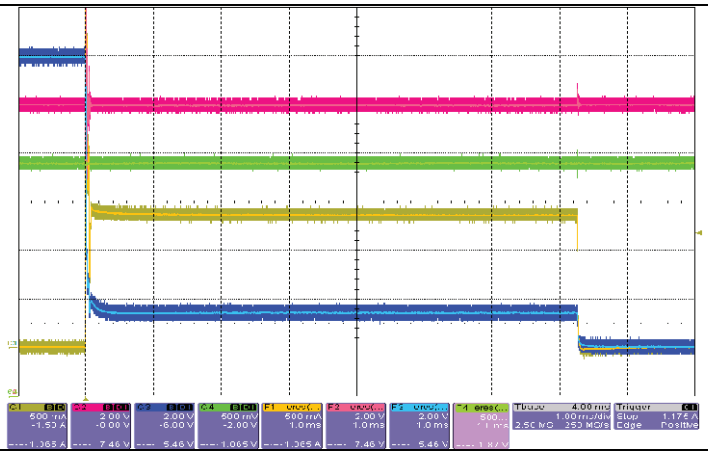
(1) Please refer to marking on board for actual R5 value

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LAB EXPERIMENT RESULT

Enable Power Up Input Voltage = 12 V R_{OUT} = 12 Ω Yellow : Enable voltage Red : Output Voltage Blue : Power Good Voltage Green : Output current	
Step Line Power Up Input Voltage = 12 V R_{OUT} = 12 Ω Yellow : Input Voltage Red : Output Voltage Blue : Power Good Voltage Green : Output current	
Output Short with 1 Ω Resistor Input Voltage = 12 V R_{OUT} = 1 Ω Yellow : Output current Red : Input Voltage Blue : Output Voltage Green : fault flag The measured current limit is 1.365 A The calculated current limit is 1.5 A	

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