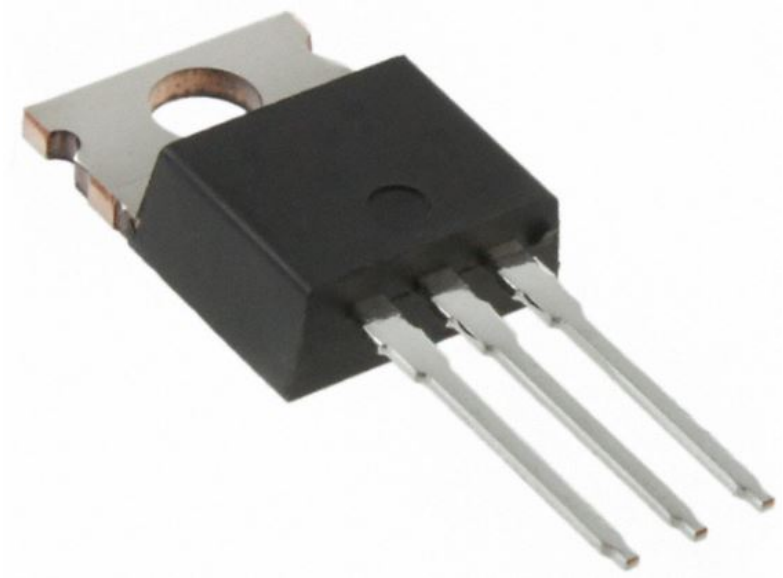


VISHAY IRF9Z34PBF Power MOSFET User Manual

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VISHAY IRF9Z34PBF Power MOSFET



Product Information

Specifications

- **Manufacturer:** Vishay Siliconix
- **Product Name:** IRF9Z34
- **Package Type:** TO-220AB
- **Configuration:** P-Channel MOSFET
- **Drain-Source Voltage (VDS):** -60 V
- **On-Resistance (RDS(on)):** 9.9 Ω
- **Gate Charge (Qg max.):** 16 nC
- **Gate-Source Charge (Qgs):** 0.14 nC
- **Gate-Drain Charge (Qgd):** 5.9 nC

Description

The IRF9Z34 is a third-generation power MOSFET from Vishay Siliconix. It offers fast switching, ruggedized device design, low on-resistance, and cost-effectiveness. The TO-220AB package is widely preferred for commercial-industrial applications with power dissipation levels up to approximately 50 W. The package has low thermal resistance and is cost-effective, making it widely accepted in the industry.

Ordering Information

Package	Lead (Pb)-free	Lead (Pb)-free and halogen-free
TO-220AB	IRF9Z34PbF	IRF9Z34PbF-BE3

Thermal Resistance Ratings

Parameter	Symbol	TYP.	MAX.
Maximum junction-to-ambient	RthJA	–	62
Case-to-sink, flat, greased surface	RthCS	0.50	1.7
Maximum junction-to-case (drain)	RthJC	–	–

Product Usage Instructions

Installation

To install the IRF9Z34 Power MOSFET, follow these steps:

1. Select an appropriate heat sink for the TO-220AB package.
2. Ensure the mounting surface is clean and free from debris.
3. Apply a thin layer of thermal grease to the case of the MOSFET.
4. Screw the MOSFET onto the heat sink using a 6-32 or M3 screw with the specified mounting torque.

Electrical Connections

Make the following electrical connections:

- Connect the drain (D) pin of the MOSFET to the load or circuit ground.
- Connect the source (S) pin of the MOSFET to the power supply ground.
- Connect the gate (G) pin of the MOSFET to the gate driver circuit.

Operating Conditions

The IRF9Z34 operates within the following conditions:

- **Operating Junction Temperature (TJ):** -55°C to +175°C
- **Storage Temperature (Tstg):** -55°C to +175°C
- **Soldering Recommendations (peak temperature):** 300°C for 10 seconds

Frequently Asked Questions (FAQ)

- **Q: What is the maximum drain-source voltage (VDS) of the IRF9Z34?**
  A: The maximum drain-source voltage is -60V.
- **Q: Is the IRF9Z34 RoHS compliant?**
  A: The datasheet provides information about RoHS-compliant and non-RoHS-compliant parts. Parts with lead (Pb) terminations are not RoHS-compliant. Please refer to the information in the datasheet for specific details.
- **Q: What is the on-resistance (RDS(on)) of the IRF9Z34?**
  A: The on-resistance is 9.9 Ω.

FEATURES

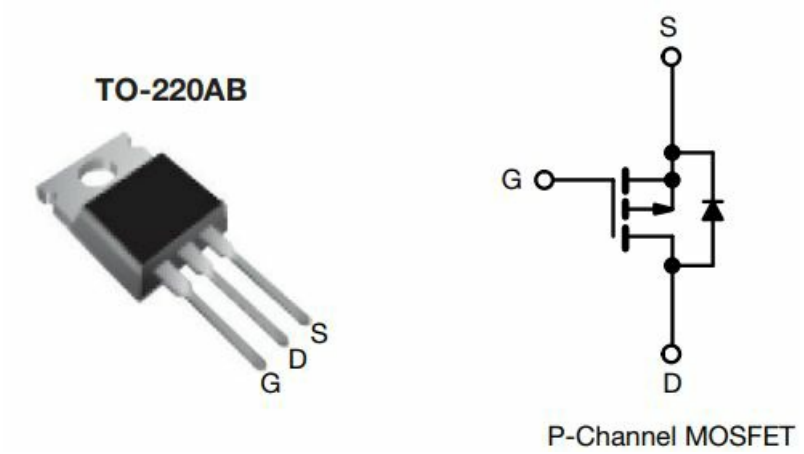
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel

- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third-generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.



PRODUCT SUMMARY

V_{DS} (V)	-60	
RDS(on) (W)	V_{GS} = -10 V	0.14
Q_g max. (nC)	34	
Q_{gs} (nC)	9.9	
Q_{gd} (nC)	16	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9Z34PbF
Lead (Pb)-free and halogen-free	IRF9Z34PbF-BE3

ABSOLUTE MAXIMUM RATINGS

(TC = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			VDS	-60	V
Gate-source voltage			VGS	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	-18	A
		T_C = 100 °C		-13	
Pulsed drain current a			IDM	-72	
Linear derating factor				0.59	W/°C
Single pulse avalanche energy b			EAS	370	mJ
Repetitive avalanche current a			IAR	-18	A
Repetitive avalanche energy a			EAR	8.8	mJ
Maximum power dissipation	T_C = 25 °C		P_D	88	W
Peak diode recovery dV/dt c			dV/dt	-4.5	V/ns
Operating junction and storage temperature range			TJ, Tstg	-55 to +175	°C
Soldering recommendations (peak temperature) d	For 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- **a.** Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- **b.** VDD = -25 V, starting TJ = 25 °C, L = 1.3 mH, Rg = 25 Ω, IAS = -18 A (see fig. 12).
- **c.** ISD ≤ -18 A, dI/dt ≤ 170 A/μs, VDD ≤ VDS, TJ ≤ 175 °C.
- **d.** 1.6 mm from case.

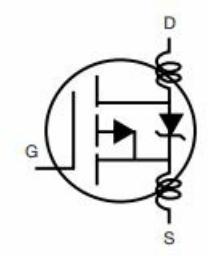
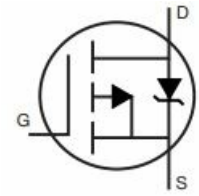
THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	RthJA	–	62	°C/W
Case-to-sink, flat, greased surface	RthCS	0.50	–	
Maximum junction-to-case (drain)	RthJC	–	1.7	

SPECIFICATIONS

(TJ = 25 °C, unless otherwise noted)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	VDS	V_{GS} = 0 V, I_D = -250 µA		-60	–	–	V
V_{DS} temperature coefficient	DV_{DS}/T_J	Reference to 25 °C, I_D = -1 mA		–	-0.060	–	V/°C
Gate-source threshold voltage	VGS(th)	V_{DS} = V_{GS}, I_D = 250 µA		-2.0	–	-4.0	V
Gate-source leakage	IGSS	V_{GS} = ± 20 V		–	–	± 100	nA
Zero gate voltage drain current	IDSS	V_{DS} = -60 V, V_{GS} = 0 V		–	–	-100	µA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 150 °C		–	–	-500	
Drain-source on-state resistance	RDS(on)	V_{GS} = -10 V	I_D = -11 A b	–	–	0.14	W
Forward transconductance	gfs	V_{DS} = -25 V, I_D = -11 A b		5.9	–	–	S
Dynamic							
Input capacitance	Ciss	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz, see fig. 5		–	1100	–	pF
Output capacitance	Coss			–	620	–	
Reverse transfer capacitance	Crss			–	100	–	
Total gate charge	Q_g	V_{GS} = -10 V	I_D = -18 A, V_{DS} = -48 V, see fig. 6 and 13 b	–	–	34	nC
Gate-source charge	Qgs			–	–	9.9	
Gate-drain charge	Qgd			–	–	16	
Turn-on delay time	td(on)	V_{DD} = -30 V, I_D = -18 A, R_g = 12 W, R_D = 1.5 W, see fig. 10 b		–	18	–	ns
Rise time	t_r			–	120	–	
Turn-off delay time	td(off)			–	20	–	
Fall time	t_f			–	58	–	
Gate input resistance	L_D	Between lead, 6 mm (0.25″) from package and center of die contact		–	4.5	–	nH

Internal drain inductance	L_S		–	7.5	–	
Internal source inductance	R_g	f = 1 MHz, open drain	0.7	–	3.9	W
Drain-Source Body Diode Characteristics						
Continuous source-drain diode c urrent	I_S	MOSFET symbol showing the in tegral reverse p -n junction diode 	–	–	-18	A
Pulsed diode forward current a	ISM		–	–	-72	
Body diode voltage	VSD	T_J = 25 °C, I_S = -18 A, V_{GS} = 0 V b	–	–	-6.3	V
Body diode reverse recovery tim e	trr	T_J = 25 °C, I_F = -18 A, dI/dt = 10 0 A/µs b	–	100	200	ns
Body diode reverse recovery cha rge	Qrr		–	0.28	0.52	µC
Forward turn-on time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- **a.** Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- **b.** Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS

(25 °C, unless otherwise noted)

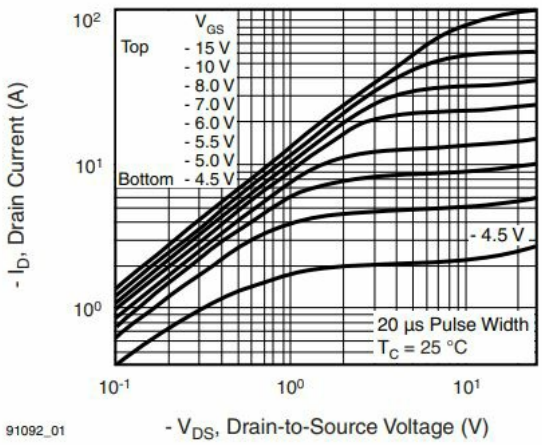


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

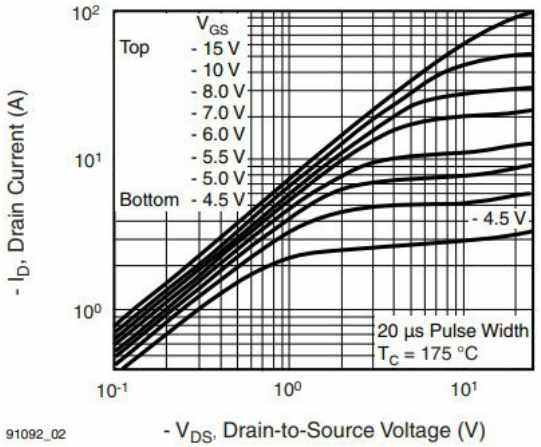


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

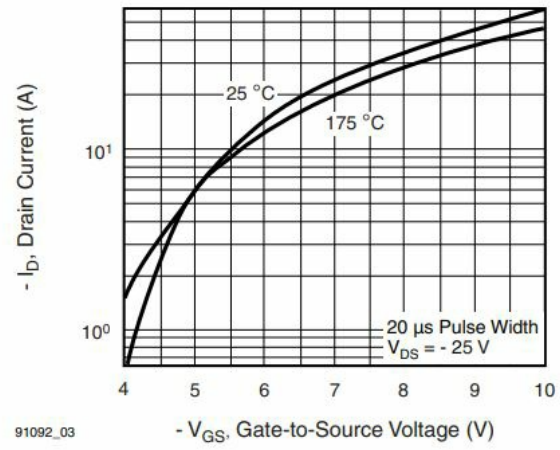


Fig. 3 - Typical Transfer Characteristics

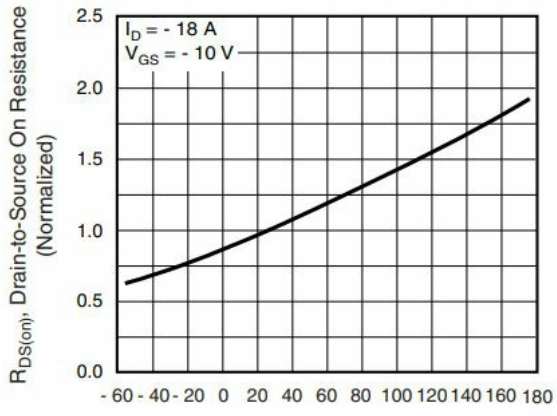


Fig. 4 - Normalized On-Resistance vs. Temperature

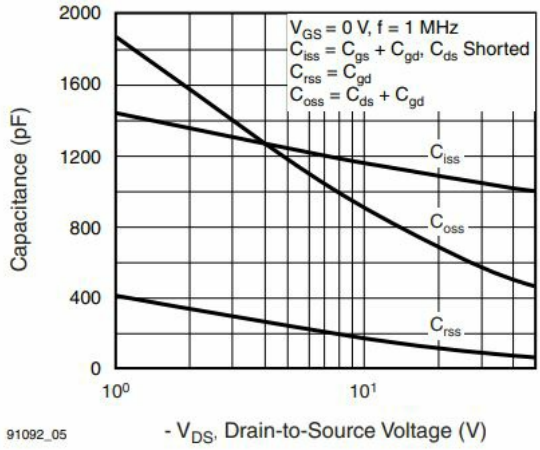


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

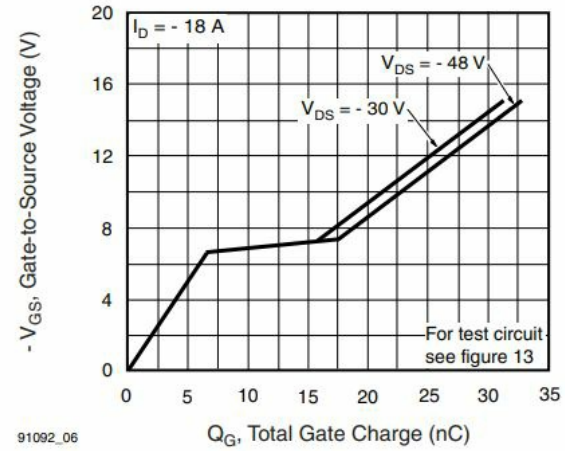


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

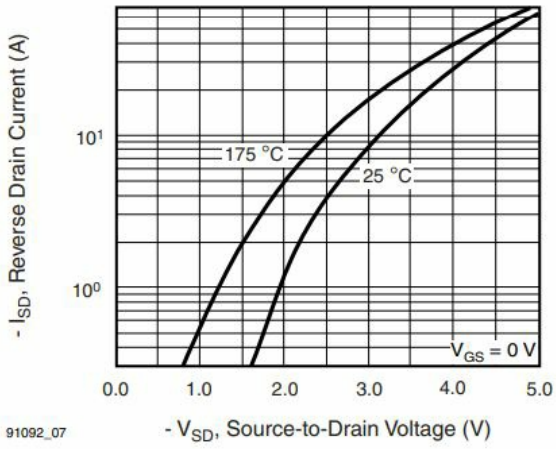


Fig. 7 - Typical Source-Drain Diode Forward Voltage

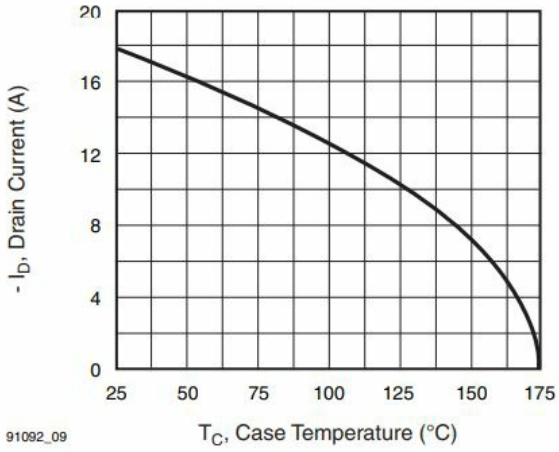


Fig. 9 - Maximum Drain Current vs. Case Temperature

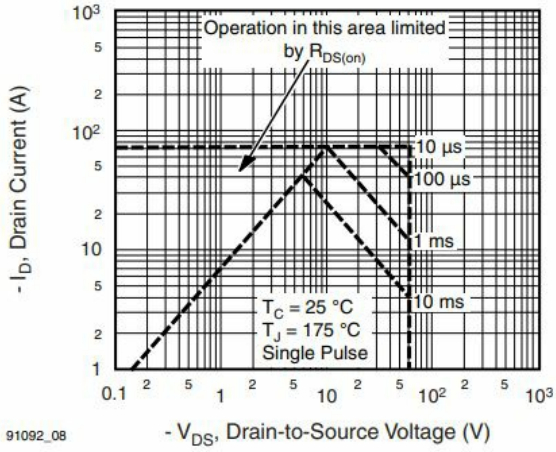


Fig. 8 - Maximum Safe Operating Area

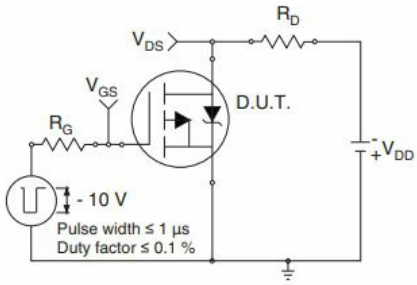


Fig. 10a - Switching Time Test Circuit

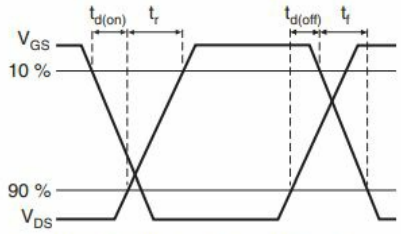


Fig. 10b - Switching Time Waveforms

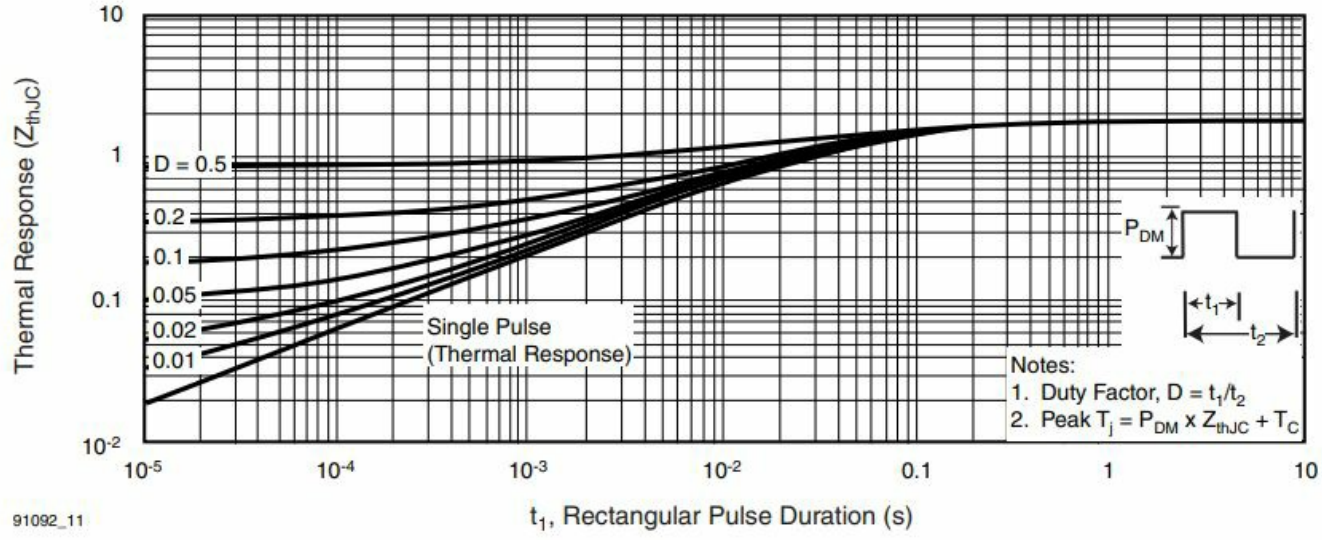


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

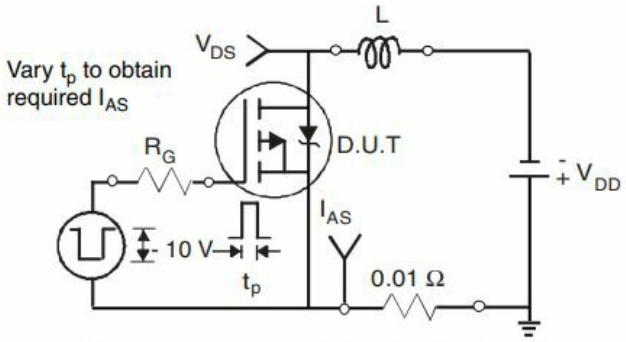


Fig. 12a - Unclamped Inductive Test Circuit

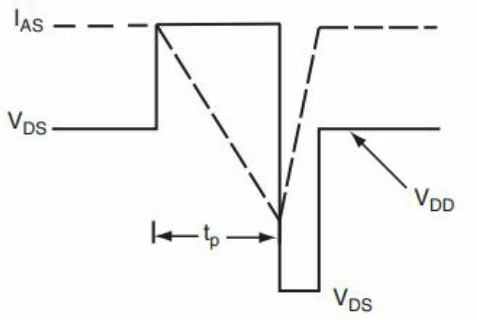


Fig. 12b - Unclamped Inductive Waveforms

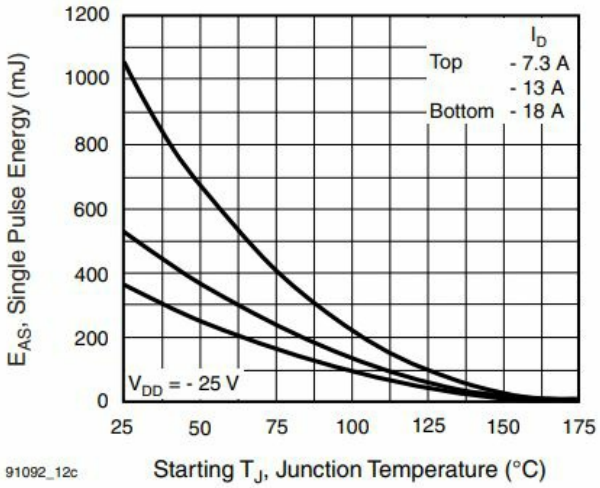


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

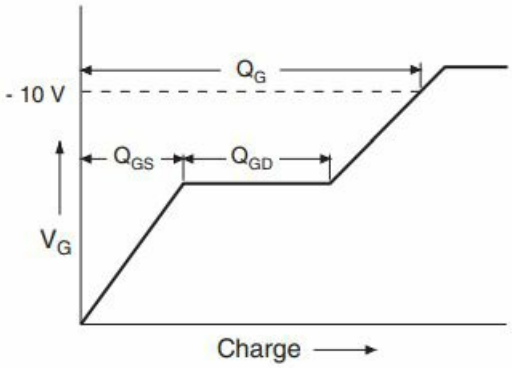


Fig. 13a - Basic Gate Charge Waveform

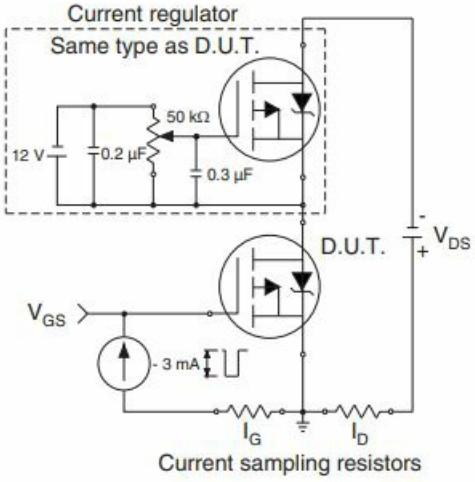


Fig. 13b - Gate Charge Test Circuit

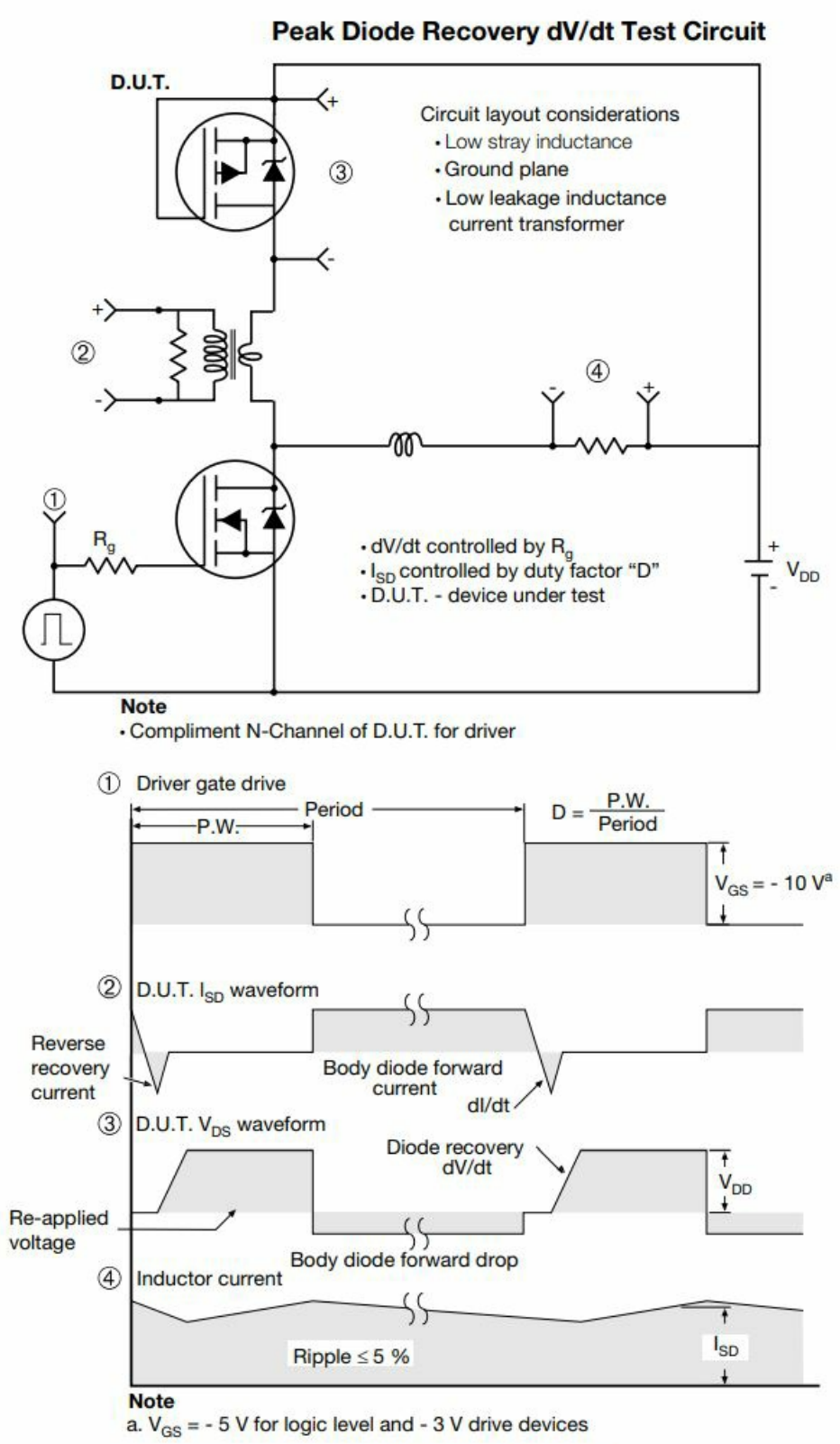


Fig. 14 - For P-Channel

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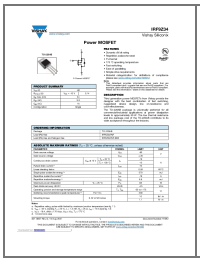
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