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ACL-7122

144-Bit Parallel Digital I/O Board

User's Manual

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How to Use This Manual

This manual is designed to help you use the ACL-7122. The manual describes how to modify various settings on the ACL-7122 card to meet your requirements. It is divided into five chapters:

- Chapter 1, "Introduction," gives an overview of the product features, applications, and specifications.
- Chapter 2, "Installation," describes how to install the ACL-7122. The layout of ACL-7122 is shown, the DIP switch setting for base address, and jumpers setting for IRQ level and interrupt status are specified.
- Chapter 3, "Digital I/O Programming," describes how to program the digital input and output channels on the ACL-7122.
- Appendix A, " I/O Port Address Map", specifies the PC's default I/O Port address map.

1

Introduction

The ACL-7122 - 144 Bit Digital I/O board is a high density parallel Digital I/O board for ISA bus-compatible computer in industrial applications. It is fully hardware and software compatible with Advantech's PCL-722.

This board provides 6 sets to emulate industry standard 8255 Programmable Peripheral Interface (PPI) chips, each offers 3 ports: PA, PB, and PC. PC is subdivided into 2 nibble-wide (4-bit) ports. Each channel has an individual connector with OPTO-22 pin assignment. It is very essential to use isolated input to prevent the ground loop problems.

The ACL-7122 is programmed using simple 8-bit I/O port commands. Users can use high level language, such as BASIC, C, or PASCAL, or low level language, such as Assembly to program the board. It is not any special software driver supported.

1.1 Features

The ACL-7122 144-Bit Parallel Digital I/O Board provides the following advanced features:

- Compact size (suitable for any size of chessis)
- 144 TTL/DTL compatible digital I/O lines
- Emulates six industry standard mode 0 of 8255 PPI
- Buffered circuits for higher driving
- Direct interface with OPTO-22 compatible I/O module
- Programmable interrupt handling
- Output status readback
- Fully hardware and software compatible with Advantech PCL-7122

1.2 Applications

- High-density programmable mixed digital input & output
- Industrial monitoring and control
- Digital I/O control
- Contact closure, switch/keyboard monitoring
- Connects with OPTO-22 compatible modules
- Useful with A/D and D/A to implement a data acquisition & control system

1.3 Specifications

Input channels	144
Input Signal	Logic High Voltage :2.0 V to 5.25V Logic Low Voltage : 0.0 V to 0.80V Logic High Current : 22.0 uA Logic Low Current : -0.2 mA
Output Signal (Port A & B)	Logic High Voltage : Minimum 2.4 V Logic Low Voltage : Maximum 0.5V Logic High Current : -2.6 mA Logic Low Current : 24.0 mA
Output Signal (Port C)	Logic High Voltage : Minimum 2.4 V Logic Low Voltage : Maximum 0.4V Logic High Current : -15.0 mA Logic Low Current : 24.0 mA
Operating Temperature	0° ~ 60° C
Storage Temperature	-20° ~ 80° C
Humidity	5% ~ 95% non-condensing
I/O Connector	50-pin male ribbon cable connector
Bus	PC/AT Bus
I/O port address	Hex 200 ~ Hex 3F8
Power Consumption	5V 1.4 A (Typical) 5V 1.8 A (Maximum)
Transfer Rate	300 K bytes/sec (Typical) 500 K bytes/sec (Maximum)
Size	Half Size (183mm X 111 mm)

2

Installation

This chapter describes how to install the ACL-7122. At first, the contents in the package and unpacking information that you should be careful are described. The jumpers and switches setting for the ACL-7122's base address and interrupt IRQ level are also specified.

2.1 What You Have

In addition to this manual, the package includes the following items:

- ACL-7122 144-bit Parallel Digital I/O Card

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

Your ACL-7122 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be done on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handing damages on the module before processing.

After opening the card module carton, exact the system module and place it only on a grounded anti-static surface component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your ACL-7122.

2.3 ACL-7122's Layout

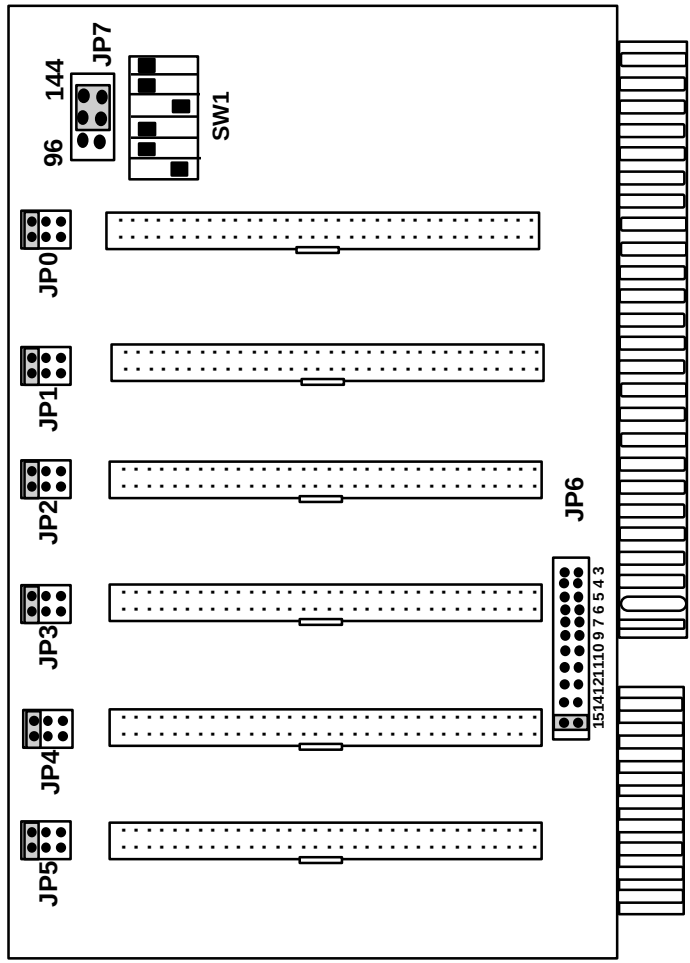


Figure 2.1

2.4 Jumper and DIP Switch Description

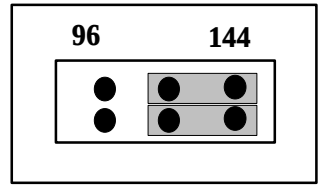
You can change the ACL-7122's base address, address parameters, and interrupt by setting DIP switches and jumpers on the card. The card's jumpers and switches are preset at the factory. Under normal circumstances, you should not need to change the jumper settings.

A jumper switch is closed (sometimes referred to as "shorted" with the plastic cap inserted over two pins of the jumper). A jumper is open with the plastic cap inserted over one or no pin(s) of the jumper.

2.5 DIO Channel No. Setting

The ACL-7122 can provide two kinds of I/O capability modes 144-bit and 96-bit, which are selected by DIP switch **JP7** (see Figure 2.2 below). The 144-bit mode requires 32 consecutive I/O address ports, and 96-bit mode just occupies 16 address ports. Generally speaking, the ACL-7122 should be left in the 144-bit mode unless this address conflicts with the addresses of other peripherals.

(Default Setting)



JP7

Figure 2.2

Note : In 96-bit mode, two or more boards can be mapped consecutively on adjacent addresses. But, the 144-bit mode, each board should have a gap of 8 addresses at least.

2.6 Base Address Setting

The ACL-7122 requires 32 or 16 consecutive address locations in I/O address space. The base address of the ACL-7122 is restricted by the following conditions.

1. The base address must be within the range 200hex to 3FFhex.

2. The base address should not conflict with any PC reserved I/O address. (refer to Appendix A)

The ACL-7122 requires 32 consecutive address locations for 144-bit mode, or 16 address locations for 96-bit mode. The I/O port base address is selectable by a 5 position DIP switch SW1 (refer to Figure 2.3). The address setting of 144-bit mode for I/O port from hex200 to hex3FE is described in Table 2.2. The address setting of 96-bit mode is described in Table 2.3.

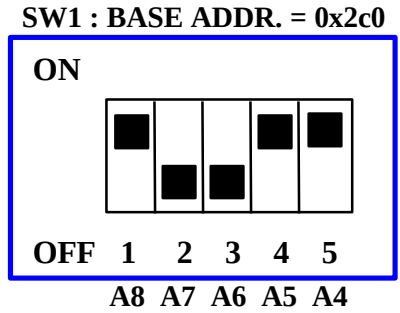


Figure 2.3

I/O port address(hex)	2 A8	3 A7	4 A6	5 A5	6 A4
200-21F	ON (0)	ON (0)	ON (0)	ON (0)	X
:					
(*) 2C0-2DF	ON (0)	OFF (1)	OFF (1)	ON (0)	X
:					
380-29F	OFF (1)	OFF (1)	OFF (1)	ON (0)	X
3A0-3BF	OFF (1)	OFF (1)	OFF (1)	OFF (1)	X
3C0-3DF	OFF (1)	OFF (1)	OFF (1)	ON (0)	X
3E0-3FF	OFF (1)	OFF (1)	OFF (1)	OFF (1)	X

(*) : default setting
X : Don't care
ON = 0 ; OFF = 1
A2, ..., A8 are corresponding to address lines of ISA bus.
A9 is always **1** (OFF).

Table 2.2 144-bit mode

Note : In 144-bit mode, the base address line A4 is not in functional status, so, do not care the position of A4 of SW1.

I/O port Address(hex)	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	ON	ON	ON	ON	ON
:					
290-29F	ON	OFF	ON	ON	OFF
2A0-2AF	ON	OFF	ON	OFF	ON
:					
3D0-3DF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF

Table 2.3 96-bit mode

How to Define a Base Address for the ACL-7122 ?

The DIP1 to DIP6 in the switch SW1 are one to one corresponding to the PC bus address line A9 to A4. A9 is always 1; A3 to A0 are always 0 with hardware. If you want to change the base address, you can only change the values of A8 to A4 (shadow area of below diagram). Following is an example, which shows you how to define the base address as **Hex 2C0**.

Base Address : **Hex 2C0**

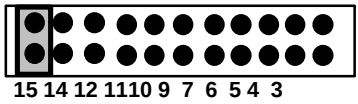
2		**C**					**0**			
1	**0**	**1**	**1**	**0**	**0**		**0**	**0**	**0**	**0**
A9	A8	A7	A6	A5	A4		A3	A2	A1	A0
OFF	**ON**	**OFF**	**OFF**	**ON**	**ON**					

2.7 Interrupt Setting

The ACL-7122 provides 11 interrupt requests IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15, which could be set for hardware interrupt generated by pins PC-0 and PC-3 of each channel. The IRQ is set by jumper JP6.(Ref. Figure 2.1)

The IRQ signal is Tri-state allowing multiple ACL-7122 boards to share the same interrupt line. For example, two ACL-7122 can set to IRQ 15 in one system.

Default Setting level : IRQ15



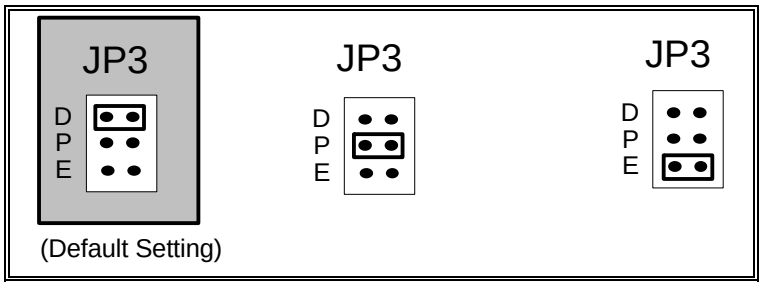
JP6

The ACL-7122 has two lines (PC-0 and PC-3) for each channel to generate hardware interrupt. The interrupt are edge-triggered, PC-0 traps a rising edge signal, which PC-3 traps a falling edge signal.

To use the interrupt, first you have to select the desired IRQ interrupt level. To determine which input generated the interrupt, you can read Port C, bit PC-0 and bit PC-3, to locate the current state of inputs.

Note : Input is not latched and no first event trapping is provided to determine which input was active first.

There are six jumpers JP0 to JP5, which are corresponding to each channel in ACL-7122, for interrupt enabled selection. The figure 2.3 below shows three status of interrupt setting for CH3.



D: Disabled Interrupt - No interrupt request
P: Programmable Interrupt - interrupt when CH3's PC4 is "Low"
E: Enable Interrupt - interrupts request

Figure 2.3

****** A Summary of Interrupt Status**

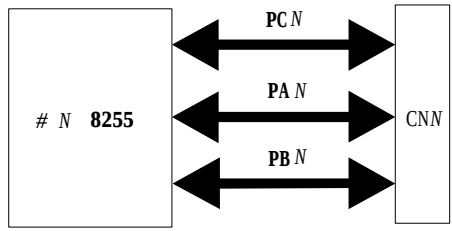
In ACL-7122, the interrupt trigger status are depended on jumper J0 to J5, and, I/O lines, PC0, PC3 and PC4. All the possibility of interrupt status are shown in the following table.

JPn(n=0...5)	PC0	PC3	PC4	Interrupt Status
 JPn	X	X	X	**No Interrupt Request**
 JPn	LOW L->H	L -> H HIGH	LOW	**Interrupt Request**
 JPn	HIGH X	X LOW	LOW	**No Interrupt Request**
 JPn	X	X	HIGH	**No Interrupt Request**
 JPn	HIGH X	X LOW	X	**Interrupt Request**
 JPn	X	X	X	**Interrupt Request**

X : Don't Care
H-> L : Rising Edge Trigger (from High to Low)
L->H : Falling Edge Trigger (from Low to High)

2.8 Connector Pin Assignment

The I/O ports of ACL-7122 emulates as six mode 0 Intel 8255 general purpose programmable peripheral interface. Figure 2.4 shows ACL-7122's equally block diagram. There are six 50-pin connectors come equipped with the ACL-7122 board, and each of them is corresponding to a mode 0 of 8255. The connector pin assignment is specified in Figure 2.5 below.



N = 0, ..., 5

Figure 2.4

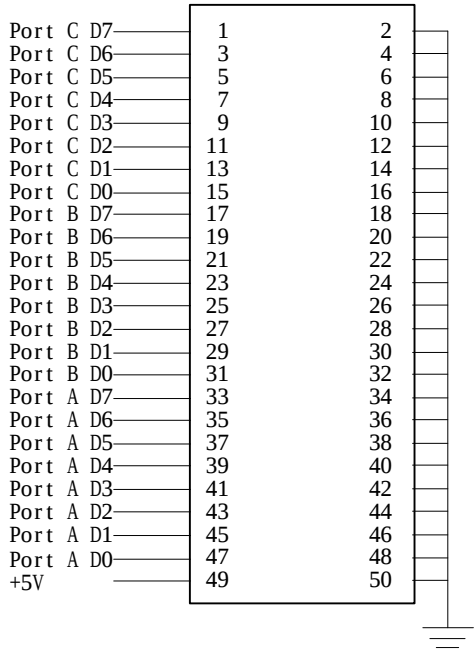


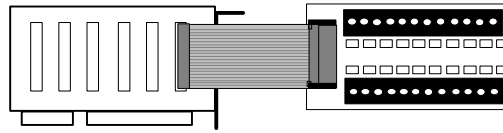
Figure 2.5 Connector Pin Assignment

2.9 Connection

There are three daughter boards to connect with ACL-7122 for DIO operation. The following diagrams show you how to configuration your ACL-7122 with different terminal boards.

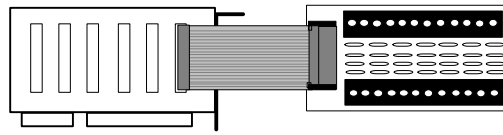
1. TB-24R

The TB-24R provides 24 Form C relays for digital output control. The connection between ACL-7122 and TB-24R is :



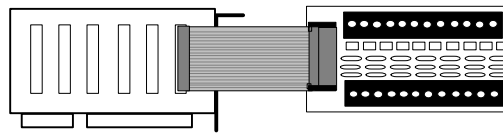
2. TB-24 P

The TB-24P provides 24 opto-isolated digital input channels, the connection between ACL-7122 and TB-24R is :



3. TB-16P8R

The TB-16P8R provides 16 opto-isolated digital input channels and 8 relay outputs, the connection between ACL-7122 and TB-16P8R is :



3

Digital I/O Programming

3.1 Register Structure & Format

The ACL-7122 needs 24 bytes of I/O address to operate. The relationship of I/O address and ports' data read / write shows as following table (Table 4.2), the default base address of below table is 2C0H.

PORT SELECT	ADDR.	NOTE
CH0 PA0	2C0H	EMULATE AS 8255 PA
CH0 PB0	2C1H	EMULATE AS 8255 PB
CH0 PC0	2C2H	EMULATE AS 8255 PC
CONTROL WORD CH0	2C3H	EMULATE AS 8255 CW
CH1 PA1	2C4H	EMULATE AS 8255 PA
CH1 PB1	2C5H	EMULATE AS 8255 PB
CH1 PC1	2C6H	EMULATE AS 8255 PC
CONTROL WORD CH1	2C7H	EMULATE AS 8255 CW
CH2 PA2	2C8H	EMULATE AS 8255 PA
CH2 PB2	2C9H	EMULATE AS 8255 PB
CH2 PC2	2CAH	EMULATE AS 8255 PC
CONTROL WORD CH2	2CBH	EMULATE AS 8255 CW
CH3 PA3	2CCH	EMULATE AS 8255 PA
CH3 PB3	2CDH	EMULATE AS 8255 PB
CH3 PC3	2CEH	EMULATE AS 8255 PC
CONTROL WORD CH3	2CFH	EMULATE AS 8255 CW
CH4 PA4	2D0H	EMULATE AS 8255 PA

CH4 PB4	2D1H	EMULATE AS 8255 PB
CH4 PC4	2D2H	EMULATE AS 8255 PC
CONTROL WORD CH4	2D3H	EMULATE AS 8255 CW
CH5 PA5	2D4H	EMULATE AS 8255 PA
CH5 PB5	2D5H	EMULATE AS 8255 PB
CH5 PC5	2D6H	EMULATE AS 8255 PC
CONTROL WORD CH5	2D7H	EMULATE AS 8255 CW

Table 4.2 Ports' I/O address table
(Base Address = 2C0H)

3.2 Mode 0 of 8255 PPI

The ACL-7122 can emulates MODE 0 of 8255 PPI, and it comes equipped with six 50-pin male IDC connectors that interface with OPTO-22 racks 8, 16, and 24.

The basic functions definition of 8255 mode 0 are :

- Two 8-bit I/O ports - PA and PB
- Two nibble-wide (4-bit) ports - PC upper and PC lower
- Any ports can be used for both input and output
- Outputs are latched whereas inputs are not latched
- 16 different input/output configurations are available

Two of the I/O lines (PC-0, PC-3) of each channel can be used to generate a hardware interrupt.

The I / O of ACL-7122 emulates as six 8255 programmable peripheral interface chips, the control word is to program PA, PB and PC as input port or output port. Table shows the summarize of control word (D0 - D4), and mode state (Mode 0 - Mode 15).

Mode	Config. Value	D4	D3	D1	D0	PORT A	PORT C UPPER	PORT B	PORT C LOWER
0	**80H**	0	0	0	0	O/P	O/P	O/P	O/P
1	**81H**	0	0	0	1	O/P	O/P	O/P	I/P
2	**82H**	0	0	1	0	O/P	O/P	I/P	O/P
3	**83H**	0	0	1	1	O/P	O/P	I/P	I/P

4	**88H**	0	1	0	0	O/P	I/P	O/P	O/P
5	**89H**	0	1	0	1	O/P	I/P	O/P	I/P
6	**8AH**	0	1	1	0	O/P	I/P	I/P	O/P
7	**8BH**	0	1	1	1	O/P	I/P	I/P	I/P
8	**90H**	1	0	0	0	I/P	O/P	O/P	O/P
9	**91H**	1	0	0	1	I/P	O/P	O/P	I/P
10	**92H**	1	0	1	0	I/P	O/P	I/P	O/P
11	**93H**	1	0	1	1	I/P	O/P	I/P	I/P
12	**98H**	1	1	0	0	I/P	I/P	O/P	O/P
13	**99H**	1	1	0	1	I/P	I/P	O/P	I/P
14	**9AH**	1	1	1	0	I/P	I/P	I/P	O/P
15	**9BH**	1	1	1	1	I/P	I/P	I/P	I/P

Table 4.1 Summarize of control word (D0 - D4) and mode state (Mode 0 - Mode 15)

3.3 Interrupt Handling

The ACL-7122 can generate a hardware interrupt to your PC. The following issues should be careful when you want to generate an interrupt trigger.

1. Interrupt IRQ level setting : make sure you already set the right IRQ level by using the jumper J6. Please refer to section 2.7 "interrupt setting".

2. Interrupt trigger status setting :

a. interrupt mode : make sure the jumper J2 is already set as *E(Enable)* or *P(PMG)* mode.

b. interrupt trigger edge : if you choose E mode, be careful the following combinations of PC-0 and PC-3:

PC-0	PC-3	Status
High	X	No Interrupt Request
Low	High >> Low	Interrupt Request
X	Low	No Interrupt Request
Low >> High	High	Interrupt Request

(X) : Don't care

c. Programmable mode: if you choice P mode, confirm the, I/O line, PC-4 is kept in TTL LOW status. Otherwise, there is no interrupt trigger will be occurred. The relatioship between PC-4, PC-3 and PC-0 is :

PC-4	PC-0	PC-3	Status
Low	High	X	No Interrupt Request
	Low	High >> Low	Interrupt Request
	X	Low	No Interrupt Request
	Low >> High	High	Interrupt Request
High	X	X	No Interrupt Request

(X) : Don't care

Note : Since the ACL-7122's Input is not latched and no first event trapping is provided to determine which input was active first.

Self Interrupt Trigger
Although the ACL-7122's interrupt signals are normal received from external peripherals. It can also generate a test output signal to emulate an interrupt being inputted from an external device. An example program is shown in the section 3.5 for reference.

3.4 Programming Notes

Before programming the ACL-7122, the following notes will help you are more skillful to control the I/O operations through the ACL-7122.

1. Default Input Mode
After power-on or hardware reset your PC system, all the ports of ACL-7122 are automatically configured as *INPUT* mode.

2. Output Latch

When an output port is programmed as output mode through control word, it will not affect the connected output device until an output instruction is executed. This means the data will not output until execute the first output instruction.

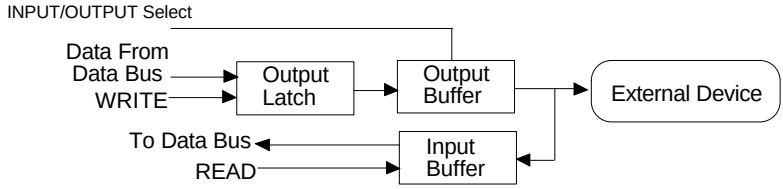


Figure 3.1 ACL-7122's Signal Direction

3. According the above ACL-7122's signal direction block diagram, some issues should be careful.

a. When a port is set as INPUT or after hardware RESET, its output buffer is *Disabled* (high impedance)

b. The output data is lactated in the *Output Latch* when it is set as OUTPUT mode.

c. When the port is set as OUTPUT, the input circuit is used as an output status read-back.

d. The data in Output Latch is an random value after power on. It has to be initialized before the port to output direction.

3.5 Programming in C language

The following parts are example programs written in C language. The first four parts are just partial programs for your reference, you can not compile them before these programs are complete.

The last program is an example for interrupt handling, you could compile it by Borland C/C++ compiler directly.

1. To initial I/O port

```
# define BASE 0x2C0      //define base address
# define CWD0 0x80       //XX refer to 8255 CW
int i;

for( i = 0 ; i < 6; i++)
{
    outportb( BASE + i * 4 + 0 , 0x00);
    outportb( BASE + i * 4 + 1 , 0x00);
    outportb( BASE + i * 4 + 2 , 0x00);
    outportb( BASE + i * 4 + 3 , CWD);
                           /* all as output */
}
```

2. To write port

```
# define BASE 0x2C0      //define base address
# define PA   0x0        // Port A
# define PB   0x1        // Port B
# define PC   0x2        // Port C
# define CWD 0x80        //ALL output to 8255 CW


outportb(BASE + 3,CWD);  //index to CH0 CW
outportb(BASE + PA ,0x23);// write 23H to CH0 PA
outportb(BASE + PB ,0x45);// write 45H to CH0 PA
outportb(BASE + PC ,0xfd);// write fdH to CH0 PA
```

3. To access port

```
# define BASE 0x2C0      //define base address
```

```
# define PA   0x0        // Port A
# define PB   0x1        // Port B
# define PC   0x2        // Port C
# define CWD 0x9B        //ALL input from 8255 CW
int pa_data, pb_data, pc_data;

outportb(BASE + 3,CWD);  //index to CH0 CW
pa_d = inportb(BASE + PA); // read from CH0 PA
pb_d = inportb(BASE + PB); // read from CH0 PB
pc_d = inportb(BASE + PC); // read from CH0 PC
```

4. To clear and enable interrupt

```
# define INDEX 0x2C0     //INDEX same as SW
                         //setting
# define DATAS 0x301     //data R/W port
# define CW1 0x3         //8255 port 0 CW index
int dummy;               //dummy data buffer
outportb(INDEX,CW1);     //index to CW
dummy = inportb(DATA);   //dummy read to clear
                         //and enable interrupt
```

5. A Complete Example Program for Interrupt Handling

```
/*************************************************/
 *  This program deno. how to generate interrupt by *
 *  the ACL-7122 itself. When you press any key, a  *
 *  beep is generated. When you press ESC key, the  *
 *  system will be quit.                            *
 *                                                  *
 *  Hardware setting :                              *
 *     Base Address : 0x2C0                         *
 *     IRQ Level    : 9   ( Jumper J6)              *
 *     Int mode     : EN  ( jumper J0)              *
 *     edge trigger : 1-2 ( rising edge)            *
 *************************************************/

#include <stdio.h>
#include <dos.h>
#include <conio.h>
```

```
#define  IRQ2       0x0a
#define  EOI        0x20
#define  BASE_ADDR  0x2c0
#define  PA         0x00
#define  PB         0x01
#define  PC         0x02
#define  CW         0x03


void interrupt isr_7122()
{
    printf("\7");            // beep
    outportb( 0x20, EOI);    // EOI of 8259
}

main()
{
    int  mask, keyin;
    void interrupt (*old_irq2_isr)();

    old_irq2_isr = getvect( IRQ2);
    setvect( IRQ2, isr_7122);
    mask = inportb( 0x21);

    outportb( BASE_ADDR + CW, 0x80);  // set PA, PB and PC
                                      // as output mode
    clrscr();                         // clear screen
    printf( " press <ESC> to QUIT \n");
    do
    {
       keyin = 0;
       printf(" press any key to genetate an interrupt
                except <ESC>\n");
       keyin = bioskey(0);

       outportb( 0x21, 0xbf & mask); // IRQ2 nonmasked

       outportb( BASE_ADDR + PC, 0x00);
       delay( 100);
       outportb( BASE_ADDR + PC, 0x08);

    } while( (keyin & 0xff) != 27); // QUIT when ESC pressed

    setvect( IRQ2, old_irq2_isr);   // restore old isr
    outportb( 0x21, mask);          // restore 8259 mask}
```

Appendix A. I/O Port Address Map

I/O Address	Device
000-01F	DMA controller 1
020-03F	interrupt controller
040-05F	Timer
060-06F	Keyboard
070-07F	Real-time clock
080-09F	DMA page register
0A0-0BF	Interrupt controller 2
0C0-0DF	DMA controller
0F0-0FF	Math coprocessor
100-1EF	not usable
1F0-1F8	Fixed disk
200-207	Game I/O
278-27F	Parallel printer port 2 (LPT2:)
2F8-2FF	Serial Port 2 (COM2:)
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1 (LPT1:)
3B0-3BF	Monochrome display
3C0-3CF	Reserved
3D0-3DF	Color graphics display
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1:)

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