EVBUM2269/D

KAI-1003 Imager Board User's Manual

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EVAL BOARD USER'S MANUAL

KAI−1003 Imager Evaluation Board Description

The KAI−1003 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two−board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI−1003 Image Sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J3). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAI−1003 Imager Board has been designed to operate the KAI−1003 with the specified performance at 20 MHz pixel clocking rate and nominal operating conditions. (See the KAI−1003 performance specification for details).

For testing and calibration purposes, the KAI−1003 Imager board provides the ability to adjust the CCD substrate bias voltages and Reset Low CCD clock level voltage by adjusting potentiometers on the board.

IMAGER BOARD INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5.0	5.1	V
−5 V_MTR Supply	−5.1	−5.0	−4.9	V
VPLUS Supply	18	20	21	V
VMINUS Supply	−21	−20	−18	V

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Comments
H1A (±)	0	±0.1	2.4	V	H1A clock
H1B (±)	0	±0.1	2.4	V	H1B clock
H2 (±)	0	±0.1	2.4	V	H2A clock
R (±)	0	±0.1	2.4	V	Reset clock
V1 (±)	0	±0.1	2.4	V	V1 clock
V2 (±)	0	±0.1	2.4	V	V2 clock
FDG	0	±0.1	2.4	V	Fast Dump clock
V3RD (±)	0	±0.1	2.4	V	V1 Clock 3rd level
VES (±)	0	±0.1	2.4	V	Electronic Shutter

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KAI−1003 IMAGER BOARD ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KAI−1003 Imager board (Refer to Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the J3 interface connector. The power supplies are de−coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and −15 V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J3 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The low and high levels of the reset CCD clock are set by potentiometers.

Please note that the silkscreen text has been removed near H1A, H2A, and H2B, as it was incorrect. The silkscreen for the Test Points is correct and may be used to probe the pixel rate clocks as shown in Table 3.

Table 3. PIXEL RATE CLOCK TEST POINT LOCATIONS

Testpoint	Pixel Rate Clock
TP8	H2A_CCD
TP10	H1B_CCD
TP12	H2B_CCD
TP13	H1A_CCD

Reset Clock One−Shot (U9; not populated)

The pulse width of the RESET_CCD clock used to be set by a programmable One−Shot. It was configured to provide a pulse width from 5 ns to 15 ns. Now, the pulse width control functionality is provided by the KSC−1000 based Timing Generator Board, and the one−shot has been bypassed by removing U9 and inserting a shorting resistor on pads 1 and 2 of U9.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The current sources for these voltage levels are high current (up to 600 mA) transistors. The V2_CCD high level clock voltage is switched from V_MID to V_HIGH once per frame to transfer the charge from the photodiodes to the vertical CCDs.

CCD FDG Driver

The KAI−1003 does not use a Fast Dump Gate (FDG) circuit. The FDG signal is located on the interface connector but is not connected beyond the TTL buffer IC.

VES Circuit

The quiescent CCD substrate voltage (VSUB) is set by a potentiometer. For electronic shutter operation, the VES signal drives a transistor amplifier circuit that AC−couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

CCD Bias Voltages

All CCD bias voltages are fixed on the KAI−1003 Imager Board except VSUB, which can be set by a potentiometer.

CCD Image Sensor

This evaluation board supports the KAI−1003 Image Sensor.

Emitter−Follower

The VOUT_CCD signals are buffered using bipolar junction transistors in an emitter−follower configuration that also provides the necessary 5 mA current sink for the CCD output circuits.

Line Drivers

The buffered VOUT_CCD signals are AC−coupled and driven from the Imager Board by operational amplifiers in a non−inverting configuration. The operational amplifiers are configured to have a gain of 1.25, to correctly drive 75 Ω video coaxial cabling from the SMB connectors.

KAI−1003 OPERATIONAL SETTINGS

The Imager board is configured to operate the KAI−1003 CCD image sensor under the following operating conditions:

Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 were correct at the time of this document¿s publication, but may be subject to change; refer to the KAI−1003 device specification.

Table 4. BIAS VOLTAGES

Description	Symbol	Min	Nom	Max	Units	Potentiometer
Output Amplifier Supply	VDD	12.0	15.0	15.0	V	
Output Amplifier Return	VSS		0		V	
Output Gate	VOG	1.8	2.0	2.2	V	
Reset Drain	VRD	10.0	10.5	11.0	V	
Ground, P−Well	GND		0		V	
Substrate	VSUB	8.0	Vsub	18.0	V	R56
Disable ESD Protection	VMIN		−8.5		V	
Output Amplifier Load Gate	VLG	1.4	1.5	1.6	V	

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 5 were correct at the time of this document's publication, but may be subject to change; refer to the KAI−1003 device specification.

Table 5. CLOCK VOLTAGES

Description	Symbol	Level	Min	Nom	Max	Units	Potentiometer
Horizontal CCD Clocks	Hxx_CCD	Low	−6.5	−6.0	−5.5	V	
		High	4.5	5.0	5.5	V	
Vertical CCD Clock V1	V1_CCD	Low	−9.0	−8.5	−8.0	V	
		High	−0.8	−0.5	0.0	V	
Vertical CCD Clock V2	V2_CCD	Low	−9.0	−8.5	−8.0	V	
		Mid	−0.8	−0.5	0.0	V	
		High	9.5	10.5	11.5	V	
Reset Clock	RESET_CCD	Low	0	TBS	5.0	V	R28
		Amplitude		5.0		V	R64
Electronic Shutter Pulse	VES_CCD		37	40	45	V	

BLOCK DIAGRAM AND PERFORMANCE DATA

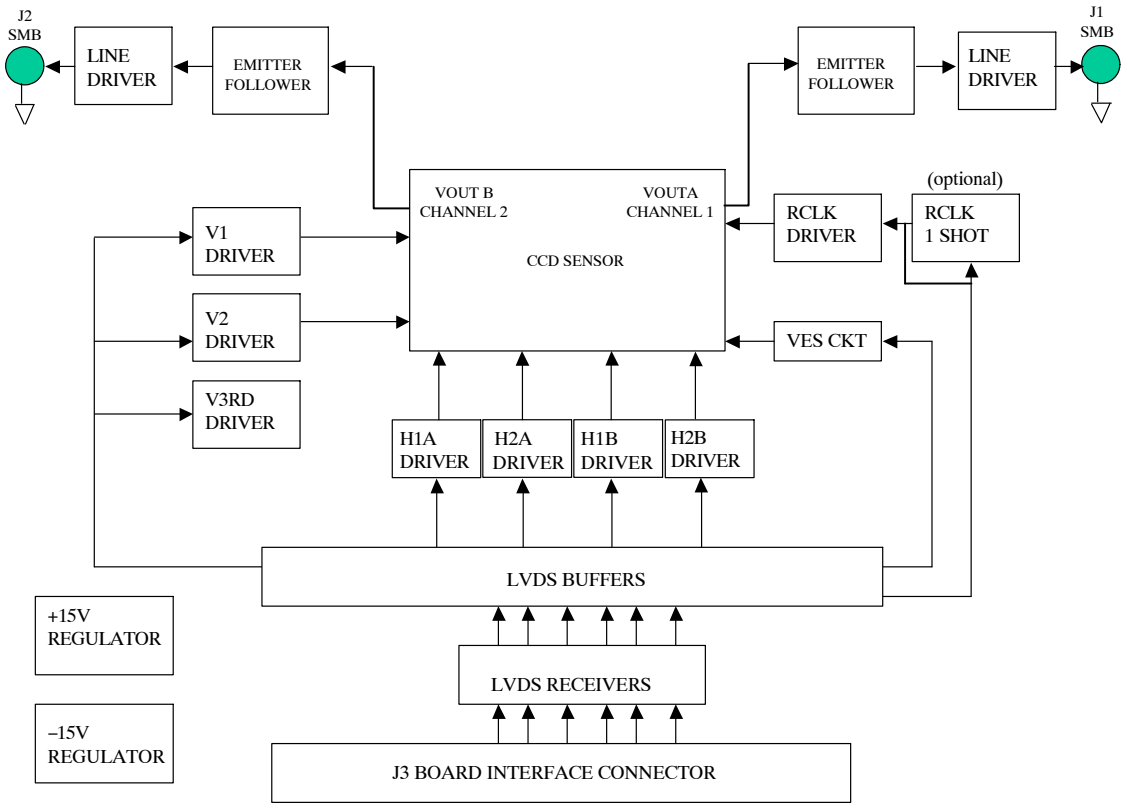


Figure 1. KAI−1003 Imager Board Block Diagram

LINEARITY

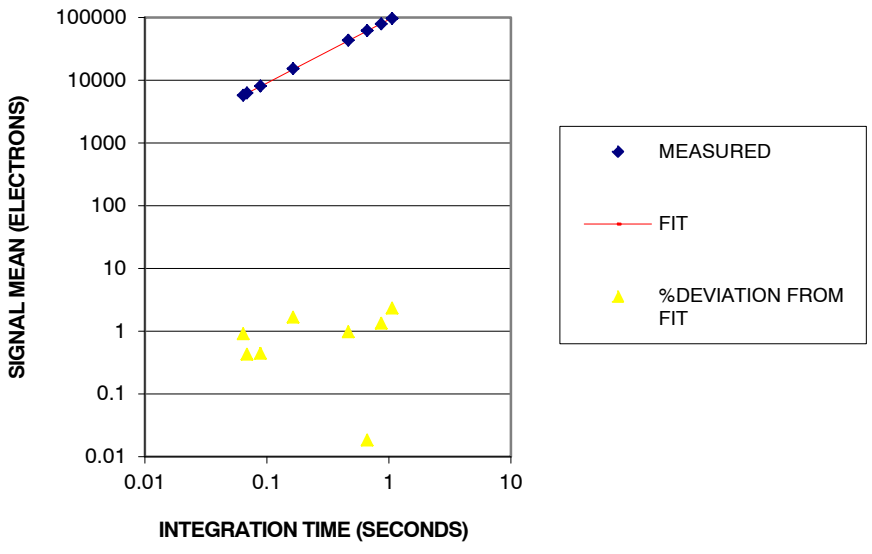


Figure 2. Measured Performance − Linearity

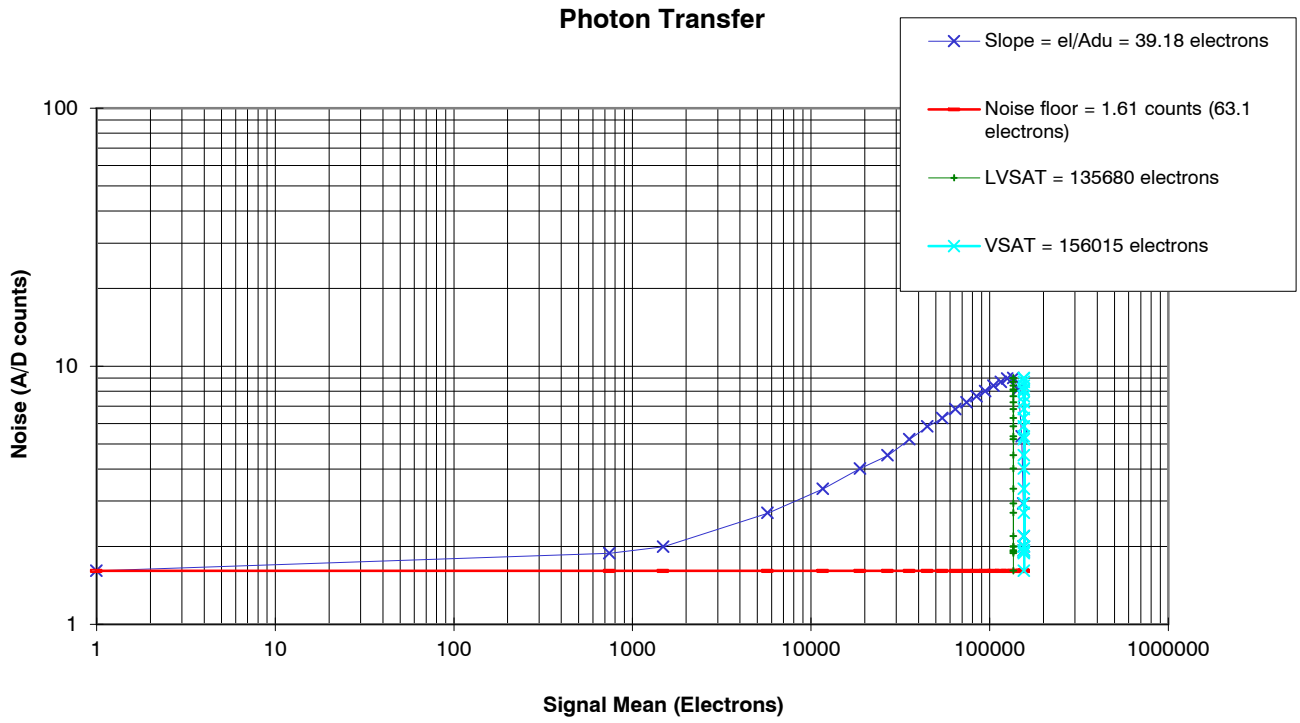


Figure 3. Measured Performance – Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J1 and J2

The emitter−follower buffered CCD_VOUT signals are driven from the Imager Board via the SMB connectors J1 and J2. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 6. J4 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES−
7	AGND	8	AGND
9	FDG+	10	FDG−
11	AGND	12	AGND
13	V3RD+	14	V3RD−
15	AGND	16	AGND
17	V2B+	18	V2B−
19	AGND	20	AGND
21	V2+	22	V2−
23	AGND	24	AGND
25	V1+	26	V1−
27	AGND	28	AGND
29	R+	30	R−
31	AGND	32	AGND
33	H2B+	34	H2B−
35	AGND	36	AGND
37	H2A+	38	H2A−
39	AGND	40	AGND
41	H1B+	42	H1B−
43	AGND	44	AGND
45	H1A+	46	H1A−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	−5 V_MTR	62	−5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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