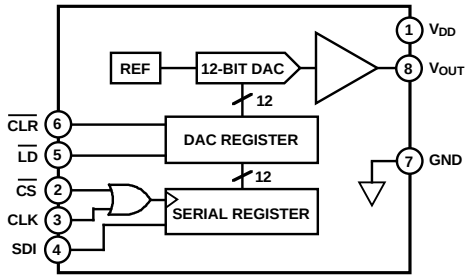
+5 V, Serial Input Complete 12-Bit DAC

DAC8512

FEATURES
Space Saving SO-8 or Mini-DIP Packages
Complete, Voltage Output with Internal Reference
1 mV/Bit with 4.095 V Full Scale
Single +5 Volt Operation
No External Components
3-Wire Serial Data Interface, 20 MHz Data Loading Rate
Low Power: 2.5 mW

APPLICATIONS
Portable Instrumentation
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

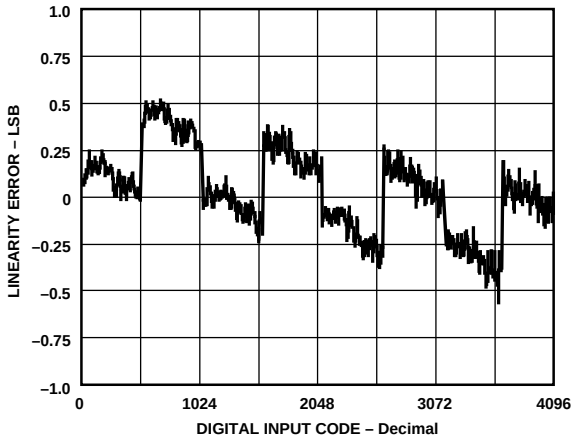
The DAC8512 is a complete serial input, 12-bit, voltage output digital-to-analog converter designed to operate from a single +5 V supply. It contains the DAC, input shift register and latches, reference and a rail-to-rail output amplifier. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease of use in +5 V only systems.

Coding for the DAC8512 is natural binary with the MSB loaded first. The output op amp can swing to either rail and is set to a range of 0 V to +4.095 V—for a one-millivolt-per-bit resolution. It is capable of sinking and sourcing 5 mA. An on-chip reference is laser trimmed to provide an accurate full-scale output voltage of 4.095 V.

Serial interface is high speed, three-wire, DSP compatible with data in (SDI), clock (CLK) and load strobe (LD). There is also a chip-select pin for connecting multiple DACs.

A CLR input sets the output to zero scale at power on or upon user demand.

The DAC8512 is specified over the extended industrial (–40°C to +85°C) temperature range. DAC8512s are available in plastic DIPs and SO-8 surface mount packages.



Linearity Error vs. Digital Input Code

REV. A

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Documentation

Data Sheet

- DAC8512: 5V, Serial Input Complete 12-Bit DAC Data Sheet

Reference Materials

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Design Resources

- DAC8512 Material Declaration
- PCN-PDN Information
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DAC8512–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Units
STATIC PERFORMANCE							
Resolution	N	Note 2		12			Bits
Relative Accuracy	INL		E Grade	–1	±1/4	+1	LSB
			F Grade	–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	No Missing Codes		–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H			+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H[3]	E Grade	4.087	4.095	4.103	V
			F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4			16		ppm/°C
ANALOG OUTPUT							
Output Current	I_{OUT}	Data = 800_H		±5	±7		mA
Load Regulation at Full Scale	L_{REG}	R_L = 402 Ω to ∞, Data = 800_H			1	3	LSB
Capacitive Load	C_L	No Oscillation[4]			500		pF
LOGIC INPUTS							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}			2.4			V
Input Leakage Current	I_{IL}					10	µA
Input Capacitance	C_{IL}					10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]							
Clock Width High	t_{CH}			30	10		ns
Clock Width Low	t_{CL}			30	10		ns
Load Pulse Width	t_{LDW}			20			ns
Data Setup	t_{DS}			15	10		ns
Data Hold	t_{DH}			15	5		ns
Clear Pulse Width	t_{CLRW}			30	20		ns
Load Setup	t_{LD1}			15			ns
Load Hold	t_{LD2}			10			ns
Select	t_{CSS}			30			ns
Deselect	t_{CSH}			20			ns
AC CHARACTERISTICS[4]							
Voltage Output Settling Time	t_S	To ±1 LSB of Final Value[5]			16		µs
DAC Glitch					15		nV s
Digital Feedthrough					15		nV s
SUPPLY CHARACTERISTICS							
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.002	0.004	%/%

NOTES

[1]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 V to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = +5.0 V ± 5%, T_A = +25°C, applies to part number DAC8512GBC only, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL		–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±0.7	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H	4.085	4.095	4.105	V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	μA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL}= 0.8 V, No Load		1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, No Load		0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load		7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, No Load		2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V, +10 V
Logic Inputs to GND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUT} to GND ..... –0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Pin Plastic DIP Package (P) ..... 103°C/W
8-Lead SOIC Package (S) ..... 158°C/W
Maximum Junction Temperature (T_J max) ..... +150°C
Operating Temperature Range .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability .

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8512 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Description	Package Option
DAC8512EP	±1	–40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FP	±2	–40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FS	±2	–40°C to +85°C	8-Lead SOIC	SO-8
DAC8512GBC	±2	+25°C	Dice	

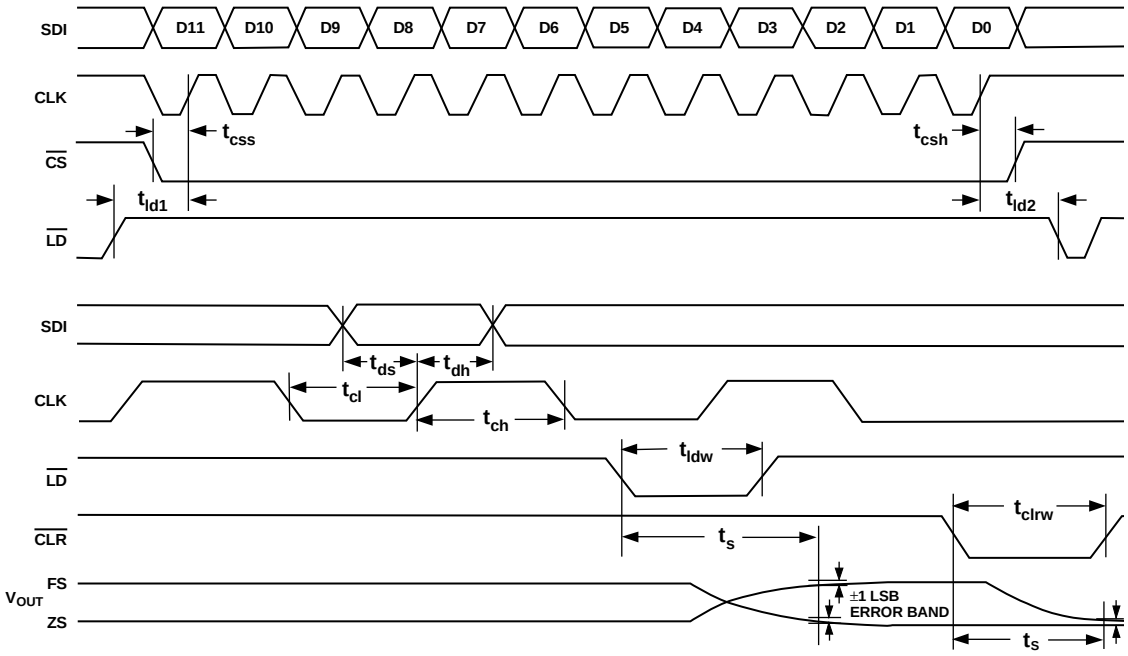


Figure 1. Timing Diagram

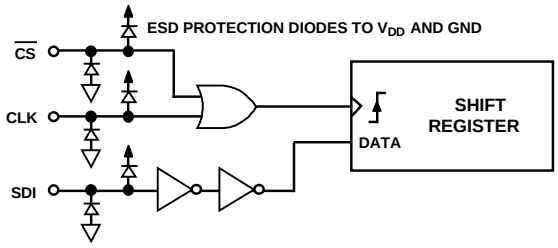


Figure 2. Equivalent Clock Input Logic

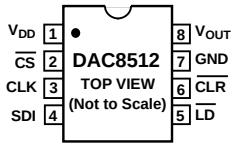
Table I. Control-Logic Truth Table

$\overline{CS}$[2]	CLK[2]	$\overline{CLR}$	$\overline{LD}$	Serial Shift Register Function	DAC Register Function
H	X	H	H	No Effect	Latched
L	L	H	H	No Effect	Latched
L	H	H	H	No Effect	Latched
L	↑+	H	H	Shift-Register-Data Advanced One Bit	Latched
↑+	L	H	H	Shift-Register-Data Advanced One Bit	Latched
H	X	H	↓–	No Effect	Updated with Current Shift Register Contents
H	X	H	L	No Effect	Transparent
H	X	L	X	No Effect	Loaded with All Zeros
H	X	↑+	H	No Effect	Latched All Zeros

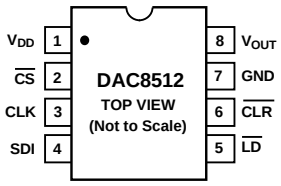
NOTES
[1]↑+ positive logic transition; ↓– negative logic transition; X = Don't Care.
[2]$\overline{CS}$ and CLK are interchangeable.
[3]Returning $\overline{CS}$ HIGH avoids an additional "false clock" of serial data input.
[4]Do not clock in serial data while $\overline{LD}$ is LOW.

PIN CONFIGURATIONS

SO-8



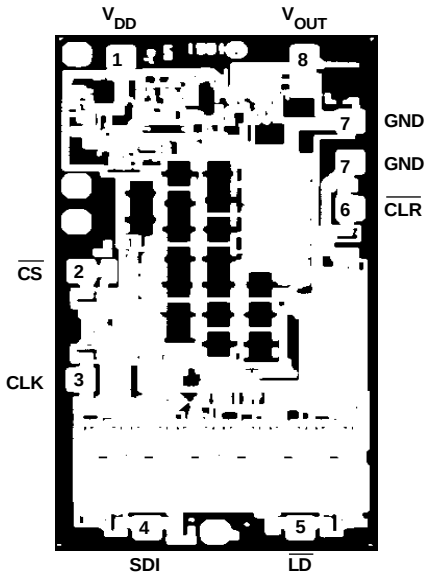
P-DIP-8 & Cerdip-8



PIN DESCRIPTIONS

Pin	Name	Description
1	V_{DD}	Positive Supply. Nominal value +5 V, ± 5%.
2	$\overline{CS}$	Chip Select. Active low input.
3	CLK	Clock input for the internal serial input shift register.
4	SDI	Serial Data Input. Data on this pin is clocked into the internal serial register on positive clock edges of the CLK pin. The Most Significant Bit (MSB) is loaded first.
5	$\overline{LD}$	Active low input which writes the serial register data into the DAC register. Asynchronous input.
6	$\overline{CLR}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale. Asynchronous input.
7	GND	Analog ground for the DAC. This also serves as the digital logic ground reference voltage.
8	V_{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD}.

NUMBER OF TRANSISTORS: 642
DIE SIZE: 0.055 inch × 0.106 inch; 5830 sq mils

OPERATION

The DAC8512 is a complete ready to use 12-bit digital-to-analog converter. It contains a voltage-switched, 12-bit, laser-trimmed DAC, a curvature-corrected bandgap reference, a rail-to-rail output op amp, a DAC register, and a serial data input register. The serial data interface consists of a CLK, serial data in (SDI), and a load strobe ($\overline{LD}$). This basic 3-wire interface offers maximum flexibility for interface to the widest variety of serial data input loading requirements. In addition a $\overline{CS}$ select is provided for multiple packaging loading and a power on reset $\overline{CLR}$ pin to simplify start or periodic resets.

D/A CONVERTER SECTION

The DAC is a 12-bit voltage mode device with an output that swings from GND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The DAC's output is buffered by a low power consumption precision amplifier. This amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

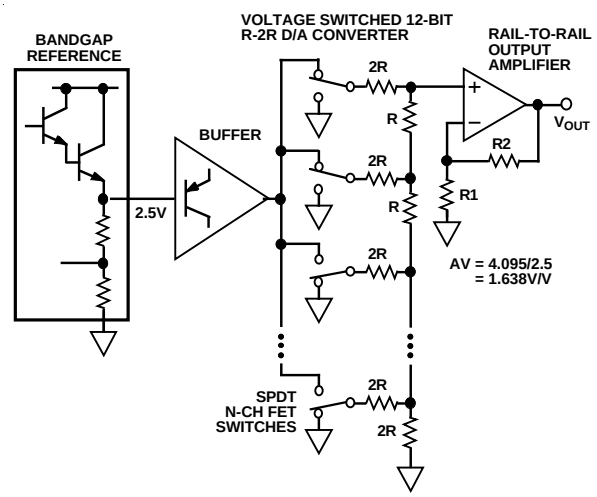


Figure 3. Equivalent DAC8512 Schematic of Analog Portion

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slowing signals vs. positive. See the oscilloscope photos in the typical performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply.

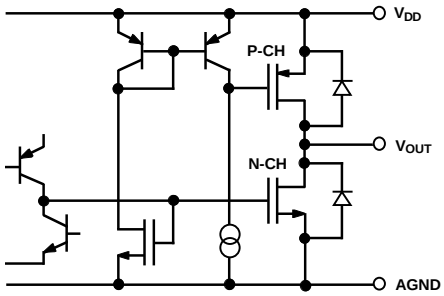


Figure 4. Equivalent Analog Output Circuit

Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull up device that can supply GND terminated loads, especially at the low supply tolerance values of 4.75 volts. Figures 5 and 6 provide information on output swing performance near ground and full-scale as a function of load. In addition to resistive load driving capability the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

POWER SUPPLY

The very low power consumption of the DAC8512 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power consumption sensitive applications it is important to note that the internal power consumption of the DAC8512 is strongly dependent on the actual logic input voltage levels present on the SDI, $\overline{CS}$, $\overline{LD}$, and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC8512 supply current as a function of the actual value of input logic voltage. Consequently use of CMOS logic vs. TTL minimizes power dissipation in the static state. A V_{IL} = 0 V on the SDI, $\overline{CS}$ and CLR pins provides the lowest standby power dissipation of 2.5 mW (500 μA × 5 V).

As with any analog system, it is recommended that the DAC8512 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC8512 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC8512 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The DAC8512 has a separate serial input register from the 12-bit DAC register that allows preloading of a new data value into the serial register without disturbing the present DAC output voltage. After the new value is fully loaded in the serial input register it can be asynchronously transferred to the DAC register by strobing the $\overline{LD}$ pin. The DAC register uses a level sensitive $\overline{LD}$ strobe that should be returned high before any new data is loaded into the serial input register. At any time the contents of the DAC register can be reset to zero by strobing the $\overline{CLR}$ pin which causes the DAC output voltage to go to zero volts. All of the timing requirements are detailed in Figure 1 along with the Table I Control-Logic Truth Table.

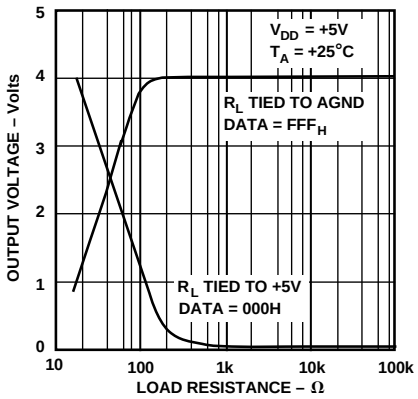


Figure 5. Output Swing vs. Load

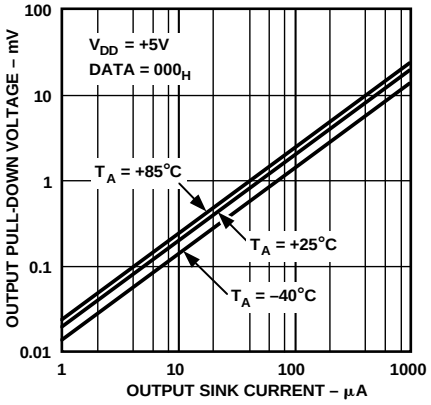


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

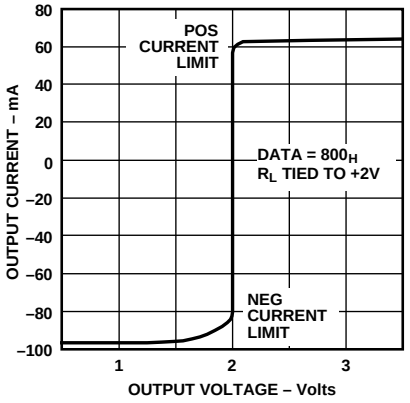


Figure 7. Short Circuit Current

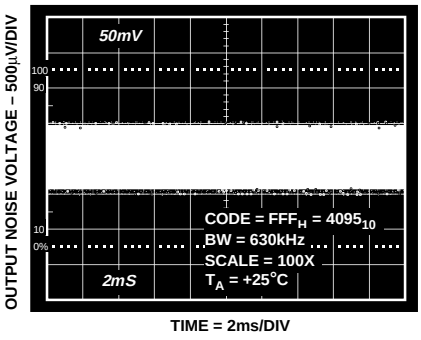


Figure 8. Broadband Noise

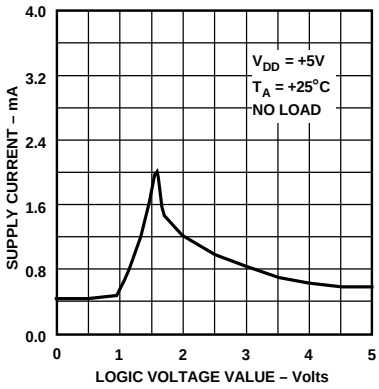


Figure 9. Supply Current vs. Logic Input Voltage

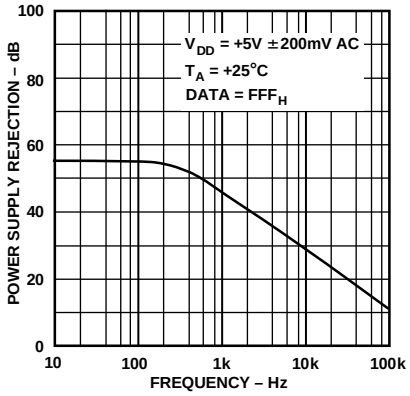


Figure 10. Power Supply Rejection vs. Frequency

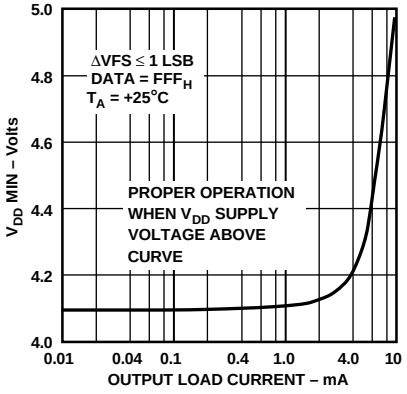


Figure 11. Minimum Supply Voltage vs. Load

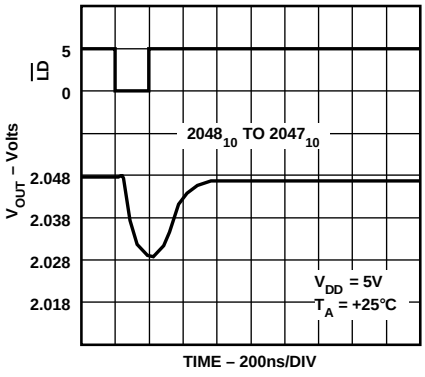


Figure 12. Midscale DAC Glitch Performance

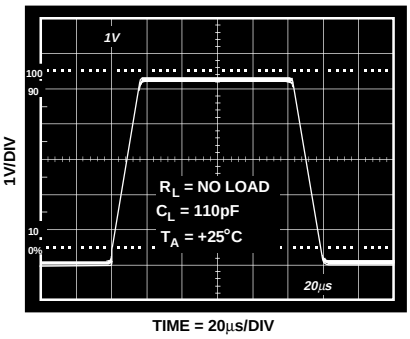


Figure 13. Large Signal Settling Time

DAC8512 — Typical Performance Characteristics

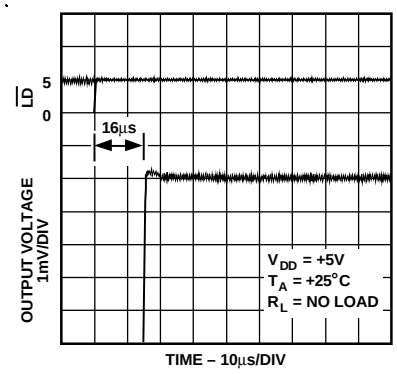


Figure 14. Rise Time Detail

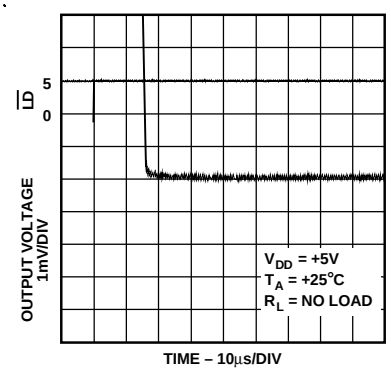


Figure 15. Fall Time Detail

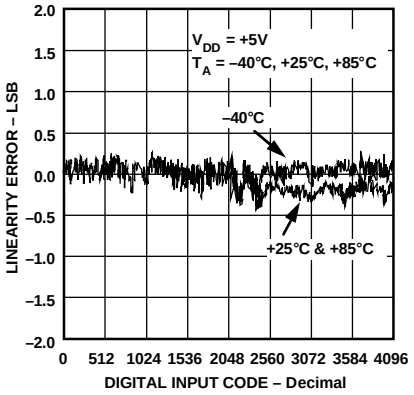


Figure 16. Linearity Error vs. Digital Code

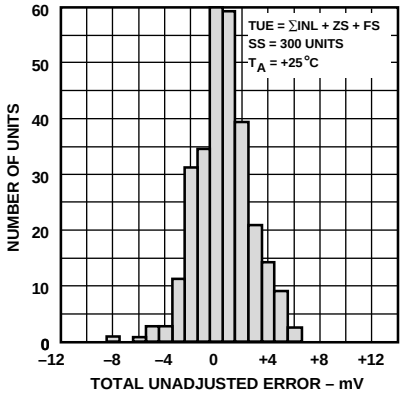


Figure 17. Total Unadjusted Error Histogram

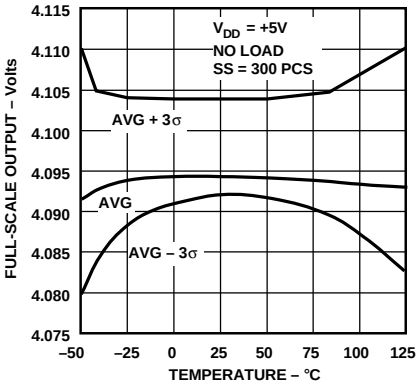


Figure 18. Full-Scale Voltage vs. Temperature

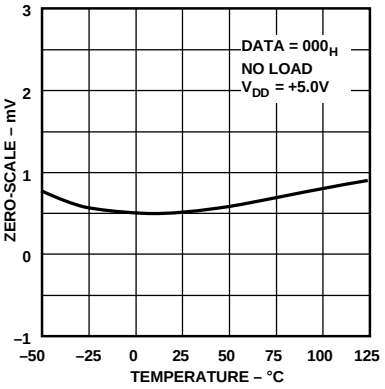


Figure 19. Zero-Scale Voltage vs. Temperature

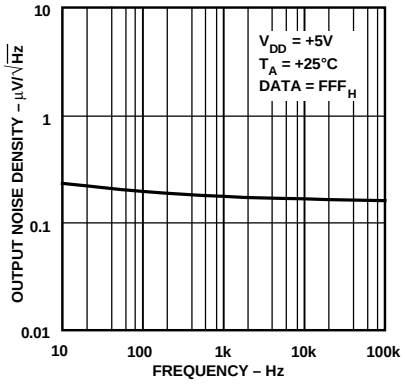


Figure 20. Output Voltage Noise vs. Frequency

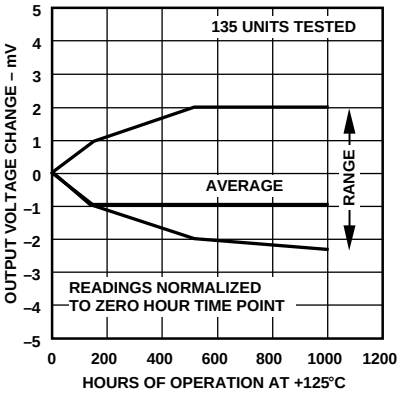


Figure 21. Long Term Drift Accelerated by Burn-In

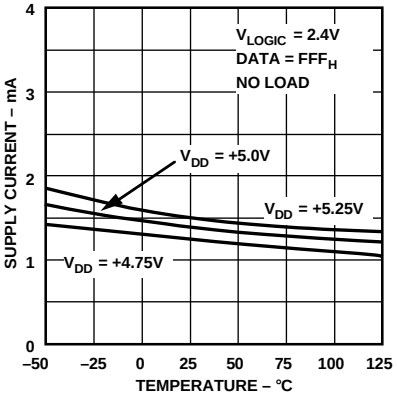


Figure 22. Supply Current vs. Temperature

APPLICATIONS SECTION

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the DAC8512 has been designed for +5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to assure that its inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC8512.

The power supply used for the DAC8512 should be well filtered and regulated. The device has been completely characterized for a +5 V supply with a tolerance of ±5%. Since a +5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Because it is convenient, a designer might be inclined to tap a logic circuit's supply for the DAC's supply. Unfortunately, this is not wise because fast logic with nanosecond transition edges induce high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise will corrupt the analog circuits internal to the DAC and cause errors. Even though their spike noise is lower in amplitude, directly tapping the output of a +5 V system supply can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, the DAC and any associated analog circuitry should be powered directly from the system power supply outputs using appropriate filtering. Figure 23 illustrates how a clean, analog-grade supply can be generated from a +5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be low ESR (Equivalent Series Resistance) type.

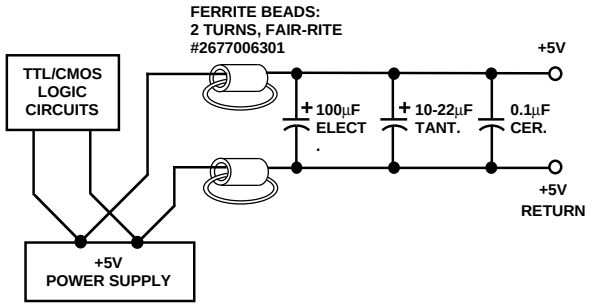


Figure 23. Properly Filtering a +5 V Logic Supply Can Yield a High Quality Analog Supply

In order to fit the DAC8512 in an 8-pin package, it was necessary to use only one ground connection to the device. The ground connection of the DAC serves as the return path for supply currents as well as the reference point for the digital input thresholds. The ground connection also serves as the supply rail for the internal voltage reference and the output amplifier. Therefore, to minimize any errors, it is recommended that the ground connection of the DAC8512 be connected to a high quality analog ground, such as the one described above. Generous bypassing of the DAC's supply goes a long way in reducing supply line-induced errors. Local supply bypassing consisting of a 10 μF tantalum electrolytic in parallel with a 0.1 μF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pin (Pin 1) and the analog ground (Pin 7). Figure 24 shows how the ground and bypass connections should be made to the DAC8512.

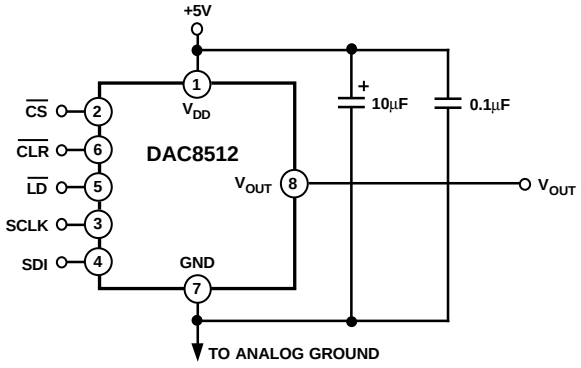


Figure 24. Recommended Grounding and Bypassing Scheme for the DAC8512

Unipolar Output Operation

This is the basic mode of operation for the DAC8512. As shown in Figure 24, the DAC8512 has been designed to drive loads as low as 2 kΩ in parallel with 500 pF. The code table for this operation is shown in Table II.

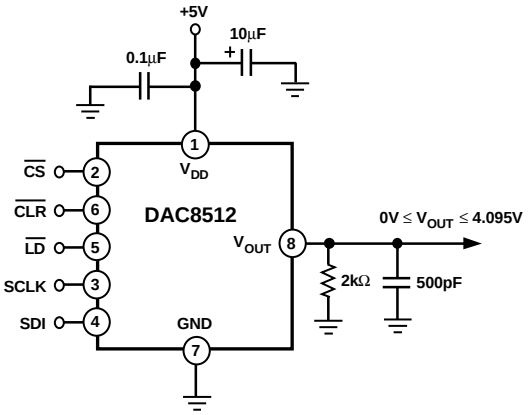


Figure 25. Unipolar Output Operation

Table II. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Operating the DAC8512 on +12 V or +15 V Supplies Only
Although the DAC8512 has been specified to operate on a single, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC8512 consumes no more than 2.5 mA, maximum, then an integrated voltage reference, such as the REF02, can be used as the DAC8512 +5 V supply. The configuration of the circuit is shown in Figure 26. Notice that the reference's output voltage requires no trimming because of the REF02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC8512 is 2.5 mA, local bypassing of the REF02's output with at least 0.1 μF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

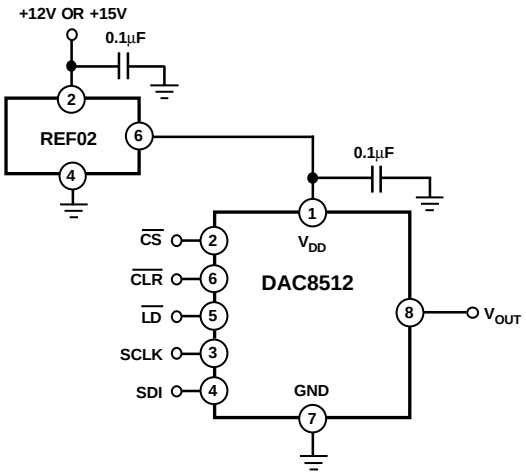


Figure 26. Operating the DAC8512 on +12 V or +15 V Supplies Using a REF02 Voltage Reference

Measuring Offset Error
One of the most commonly specified endpoint errors associated with real world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single-supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC8512, for example, the zero-scale error is specified to be ±3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error.

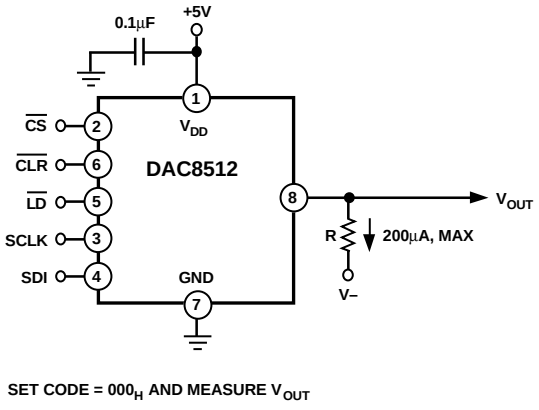


Figure 27. Measuring Zero-Scale or Offset Error

By adding a pull-down resistor from the output of the DAC8412 to a negative supply as shown in Figure 27, offset errors can now be read at zero code. This configuration forces the output p-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 μA, maximum.

Bipolar Output Operation
Although the DAC8512 has been designed for single-supply operation, bipolar operation is achievable using the circuit illustrated in Figure 28. The circuit uses a single-supply, rail-to-rail OP295 op amp and the REF03 to generate the –2.5 V reference required to level-shift the DAC output voltage. Note that the –2.5 V reference was generated without the use of precision resistors. The circuit has been configured to provide an output voltage in the range $-5\ V \le V_{OUT} \le +5\ V$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table III provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\ mV \times Digital\ Code \times \frac{R4}{R1} + 2.5 \times \frac{R4}{R2}$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\ mV \times Digital\ Code + 5\ V$$

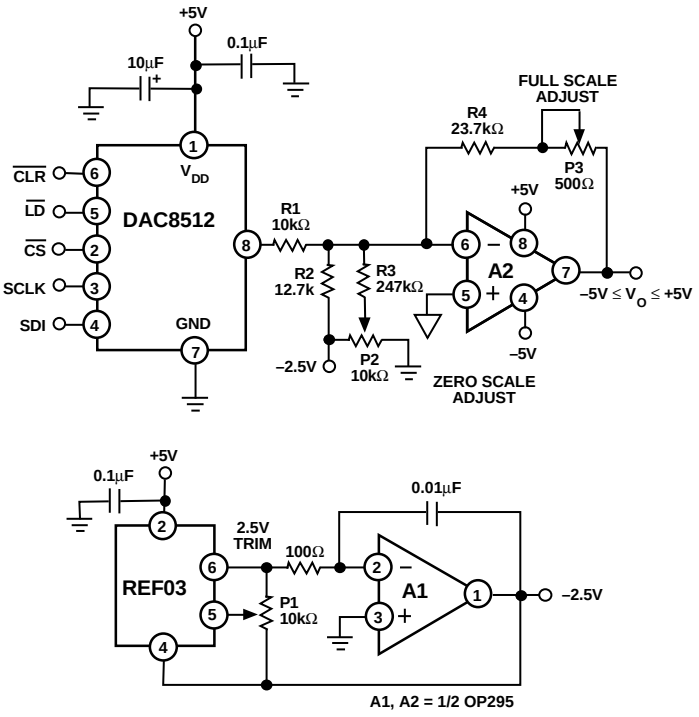


Figure 28. Bipolar Output Operation

Table III. Bipolar Code Table

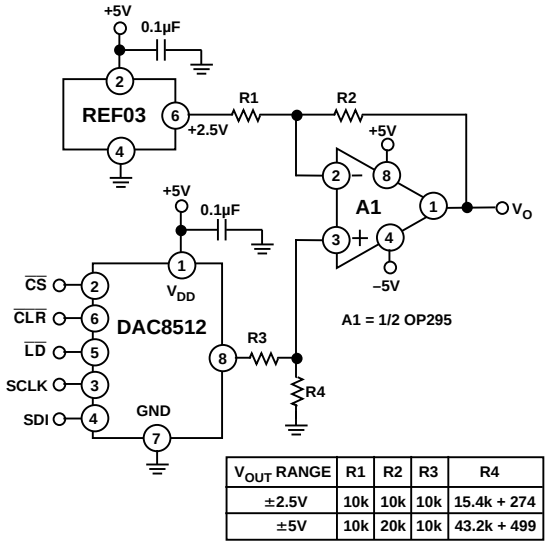
Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	–4.9976
801	2049	–2.44E–3
800	2048	0
7FF	2047	+2.44E–3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, and R4 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 29 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim. The output voltage is coded in offset binary and is given by:

$$V_O = 1\ mV \times Digital\ Code \times \left(\frac{R4}{R3+R4}\right) \times \left(1+\frac{R2}{R1}\right)$$

$$-2.5 \times \frac{R2}{R1}$$



V_{OUT} RANGE	R1	R2	R3	R4
±2.5V	10k	10k	10k	15.4k + 274
±5V	10k	20k	10k	43.2k + 499

Figure 29. Bipolar Output Operation without Trim

For the ±2.5 V output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\ mV \times Digital\ Code - 2.5\ V$$

Similarly, for the ±5 V output range, the transfer equation becomes:

$$V_O = 2.44\ mV \times Digital\ Code - 5\ V$$

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, +12 V, +15 V, and/or +5 V are only available. Shown in Figure 30 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of –5 V for current loadings in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a +12 V supply.

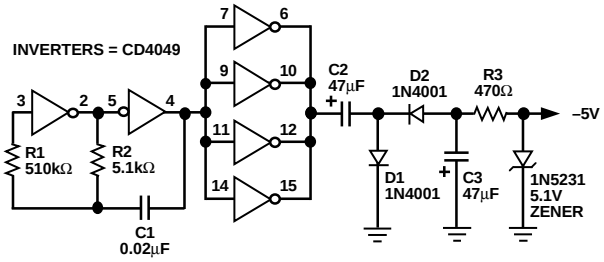


Figure 30. Generating a –5 V Supply When Only +12 V or +15 V Is Available

A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 31 shows the DAC8512 controlling a high-compliance precision current source using an AMP05 instrumentation amplifier. The AMP05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS}. Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{OUT} = \frac{V_{IN}}{R_{CS}}$$

If R_{CS} equals 100 Ω, the output current is limited to +10 mA with a 1 V input. Therefore, each DAC LSB corresponds to 2.4 µA. If a bipolar output current is required, then the circuit in Figure 28 can be modified to drive the AMP05's reference pin with a ±1 V input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V. Fine gain adjustment can be accomplished by adjusting R1 or R2.

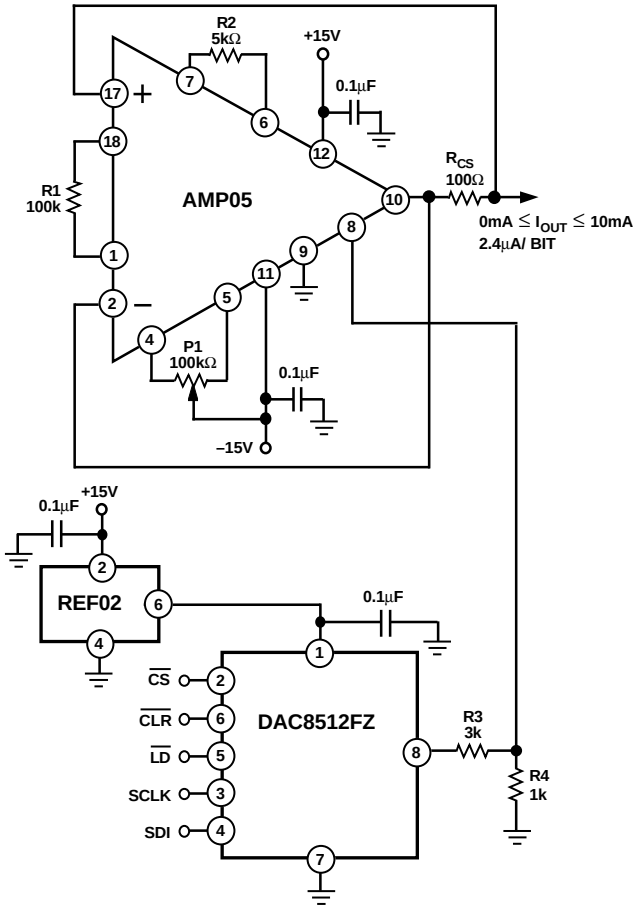


Figure 31. A High-Compliance, Digitally Controlled Precision Current Source

A Single-Supply, Programmable Current Source

The circuit in Figure 32 shows how the DAC8512 can be used with an OP295 single-supply, rail-to-rail output op amp to provide a digitally programmable current sink from V_{SOURCE} that consumes less than 3.8 mA, maximum. The DAC's output voltage is applied across R1 by placing the 2N2222 transistor in the OP295's feedback loop. For the circuit values shown, the full-scale output current is 1 mA which is given by the following equation:

$$I_{OUT} = \frac{DW \times 4.095V}{R1}$$

where DW = DAC8512's binary digital input code.

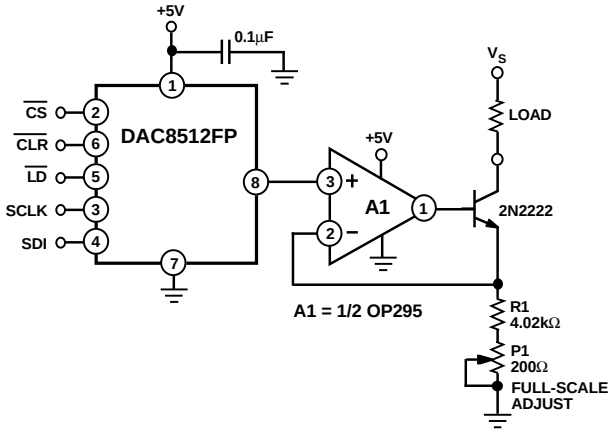


Figure 32. A Single-Supply, Programmable Current Source

The usable output voltage range of the current sink is +5 V to +60 V. The low limit of the range is controlled by transistor saturation, and the high limit is controlled by the collector-base breakdown voltage of the 2N2222.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC8512s is shown in Figure 33. The required upper and lower limits for the test are loaded into each DAC individually by controlling HDAC/$\overline{\text{LDAC}}$. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

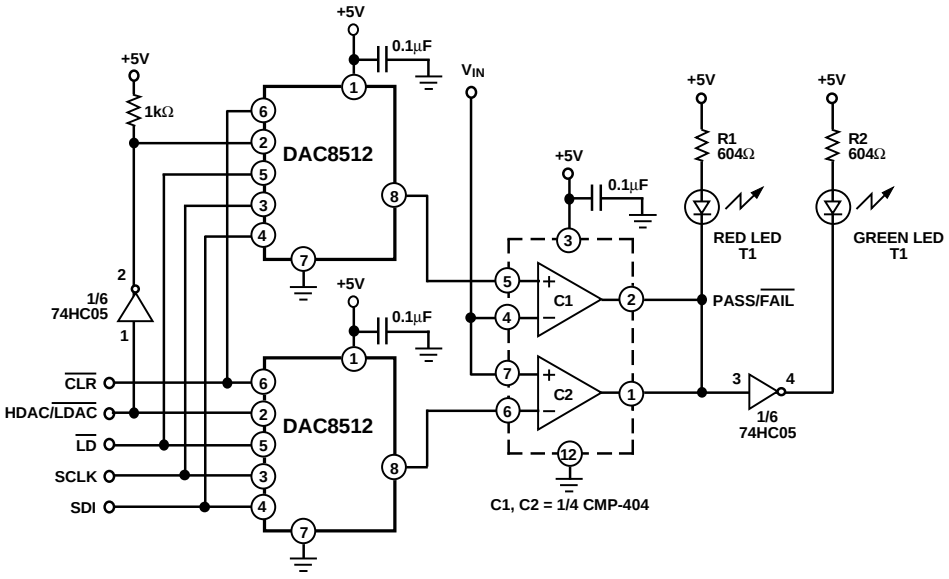


Figure 33. A Digitally Programmable Window Detector

Opto-Isolated Interfaces for Process Control Environments

In many process control type applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide isolation in excess of 3 kV. The serial loading structure of the DAC8512 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum.

Illustrated in Figure 34 is an opto-isolated interface using the DAC8512. In this circuit, the $\overline{CS}$ line is always LOW to enable the DAC, and the 10 kΩ/1 µF combination connected to the DAC's $\overline{CLR}$ pin sets a turn-on time constant of 10 ms to reset the DAC upon application of power. Three opto-couplers are then used for the SDI, SCLK, and $\overline{LD}$ lines.

Often times reducing the number of interface lines to two lines is required in many control environments. The circuit illustrated in Figure 35 shows how to convert a two-line interface into the three control lines required to control the DAC8512 without using one shots. This technique uses a counter to keep track of the clock cycles and, when all the data has been input to the DAC, the external logic generates the $\overline{LD}$ pulse.

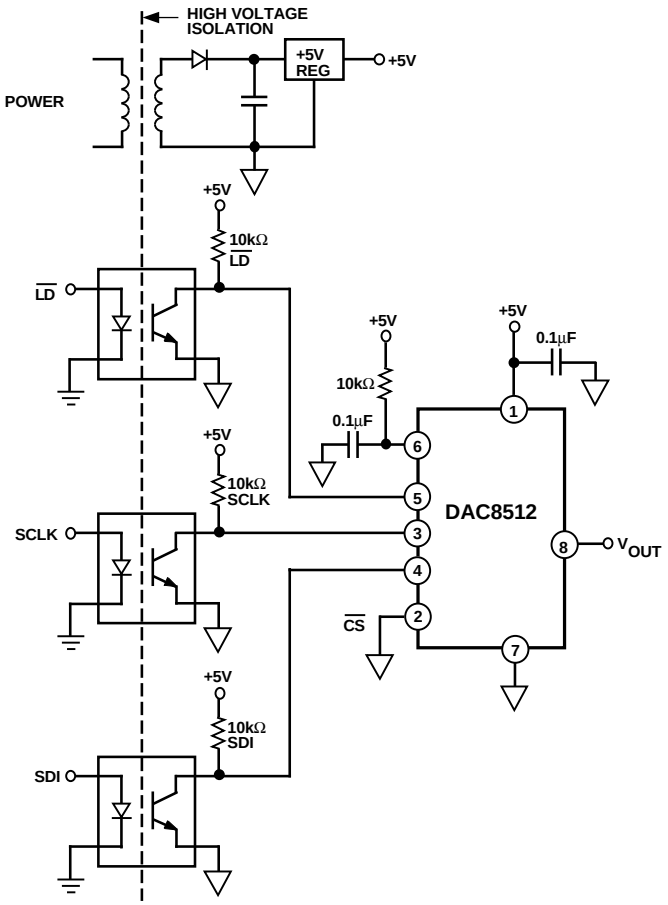


Figure 34. An Opto-Isolated DAC Interface

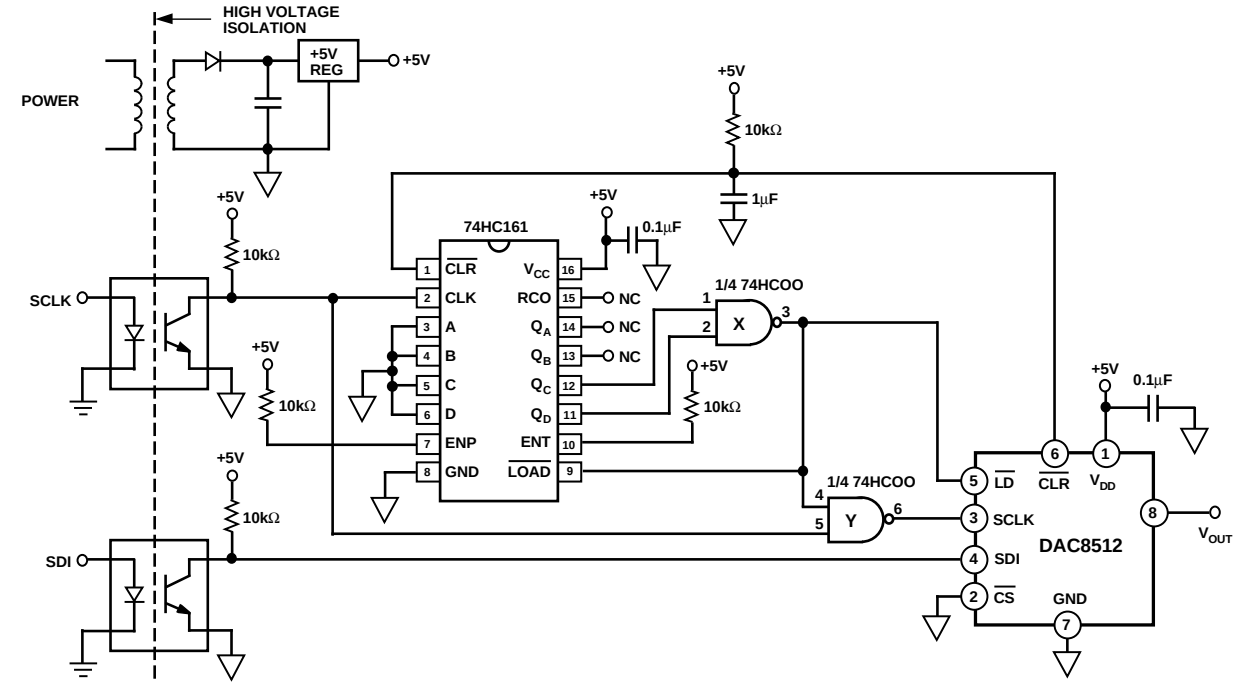


Figure 35. A Two-Wire, Opto-Isolated DAC Interface

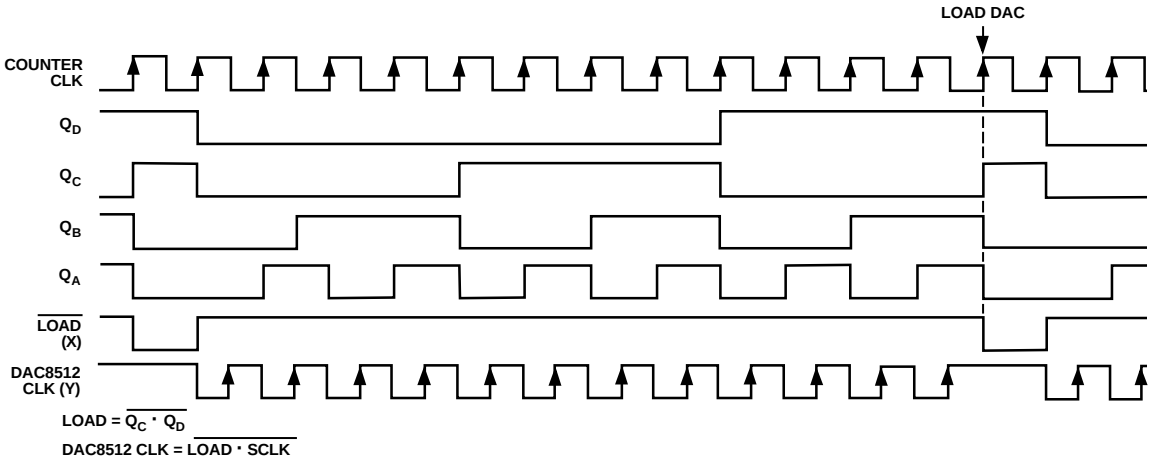


Figure 36. Opto-Isolated Two-Wire Serial Interface Timing Diagram

The timing diagram of Figure 36 can be used to understand the operation of the circuit. Only two opto-couplers are used in the circuit; one for SCLK and one for SDI. The 74HC161 counter in incremented on every rising edge of the clock. Additionally, the data is loaded into the DAC8512 on the falling edge of the clock by inverting the serial clock using gate "Y." The timing diagram shows that after the twelfth bit has been clocked the output of the counter is binary 1011. On the very next rising clock edge, the output of the counter changes to binary 1100 upon which the output of gate "X" goes LOW to generate the $\overline{\text{LD}}$ pulse. The $\overline{\text{LD}}$ signal is connected to both the DAC's $\overline{\text{LD}}$ and the counter's LOAD pins to prevent the thirteenth rising clock edge from advancing the DAC's internal shift register. This prevents false loading of data into the DAC8512. Inverting the DAC's serial clock allows sufficient time from the CLK edge to the $\overline{\text{LD}}$ edge, and from the $\overline{\text{LD}}$ edge to the next clock pulse all of which satisfies the timing requirements for loading the DAC8512.

After loading one address of the DAC, the entire process can repeated to load another address. If the loading is complete, then the clock must stop after the thirteenth pulse of the final load. The DAC's clock input will be pulled high and the counter reset to zero. As was shown in Figure 35, both the 74HC161's and the DAC8512's $\overline{\text{CLR}}$ pins are connected to a simple R-C timing circuit that resets both ICs when the power in turned on. The circuit's time constant should be set longer than the power supply turn-on time and, in this circuit, is set to 10 ms, which should be adequate for most systems. This same two-wire interface can be used for other three-wire serial input DACs.

Decoding Multiple DAC8512s

The $\overline{\text{CS}}$ function of the DAC8512 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DAC's $\overline{\text{CS}}$ input is asserted to transfer its serial input register contents into the destination DAC register. In this circuit, shown in Figure 37, the $\overline{\text{CS}}$ timing is generated by a 74HC139 decoder and should follow the DAC8512's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its ENABLE input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' $\overline{\text{CLR}}$ pins resets all DAC outputs to zero during power-up.

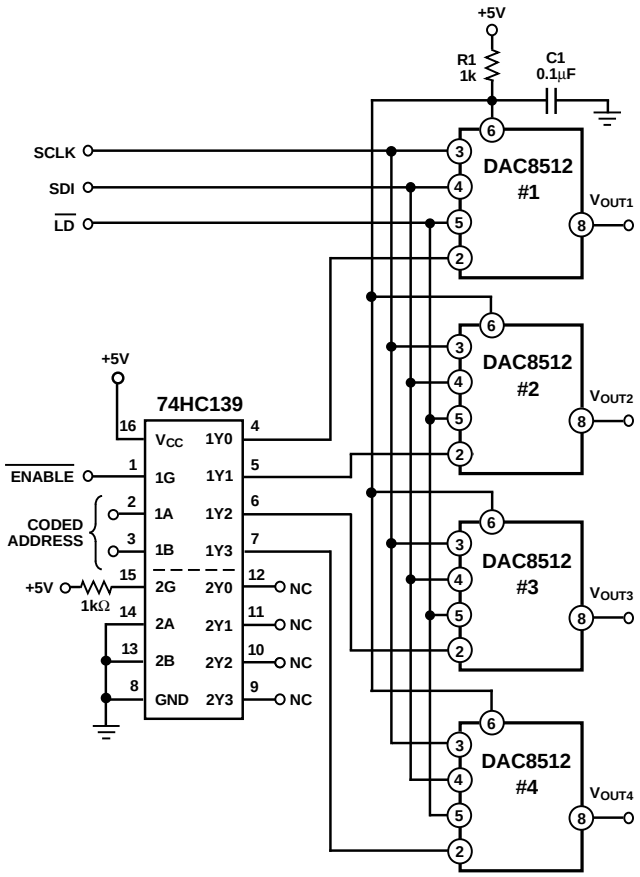


Figure 37. Decoding Multiple DAC8512s Using the $\overline{CS}$ Pin

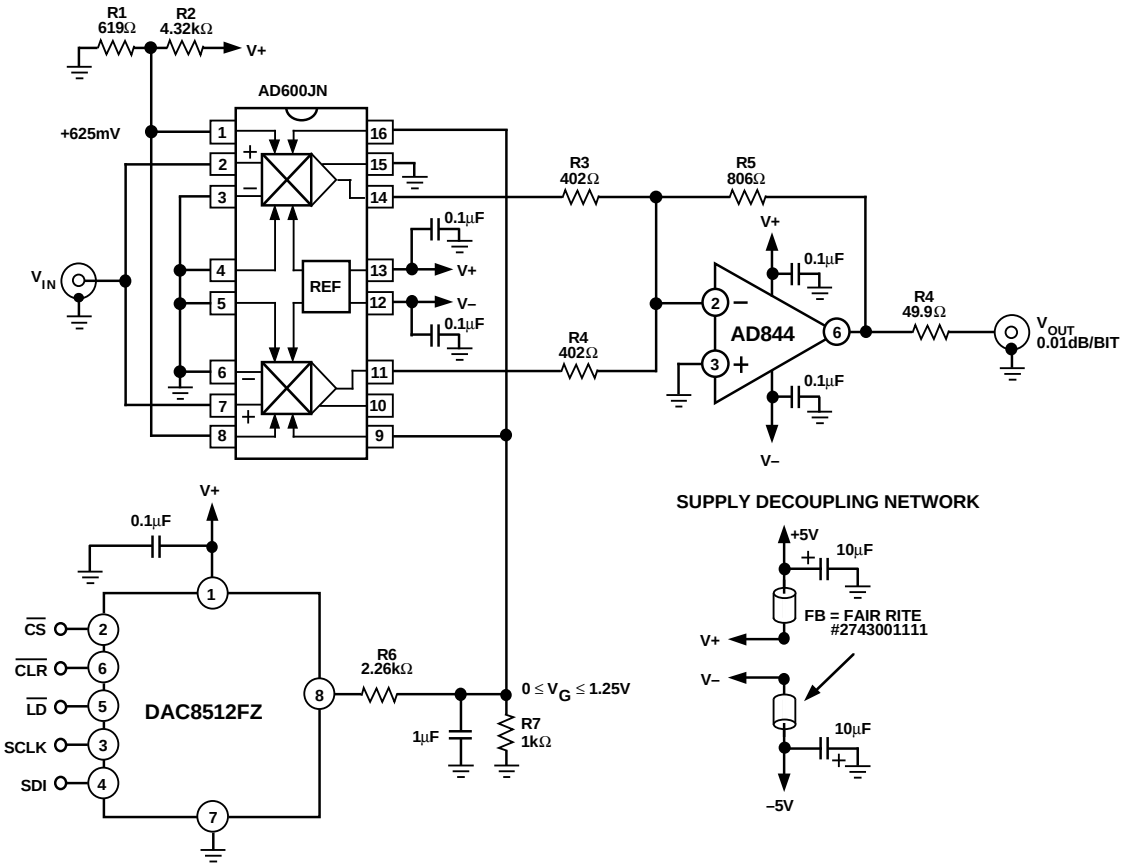


Figure 38. A Digitally Controlled, Ultralow Noise VCA

A Digitally Controlled, Ultralow Noise VCA

The circuit in Figure 38 illustrates how the DAC8512 can be used to control an ultralow noise VCA, using the AD600/AD602. The AD600/AD602 is a dual, low noise, wideband, variable gain amplifier based on the X-AMP topology.* Both channels of the AD600 are wired in parallel to achieve a wideband VCA which exhibits an RTI (Referred To Input) noise voltage spectral density of approximately 1 nV/$\sqrt{\text{Hz}}$. The output of the VCA requires an AD844 configured in a gain of 4 to account for signal loss due to input and output 50 Ω terminations. As configured, the total gain in the circuit is 40 dB.

Since the output of the DAC8512 is single quadrant, it was necessary to offset the AD600's gain control voltage so that the gain of the circuit is 0 dB for zero scale and 40 dB at full scale. This was achieved by setting C1LO and C2LO to +625 mV using R1 and R2. Next, the output of the DAC8512 was scaled so that the gain of the AD600 equaled 20 dB when the digital input code equaled 800_H. The frequency response of the VCA as a function of digital code is shown in Figure 39.

*For more details regarding the AD600 or AD602, please consult the AD600/AD602 data sheet.

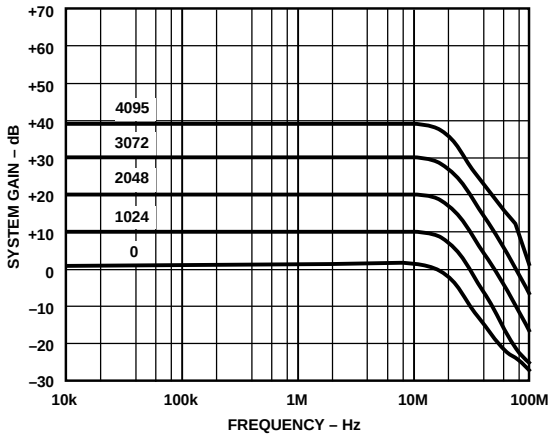


Figure 39. VCA Frequency Response vs. Digital Code

A Serial DAC, Audio Volume Control

The DAC8512 is well suited to control digitally the gain or attenuation of a voltage controlled amplifier. In professional audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 40 illustrates a volume control application using the DAC8512 to control the attenuation of the SSM2018.

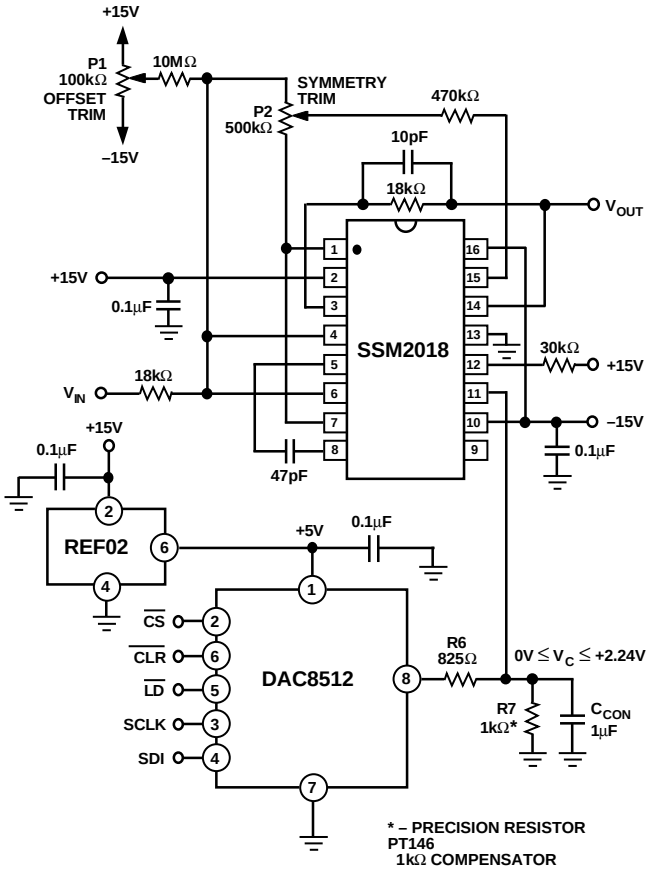


Figure 40. A Serial DAC, Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC8512. The SSM2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC8512. Since the SSM2018 exhibits a gain constant of –28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table IV illustrates the attenuation vs. digital code of the volume control circuit.

Table IV. SSM-2018 VCA Attenuation vs. DAC8512 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM2018's gain constant temperature coefficient of –3300 ppm/°C, a 1 kΩ, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of +3500 ppm/°C is used. A C_{CON} of 1 μF provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM2018 data sheet.

Information regarding the PT146 1 kΩ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, Fl 34647
(813) 541-5771

An Isolated, Programmable, 4-20 mA Process Controller

In many process control system, applications, two-wire current transmitters are used to transmit analog signals through noisy environments. These current transmitters use a "zero-scale" signal current of 4 mA that can be used to power the transmitter's signal conditioning circuitry. The "full-scale" output signal in these transmitters is 20 mA. The converse approach to process control can also be used; a low-power, programmable current source can be used to control remotely located sensors or devices in the loop.

A circuit that performs this function is illustrated in Figure 41. Using the DAC8512 as the controller, the circuit provides a programmable output current of 4 mA to 20 mA, proportional to the DAC's digital code. Biasing for the controller is provided by the REF02 and requires no external trim for two reasons:

(1) the REF02's tight initial output voltage tolerance and (2) the low supply current consumption of both the OP90 and the DAC8512. The entire circuit, including opto-couplers, consumes less than 3 mA from the total budget of 4 mA. The OP90 regulates the output current to satisfy the current summation at the noninverting node of the OP-90. The KCL equation at Pin 3 is given by:

$$I_{OUT} = \frac{1}{R7} \times \left(\frac{1\ mV \times Digital\ Code \times R3}{R1} + \frac{V_{REF} \times R3}{R2} \right)$$

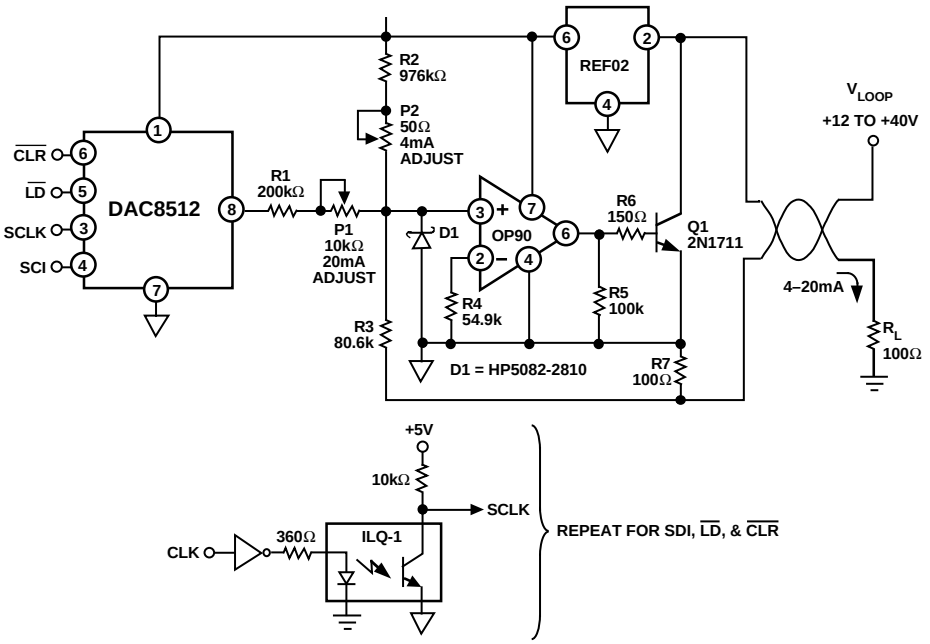


Figure 41. An Isolated, Programmable, 4-20 mA Process Controller

For the values shown in Figure 41,

$$I_{OUT} = 3.9\ \mu A \times Digital\ Code + 4\ mA$$

giving a full-scale output current of 20 mA when the DAC8512's digital code equals FFF_H. Offset trim at 4 mA is provided by P2, and P1 provides the circuit's gain trim at 20 mA. These two trims do not interact because the noninverting input of the OP90 is at virtual ground. The Schottky diode, D1, is required in this circuit to prevent loop supply power-on transients from pulling the noninverting input of the OP90 more than 300 mV below its inverting input. Without this diode, such transients could cause phase reversal of the OP90 and possible latchup of the controller. The loop supply voltage compliance of the circuit is limited by the maximum applied input voltage to the REF02 and is from +12 V to +40 V.

MICROPROCESSOR INTERFACING

DAC8512–MC68HC11 Interface

The circuit illustrated in Figure 42 shows a serial interface between the DAC8512 and the MC68HC11 8-bit microcontroller. SCK of the 68HC11 drives SCLK of the DAC8512, while the MOSI output drives the serial data line, SDI, of the DAC8512. The DAC's $\overline{CLR}$, $\overline{LD}$, and $\overline{CS}$ signals are derived from port lines PC1, PD5, and PC0, respectively, as shown.

For correct operation of the serial interface, the 68HC11 should be configured such that its CPOL bit is set to 1 and its CPHA bit is also set to 1. When the serial data is to be transmitted to the DAC, PC0 is taken low, asserting the DAC's $\overline{CS}$ input. When the 68HC11 is configured in this manner, serial data on

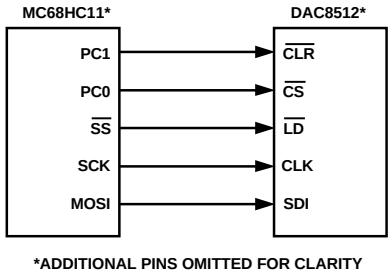


Figure 42. DAC8512–MC68HC11 Interface

MOSI is valid on the rising edge of SCLK. The 68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight rising clock edges occurring in the transmit cycle. To load data to the DAC8512's input serial register, PC0 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the DAC8512. During the second byte load, the first four most significant bits of the first byte are pushed out of the DAC's input shift register. At the end of the second byte load, PC0 is then taken high. To prevent an accidental advancing of the internal shift register, SCLK must already be asserted before PC0 is taken high. To transfer the contents of the input shift register to the DAC register, PD5 is taken low, asserting the DAC's $\overline{LD}$ input. The DAC's $\overline{CLR}$ input, controlled by the 68HC11's PC1 port, provides an asynchronous clear function, setting the DAC output to zero. Included in this section is the source code for operating the DAC8512—M68HC11 interface.

DAC8512–M68HC11 Interface Program Source Code

```
*
PORTC       EQU         $1003       Port C control register
*                                   "0,0,0,0;0,0,CLR/,CS/"
DDRC        EQU         $1007       Port C data direction
PORTD       EQU         $1008       Port D data register
*                                   "0,0,LD/,SCLK;SDI,0,0,0
DDRD        EQU         $1009       Port D data direction
SPCR        EQU         $1028       SPI control register
*                                   "SPIE,SPE,DWOM,MSTR;CPOL,CPHA,SPRl,SPR0"
SPSR        EQU         $1029       SPI status register
*                                   "SPIF,WCOL,0,MODF;0,0,0,0"
SPDR        EQU         $102A       SPI data register; Read-Buffer; Write-Shifter
*

* SDI RAM variables:                SDI1 is encoded from 0 (Hex) to F (Hex)
*                                   SDI2 is encoded from 00 (Hex) to FF (Hex)
*                                   DAC requires two 8-bit loads; upper 4 bits of SDI1
*                                   are ignored.
*
SDI1        EQU         $00         SDI packed byte 1 "0,0,0,0;MSB,DB10,DB9,DB8"
SDI2        EQU         $01         SDI packed byte 2 "DB7,DB6,DB5,DB4;DB3,DB2,DB1,DB0"
*
            ORG         $C000       Start of user's RAM in EVB
INIT        LDS         #$CFFF      Top of C page RAM
*
            LDAA        #$03        0,0,0,0;0,0,1,1
*                                   CLR/-Hi, CS/-Hi
            STAA        PORTC       Initialize Port C Outputs
            LDAA        #$03        0,0,0,0;0,0,1,1
            STAA        DDRC        CLR/ and CS/ are now enabled as outputs
*
            LDAA        #$30        0,0,1,1;0,0,0,0
*                                   LDI-Hi,SCLK-Hi,SDI-Lo
            STAA        PORTD       Initialize Port D Outputs
            LDAA        #$38        0,0,1,1;1,0,0,0
            STAA        DDRD        LD/,SCLK, and SDI are now enabled as outputs
*
            LDAA        #$5F
            STAA        SPCR        SPI is Master,CPHA=1,CPOL=1,Clk rate=E/32
*
            BSR         UPDATE      Xfer 2 8-bit words to DAC8512
            JMP         $E000       Restart BUFFALO
*
UPDATE      PSHX                    Save registers X, Y, and A
            PSHY
            PSHA
*
            LDAA        #$0A        0,0,0,0;1,0,1,0
            STAA        SDI1        SDI1 is set to 0A (Hex)
*
            LDAA        #$AA        1,0,1,0;1,0,1,0
            STAA        SDI2        SDI2 is set to AA (Hex)
*
            LDX         #SDI1       Stack pointer at 1st byte to send via SDI
            LDY         #$1000      Stack pointer at on-chip registers
*
            BCLR        PORTC,Y     $02 Assert CLR/
            BSET        PORTC,Y     $02 De-assert CLR/
*
            BCLR        PORTC,Y     $01 Assert CS/
*
```

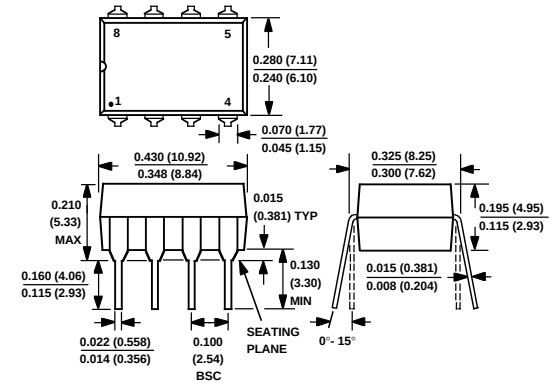
```
TFRLP   LDAA    0,X     Get a byte to transfer via SPI
        STAA    SPDR    Write SDI data reg to start xfer
*
WAIT    LDAA    SPSR    Loop to wait for SPIF
        BPL     WAIT    SPIF is the MSB of SPSR
*                       (when SPIF is set, SPSR is negated)
        INX             Increment counter to next byte for xfer
        CPX     #SDI2+1 Are we done yet ?
        BNE     TFRLP   If not, xfer the second byte
*
*Update DAC output with contents of DAC register
*
        BCLR    PORTD,Y $20 Assert LD/
        BSET    PORTD,Y $20 Latch DAC register
*
        BSET    PORTC,Y $01 De-assert CS/

        PULA When done, restore registers X, Y & A
        PULY
        PULX
        RTS             ** Return to Main Program **
```

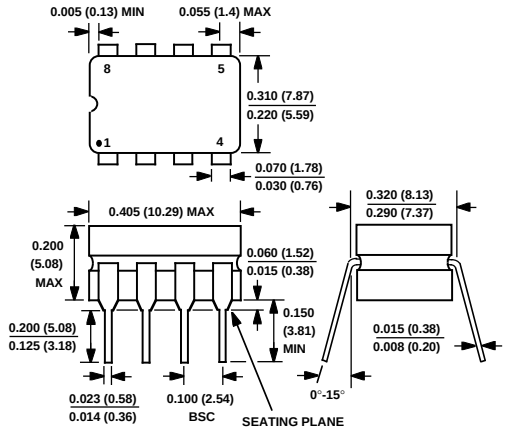
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

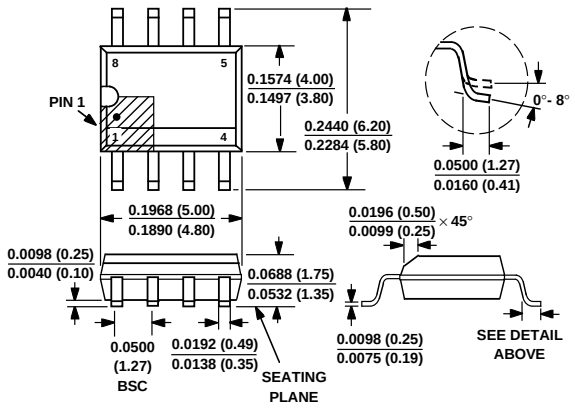
8-Pin Plastic DIP (P Suffix)



8-Pin Cerdip (Z Suffix)



8-Lead SOIC (S Suffix)



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