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MAX98090AETL+ MAX98090AETL+T MAX98090BETL+

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MAX98090

Ultra-Low Power Stereo Audio Codec

General Description

The MAX98090 is a fully integrated audio codec whose high-performance, ultra-low power consumption and small footprint make it ideal for portable applications.

The device features a highly flexible input scheme with six input pins (WLP) that can be configured as analog or digital microphone inputs, differential or single-ended line inputs, or as full-scale direct differential inputs. Analog inputs can be routed to the record path ADC or directly to any analog output mixer.

The device accepts master clock frequencies of either 256 x f_S or from 10MHz to 60MHz. The digital audio interface supports master or slave mode operation, sample rates from 8kHz to 96kHz, and standard PCM formats such as I²S, left/right-justified, and TDM.

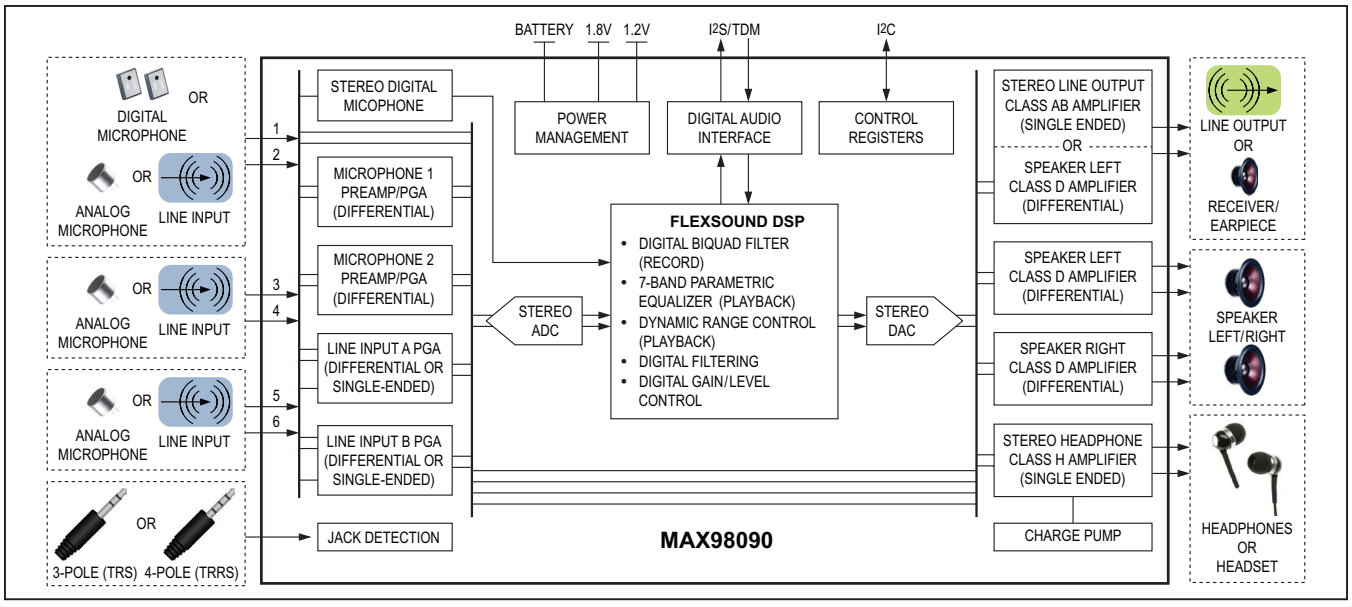
The record/playback paths feature FlexSound® technology DSP. This includes digital gain and filtering, a biquad filter (record), dynamic range control (playback), and a seven band parametric equalizer (playback) that can improve loudspeaker performance by optimizing the frequency response.

The stereo Class D speaker amplifier provides efficient amplification, features low radiated emissions, supports filterless operation, and can drive both 4Ω and 8Ω loads. The DirectDrive® stereo Class H headphone amplifier provides a ground referenced output eliminating the need for large DC-blocking capacitors. The device also includes a differential receiver (earpiece) amplifier that can be reconfigured as a stereo single-ended line output.

Features and Benefits

- 102dB DR Stereo DAC to HP (8kHz < f_S < 96kHz)
- 3.6mW Stereo Playback Power Consumption
- 99dB DR Stereo ADC (8kHz < f_S < 96kHz)
- 4.2mW Stereo Record Power Consumption
- 3 Stereo Single-Ended/Differential Analog Microphone/Line Inputs (WLP Version)
- Stereo PDM Digital Microphone Input
- Master Clock Frequencies from 256 x f_S to 60MHz
- I²S/LJ/RJ/TDM Digital Audio Interface
- FlexSound Technology Signal Processing
  - Record Path Biquad Filter
  - Playback Path 7-Band Parametric EQ
  - Playback Path Automatic Level Control
  - Digital Filtering and Gain/Level Control
- Stereo Low EMI Class D Speaker Amplifiers
  - 3.2W/Channel (R_L = 4Ω, V_{SPK_VDD} = 5V, WLP)
  - 1.8W/Channel (R_L = 8Ω, V_{SPK_VDD} = 5V, WLP)
- Stereo DirectDrive Class H Headphone Amplifier Jack Detection and Identification
- Differential Receiver Amplifier/Stereo Line Output
- Extensive Click-and-Pop Reduction Circuitry
- RF Immune Analog Inputs and Outputs
- Programmable Microphone Bias
- I²C Control Interface with Two Address Options
- 49-Bump 0.4mm WLP and 40-Pin TQFN Packages

Simplified Block Diagram



For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX98090.related.

***Ordering Information* appears at end of data sheet.**

19-6492; Rev 2; 8/13

maxim integrated™

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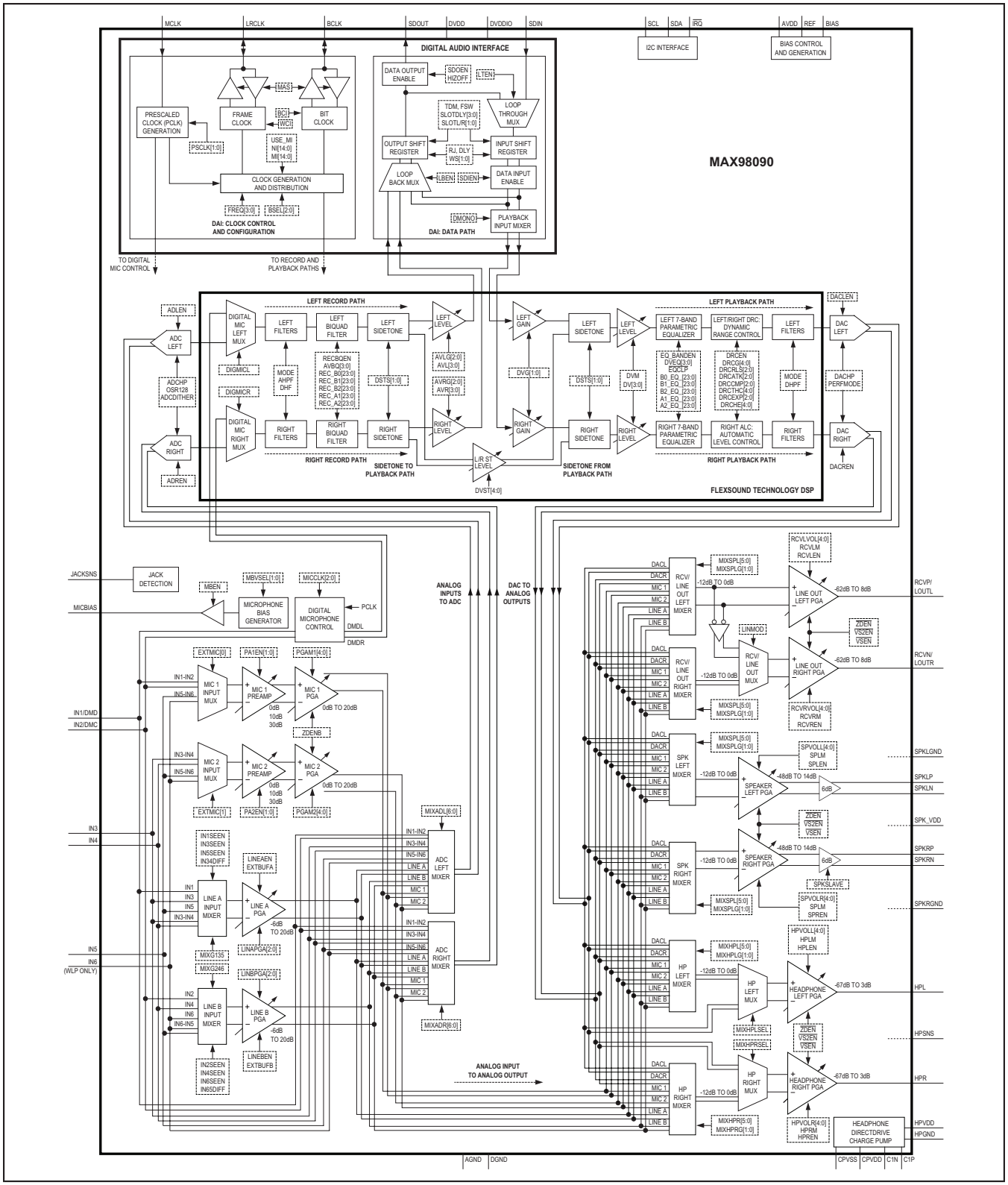
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Functional Diagram



Absolute Maximum Ratings

(Voltages with respect to AGND, unless otherwise noted.)
AVDD, DVDD, HPVDD .....-0.3V to +2.2V
SPKLVDD, SPKRVDD, DVDDIO .....-0.3V to +6.0V
DGND, HPGND, SPKLGND, SPKRGND.....-0.1V to +0.1V
CPVDD .....(V_{HPGND} - 0.3V) to (V_{HPGND} + 2.2V)
CPVSS .....(V_{HPGND} - 2.2V) to (V_{HPGND} + 0.3V)
C1N .....(V_{CPVSS} - 0.3V) to (V_{HPGND} + 0.3V)
C1P..... (V_{HPGND} - 0.3V) to (V_{CPVDD} + 0.3V)
MICBIAS..... -0.3V to ($V_{SPKLVDD}$ + 0.3V)
REF, BIAS ..... -0.3V to (V_{AVDD} + 0.3V)
MCLK, SDIN, SDA, SCL, $\overline{IRQ}$.....-0.3V to +6.0V
LRCLK, BCLK, SDOUT..... -0.3V to (V_{DVDDIO} + 0.3V)
IN1, IN2, IN3, IN4, IN5, IN6 .....-0.3V to +2.2V
HPSNS .....(V_{HPGND} - 0.3V) to (V_{HPGND} + 0.3V)
HPL, HPR.....(V_{CPVSS} - 0.3V) to (V_{CPVDD} + 0.3V)
RCVP/LOUTL.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
RCVN/LOUTR.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKLP, SPKLN .....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKRP, SPKRN .....($V_{SPKRGND}$ - 0.3V) to ($V_{SPKRVDD}$ + 0.3V)
JACKSNS.....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 23.8mW/°C above +70°C).....1.9W
TQFN (derate 35.7mW/°C above +70°C).....2.86W
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....42°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range		Guaranteed by PSRR (Note 3)	$V_{SPKLVDD}$, V_{SPKVDD}, $V_{SPKRVDD}$	2.8	3.7	5.5	V
			V_{AVDD}, V_{HPVDD}	1.65	1.8	2	
			V_{DVDD}	1.08	1.2	1.98	
			V_{DVDDIO}	1.65	1.8	3.6	
Quiescent Supply Current (Note 4)	I_{VDD}	Full-duplex 8kHz mono, receiver output	Analog		1.94	3.5	mA
			Speaker		0.73	2	
			Digital		0.97	1.2	
		DAC playback 48kHz stereo, headphone outputs	Analog		1.45	2	
			Speaker		0	0.005	
			Digital		1.04	1.3	
		DAC playback 48kHz stereo, speaker outputs	Analog		0.91	2.4	
			Speaker		2.18	3	
			Digital		1.05	1.3	

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REF Voltage					1.25		V
BIAS Voltage		BIAS from resistive division (BIAS_MODE = 0)			0.90		V
		BIAS from bandgap (BIAS_MODE = 1)			0.78		
Shutdown Supply Current (Note 4)		T_A = +25°C	Analog		1	10	µA
			Speaker		1	5	
			Digital		2.1	20	
Shutdown to Full Operation					10		ms
DIFFERENTIAL INPUT (ANALOG MICROPHONE) TO ADC RECORD PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, MODE = 1 (FIR audio), A-weighting filter applied			97		dB
		f_S = 8kHz, MODE = 0 (IIR voice), A-weighting filter applied		90	96		dB
Total Harmonic Distortion + Noise	THD+N	A_{V_MICPRE} = 20dB, V_{IN} = 90mV_{RMS}, f = 1kHz,			-82	-75	dB
		A_{V_MICPRE} = 0dB, V_{IN} = 900mV_{RMS}, f = 1kHz			-91		
		A_{V_MICPRE} = 30dB, V_{IN} = 28.5mV_{RMS}, f = 1kHz			-73		
Common-Mode Rejection Ratio	CMRR	f = 217Hz, V_{IN_CM} = 100mV_{P-P}			59		dB
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{AVDD} = 1.65V to 2.0V, input referred		40	57		dB
		V_{RIPPLE} = 100mV_{P-P}, input referred	f = 217Hz		60		
			f = 1kHz		60		
			f = 10kHz		59		
Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output	MODE = 0 (voice) 8kHz		2.2		ms
			MODE = 0 (voice) 16kHz		1.1		
			MODE = 1 (music) 8kHz		4.5		
			MODE = 1 (music) 48kHz		0.8		

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error		DC accuracy			1	6.2	%
DIFFERENTIAL (ANALOG MICROPHONE) PREAMP and PGA							
Full-Scale Input		A_{V_MICPRE} = 0dB			1		V_{RMS}
Microphone Preamplifier Gain	A_{V_MICPRE}	(Note 6)	PA_EN[1:0] = 01		0		dB
			PA_EN[1:0] = 10	19	20	21	
			PA_EN[1:0] = 11	29	30	31	
Microphone Level Adjust Gain (PGA)	A_{V_MICPGA}	(Note 6)	PGAM_[4:0] = 0x00	19	20	21	dB
			PGAM_[4:0] = 0x14		0		
MIC Input Resistance	R_{IN_MIC}	All gain settings, measured at IN_ (measured single-ended)		28	50		kΩ
MICROPHONE BIAS							
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA, MBVSEL[1:0] = 00		2.1	2.2	2.3	V
		I_{LOAD} = 1mA, MBVSEL[1:0] = 01		2.3	2.4	2.5	
		I_{LOAD} = 1mA, MBVSEL[1:0] = 10		2.475	2.57	2.7	
		I_{LOAD} = 1mA, MBVSEL[1:0] = 11		2.7	2.8	2.9	
Load Regulation		I_{LOAD} = 1mA to 2mA, MBVSEL[1:0] = 00	WLP		±0.085	±0.5	mV
			TQFN		±0.085	±0.75	
Line Regulation		$V_{SPKLVDD}$ = 2.8V to 5.5V, MBVSEL[1:0] = 00			±0.01	±1	mV
Ripple Rejection		$V_{RIPPLE (SPKLVDD)}$ = $100mV_{P-P}$	f = 217Hz		95		dB
			f = 1kHz		97		
			f = 10kHz		85		
Noise Voltage		A-weighted, f = 20Hz to 20kHz			7.4		$µV_{RMS}$
		f = 1kHz			52.3		$nV/\sqrt{Hz}$
SINGLE-ENDED (LINE) INPUT TO ADC PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, f_{MCLK} = 12.288MHz, MODE = 1 (FIR audio)			98		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $0.222V_{RMS}$, f = 1kHz			-85	-80	dB
SINGLE-ENDED (LINE) INPUT PGA							
Full-Scale Input	V_{IN}				0.5		V_{RMS}
		$A_{V_EXTERNAL}$ = -6dB, EXTBUF = 1			1		

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Input Level Adjust Gain (PGA)	$A_{V_LINEPGA}$	(Note 6)	PGALIN = 0x0	18	20	21.5	dB
			PGALIN = 0x1	13	14	15	
			PGALIN = 0x2	2	3	4	
			PGALIN = 0x3	-1	0	+1	
			PGALIN = 0x4	-4	-3	-2	
			PGALIN = 0x5, 0x6, 0x7	-7	-6	-5	
Line Input Amplifier Gain	$A_{V_LINEAMP}$	Single-ended only			6		dB
Input Resistance	R_{IN}			14	20		kΩ
Feedback Resistance	R_{IN_FB}	T_A = +25°C		19	20	21	kΩ
DIGITAL LOOP-THROUGH: RECORD OUTPUT TO PLAYBACK INPUT PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, f_{MCLK} = 12.288MHz, MODE = 1 (FIR audio)			97		dB
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, f_S = 48kHz, f_{MCLK} = 12.288MHz, MODE = 1 (FIR audio)			-83	-72	dB
DAC PLAYBACK PATH TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, f_{MCLK} = 12.288MHz			100		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 20mW, R_{REC} = 32Ω			-68	-58	dB
DIFFERENTIAL ANALOG INPUT TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 5)	DR			90	96		dB
Total Harmonic Distortion + Noise	THD+N				-71		dB
Power-Supply Rejection Ratio (Note 3)	PSRR	$V_{SPKLVDD}$ = 2.8V to 5.5V		68.4	80		dB
		V_{RIPPLE} = 100mV_{P-P}	f = 217Hz		77		
			f = 1kHz		77		
			f = 10kHz		69		
RECEIVER AMPLIFIER (Note 7)							
Output Power	P_{OUT}	R_{REC} = 32Ω, f = 1kHz, THD < 1%, BIAS_MODE = 0			97		mW
		R_{REC} = 32Ω, f = 1kHz, THD < 1%, BIAS_MODE = 1			74		
Full-Scale Output		A_{V_RECPGA} = 0dB (Note 8)			1		V_{RMS}
Receiver Volume Control (PGA)	A_{V_RECPGA}	(Notes 6 and 9)	RCVLVOL = 0x00	-63	-61	-59.5	dB
			RCVLVOL = 0x1F	+7.2	+8	+8.75	

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Volume Control Step Size (Note 9)		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -62dB			4		
Mute Attenuation		f = 1kHz		87	97		dB
Output Offset Voltage	V_{OS}	A_{V_REC} = -62dB, T_A = +25°C				±3	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, A_{V_REC} = 0dB	Into shutdown		-67		dBV
			Out of shutdown		-68		
Capacitive Drive Capability		No sustained oscillations	R_L = 32Ω		500		pF
			R_L = ∞		100		
DAC PLAYBACK PATH TO LINEOUT AMPLIFIER PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, f_{MCLK} = 12.288MHz			100		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_{LOUT} = 10kΩ ($0.5V_{RMS}$ output level)			-86	-70	dB
SINGLE-ENDED ANALOG INPUT TO LINE OUT AMPLIFIER PATH							
Dynamic Range (Note 5)	DR				98		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, R_{LOUT} = 10kΩ ($0.5V_{RMS}$ output level)			-86		dB
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{SPK_VDD} = 2.8V to 5.5V		60	74		dB
		V_{RIPPLE} = $100mV_{P-P}$	f = 217Hz		74		
			f = 1kHz		74		
			f = 10kHz		73		
LINE OUT AMPLIFIER (Note 7)							
Full-Scale Output		(Note 8)			0.707		V_{RMS}
Line Output Amplifier Gain	$A_{V_LOUTAMP}$				-3		dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Output Volume Control (PGA)	$A_{V_LOUTPGA}$	(Notes 6 and 9)	RCV_VOL = 0x00	-63	-61	-59.5	dB
			RCV_VOL = 0x1F	+7.2	+8	+8.75	
Volume Control Step Size (Note 9)		8dB to 6dB			0.5		dB
		6dB to 0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -62dB			4		
Mute Attenuation		f = 1kHz		87	97		dB
Capacitive Drive Capability		No sustained oscillations	R_{LOUT} = 1kΩ		500		pF
			R_{LOUT} = ∞		100		
DAC PLAYBACK PATH TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 5)	DR				91		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, Z_{SPK} = 8Ω + 68µH, f_{MCLK} = 12.288MHz			-70		dB
Crosstalk		SPKL to SPKR and SPKR to SPKL, P_{OUT} = 640mW, f = 1kHz			-104		dB
Output Noise					27		μV_{RMS}
DIFFERENTIAL ANALOG INPUT TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 5)	DR	Output referenced to $2V_{RMS}$			91		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, Z_{SPK} = 8Ω + 68µH			-70		dB
Output Noise					28		μV_{RMS}
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{SPK_VDD}= 2.8V to 5.5V		50	80		dB
		V_{RIPPLE} = $100mV_{P-P}$	f = 217Hz		68		
			f = 1kHz		67		
			f = 10kHz		61		

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SPEAKER AMPLIFIER (Note 7)							
Output Power	P_{OUT}	f = 1kHz, THD+N = 1%, Z_{SPK} = 8Ω + 68µH, WLP package	V_{SPK_VDD} = 5.0V		1450		mW
			V_{SPK_VDD} = 4.2V		1000		
			V_{SPK_VDD} = 3.7V		780		
			V_{SPK_VDD} = 3.3V		600		
			V_{SPK_VDD} = 3.0V		500		
		f = 1kHz, THD+N = 10%, Z_{SPK} = 8Ω + 68µH, WLP package	V_{SPK_VDD} = 5.0V		1800		
			V_{SPK_VDD} = 4.2V		1250		
			V_{SPK_VDD} = 3.7V		970		
			V_{SPK_VDD} = 3.3V		760		
			V_{SPK_VDD} = 3.0V		620		
Output Power	P_{OUT}	f = 1kHz, THD+N = 1%, Z_{SPK} = 4Ω + 33µH, WLP package	V_{SPK_VDD} = 5.0V		2600		mW
			V_{SPK_VDD} = 4.2V		1800		
			V_{SPK_VDD} = 3.7V		1400		
			V_{SPK_VDD} = 3.3V		1100		
			V_{SPK_VDD} = 3.0V		900		
		f = 1kHz, THD+N = 10%, Z_{SPK} = 4Ω + 33µH, WLP package	V_{SPK_VDD} = 5.0V		3250		
			V_{SPK_VDD} = 4.2V		2250		
			V_{SPK_VDD} = 3.7V		1700		
			V_{SPK_VDD} = 3.3V		1350		
			V_{SPK_VDD} = 3.0V		1100		
Full-Scale Output		A_{V_SPK} = +6dB (Note 8)			2		V_{RMS}
Speaker Output Amplifier Gain	A_{V_SPKAMP}				+6		dB
Speaker Volume Control (PGA)	A_{V_SPKPGA}	(Notes 6 and 9)	SPVOLL = 0x00	-51	-48	-44.5	dB
			SPVOLR = 0x1F	13	14	15	
Volume Control Step Size (Note 9)		14dB to 9dB			0.5		dB
		+9dB to -6dB			1		
		-6dB to -14dB			2		
		-14dB to -32dB			3		
		-32dB to -48dB			4		
Mute Attenuation		f = 1kHz		76	84		dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Offset Voltage	V_{OS}	A_{V_SPKPGA} = -62dB, T_A = +25°C			±0.5	±4	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, A_{V_SPK} = 0dB	Into shutdown		-65		dBV
			Out of shutdown		-65		
DAC PLAYBACK PATH TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 5)	DR	f_S = 48kHz, f_{MCLK} = 12.288MHz	Master or slave mode		102		dB
			Slave mode	94			
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 10mW	R_{HP} = 16Ω		-86	-77	dB
			R_{HP} = 32Ω		-88		
		f = 1kHz, V_{OUT} = $1V_{RMS}$, R_{HP} = 10kΩ			-88		
Crosstalk		f = 1kHz, V_{IN} = -1dBFS, R_{HP} = 10kΩ			-105		dB
		HPL to HPR and HPR to HPL, P_{OUT} = 5mW, f = 1kHz, R_{HP} = 32Ω			-104		dB
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		70	80		dB
		V_{RIPPLE} = $100mV_{P-P}$, A_{V_HP} = 0dB	f = 217Hz		79		
			f = 1kHz		79		
			f = 10kHz		74		
DAC Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from digital input to analog output	MODE = 0 (voice) 8kHz		2.2		ms
			MODE = 0 (voice) 16kHz		1.1		
			MODE = 1 (music) 8kHz		4.5		
			MODE = 1 (music) 48kHz		0.76		
Gain Error					1	5	%
Channel Gain Mismatch					1		%
SINGLE-ENDED ANALOG INPUT TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 5)		A_{V_LINE} = 0dB A_{V_HPPGA} = 0 dB			101		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $250mV_{RMS}$, f =1kHz			-80		dB
Crosstalk		HPL to HPR and HPR to HPL, P_{OUT} = 5mW, f = 1kHz, R_{HP} = 32Ω			-94		dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		40	60		dB
		V_{RIPPLE} = 100mV_{P-P}, A_{V_TOTAL} = 0dB	f = 217Hz		61		
			f = 1kHz		61		
			f = 10kHz		60		
HEADPHONE AMPLIFIER (Note 7)							
Output Power	P_{OUT}	f = 1kHz, THD = 1%	R_{HP} = 16Ω	20	40		mW
			R_{HP} = 32Ω		30		
Total Harmonic Distortion + Noise	THD+N	R_{HP} = 16Ω, P_{OUT} = 10mW, f = 1kHz			-88	-77	dB
		R_{HP} = 10kΩ, V_{OUT} = 1V_{RMS}, f = 1kHz			-88		
Full-Scale Output		A_{VHP} = 0dB (Note 8)			1		V_{RMS}
Headphone Volume Control (PGA)	A_{V_HPPGA}		HPVOL_ = 0x00	-69	-67	-65	dB
			HPVOL_ = 0x1F	2.5	3	3.5	
Volume Control Step Size (Note 9)		+3dB to +1dB			0.5		dB
		+1dB to -5dB			1		
		-5dB to -19dB			2		
		-19dB to -43dB			3		
		-43dB to -67dB			4		
Mute Attenuation		f = 1kHz			110		dB
Output Offset Voltage	V_{OS}	AV_HP = -67dB	T_A = +25°C		±0.5	±1	mV
			T_A = T_{MIN} to T_{MAX}			±3	
Capacitive Drive Capability		No sustained oscillations	R_{HP} = 32Ω		500		pF
			R_{HP} = ∞		100		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, A_{V_HP} = -67dB	Into shutdown		-73		dBV
			Out of shutdown		-73		
JACK DETECTION							
JACKSNS High Threshold	V_{TH_HIGH}	MICBIAS enabled		0.80 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
		MICBIAS disabled		0.80 x $V_{SPKLVDD}$	0.95 x $V_{SPKLVDD}$	0.98 x $V_{SPKLVDD}$	

Electrical Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JACKSNS Low Threshold	V_{TH_LOW}	MICBIAS enabled	0.06 x $V_{MICBIAS}$	0.10 x $V_{MICBIAS}$	0.17 x $V_{MICBIAS}$	V
		MICBIAS disabled	0.06 x $V_{SPKLVDD}$	0.10 x $V_{SPKLVDD}$	0.17 x $V_{SPKLVDD}$	
JACKSNS Sense Voltage	V_{SENSE}	MICBIAS disabled		$V_{SPKLVDD}$		V
JACKSNS Strong Pullup Resistance	R_{SPU}	MICBIAS disabled, JDWK = 0	1.9	2.4	2.7	kΩ
JACKSNS Weak Pullup Current	I_{WPU}	MICBIAS disabled, JDWK = 1		5	12	µA
JACKSNS Glitch Debounce Period	t_{GLITCH}	JDEB = 00		25		ms
		JDEB = 11		200		

Digital Filter Specifications

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD}= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECORD PATH LEVEL CONTROL						
Record Level Adjust Range	A_{V_ADCLVL}	AVL/AVR = 0xF to 0x0 (Note 6)	-12		+3	dB
Record Level Adjust Step Size				1		dB
Record Gain Adjust Range	$A_{V_ADCGAIN}$	AVLG/AVRG = 0x0 to 0x3 (Note 6)	0		42	dB
Record Gain Adjust Step Size				6		dB
RECORD PATH VOICE MODE IIR LOWPASS FILTER (MODE = 0)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.444 x f_S			Hz
		-3dB cutoff	0.449 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		0.1	dB
Stopband Cutoff	f_{SLP}				0.47 x f_S	Hz
Stopband Attenuation		f > f_{SLP}	74			dB
RECORD PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, f_{LRCLK} < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.48 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation		f < f_{SLP}	60			dB
RECORD PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 1, f_{LRCLK} > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple Limit cutoff	0.208 x f_S			Hz
		-3dB cutoff	0.28 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.45 x f_S	Hz
Stopband Attenuation		f < f_{SLP}	60			dB

Digital Filter Specifications (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD}= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECORD PATH DC-BLOCKING HIGHPASS FILTER							
DC Attenuation	A_{V_ADCHPF}	AHPF = 1			90		dB
RECORD PATH PROGRAMMALE BIQUAD FILTER							
Preattenuator Gain Range				-15		0	dB
Preattenuator Step Size					1		dB
Cutoff Frequency		Highpass filter		0.0008 x f_S			Hz
		High-frequency shelving filter		0.02 x f_S			
		Lowpass filter		0.002 x f_S			
		Low-frequency shelving filter		0.0008 x f_S			
		Peak filter		0.0008 x f_S			
Quality Factor	Q	Peak filter				10	
DIGITAL SIDETONE: RECORD PATH TO PLAYBACK PATH (MODE = 0)							
Sidetone Level Adjust Range	A_{V_STLVL}	DVST = 0x1F to 0x01		-60.5		-0.5	dB
Sidetone Level Adjust Step Side					2		dB
Sidetone Path Phase Delay		f_{IN} = 1kHz, full-scale amplitude, highpass filter disabled	f_S = 8kHz		1.8		ms
			f_S = 16kHz		0.9		
PLAYBACK PATH LEVEL CONTROL							
Playback Path Attenuation Range	A_{V_DACLVL}	DV = 0xF to 0x0 (Note 6)		-15		0	dB
Playback Path Attenuation Step Size					1		dB
Playback Path Gain Adjust Range	$A_{V_DACGAIN}$	DVG = 00 to 11 (Note 6)		0		18	dB

Digital Filter Specifications (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD}= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 10)

Playback Path Gain Adjust Step Size				6		dB
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
PLAYBACK PATH VOICE MODE IIR LOWPASS FILTER (MODE = 0)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.448 x f_S			Hz
		-3dB cutoff	0.451 x f_S			
Passband Ripple		$f < f_{PLP}$	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.476 x f_S	Hz
Stopband Attenuation (Note 11)		$f > f_{SLP}$	75			dB
PLAYBACK PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, f_{LRCLK} < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		$f < f_{PLP}$	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 11)		$f > f_{SLP}$	60			dB
PLAYBACK PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE1 = 1, DHF = 1 for f_{LRCLK} > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Passband Ripple		$f < f_{PLP}$	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation (Note 11)		$f < f_{SLP}$	60			dB

Digital Filter Specifications (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD}= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 10)

PLAYBACK PATH DC-BLOCKING HIGHPASS FILTER						
DC Attenuation		DHPF = 1		89		dB
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
PLAYBACK PATH DYNAMIC RANGE CONTROL						
Gain Range			0		12	dB
Compression Threshold			-31		0	dBFS
Expansion Threshold			-66		-35	dBFS
Attack Time			0.0005		0.2	s
Release Time			0.0625		8	s
PLAYBACK PATH PARAMETRIC EQUALIZER						
Number of Bands				7		Bands
Per Band Gain Range			-12		+12	dB
Preattenuator Gain Range			-15		0	dB
Preattenuator Step Size				1		dB
Cutoff Frequency		Highpass filter	0.0008 x f_S			Hz
		High-frequency shelving filter	0.02 x f_S			
		Lowpass filter	0.002 x f_S			
		Low-frequency shelving filter	0.0008 x f_S			
		Peak filter	0.0008 x f_S			
Quality Factor	Q	Peak filter			10	

Digital Input/Output Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK						
Input High Voltage	V_{IH}		1.26			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDIO} = 2.0V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDIN, BCLK, LRCLK (Input)						
Input High Voltage	V_{IH}		0.7 x V_{DVDDIO}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDDIO}	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDIO} = 3.6V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
BCLK, LRCLK, SDOUT (Output)						
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{DVDDIO} - 0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDIO} = 2.0V, T_A = +25°C, high-impedance state	-1		+1	µA
SDA, SCL (Input)						
Input High Voltage	V_{IH}		0.7 x V_{DVDDIO}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDDIO}	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDIO} = 2.0V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDA, $\overline{IRQ}$ (Output)						
Output Low Voltage	V_{OL}	V_{DVDDIO} = 1.65V, I_{OH} = 3mA			0.2 x V_{DVDDIO}	V
Output High Current	I_{OH}	V_{DVDDIO} = 1.65V, I_{OL} = 3mA			1	µA

Digital Input/Output Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE DATA (DMD) INPUT						
Input High Voltage	V_{IH}		0.65 x V_{DVDDIO}			V
Input Low Voltage	V_{IL}				0.35 x V_{DVDDIO}	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDIO} = 2.0V, T_A = +25°C	-25		+25	µA
Input Capacitance				10		pF
DIGITAL MICROPHONE CLOCK (DMC) OUTPUT						
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{AVDD} - 0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V

Input Clock Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD}= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, AV_RCV = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	f_S = 8kHz, voice mode filters (MODE = 0)		2.048		60	MHz
		f_S = 48kHz, music mode filters (MODE = 1)		10		60	
		f_S = 96kHz, music mode filters (MODE = 1)		12.288		60	
MCLK Input Duty Cycle		PSCLK = 01		40	50	60	%
		PSCLK = 10 or 11		30		70	
Maximum MCLK Input Jitter					1		ns
LRCLK Sample Rate (Note 12)	f_{LRCLK}	DHF = 0		8		48	kHz
		DHF = 1		48		96	
DAI LRCLK Average Frequency Error (Note 13)		FREQ = 0x8 to 0xF		0		0	%
		FREQ = 0x0		-0.025		+0.025	
Minimum PCLK to LRCLK Frequency Ratio		8kHz ≤ f_S ≤ 48kHz, voice mode filters (MODE = 0), DHF = 0	OSR = 128 or 64	256 x f_S			f_{PCLK}
		8kHz ≤ f_S ≤ 48kHz, music mode filters (MODE = 1), DHF = 0	OSR = 128	256 x f_S			
			OSR = 64	208 x f_S			
		48kHz < f_S ≤ 96kHz, music mode filters (MODE = 1), DHF = 1	OSR = 64	128 x f_S			
PLL Lock Time					2	7	ms
Maximum LRCLK Input Jitter to Maintain PLL Lock						±100	ns
Soft-Start/Stop Time					10		ms

Digital Audio Interface Timing Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS							
BCLK Cycle Time	t_{BCLK}	Slave mode		80			ns
BCLK High Time	t_{BCLKH}	Slave mode		20			ns
BCLK Low Time	t_{BCLKL}	Slave mode		20			ns
BCLK or LRCLK Rise and Fall Time	t_r, t_f	Master mode, C_L = 15pF			5		ns
SDIN to BCLK Setup Time	t_{SETUP}			20			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$	Slave mode		20			ns
SDIN to BCLK Hold Time	t_{HOLD}			20			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$	Slave mode		20			ns
Minimum Delay Time from LSB BCLK Falling Edge to High-Impedance State	t_{HIZOUT}	Master mode	TDM = 1		20		ns
			TDM = 1, FSW = 1		20		
			TDM = 1, FSW = 0		20		
			TDM = 0, DLY = 1		20		
LRCLK Rising Edge to SDOUT MSB Delay	t_{SYNCTX}	C = 30pF, TDM = 1, FSW = 1				40	ns
BCLK to SDOUT Delay	t_{CLKTX}	C = 30pF	TDM = 1, BCLK rising edge			50	ns
			TDM = 0			50	
Delay Time from BCLK to LRCLK	$t_{CLKSYNC}$	Master mode	TDM = 1	-15		+15	ns
			TDM = 0			0.8 x t_{BCLK}	

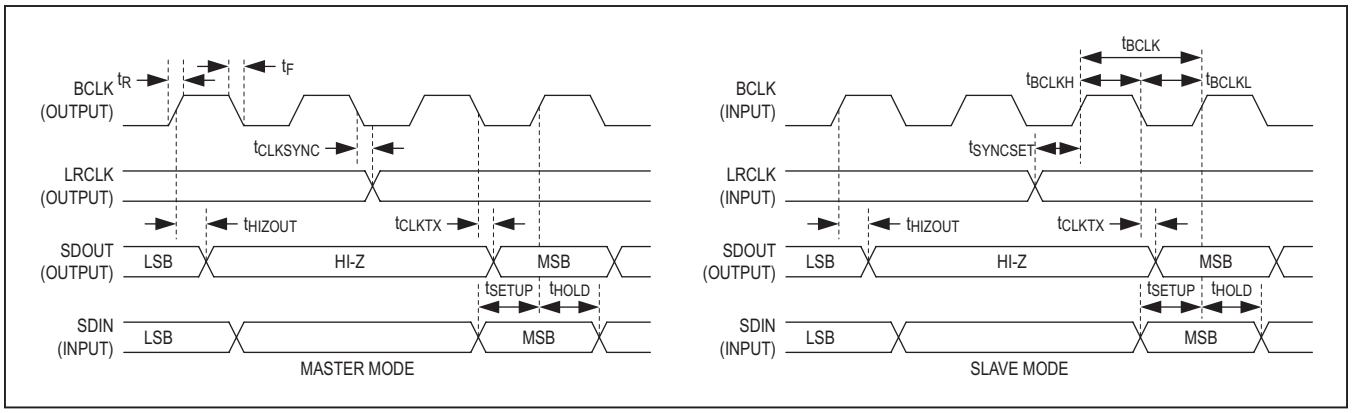


Figure 1. I²S Audio Interface Timing Diagrams (TDM = 0)

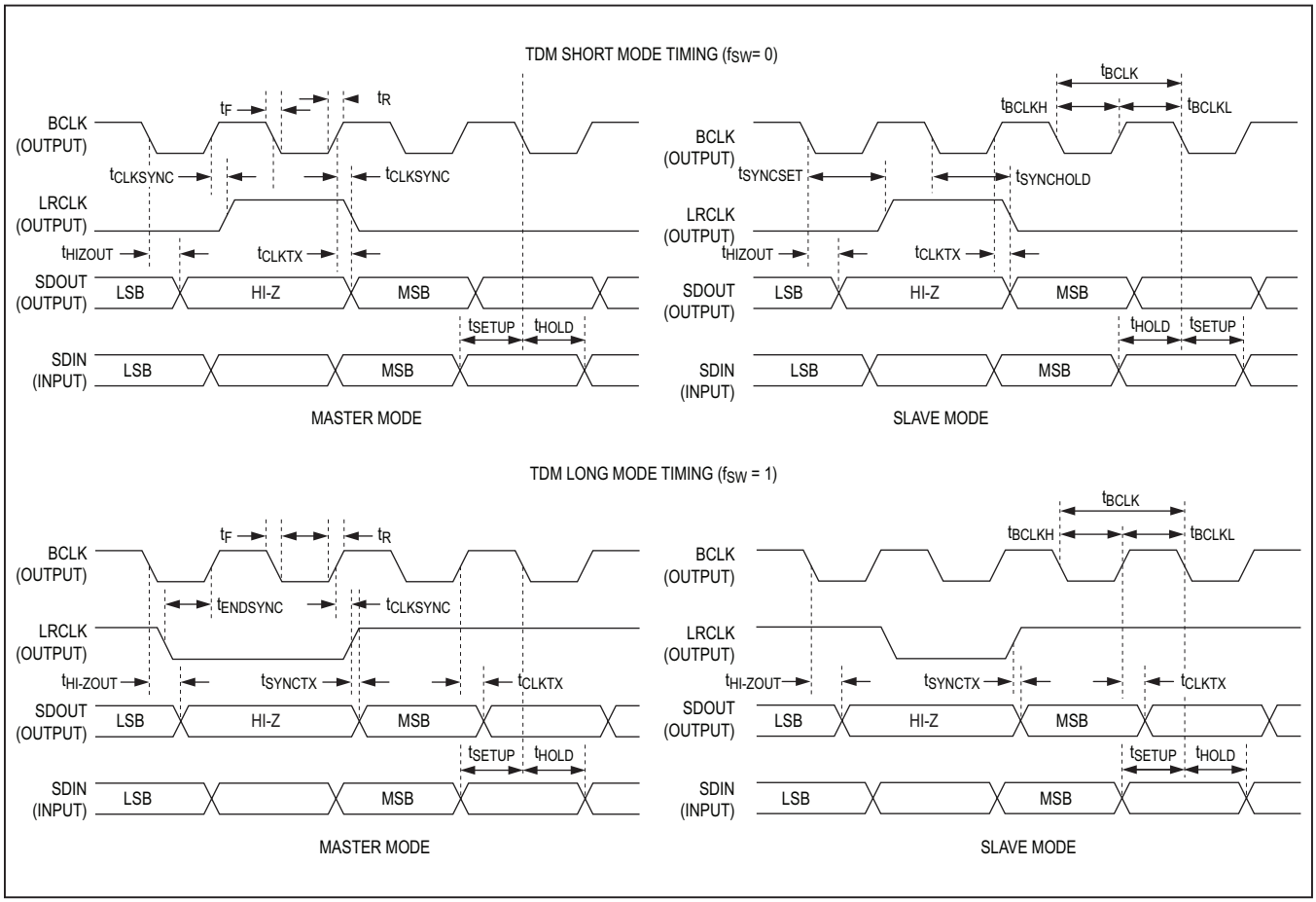


Figure 2. TDM Audio Interface Short Mode Timing Diagram (TDM = 1, BCI = 1)

I²C Timing Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}	Guaranteed by SCL pulse width low and high	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	R_{PU} = 475Ω, C_B = 100pF, 400pF	0		900	ns
		Transmitting	0		900	
		Receiving			0	
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 14)	20 + 0.1 x C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 14)	20 + 0.1 x C_B		300	ns
SDA Transmitting Fall Time	t_F	R_{PU} = 475Ω, C_B = 100pF to 400pF (Note 14)	20 + 0.1 x C_B		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B	Guaranteed by SDA transmitting fall time			400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

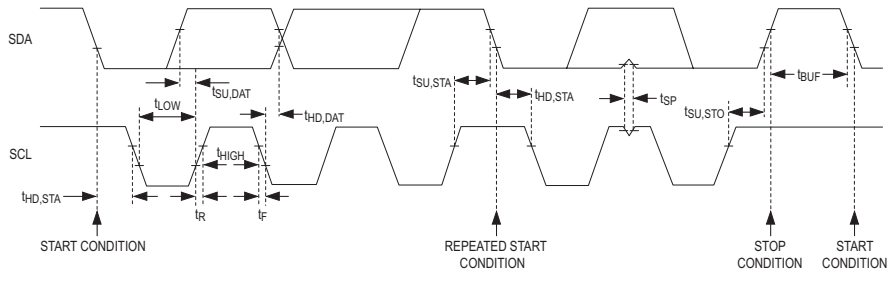


Figure 3. I²C Interface Timing Diagram

Digital Microphone Timing Characteristics

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE TIMING CHARACTERISTICS						
DMC Frequency	f_{DMC}	MICCLK = 000		$f_{PCLK}/2$		MHz
		MICCLK = 001		$f_{PCLK}/3$		
		MICCLK = 010		$f_{PCLK}/4$		
		MICCLK = 011		$f_{PCLK}/5$		
		MICCLK = 100		$f_{PCLK}/6$		
		MICCLK = 101		$f_{PCLK}/8$		
DMD to DMC Setup Time	$t_{SU,MIC}$	Either clock edge	20			ns
DMD to DMC Hold Time	$t_{HD,MIC}$	Either clock edge	0			ns

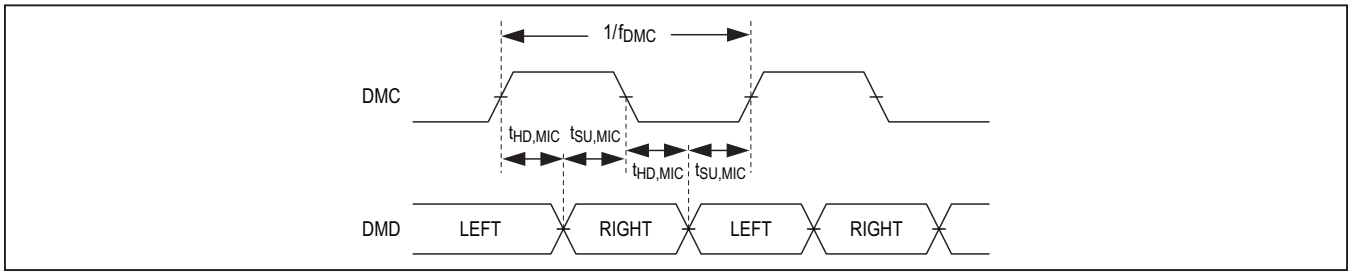


Figure 4. Digital Microphone Timing Diagram

Note 2: The MAX98090 is 100% production tested at T_A =+25°C. Specifications over temperature limits are guaranteed by design.
Note 3: BIAS derived from a bandgap reference (BIAS_MODE = 1).
Note 4: Analog supply current = AVDD + HPVDD, speaker supply current = SPKLVDD + SPKRVDD, and digital supply current = DVDD + DVDDIO.
Note 5: Dynamic range measurements are performed with the EIAJ method (a -60dBFS output signal at 1kHz, A-weighted and normalized to 0dBFS; f = 20Hz – 20kHz).
Note 6: Gain measured relative to the 0dB setting.
Note 7: Performance measured using DAC Inputs, unless otherwise stated.
Note 8: Full-scale analog output with 0dB of programmable gain, and a 0dBFS DAC input amplitude, a $1V_{RMS}$ differential analog input amplitude, or a $0.5V_{RMS}$ single-ended analog input amplitude.
Note 9: Performance measured using an analog input to amplifier output path.
Note 10: Digital filter performance is invariant over temperature and production tested at T_A = +25°C.
Note 11: The filter specification is accurate only for synchronous clocking modes (integer MCLK to LRCLK ratio).
Note 12: f_{LRCLK} may be any rate in the indicated range. Asynchronous and non-integer f_{MCLK}/f_{LRCLK} ratios can exhibit some full-scale performance degradation compared to synchronous integer ratios.
Note 13: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 14: C_B is in pF.

Quiescent Power Consumption

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
DIGITAL AUDIO INPUT TO PLAYBACK PATH TO HEADPHONE OUTPUT (MUSIC FILTERS)							
Stereo DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω	1.39	1.28	1.04	0.02	0.00	6.05	102
Stereo DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω, low power mode	0.94	0.51	1.02	0.02	0.00	3.84	99
Stereo DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω, dynamic range control enabled	1.39	1.28	1.11	0.02	0.00	6.14	102
Stereo DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω, parametric equalizer enabled	1.39	1.28	1.65	0.02	0.00	6.78	102
Stereo DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 96kHz, 20-bit, music filters, R_{LOAD} = 32Ω	1.39	1.28	1.17	0.02	0.00	6.21	102
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 44.1kHz, 20-bit, music filters, R_{LOAD} = 32Ω	1.40	1.29	1.00	0.02	0.00	6.03	102
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 44.1kHz, 20-bit, music filters, R_{LOAD} = 32Ω, low power mode	0.96	0.51	1.00	0.02	0.00	3.85	99

Quiescent Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
DIGITAL AUDIO INPUT TO PLAYBACK PATH TO HEADPHONE OUTPUT (VOICE FILTERS)							
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	1.35	1.28	0.89	0.02	0.00	5.81	101
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	0.91	0.51	0.89	0.02	0.00	3.62	98.5
Mono DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	0.78	0.69	0.82	0.02	0.00	3.64	101
Mono DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	0.56	0.30	0.82	0.02	0.00	2.55	98.5
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	1.35	1.28	0.94	0.02	0.00	5.87	99
Stereo DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	0.91	0.50	0.94	0.02	0.00	3.68	97
DIGITAL AUDIO INPUT TO PLAYBACK PATH TO SPEAKER OUTPUT							
Stereo DAC Playback to Speaker Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH	1.10	0.00	1.04	0.02	2.18	11.47	91
Stereo DAC Playback to Speaker Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH, low power mode	0.91	0.00	1.03	0.02	2.18	10.93	91
Mono DAC Playback to Speaker Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH	0.65	0.00	0.90	0.02	1.11	6.36	91
Mono DAC Playback to Speaker Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH, low power mode	0.51	0.00	0.90	0.02	1.11	6.09	91
Stereo DAC Playback to Speaker Output f_{MCLK} = 12.288MHz, f_S = 96kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH	1.21	0.00	1.17	0.02	2.18	11.61	91
Stereo DAC Playback to Speaker Output f_{MCLK} = 13MHz, f_S = 44.1kHz, 20-bit, music filters, R_{LOAD} = 8Ω, L_{LOAD} = 68µH	1.21	0.00	1.06	0.02	2.18	11.50	91

Quiescent Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
ANALOG AUDIO LINE INPUT TO DIGITAL RECORD PATH OUTPUT							
Stereo Differential Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	3.09	0.00	1.38	0.02	0.00	7.19	98
Stereo Differential Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	1.97	0.00	1.39	0.02	0.00	5.21	98
Stereo Differential Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, Digital Biquad Filter Enabled	3.10	0.00	1.46	0.02	0.00	7.30	98
Mono Differential Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	1.86	0.00	1.10	0.02	0.00	4.65	98
Stereo Single-Ended Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	3.19	0.00	1.35	0.02	0.00	7.33	97
Stereo Single-Ended Line Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	2.02	0.00	1.35	0.02	0.00	5.24	97
Stereo Single-Ended Line Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters	2.90	0.00	0.90	0.02	0.00	6.28	98
Stereo Single-Ended Line Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters low power mode	1.73	0.00	0.90	0.02	0.00	4.20	97

Quiescent Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
ANALOG MICROPHONE INPUT TO DIGITAL RECORD PATH OUTPUT (MUSIC FILTERS)							
Stereo Analog Microphone Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	3.50	0.00	1.36	0.02	0.00	7.88	97
Stereo Analog Microphone Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	2.22	0.00	1.38	0.02	0.00	5.65	97
Mono Analog Microphone Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	2.02	0.00	1.05	0.02	0.00	4.90	97
Mono Analog Microphone Input to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	1.35	0.00	1.08	0.02	0.00	3.74	97
ANALOG MICROPHONE INPUT TO DIGITAL RECORD PATH OUTPUT (VOICE FILTERS)							
Stereo Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters	3.20	0.00	0.91	0.02	0.00	6.81	99
Stereo Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters low power mode	1.93	0.00	0.92	0.02	0.00	4.57	98
Mono Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters	1.87	0.00	0.82	0.02	0.00	4.35	99
Mono Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters low power mode	1.20	0.00	0.83	0.02	0.00	3.18	98
Stereo Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters	3.26	0.00	1.11	0.02	0.00	7.16	98
Stereo Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters low power mode	1.98	0.00	1.12	0.02	0.00	4.91	97
Mono Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters	1.90	0.00	0.94	0.02	0.00	4.54	98
Mono Analog Microphone Input to Record Path f_{MCLK} = 13MHz, f_S = 16kHz, 16-bit, voice filters low power mode	1.23	0.00	0.94	0.02	0.00	3.35	97

Quiescent Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
ANALOG AUDIO INPUT DIRECT TO DIGITAL RECORD PATH OUTPUT							
Stereo Differential Input Direct to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	2.85	0.00	1.39	0.02	0.00	6.76	99
Stereo Differential Input Direct to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	1.84	0.00	1.39	0.02	0.00	4.98	98
Mono Differential Input Direct to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters	1.61	0.00	1.08	0.02	0.00	4.20	99
Mono Differential Input Direct to Record Path f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, low power mode	1.09	0.00	1.09	0.02	0.00	3.29	98
ANALOG AUDIO INPUT TO ANALOG AUDIO OUTPUT							
Stereo Single-Ended Line Input to Headphones (R_{LOAD} = 32Ω)	1.12	2.42	0.00	0.00	0.00	6.34	99
Mono Single-Ended Line Input to Headphones (R_{LOAD} = 32Ω)	0.72	1.57	0.00	0.00	0.00	3.41	99
Stereo Differential Line Input to Headphones (R_{LOAD} = 32Ω)	1.07	1.26	0.00	0.00	0.00	4.19	100
Stereo Differential Line Input to Speaker Output (R_{LOAD} = 8Ω, L_{LOAD} = 68µH)	0.36	0.00	0.00	0.00	2.08	8.34	91
Mono Differential Line Input to Speaker Output (R_{LOAD} = 8Ω, L_{LOAD} = 68µH)	0.31	0.00	0.00	0.00	1.04	4.42	91
Stereo Single-Ended Line Input to Line Output (R_{LOAD} = 10kΩ)	0.76	0.00	0.00	0.00	0.74	4.12	99

Quiescent Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V, slave mode operation.)

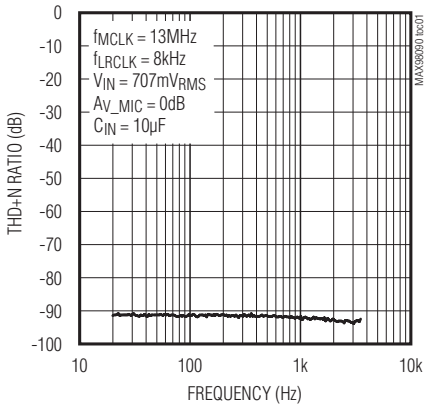
DEVICE MODE AND CONFIGURATION	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDIO} (mA)	I_{SPK_VDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
FULL-DUPLEX AUDIO OPERATION							
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Receiver Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	2.67	0.00	0.95	0.02	0.73	8.61	REC: 99 PB: 100
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Receiver Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	1.94	0.00	0.95	0.02	0.73	7.31	REC: 99 PB: 98
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω	2.69	0.69	1.22	0.02	0.00	7.51	REC: 97 PB: 102
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output f_{MCLK} = 12.288MHz, f_S = 48kHz, 20-bit, music filters, R_{LOAD} = 32Ω, low power mode	1.80	0.30	1.24	0.02	0.00	5.26	REC: 97 PB: 99
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	2.54	0.69	0.95	0.02	0.00	6.93	REC: 99 PB: 102
Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	1.66	0.30	0.96	0.02	0.00	4.67	REC: 99 PB: 99
Stereo Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphones f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω	4.44	1.28	1.14	0.02	0.00	11.54	REC: 99 PB: 102
Stereo Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphones f_{MCLK} = 13MHz, f_S = 8kHz, 16-bit, voice filters, R_{LOAD} = 32Ω, low power mode	2.73	0.51	1.15	0.02	0.00	7.18	REC: 99 PB: 99

Typical Operating Characteristics

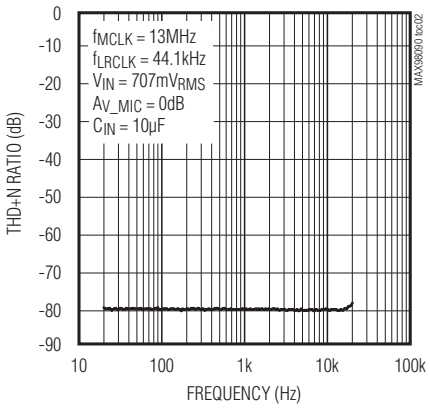
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT

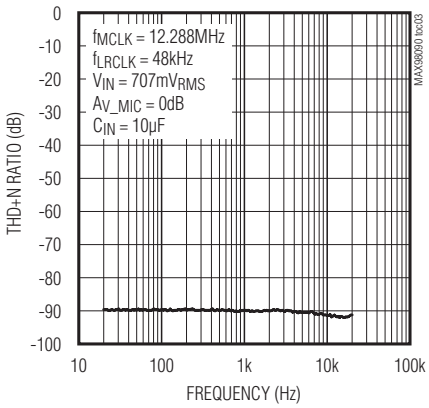
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



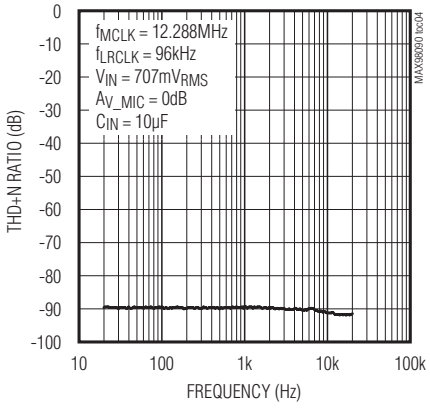
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



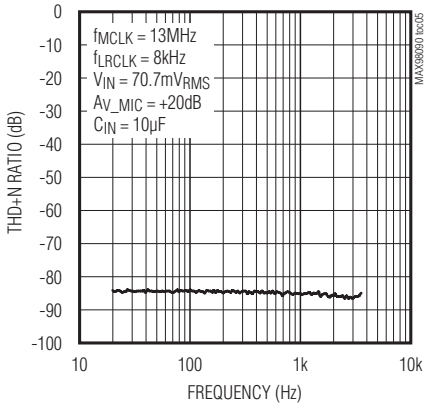
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



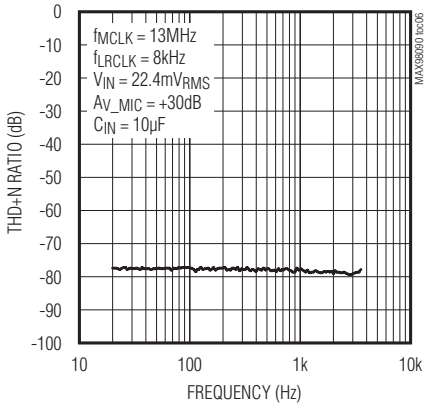
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)

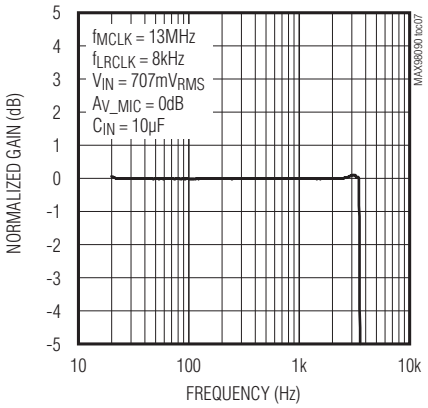


Typical Operating Characteristics (continued)

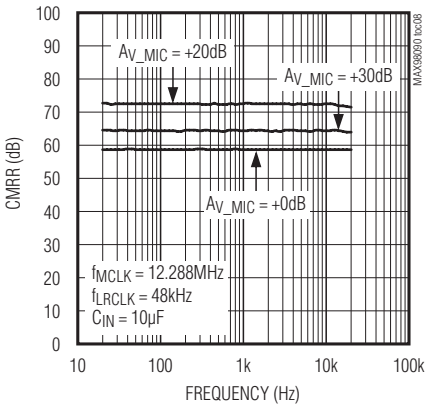
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

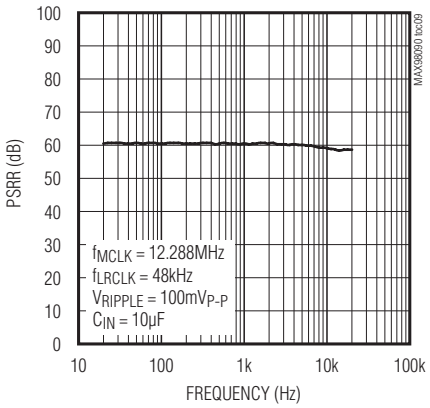
GAIN vs. FREQUENCY (MIC TO ADC)



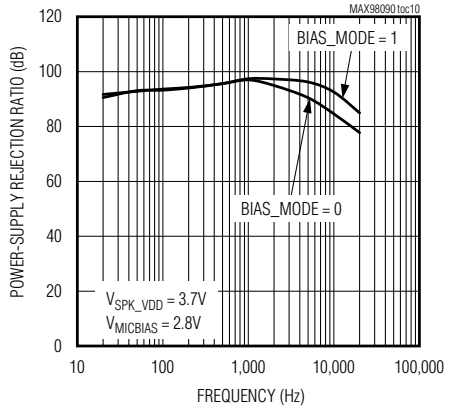
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



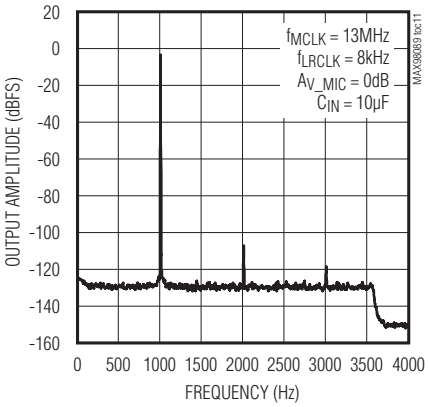
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



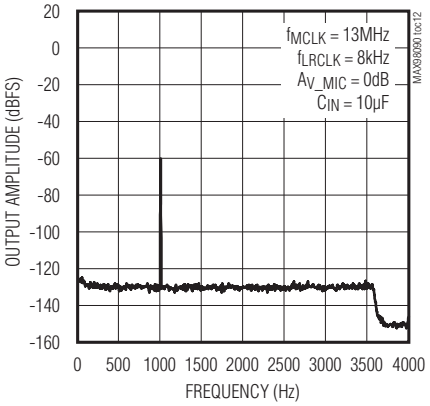
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPK_VDD to MICBIAS)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)

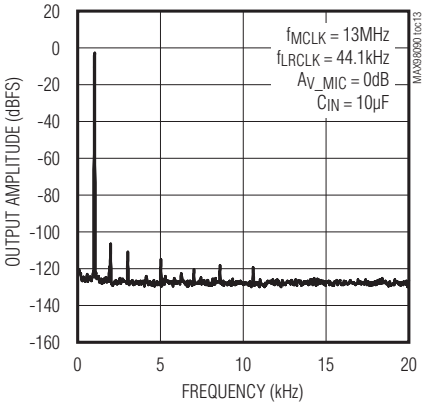


Typical Operating Characteristics (continued)

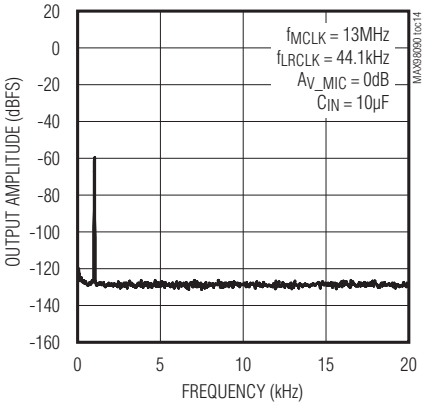
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

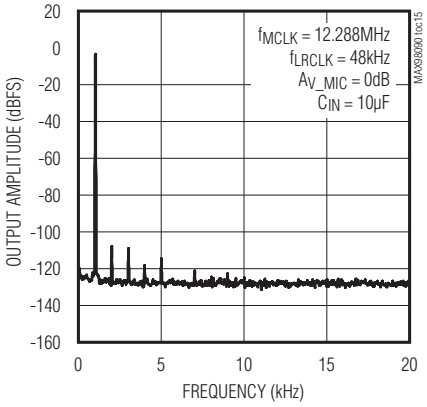
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)



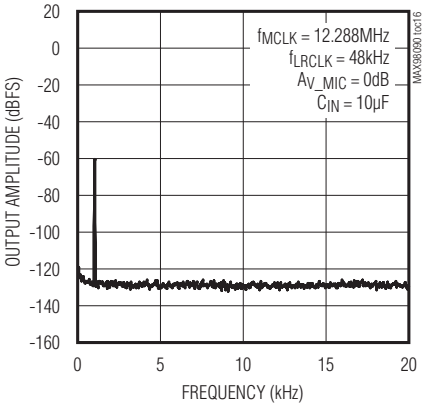
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)



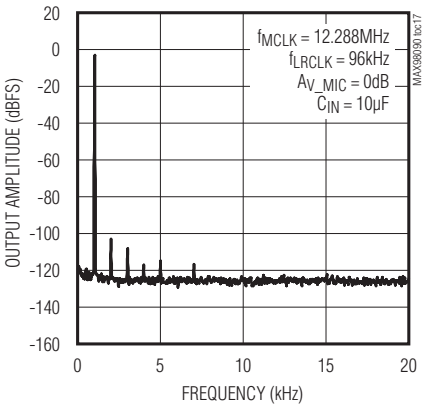
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)



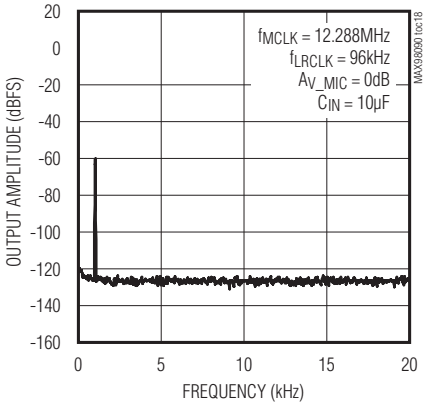
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)

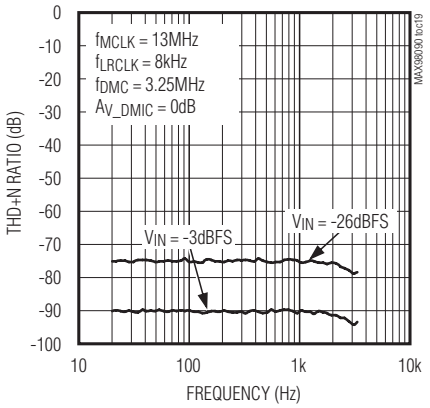


Typical Operating Characteristics (continued)

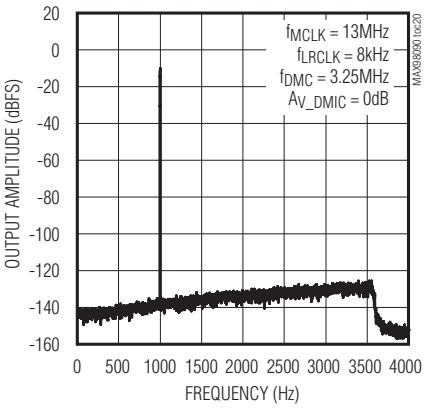
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DIGITAL MICROPHONE INPUT TO RECORD PATH OUTPUT

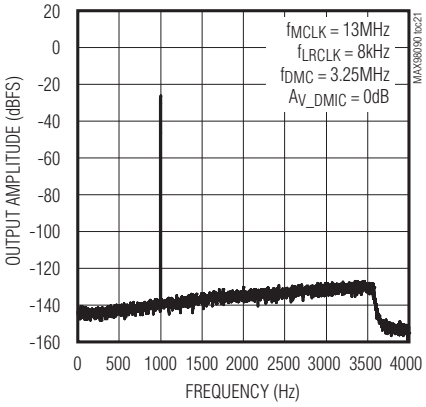
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)



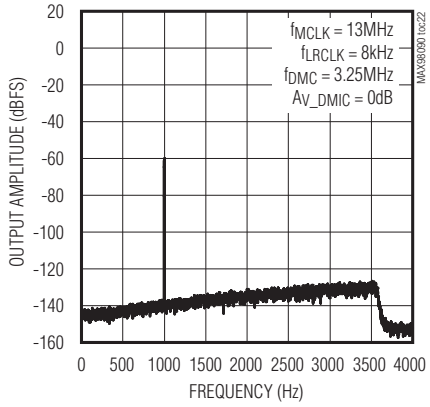
INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)



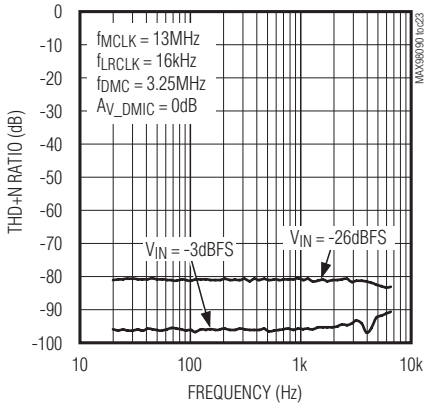
INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)



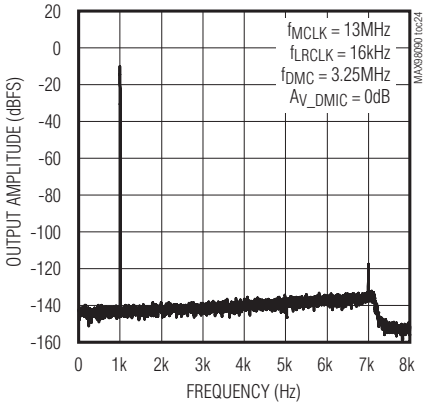
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)



INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)

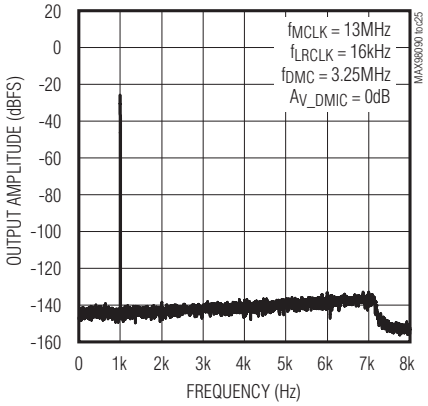


Typical Operating Characteristics (continued)

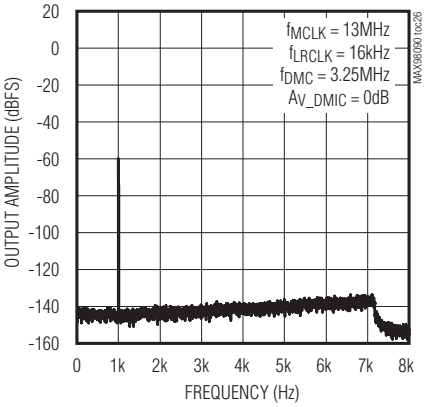
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DIGITAL MICROPHONE INPUT TO RECORD PATH OUTPUT (CONTINUED)

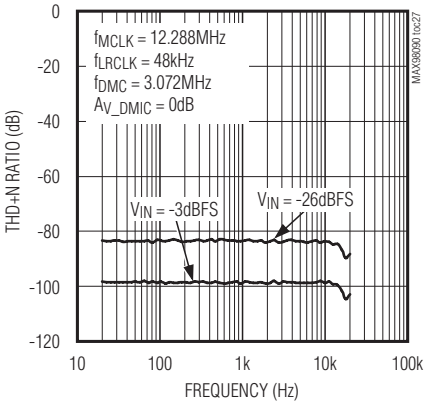
INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)



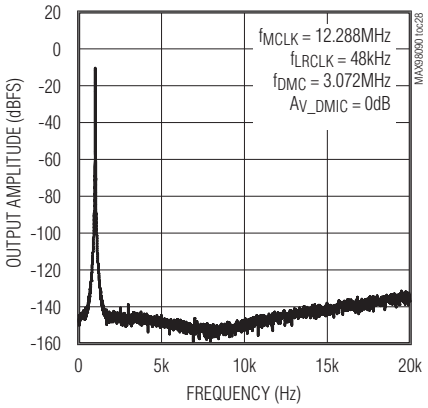
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)



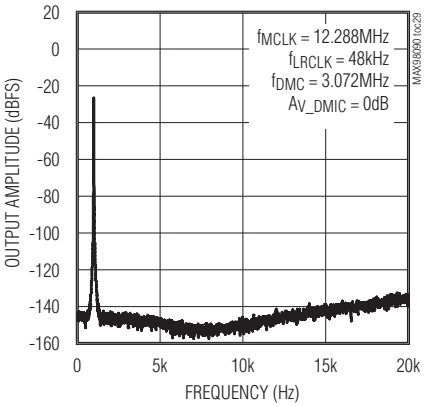
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)



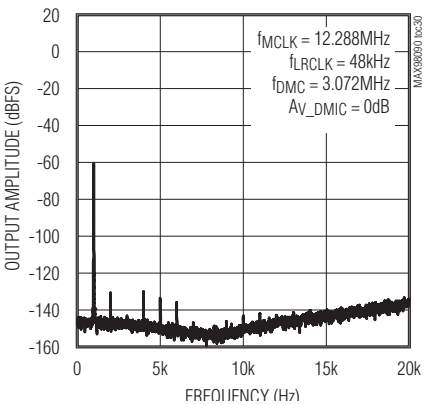
INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)



INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)

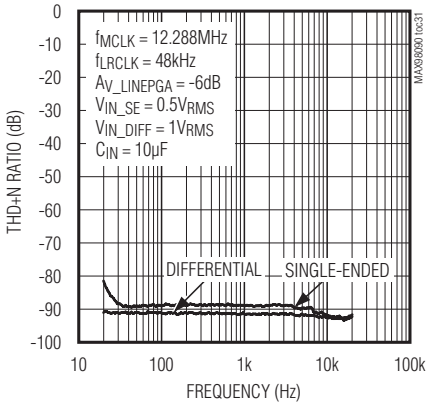


Typical Operating Characteristics (continued)

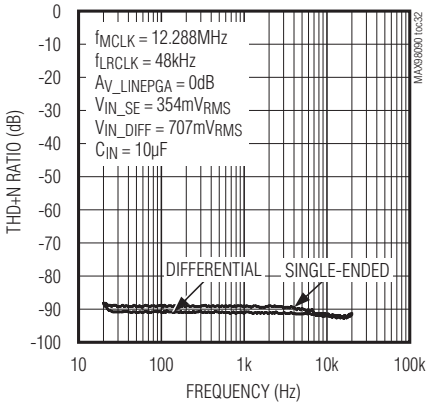
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO ADC RECORD PATH OUTPUT

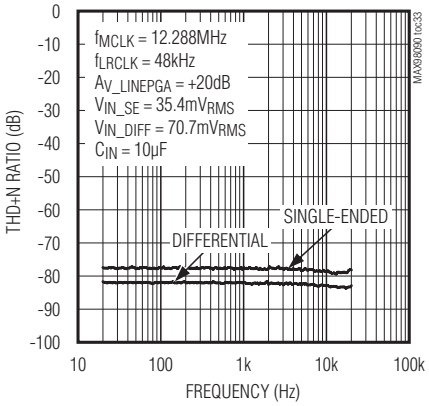
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



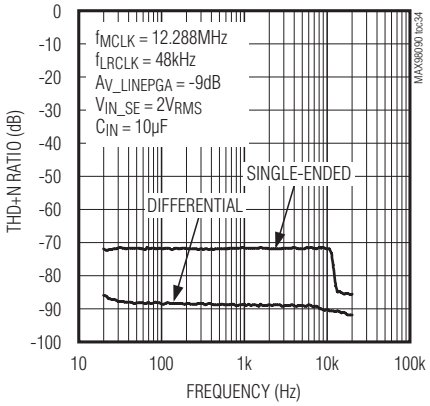
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



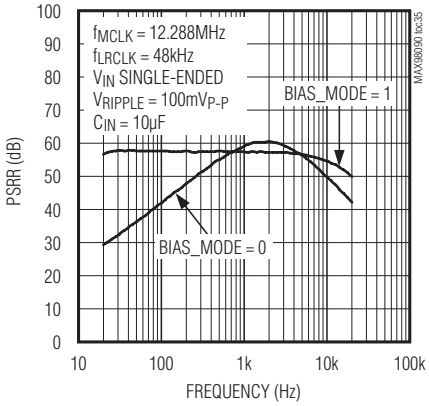
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



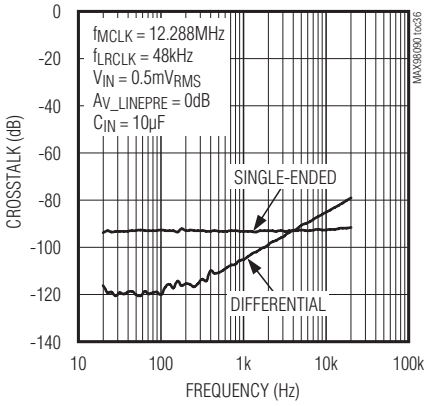
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC)



CROSSTALK vs. FREQUENCY (LINE TO ADC)

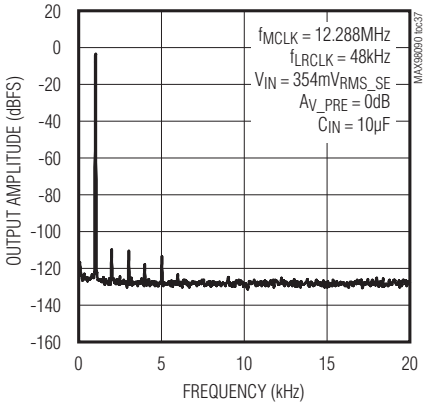


Typical Operating Characteristics (continued)

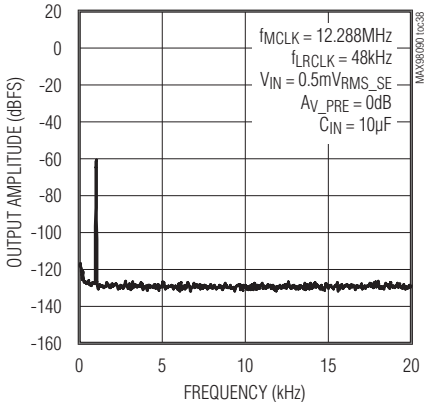
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

INBAND OUTPUT SPECTRUM vs. FREQUENCY,-3dBFS INPUT (LINE TO ADC)

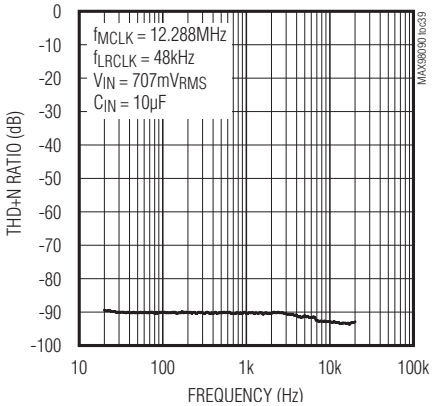


INBAND OUTPUT SPECTRUM vs. FREQUENCY, -60dBFS INPUT (LINE TO ADC)

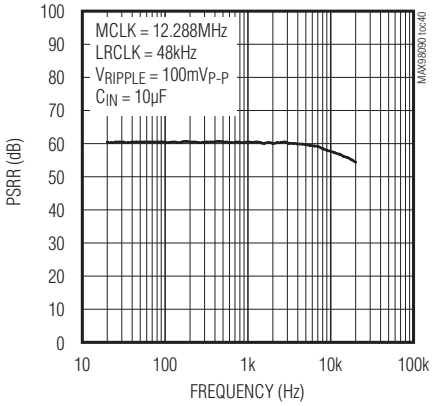


DIRECT ANALOG INPUT TO ADC RECORD PATH OUTPUT

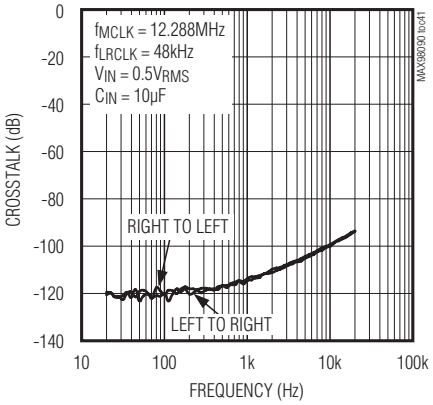
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)



CROSSTALK vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)

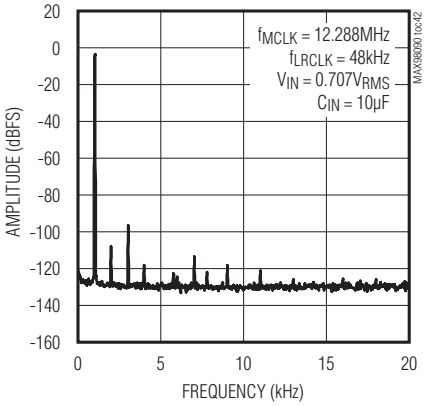


Typical Operating Characteristics (continued)

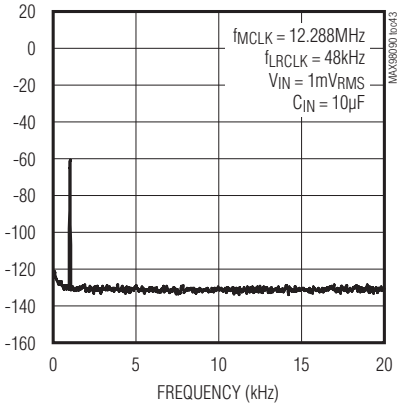
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DIRECT ANALOG INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

INBAND OUTPUT SPECTRUM, -3dBFS (INPUT DIRECT TO ADC MIXER)

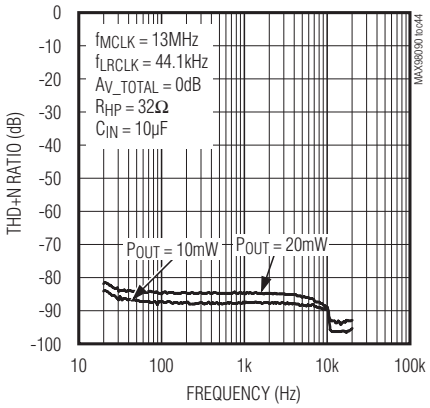


INBAND OUTPUT SPECTRUM, -60dBFS (INPUT DIRECT TO ADC MIXER)

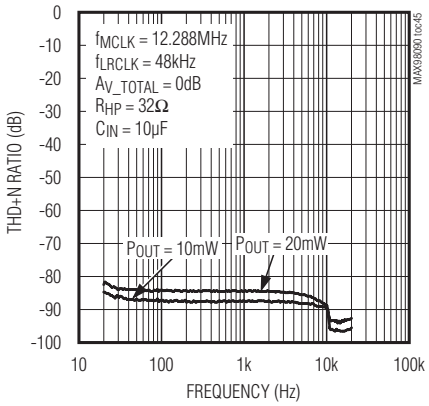


ADC RECORD PATH TO DAC PLAYBACK INTERNAL LOOP THROUGH

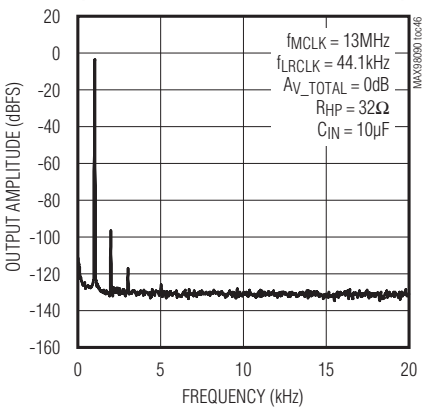
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)

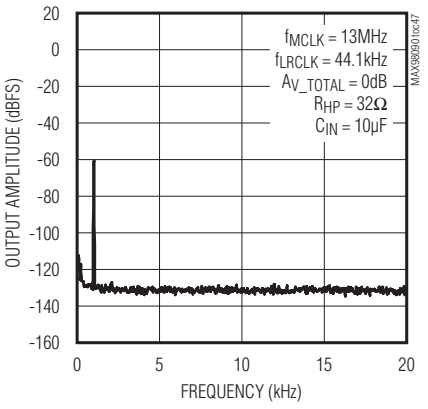


Typical Operating Characteristics (continued)

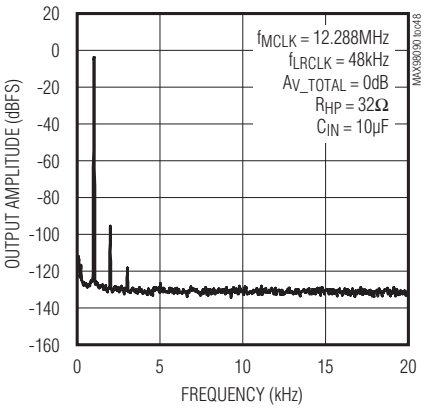
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

ADC RECORD PATH TO DAC PLAYBACK INTERNAL LOOP THROUGH (CONTINUED)

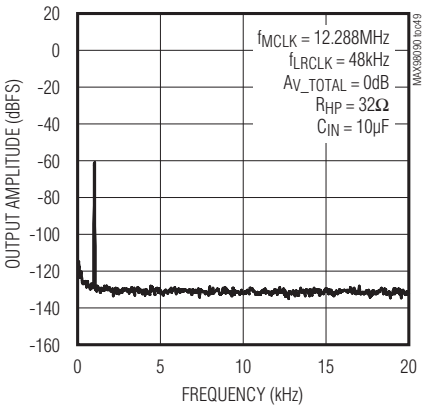
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)

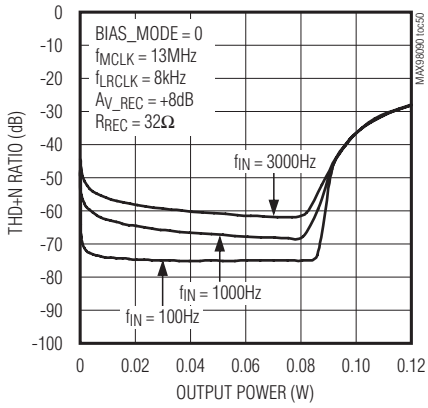


INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)

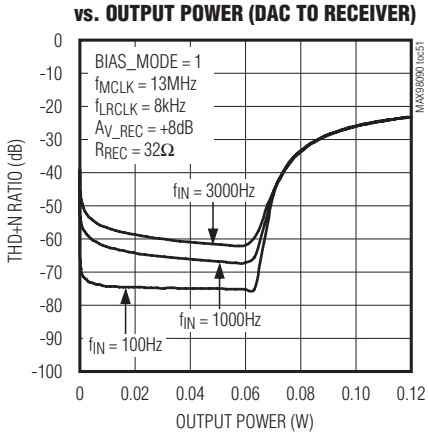


DAC PLAYBACK PATH INPUT TO RECEIVER OUTPUT

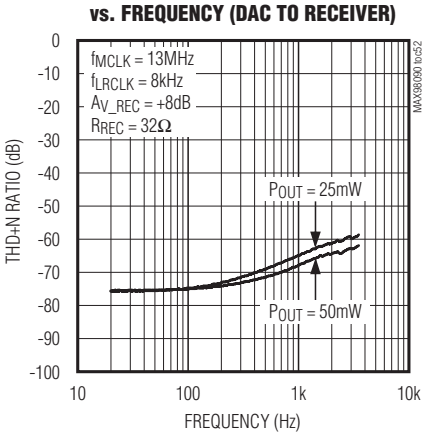
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO RECEIVER)



TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (DAC TO RECEIVER)



TOTAL HARMONIC DISTORTION vs. FREQUENCY (DAC TO RECEIVER)

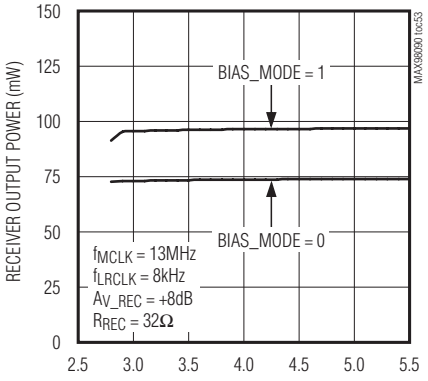


Typical Operating Characteristics (continued)

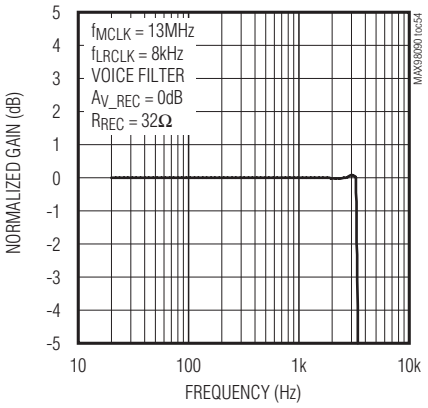
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO RECEIVER OUTPUT (CONTINUED)

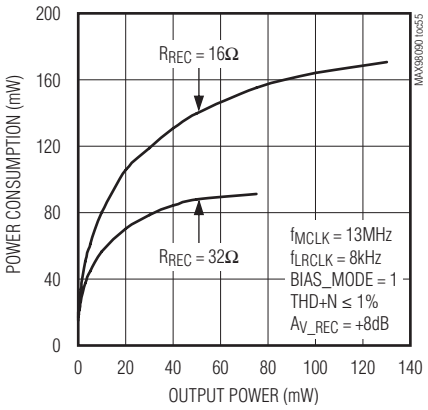
OUTPUT POWER vs. SPEAKER SUPPLY VOLTAGE (DAC TO RECEIVER)



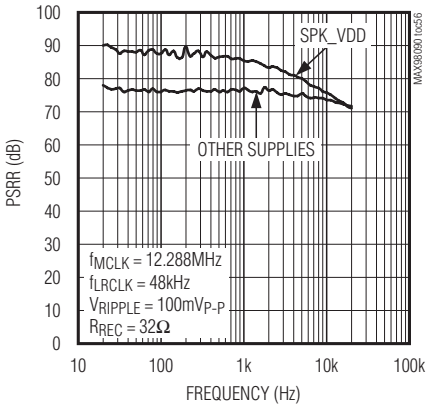
GAIN vs. FREQUENCY (DAC TO RECEIVER)



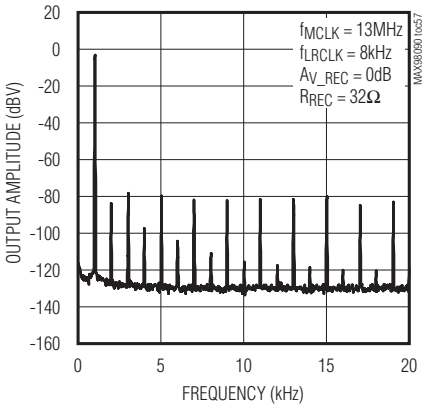
POWER CONSUMPTION vs. OUTPUT POWER (DAC TO RECEIVER)



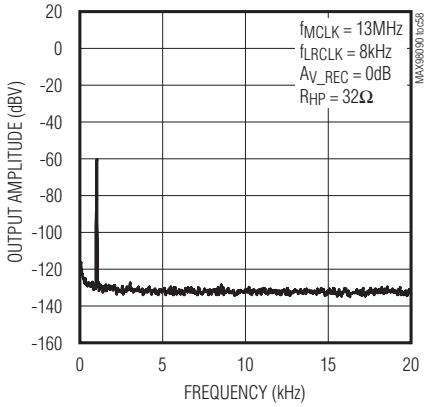
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO RECEIVER)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO RECEIVER)

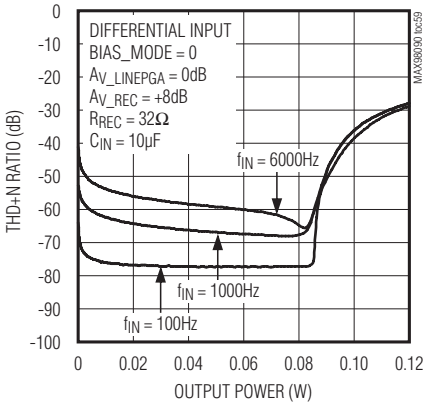


Typical Operating Characteristics (continued)

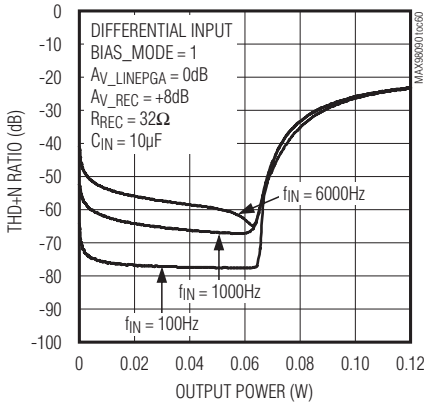
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO RECEIVER OUTPUT

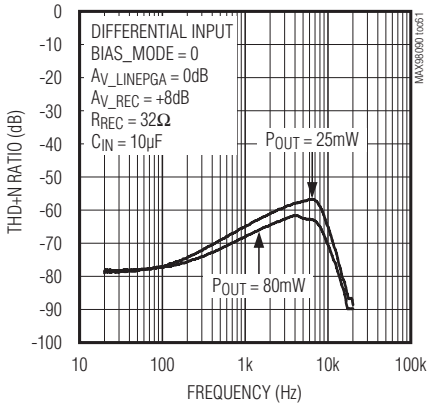
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)



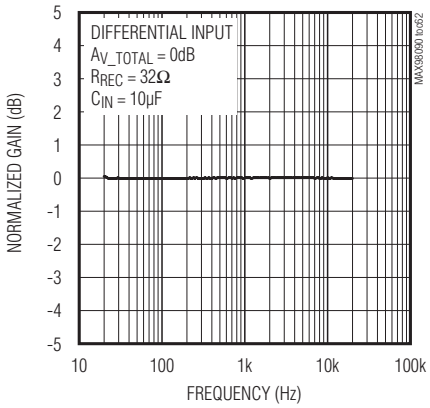
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)



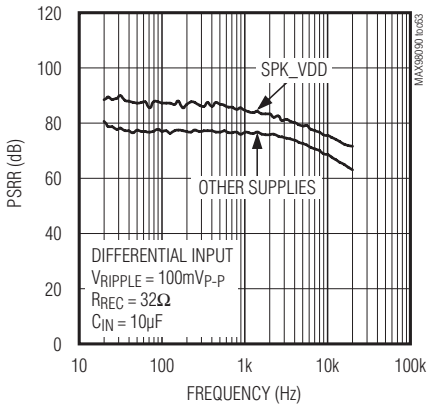
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO RECEIVER)



GAIN vs. FREQUENCY (LINE TO RECEIVER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO RECEIVER)

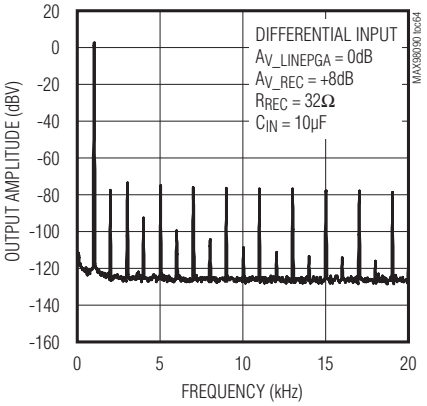


Typical Operating Characteristics (continued)

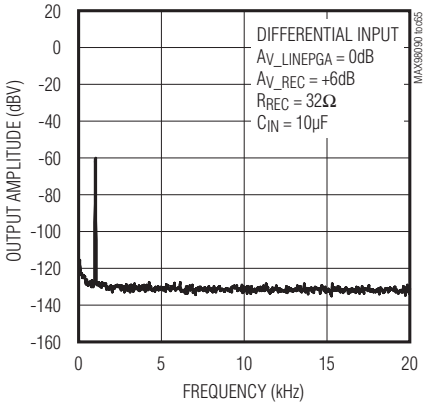
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO RECEIVER OUTPUT (CONTINUED)

INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE TO RECEIVER)

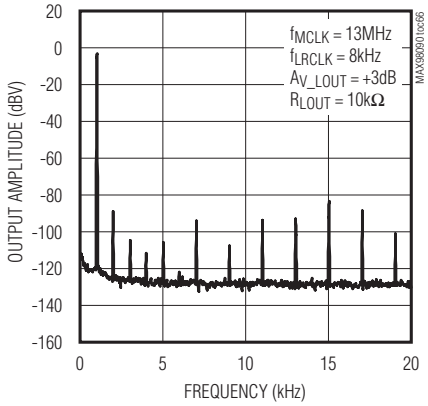


INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE TO RECEIVER)

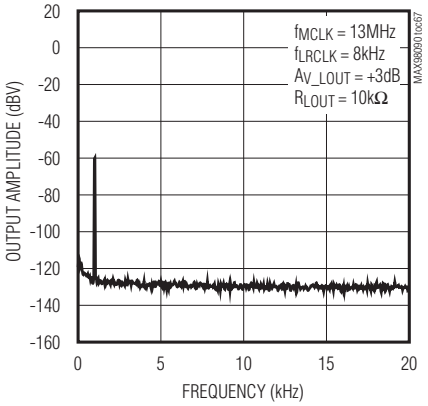


DAC PLAYBACK PATH INPUT TO LINE OUTPUT

INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO LINE OUT)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO LINE OUT)

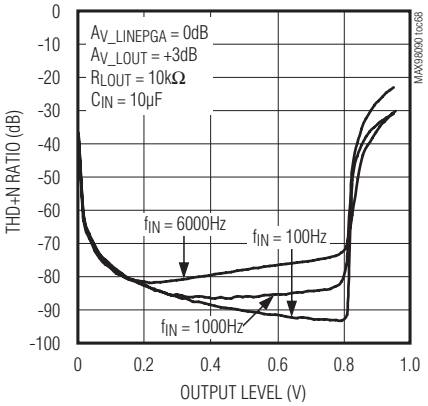


Typical Operating Characteristics (continued)

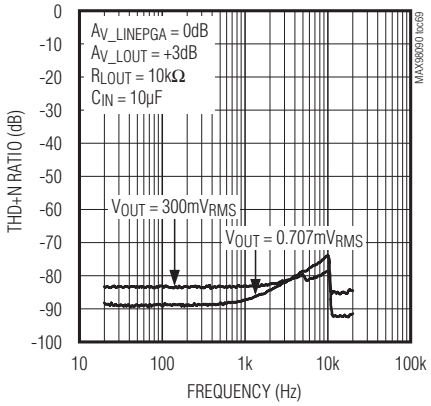
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO LINE OUTPUT

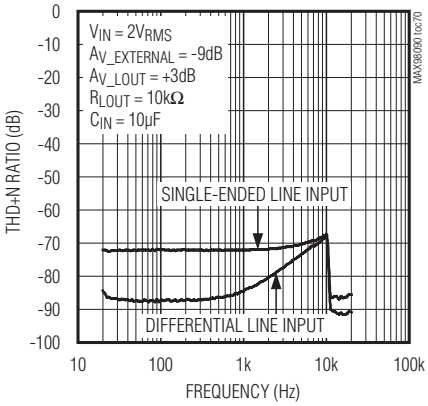
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL (LINE IN TO LINE OUT)



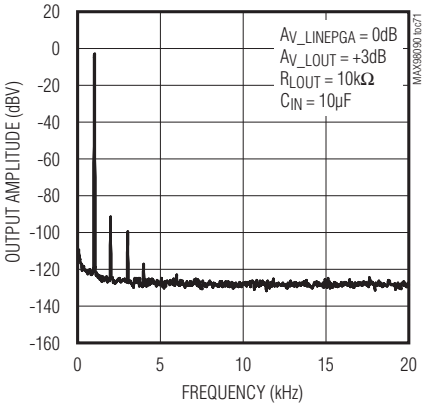
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)



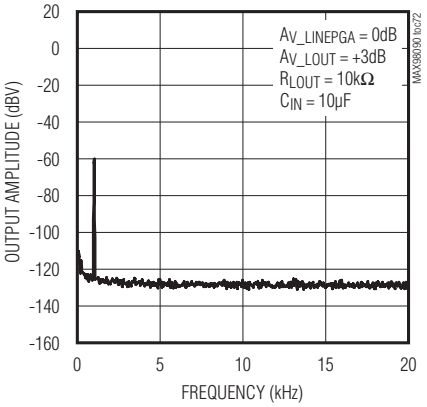
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)



INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE IN TO LINE OUT)



INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE IN TO LINE OUT)

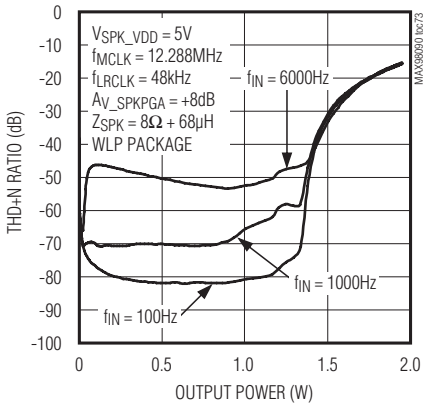


Typical Operating Characteristics (continued)

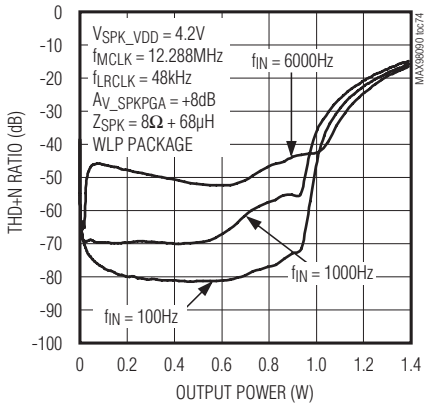
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT

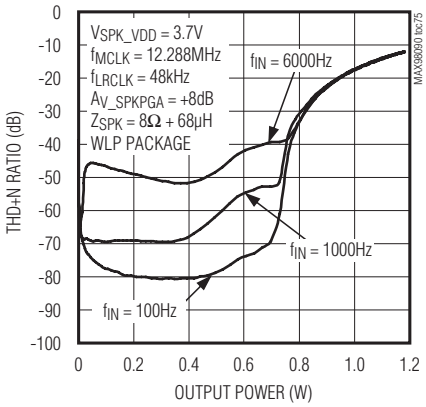
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



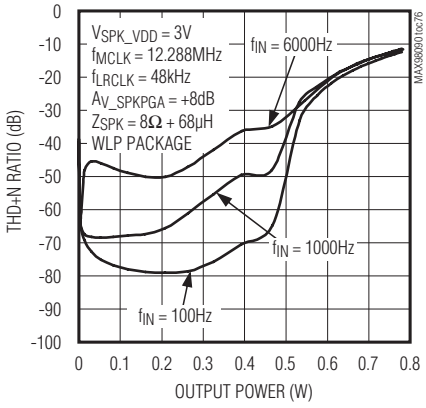
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



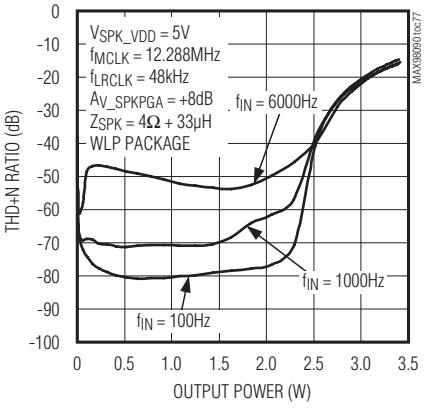
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



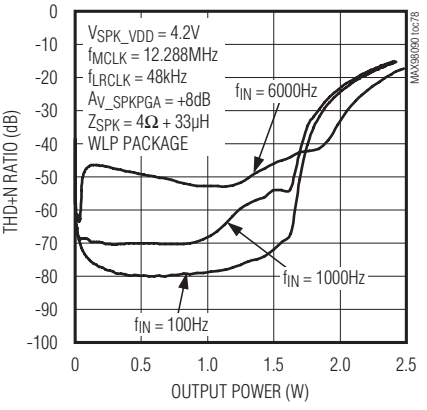
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)

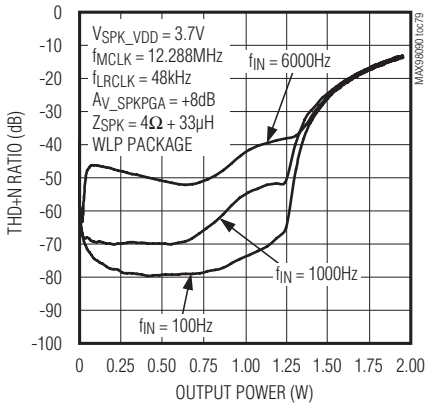


Typical Operating Characteristics (continued)

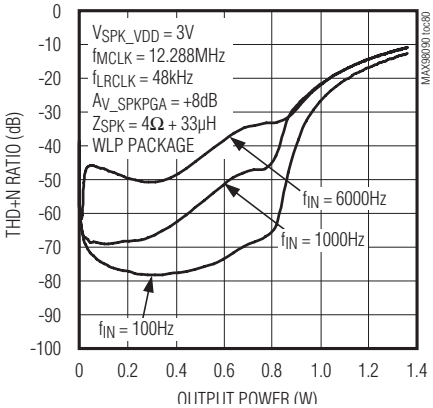
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

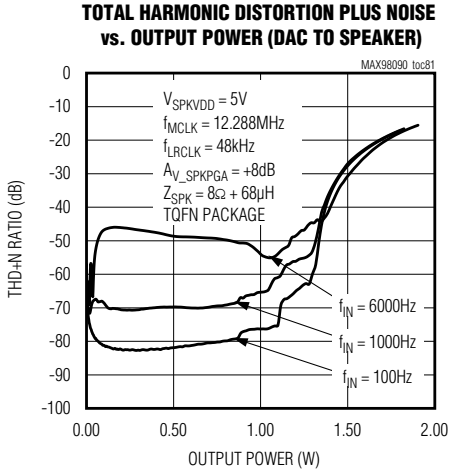
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



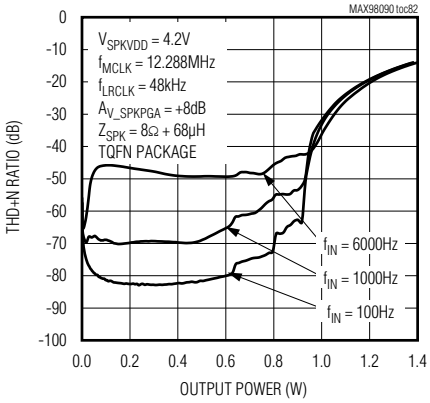
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



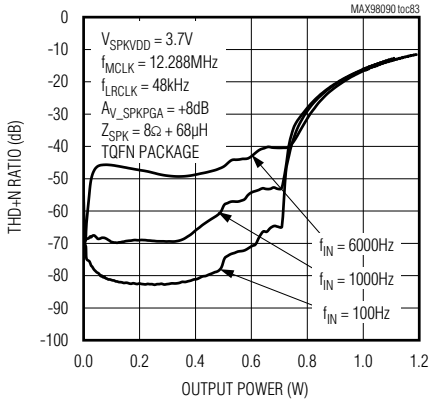
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



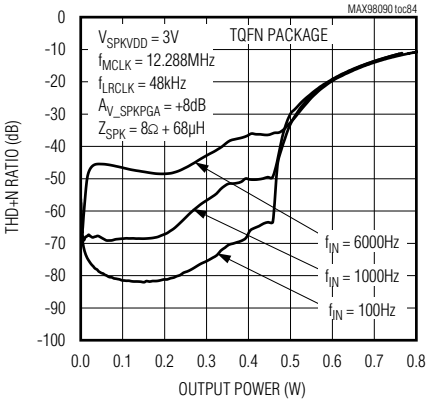
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)

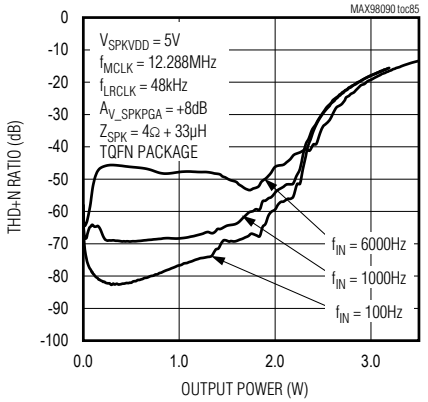


Typical Operating Characteristics (continued)

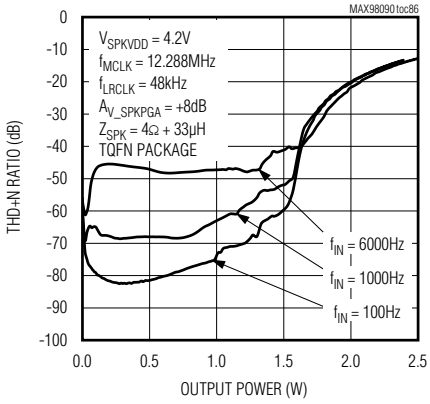
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

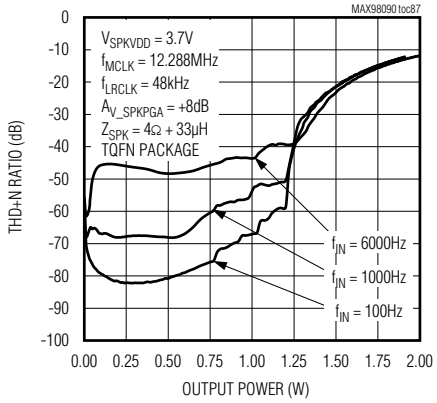
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



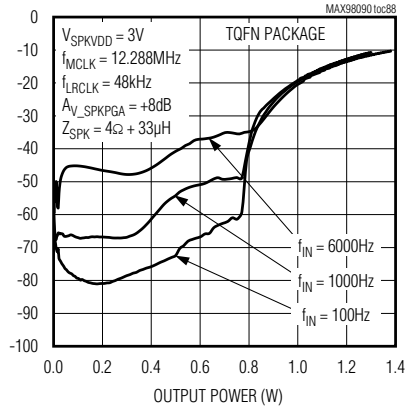
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



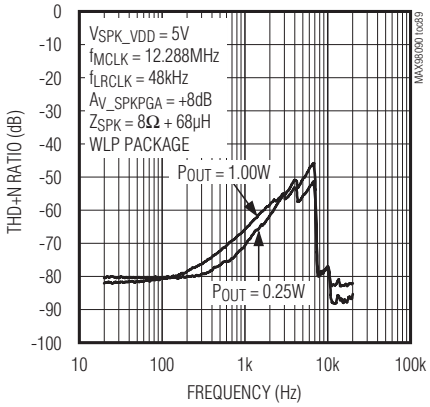
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



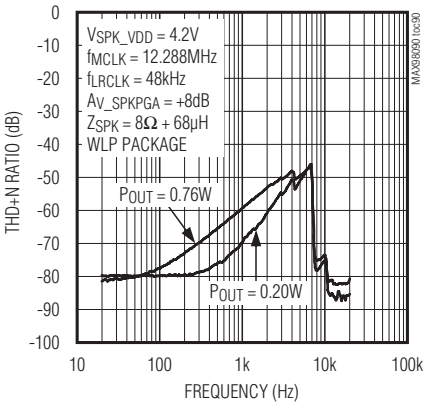
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)

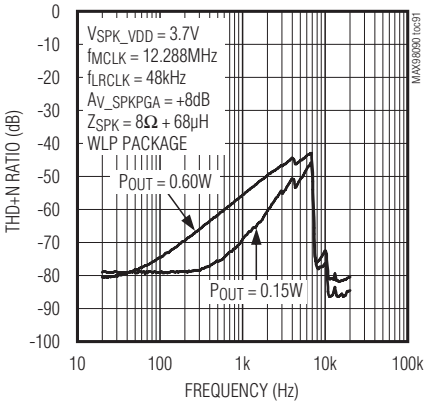


Typical Operating Characteristics (continued)

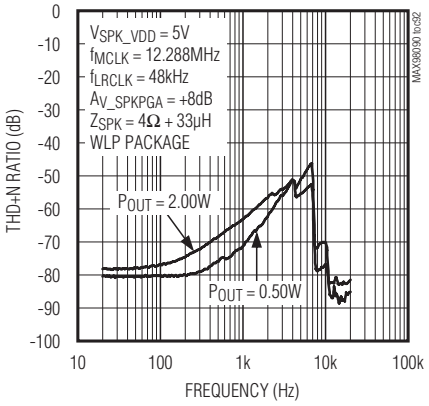
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

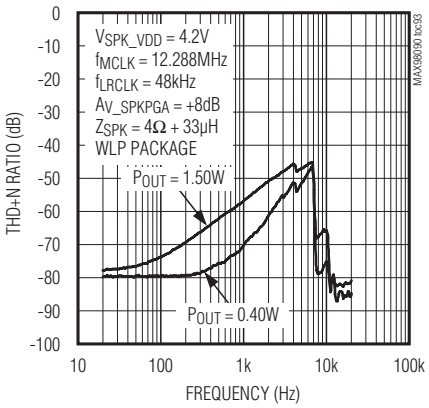
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



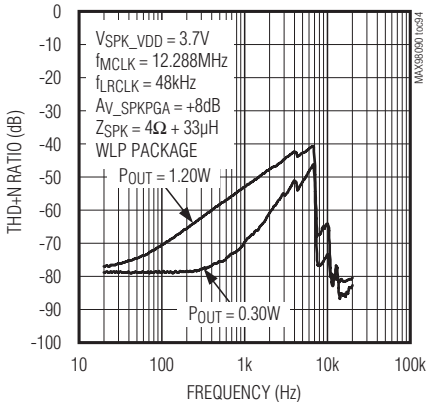
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



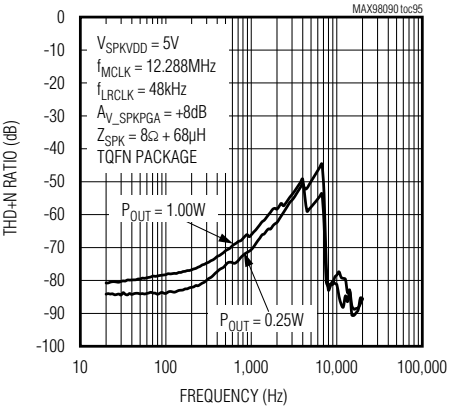
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



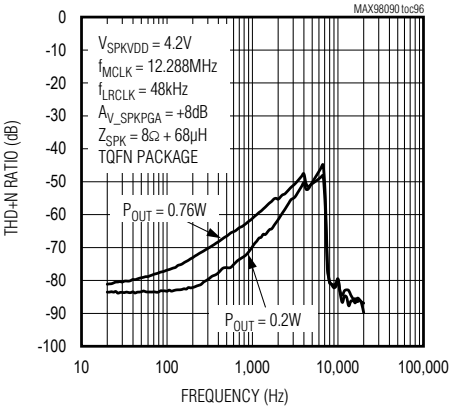
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)

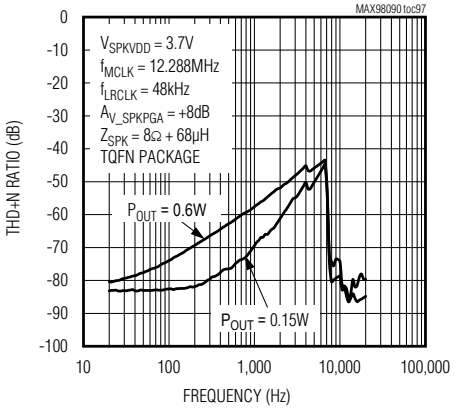


Typical Operating Characteristics (continued)

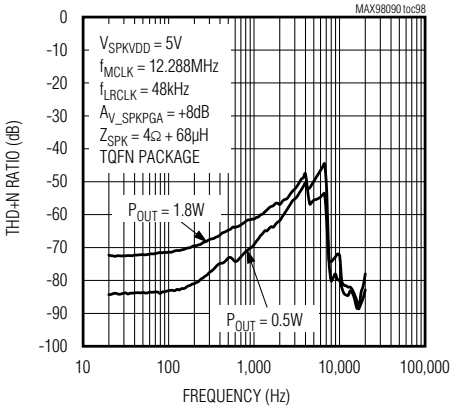
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

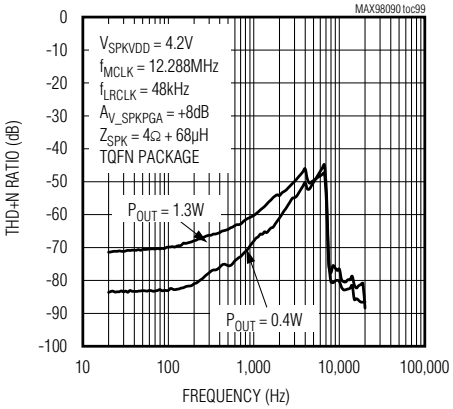
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



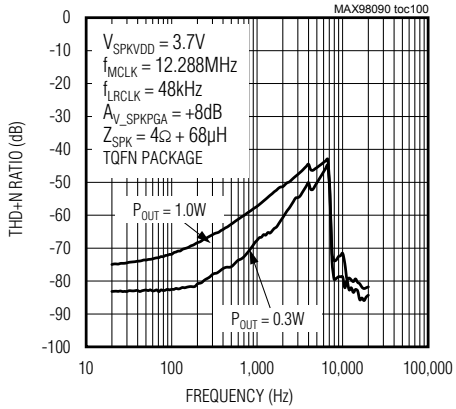
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



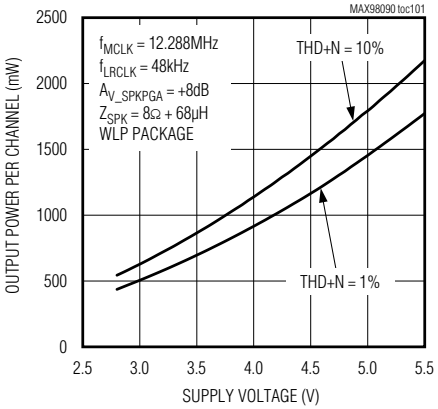
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



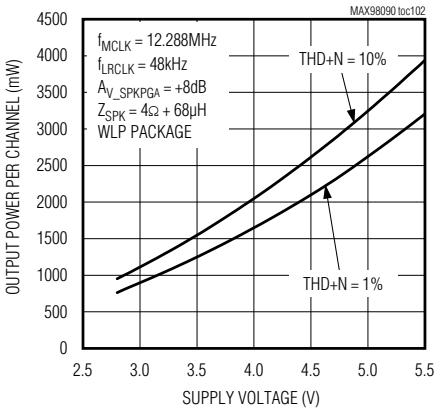
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)

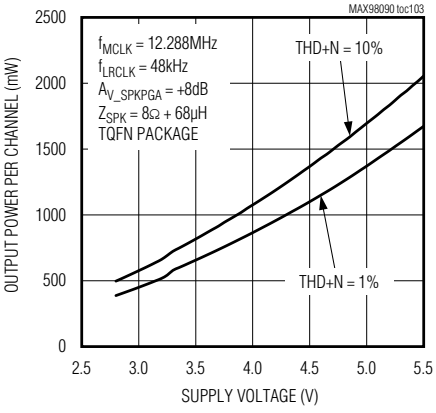


Typical Operating Characteristics (continued)

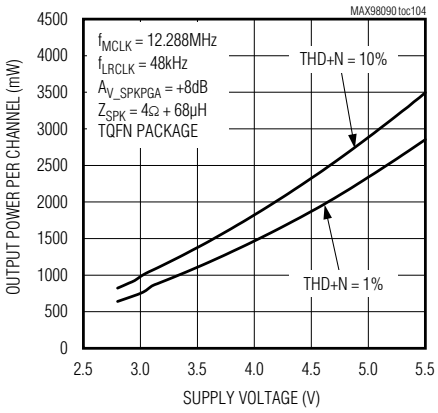
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

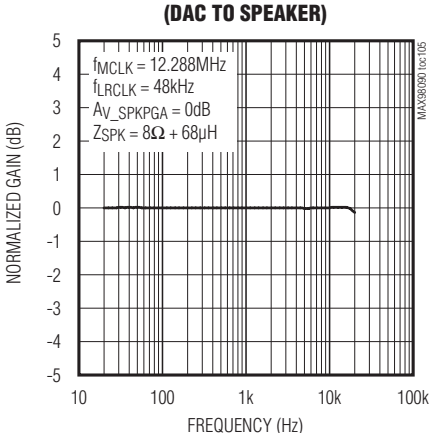
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



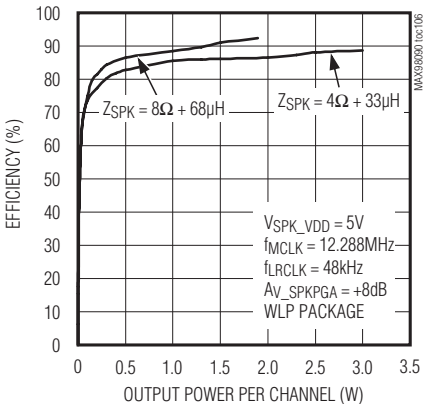
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



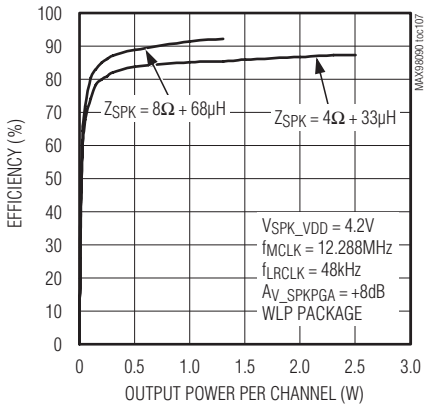
GAIN vs. FREQUENCY (DAC TO SPEAKER)



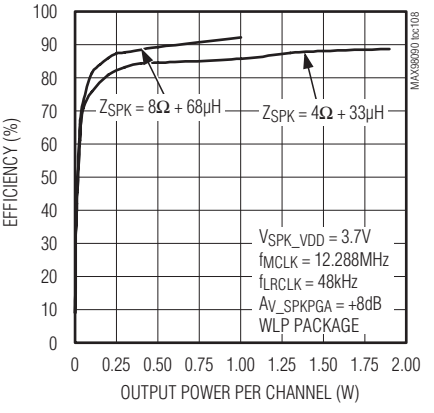
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)

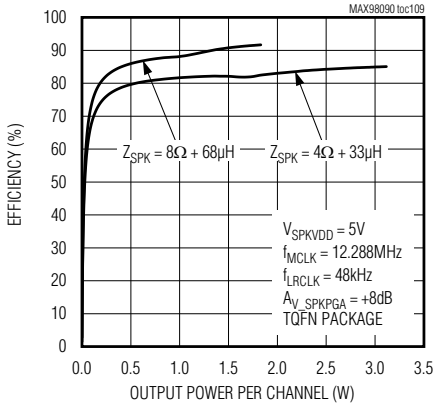


Typical Operating Characteristics (continued)

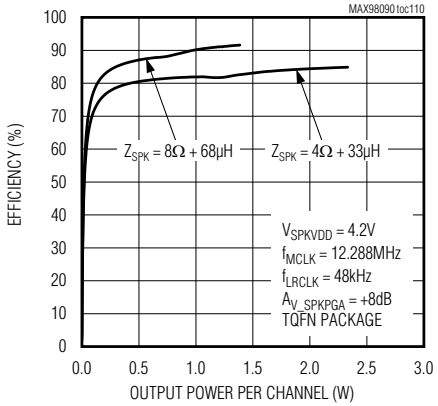
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

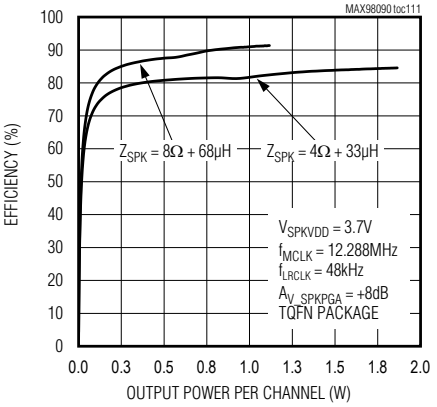
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



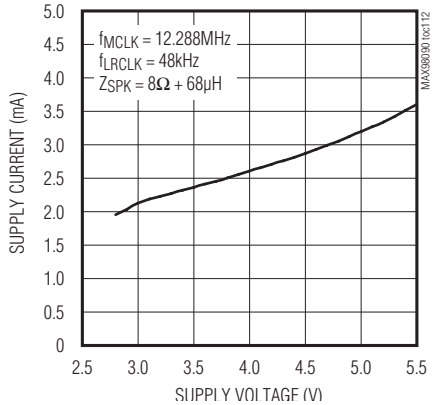
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



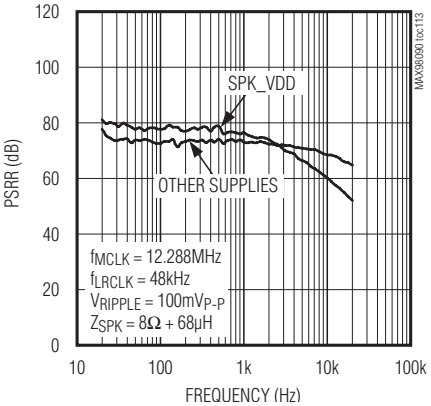
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



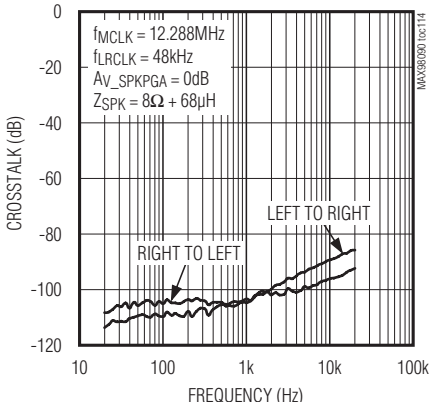
SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO SPEAKER)



CROSSTALK vs. FREQUENCY (DAC TO SPEAKER)

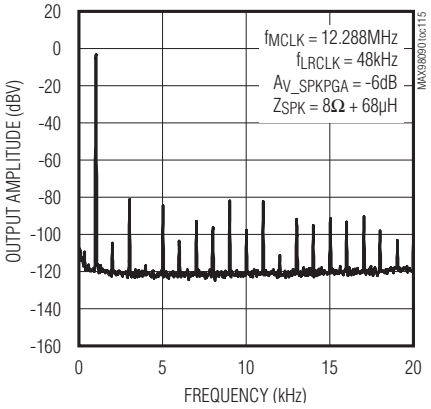


Typical Operating Characteristics (continued)

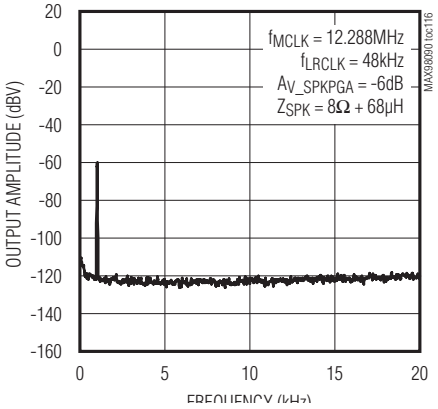
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

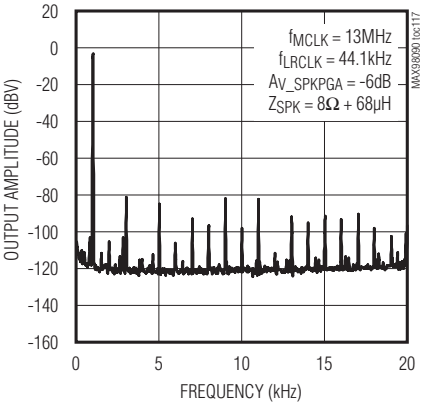
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)



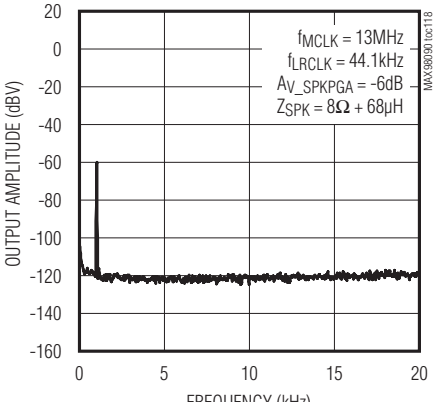
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)



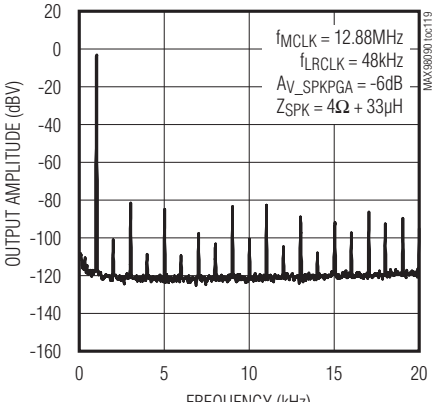
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)

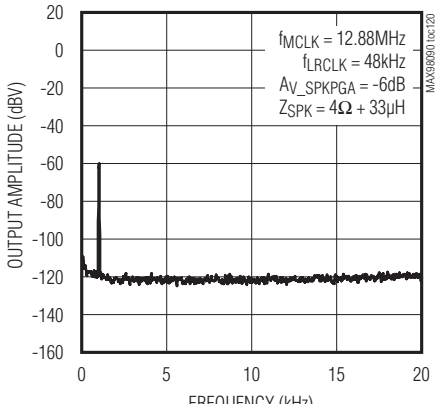


Typical Operating Characteristics (continued)

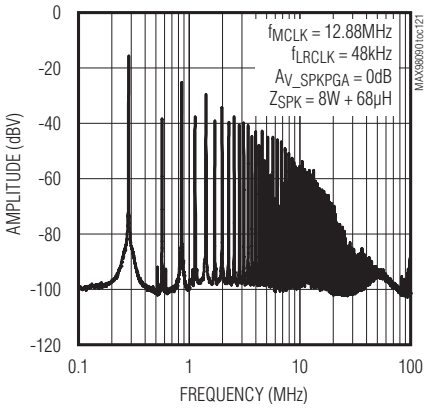
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)

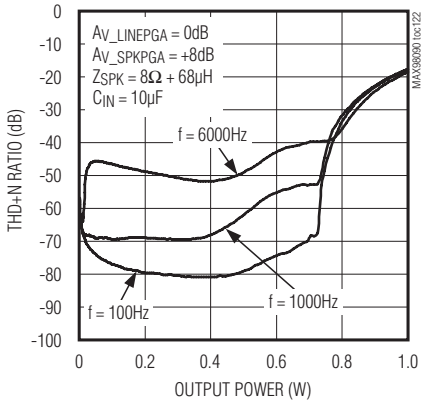


WIDEBAND FREQUENCY SPECTRUM (DAC TO SPEAKER)

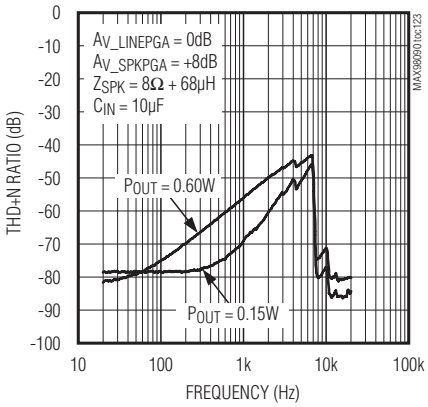


LINE INPUT TO SPEAKER OUTPUT

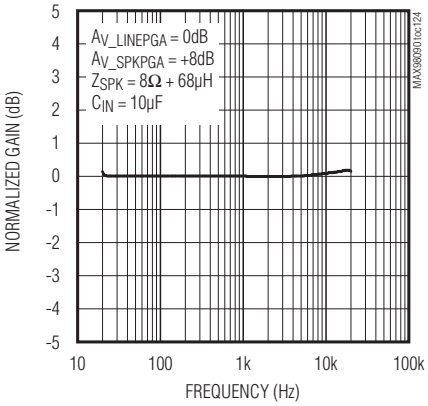
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)



GAIN vs. FREQUENCY (LINE TO SPEAKER)

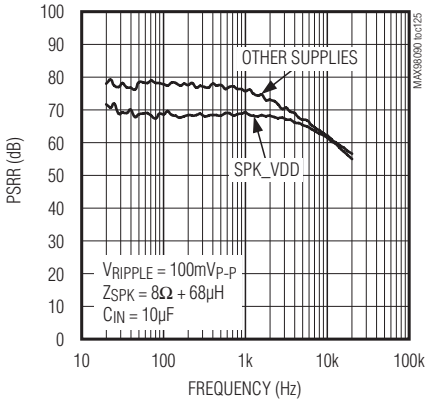


Typical Operating Characteristics (continued)

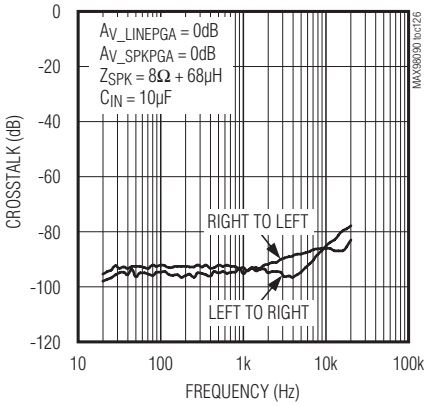
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO SPEAKER OUTPUT (CONTINUED)

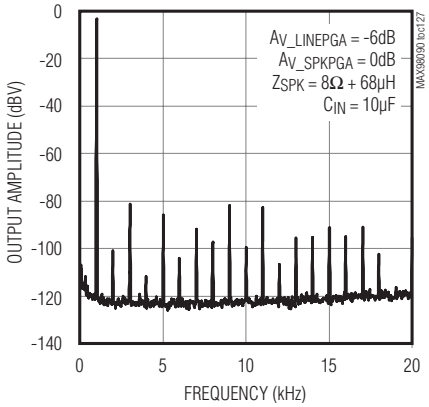
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO SPEAKER)



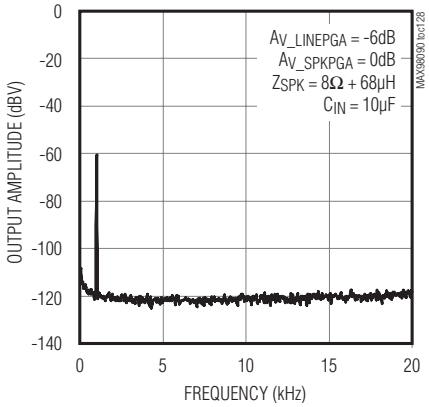
CROSSTALK vs. FREQUENCY (LINE TO SPEAKER)



INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE TO SPEAKER)



INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE TO SPEAKER)

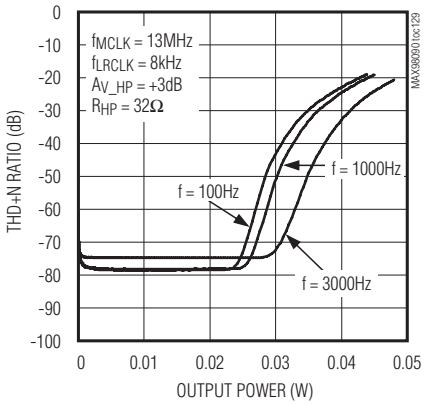


Typical Operating Characteristics (continued)

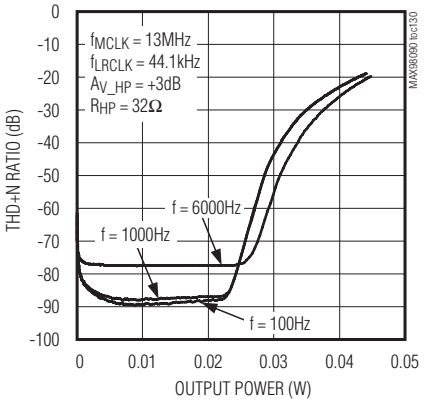
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT

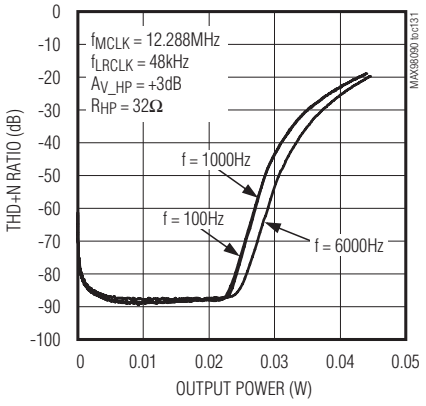
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



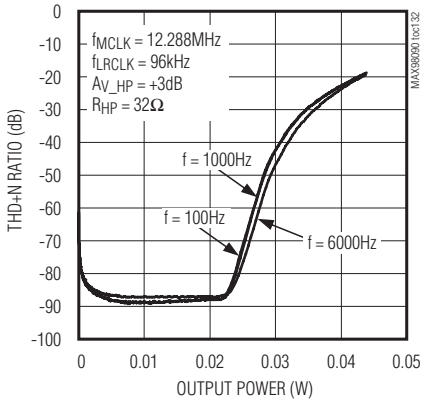
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



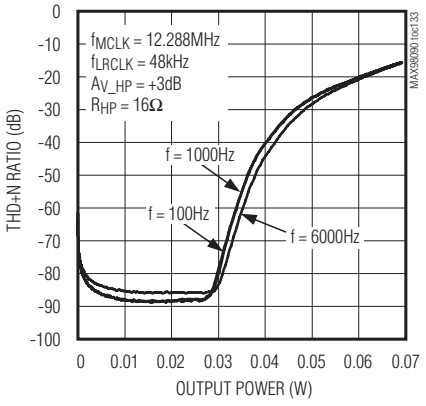
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



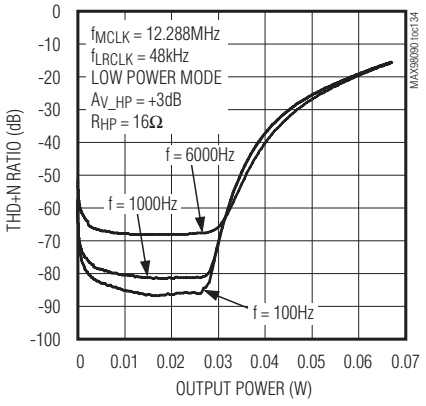
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)

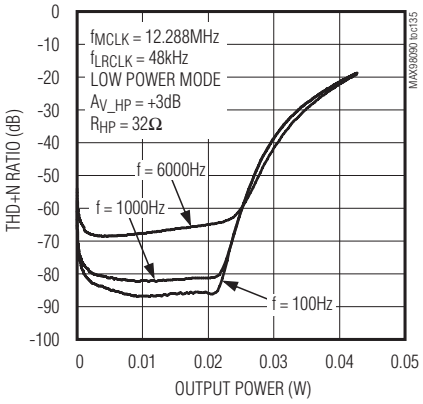


Typical Operating Characteristics (continued)

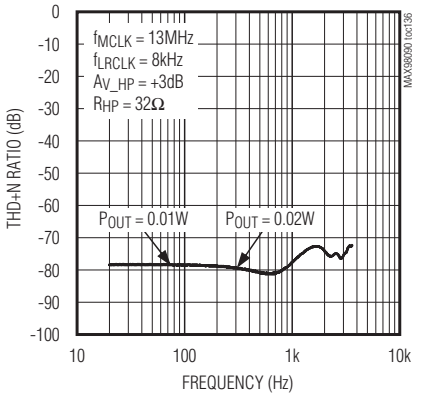
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

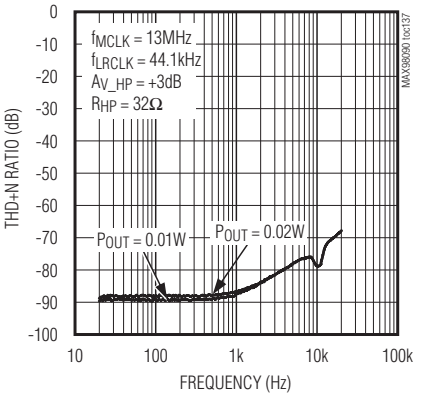
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



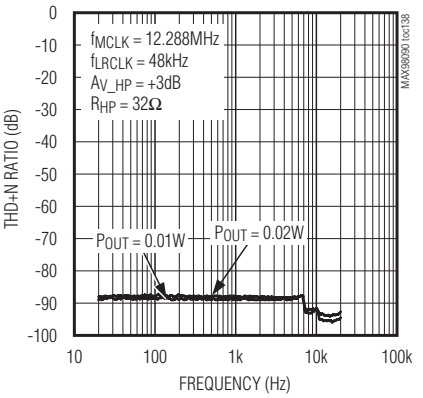
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



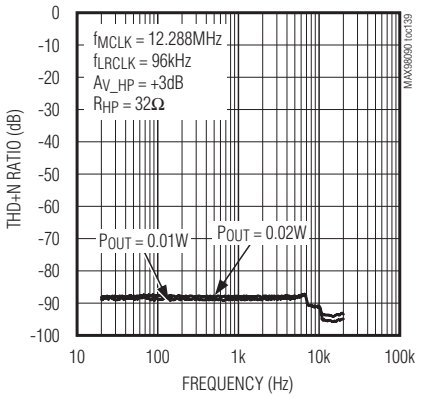
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



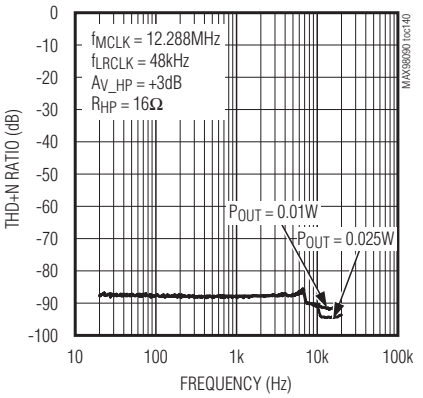
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)

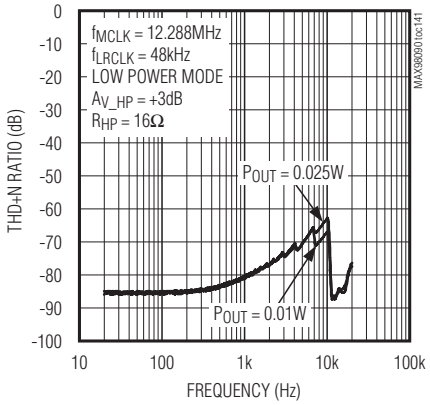


Typical Operating Characteristics (continued)

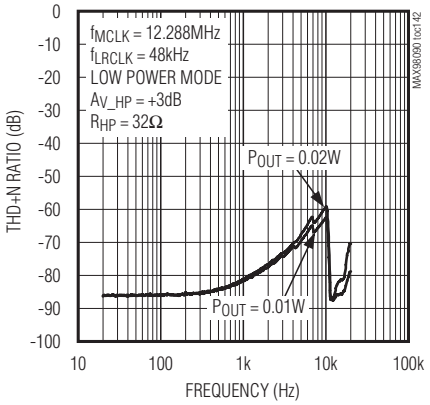
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

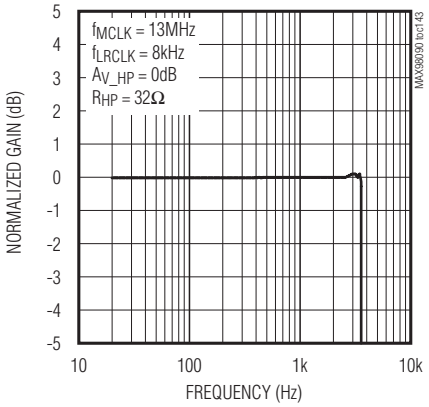
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



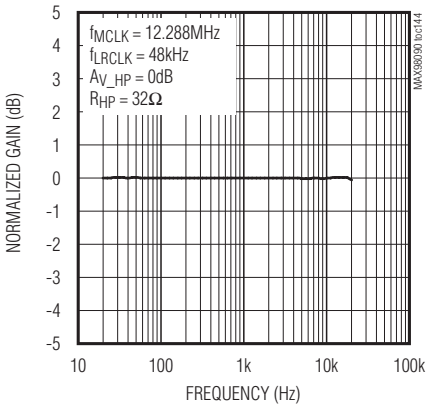
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



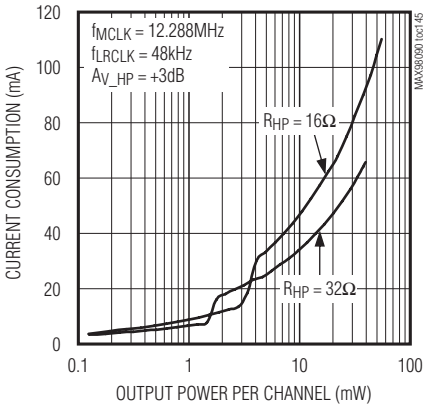
GAIN vs. FREQUENCY (DAC TO HEADPHONE)



GAIN vs. FREQUENCY (DAC TO HEADPHONE)



POWER CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)

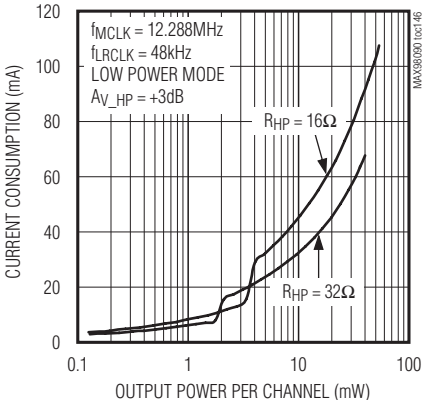


Typical Operating Characteristics (continued)

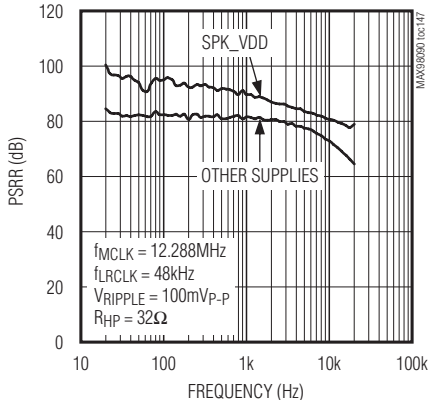
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

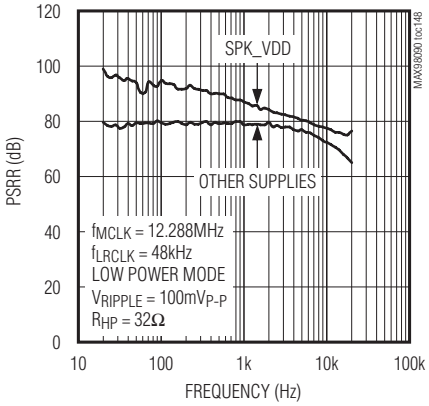
POWER CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)



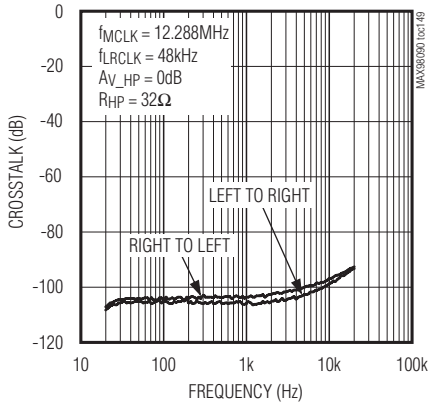
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



CROSSTALK vs. FREQUENCY (DAC TO HEADPHONE)

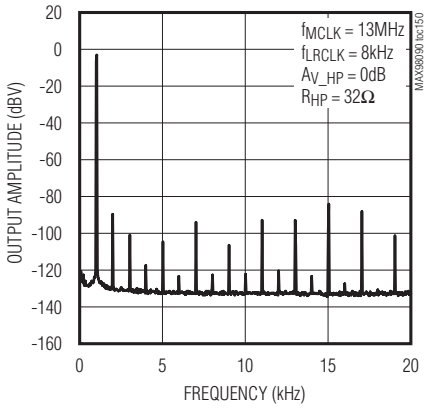


Typical Operating Characteristics (continued)

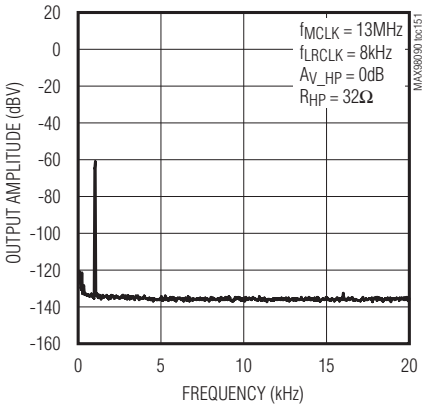
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

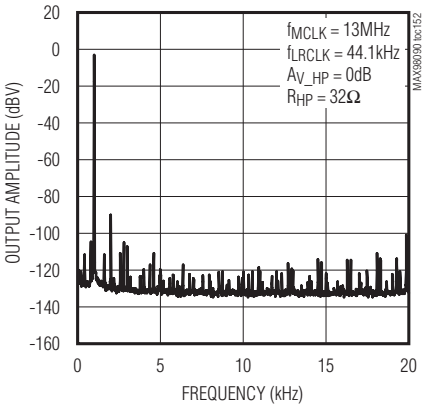
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)



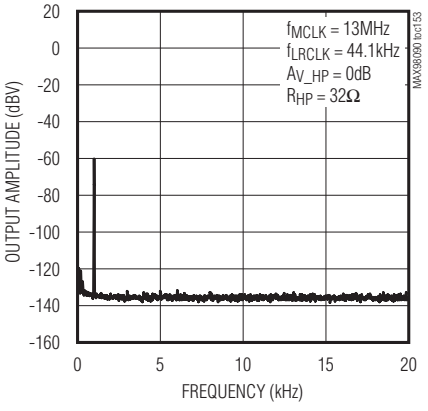
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)



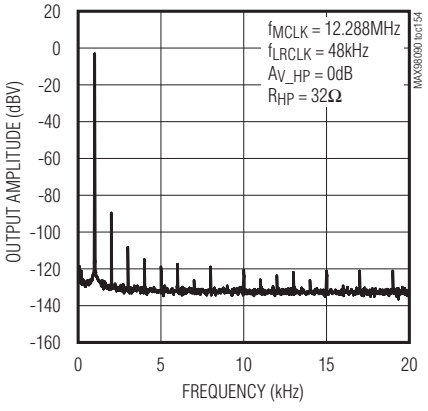
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)



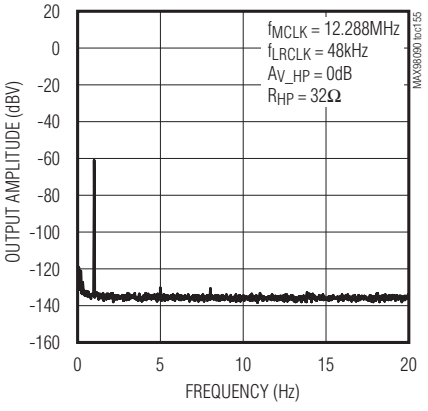
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)

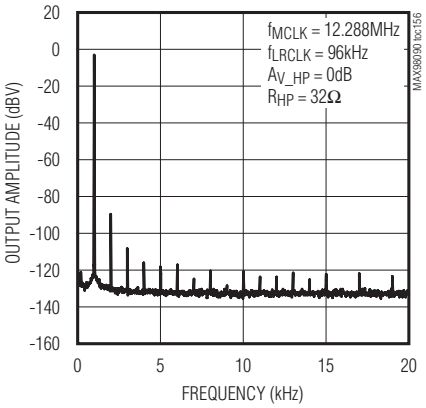


Typical Operating Characteristics (continued)

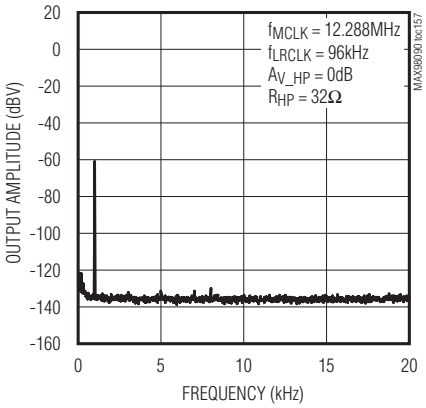
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

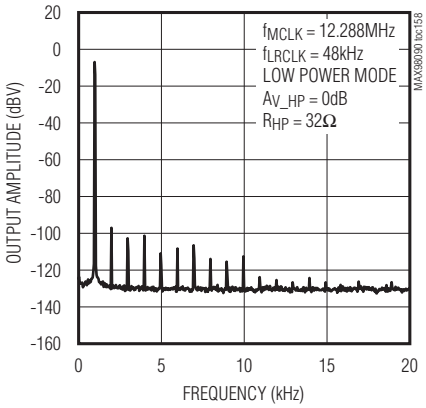
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)



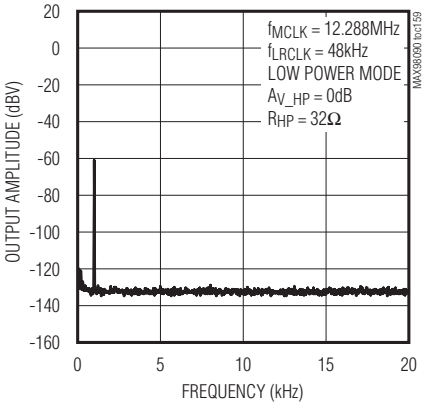
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)



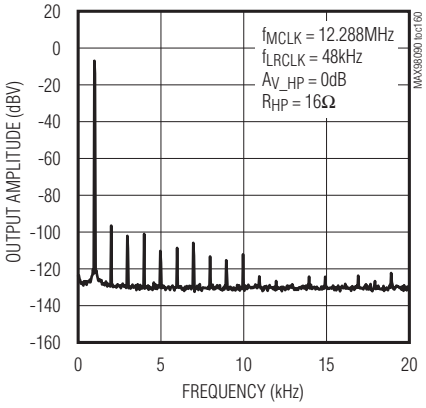
INBAND OUTPUT SPECTRUM, -6dBFS INPUT (DAC TO HEADPHONE)



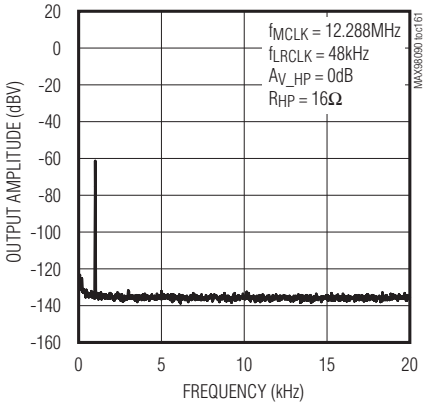
INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -6dBFS INPUT (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)

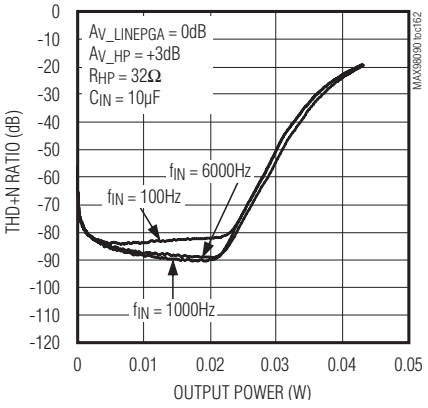


Typical Operating Characteristics (continued)

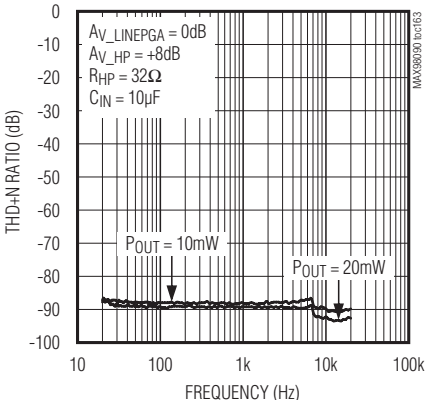
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO HEADPHONE OUTPUT

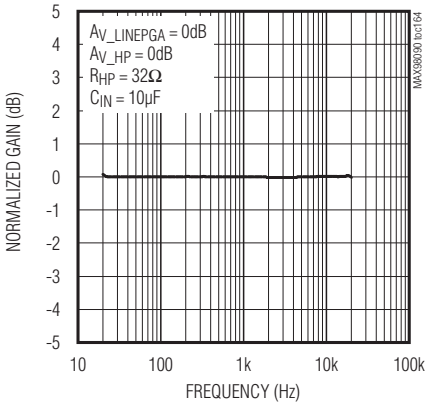
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO HEADPHONE)



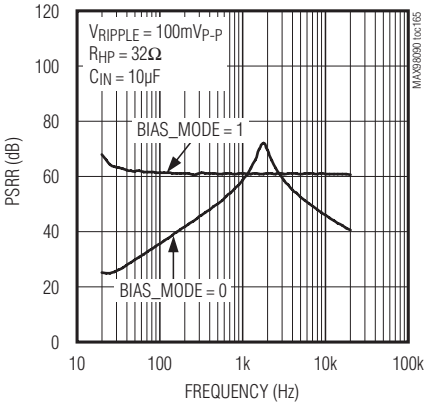
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO HEADPHONE)



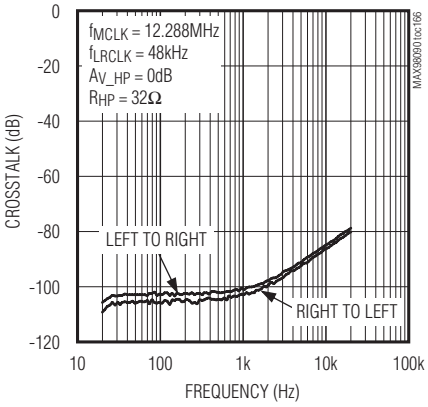
GAIN vs. FREQUENCY (LINE TO HEADPHONE)



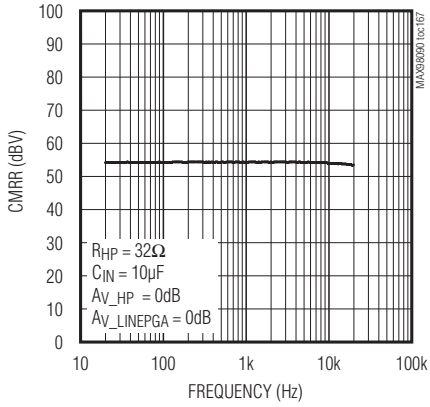
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)



CROSSTALK vs. FREQUENCY (LINE TO HEADPHONE)



COMMON-MODE REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)

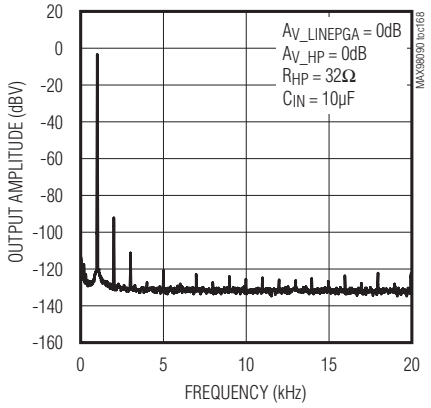


Typical Operating Characteristics (continued)

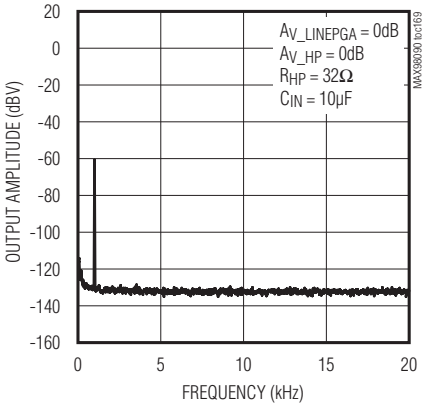
(V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = 1.8V, V_{DVDD} = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = V_{SPKVDD} = 3.7V. Receiver load (R_{RCV}) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads (R_{LOUT}) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. R_{RCV} = ∞, R_{LOUT} = ∞, R_{HP} = ∞, Z_{SPK} = ∞. C_{REF} = 2.2µF, C_{BIAS} = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = C_{CPVDD} = C_{CPVSS} = 1µF. $A_{V_MICPRE_}$ = $A_{V_MICPGA_}$ = $A_{V_LINEPGA_}$ = 0dB, A_{V_ADCLVL} = $A_{V_ADCGAIN}$ = 0dB, A_{V_DACLVL} = $A_{V_DACGAIN}$ = 0dB, $A_{V_MIXGAIN}$ = 0dB, A_{V_RCV} = A_{V_LOUT} = A_{V_HP} = A_{V_SPK} = 0dB. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, MAS = 0, 20-bit source data. T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

LINE INPUT TO HEADPHONE OUTPUT (CONTINUED)

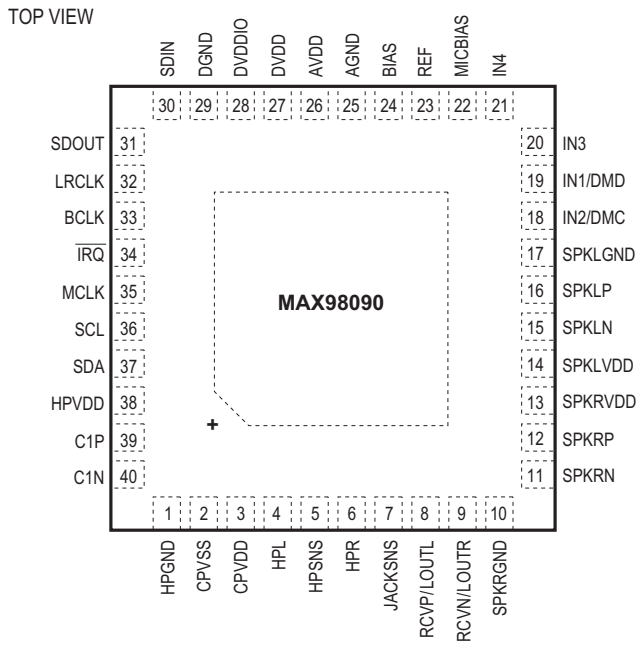
INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO HEADPHONE)

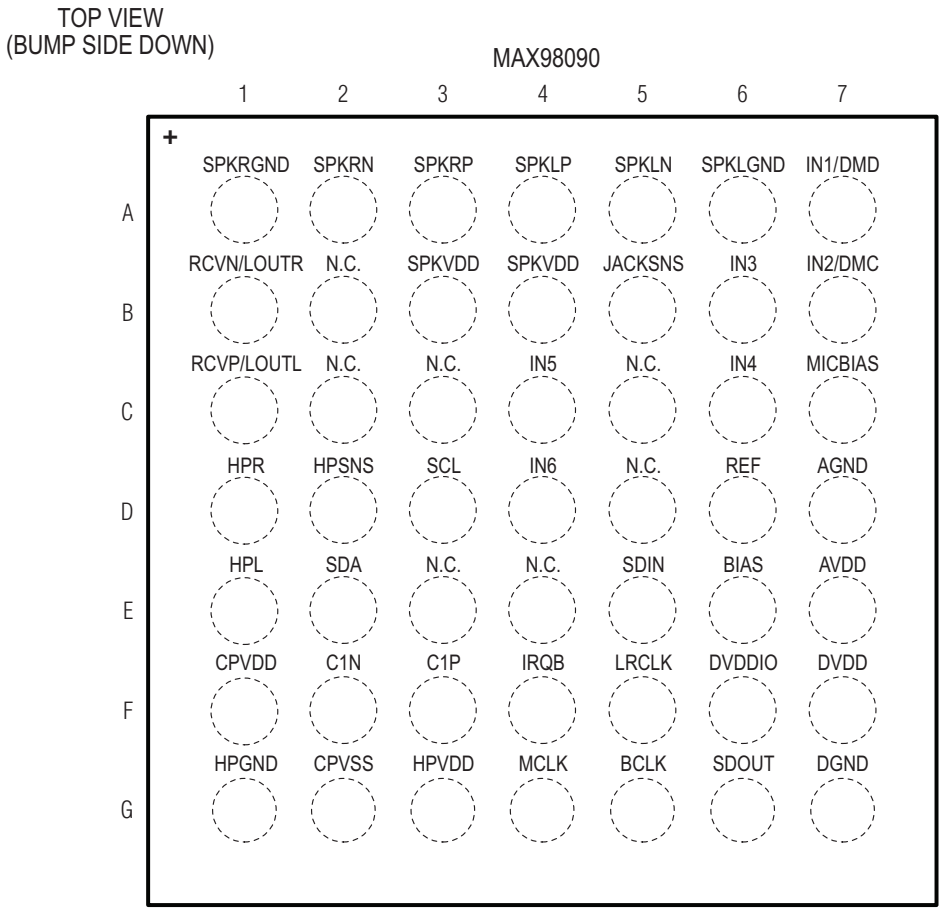


Bump/Pin Configurations



TQFN
(5mm x 5mm x 0.75mm)

Bump/Pin Configurations (continued)



WLP
(3.15mm x 3.15mm, 0.4 pitch)

Bump/Pin Descriptions

PIN	BUMP	MAX98090	FUNCTION
TQFN	WLP		
1	G1	HPGND	Headphone Ground
2	G2	CPVSS	Inverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
3	F1	CPVDD	Noninverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
4	E1	HPL	Left-Channel Headphone Output
5	D2	HPSNS	Headphone Amplifier Ground Sense. Connect to the headphone jack ground terminal or connect to ground.
6	D1	HPR	Right-Channel Headphone Output
7	B5	JACKSNS	Jack detection Input. Connect to the microphone terminal of the headset jack to detect jack activity.
8	C1	RCVP/LOUTL	Positive Earpiece Amplifier Output/Left Line Output
9	B1	RCVN/LOUTR	Negative Earpiece Amplifier Output/Right Line Output
10	A1	SPKRGND	Right Speaker Amplifier Ground
11	A2	SPKRN	Negative Right-Channel Class D Speaker Output
12	A3	SPKRP	Positive Right-Channel Class D Speaker Output
13	—	SPKRVDD	Right Speaker Power Supply. Bypass to SPKRGND with a 1µF capacitor and a single 10µF bulk capacitor shared with SPKLVDD.
14	—	SPKLVDD	Left Speaker and Microphone Bias Power Supply. Bypass to SPKLGND with a 1µF capacitor and a single 10µF bulk capacitor shared with SPKRVDD.
15	A5	SPKLN	Negative Left-Channel Class D Speaker Output
16	A4	SPKLP	Positive Left-Channel Class D Speaker Output
17	A6	SPKLGND	Left Speaker Amplifier Ground.
18	B7	IN2/DMC	Negative Differential Microphone 1 Input or single-ended Line Input 2. AC-couple with a series 1µF capacitor. Can be retasked as a digital microphone clock output.
19	A7	IN1/DMD	Positive Differential Microphone 1 Input or single-ended Line Input 1. AC-couple with a series 1µF capacitor. Can be retasked as a digital microphone data input.
20	B6	IN3	Positive Differential Microphone 2 Input or single-ended Line Input 3. AC-couple with a series 1µF capacitor.
21	C6	IN4	Negative Differential Microphone 2 Input or single-ended Line input 4. AC-couple with a series 1µF capacitor.
22	C7	MICBIAS	Low-Noise Microphone Bias Voltage Output. Bypass to SPKLGND with a 1µF capacitor. The bias voltage is programmable. An external resistor in the 2.2kΩ to 1kΩ range should be used to set the microphone current.
23	D6	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor.
24	E6	BIAS	Common-Mode Reference Voltage. Bypass to AGND with a 1µF capacitor.
25	D7	AGND	Analog Ground.
26	E7	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
27	F7	DVDD	Digital Power Supply. Bypass to DGND with a 1µF capacitor.
28	F6	DVDDIO	Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.

Bump/Pin Descriptions (continued)

PIN	BUMP	MAX98090	FUNCTION
TQFN	WLP		
29	G7	DGND	Digital Ground
30	E5	SDIN	Digital Audio Serial Data Playback Input. The input voltage is referenced to DVDDIO.
31	G6	SDOUT	Digital Audio Serial Data Record Output. The output voltage is referenced to DVDDIO.
32	F5	LRCLK	Digital Audio Left-Right Clock Input/Output. LRCLK is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLK is a frame sync pulse. LRCLK is an input when the device is in slave mode and an output when in master mode. The input voltage is referenced to DVDDIO.
33	G5	BCLK	Digital Audio Bit Clock Input/Output. BCLK is an input when the device is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDIO.
34	F4	IRQ	Active-Low Hardware Interrupt Output. Connect a 10kΩ pullup resistor to V_{DD}.
35	G4	MCLK	Master Clock Input. Acceptable input frequency range is either 256 x f_S or from 10MHz to 60MHz.
36	D3	SCL	I^2C Serial Clock Input. Connect a pullup resistor to DVDD for full output swing.
37	E2	SDA	I^2C Serial Data Input/Output. Connect a pullup resistor to DVDD for full output swing.
38	G3	HPVDD	Headphone Power Supply. Bypass to HPGND with a 10µF bulk capacitor with a parallel 0.1µF capacitor as close as possible to the device.
39	F3	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
40	F2	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
—	B3, B4	SPKVDD	Speaker and Microphone Bias Power Supply. Bypass each bump to SPK_GND with a 1µF capacitor with a single shared 10µF bulk capacitor.
—	C4	IN5	Auxiliary Positive Differential Microphone Input or Single-Ended Line Input. AC-couple with a series 1µF capacitor.
—	D4	IN6	Auxiliary Negative Differential Microphone Input or Single-Ended Line Input. AC-couple with a series 1µF capacitor.
—	B2, C2, C3, C5, D5, E3, E4	N.C.	Not Connected Internally

Detailed Description

The MAX98090 is a fully integrated stereo audio codec with FlexSound audio processing and integrated input and output audio amplifiers.

The device features either six (WLP package) or four (TQFN package) flexible analog inputs. Each pair can be configured as a differential analog microphone input, a stereo single ended or differential line input(s), or as a reduced power, direct differential analog input to the ADC mixer. One input pair, IN1/IN2, can also be retasked to support two digital microphones. As a result, two microphones (either analog or digital) can be recorded from simultaneously. The input analog signals can be amplified by up to 50dB, and then are either recorded by the stereo ADC or routed directly to the analog output mixers for playback.

The ADC supports sample rates between 8kHz and 96kHz, features two performance modes, and provides two oversampling rate options. The ADC to DAI digital record path features both voice (IIR) and Music (FIR) filtering, an optional DC-blocking highpass filter, a fully configurable biquad filter, and a -12dB to +45dB range of programmable digital gain and level control.

The digital audio interface (DAI) can simultaneously transmit and receive separate and distinct stereo audio signals. The DAI supports a wide range of PCM digital audio formats including I^2S, left justified (LJ), right justified (RJ), and four slot TDM.

As with the record path, the DAI to DAC playback path supports sample rates from 8kHz to 96kHz, both voice (IIR) and music (FIR) filtering (high stop band attenuation at $f_S/2$), optional DC blocking filters, and a -15dB to +18dB range of programmable digital gain and level control. In addition, the playback path also features a 7-band parametric biquad equalizer, dynamic range control (DRC), and a summing digital sidetone from the record path DSP. The device includes three analog output drivers. The first is a Class AB differential receiver/earpiece amplifier. Alternatively, the receiver amplifier can also be configured as a stereo single-ended line output driver.

The second is an integrated, filterless, Class D stereo speaker amplifier. This amplifier provides efficient amplification for two speakers, and includes active emissions limiting to minimize the radiated emissions (EMI) traditionally associated with Class D. The right channel features a slave mode, in which the switching is synchronized to that of the left channel to eliminate the beat tone that can occur with asynchronous operation. In most systems with short speaker traces, no Class D output filtering is required.

The third is a Class H, ground referenced stereo headphone amplifier featuring Maxim's second generation DirectDrive architecture. The Class H headphone amplifier features an internal charge pump that generates both a positive and negative supply for the headphone amplifier. This provides a ground referenced output signal that eliminates the need for either DC-blocking capacitors or a midrail bias for the headphone jack ground return. The headphone dedicated ground sense current return reduces crosstalk and output noise. A tracking circuit monitors the signal level and automatically selects the appropriate switching frequency and supply voltage level. For low signal levels, the charge pump switches at a reduced frequency and outputs $\pm V_{HPVDD}/2$ for improved efficiency. When the signal amplitude increases, the charge-pump switching frequency also increases, and continues to output $\pm V_{HPVDD}/2$. For high signal levels, the charge pump outputs full-scale rails at $\pm V_{HPVDD}$ to maximize output power.

The device also includes several additional features such as a programmable external microphone bias, configurable jack detection and identification, extensive click-and-pop reduction circuitry, power and performance management settings, and a full range of quick configuration options.

Device I^2C Register Map

Table 1 lists all of the registers, their addresses, and power-on-reset (PoR) states. Registers 0x01, 0x02, and 0xFF are read only. Registers 0x01, 0x02, and 0xFF are read only. Registers 0x06 to 0x0B (quick setup) are write only (push button). All of the remaining registers are read/write. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted.

Table 1. MAX98090 Control Register Map

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
RESET/STATUS/INTERRUPT REGISTERS											
0x00	SOFTWARE RESET	W	SWRESET	—	—	—	—	—	—	—	0x00
0x01	DEVICE STATUS	CoR	CLD	SLD	ULK	—	—	JDET	DRCACT	DRCCLP	0x00
0x02	JACK STATUS	R	—	—	—	—	—	LSNS	JKSNS	—	0x00
0x03	INTERUPT MASKS	R/W	ICLD	ISLD	IULK	—	—	IJDET	IDRCACT	IDRCCLP	0x04
QUICK SETUP REGISTERS											
0x04	SYSTEM CLOCK	W	26M	19P2M	13M	12P288M	12M	11P2896M	—	$256F_S$	0x00
0x05	SAMPLE RATE	W	—	—	SR_96K	SR_32K	SR_48K	SR_44K1	SR_16K	SR_8K	0x00
0x06	DAI INTERFACE	W	—	—	RJ_M	RJ_S	LJ_M	LJ_S	I2S_M	I2S_S	0x00
0x07	DAC PATH	W	DIG2_HP	DIG2_ EAR	DIG2_ SPK	DIG2_ LOUT	—	—	—	—	0x00
0x08	MIC/DIRECT TO ADC	W	IN12_MIC1	IN34_ MIC2	—	—	IN12_ DADC	IN34_ DADC	***IN56_ DADC***	—	0x00
0x09	LINE TO ADC	W	IN12S_AB	IN34S_AB	***IN56S_AB***	IN34D_A	***IN65D_B***	—	—	—	0x00
0x0A	ANALOG MIC LOOP	W	IN12_ M1HPL	IN12_ M1SPKL	IN12_ M1EAR	IN12_ M1LOUTL	IN34_ M2HPR	IN34_ M2SPKR	IN34_ M2EAR	IN34_ M2LOUTR	0x00
0x0B	ANALOG LINE LOOP	W	IN12S_ ABHP	IN34D_ ASPKL	IN34D_ AEAR	IN12S_ ABLOUT	IN34S_ ABHP	***IN65D _BSPKR***	***IN65D_ BEAR***	IN34S_ ABLOUT	0x00
RESERVED REGISTER											
0x0C	RESERVED	—	—	—	—	—	—	—	—	—	0x00
ANALOG INPUT CONFIGURATION REGISTERS											
0x0D	LINE INPUT CONFIG.	R/W	IN34DIFF	***IN65DIFF***	IN1SEEN	IN2SEEN	IN3SEEN	IN4SEEN	***IN5SEEN***	***IN6SEEN***	0x00
0x0E	LINE INPUT LEVEL	R/W	MIXG135	MIXG246	LINAPGA[2:0]			LINBPGA[2:0]			0x1B
0x0F	INPUT MODE	R/W	EXTBUFA	EXTBUFB	—	—	—	—	***EXT_MIC[1:0]***		0x00
0x10	MIC1 INPUT LEVEL	R/W	—	PA1EN[1:0]	PGAM1[4:0]						0x14
0x11	MIC2 INPUT LEVEL	R/W	—	PA2EN[1:0]	PGAM2[4:0]						0x14
MICROPHONE CONFIGURATION REGISTERS											
0x12	MIC BIAS VOLTAGE	R/W	—	—	—	—	—	—	MBVSEL[1:0]		0x00
0x13	DIGITAL MIC ENABLE	R/W	—	MICCLK[2:0]			—	—	DIGMICR	DIGMICL	0x00
0x14	DIGITAL MIC CONFIG.	R/W	DMIC_COMP[3:0]				—	—	DMIC_FREQ[1:0]		0x00

Note: *Register bits in* ***bold italics*** *are for the WLP package only.*

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
ADC PATH AND CONFIGURATION REGISTERS											
0x15	LEFT ADC MIXER	R/W	—	MIXADL[6:0]							0x00
0x16	RIGHT ADC MIXER	R/W	—	MIXADR[6:0]							0x00
0x17	LEFT RECORD LEVEL	R/W	—	AVLG[2:0]			AVL[3:0]				0x03
0x18	RIGHT RECORD LEVEL	R/W	—	AVRG[2:0]			AVR[3:0]				0x03
0x19	RECORD BIQUAD LEVEL	R/W	—	—	—	—	AVBQ[3:0]				0x00
0x1A	RECORD SIDETONE	R/W	DSTS[1:0]		—	DVST[4:0]					0x00
CLOCK CONFIGURATION REGISTERS											
0x1B	SYSTEM CLOCK	R/W	—	—	PSCLK[1:0]		—	—	—	—	0x00
0x1C	CLOCK MODE	R/W	FREQ[3:0]				—	—	—	USE_MI	0x00
0x1D	CLOCK RATIO NI MSB	R/W	—	NI[14:8]							0x00
0x1E	CLOCK RATIO NI LSB	R/W	NI[7:0]								0x00
0x1F	CLOCK RATIO MI MSB	R/W	MI[15:8]								0x00
0x20	CLOCK RATIO MI LSB	R/W	MI[7:0]								0x00
0x21	MASTER MODE	R/W	MAS	—	—	—	—	BSEL[2:0]			0x00
INTERFACE CONTROL REGISTERS											
0x22	INTERFACE FORMAT	R/W	—	—	RJ	WCI	BCI	DLY	WS[1:0]		0x00
0x23	TDM CONTROL	R/W	—	—	—	—	—	—	FSW	TDM	0x00
0x24	TDM FORMAT	R/W	SLOTL[1:0]		SLOTR[1:0]		SLOTDLY[3:0]				0x00
0x25	I/O CONFIGURATION	R/W	—	—	LTEN	LBEN	DMONO	HIZOFF	SDOEN	SDIEN	0x00
0x26	FILTER CONFIGURATION	R/W	MODE	AHPF	DHPF	DHF	—	—	—	—	0x80
0x27	DAI PLAYBACK LEVEL	R/W	DVM	—	DVG[1:0]		DV[3:0]				0x00
0x28	EQ PLAYBACK LEVEL	R/W	—	—	—	$\overline{\text{EQCLP}}$	DVEQ[3:0]				0x00

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
HEADPHONE (HP) CONTROL REGISTERS											
0x29	LEFT HP MIXER	R/W	—	—	MIXHPL[5:0]						0x00
0x2A	RIGHT HP MIXER	R/W	—	—	MIXHPR[5:0]						0x00
0x2B	HP CONTROL	R/W	—	—	MIXHP RSEL	MIXHP LSEL	MIXHPRG[1:0]		MIXHPLG[1:0]		0x00
0x2C	LEFT HP VOLUME	R/W	HPLM	—	—	HPVOLL[4:0]					0x1A
0x2D	RIGHT HP VOLUME	R/W	HPRM	—	—	HPVOLR[4:0]					0x1A
SPEAKER (SPK) CONFIGURATION REGISTERS											
0x2E	LEFT SPK MIXER	R/W	—	—	MIXSPL[5:0]						0x00
0x2F	RIGHT SPK MIXER	R/W	—	SPK_ SLAVE	MIXSPR[5:0]						0x00
0x30	SPK CONTROL	R/W	—	—	—	—	MIXSPRG[1:0]		MIXSPLG[1:0]		0x00
0x31	LEFT SPK VOLUME	R/W	SPLM	—	SPVOLL[5:0]						0x2C
0x32	RIGHT SPK VOLUME	R/W	SPRM	—	SPVOLR[5:0]						0x2C
DYNAMIC RANGE CONTROL (DRC) CONFIGURATION REGISTERS											
0x33	DRC TIMING	R/W	DRCEN	DRCRLS[2:0]			—	DRCATK[2:0]			0x00
0x34	DRC COMPRESSOR	R/W	DRCCMP[2:0]			DRCTHC[4:0]					0x00
0x35	DRC EXPANDER	R/W	DRCEXP[2:0]			DRCTHE[4:0]					0x00
0x36	DRC GAIN	R/W	—	—	—	DRCG[4:0]					0x00
RECEIVER (RCV OR EARPIECE) AND LINE OUTPUT (LOUT) REGISTERS											
0x37	RCV/LOUTL MIXER	R/W	—	—	MIXRCVL[5:0]						0x00
0x38	RCV/LOUTL CONTROL	R/W	—	—	—	—	—	—	MIXRCVLG[1:0]		0x00
0x39	RCV/LOUTL VOLUME	R/W	RCVLM	—	—	RCVLVOL[4:0]					0x15
0x3A	LOUTR MIXER	R/W	LINMOD	—	MIXRCVR[5:0]						0x00
0x3B	LOUTR CONTROL	R/W	—	—	—	—	—	—	MIXRCVRG[1:0]		0x00
0x3C	LOUTR VOLUME	R/W	RCVRM	—	—	RCVRVOL[4:0]					0x15
JACK DETECT AND ENABLE REGISTERS											
0x3D	JACK DETECT	R/W	JDETEN	JDWK	—	—	—	—	JDEB[1:0]		0x00
0x3E	INPUT ENABLE	R/W	—	—	—	MBEN	LINEAEN	LINEBEN	ADREN	ADLEN	0x00
0x3F	OUTPUT ENABLE	R/W	HPREN	HPLEN	SPREN	SPLEN	RCVLEN	RCVREN	DAREN	DALEN	0x00
0x40	LEVEL CONTROL	R/W	—	—	—	—	—	$\overline{\text{ZDEN}}$	$\overline{\text{VS2EN}}$	$\overline{\text{VSEN}}$	0x00

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0x41	DSP FILTER ENABLE	R/W	—	—	—	—	RECBQEN	EQ3BAND EN	EQ5BAND EN	EQ7BAND EN	0x00
BIAS AND POWER MODE CONFIGURATION REGISTERS											
0x42	BIAS CONTROL	R/W	—	—	—	—	—	—	—	BIAS_ MODE	0x00
0x43	DAC CONTROL	R/W	—	—	—	—	—	—	PERF MODE	DACHP	0x00
0x44	ADC CONTROL	R/W	—	—	—	—	—	OSR128	ADC DITHER	ADCHP	0x06
0x45	DEVICE SHUTDOWN	R/W	$\overline{\text{SHDN}}$	—	—	—	—	—	—	—	0x00
PLAYBACK PARAMETRIC EQUALIZER BAND 1: BIQUAD FILTER COEFFICIENT REGISTERS											
0x46	EQUALIZER BAND 1 COEFFICIENT B0	R/W	B0_1[23:16]								—
0x47		R/W	B0_1[15:8]								—
0x48		R/W	B0_1[7:0]								—
0x49	EQUALIZER BAND 1 COEFFICIENT B1	R/W	B1_1[23:16]								—
0x4A		R/W	B1_1[15:8]								—
0x4B		R/W	B1_1[7:0]								—
0x4C	EQUALIZER BAND 1 COEFFICIENT B2	R/W	B2_1[23:16]								—
0x4D		R/W	B2_1[15:8]								—
0x4E		R/W	B2_1[7:0]								—
0x4F	EQUALIZER BAND 1 COEFFICIENT A1	R/W	A1_1[23:16]								—
0x50		R/W	A1_1[15:8]								—
0x51		R/W	A1_1[7:0]								—
0x52	EQUALIZER BAND 1 COEFFICIENT A2	R/W	A2_1[23:16]								—
0x53		R/W	A2_1[15:8]								—
0x54		R/W	A2_1[7:0]								—

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
PLAYBACK PARAMETRIC EQUALIZER BAND 2: BIQUAD FILTER COEFFICIENT REGISTERS											
0x55	EQUALIZER BAND 2 COEFFICIENT B0	R/W	B0_2[23:16]								—
0x56		R/W	B0_2[15:8]								—
0x57		R/W	B0_2[7:0]								—
0x58	EQUALIZER BAND 2 COEFFICIENT B1	R/W	B1_2[23:16]								—
0x59		R/W	B1_2[15:8]								—
0x5A		R/W	B1_2[7:0]								—
0x5B	EQUALIZER BAND 2 COEFFICIENT B2	R/W	B2_2[23:16]								—
0x5C		R/W	B2_2[15:8]								—
0x5D		R/W	B2_2[7:0]								—
0x5E	EQUALIZER BAND 2 COEFFICIENT A1	R/W	A1_2[23:16]								—
0x5F		R/W	A1_2[15:8]								—
0x60		R/W	A1_2[7:0]								—
0x61	EQUALIZER BAND 2 COEFFICIENT A2	R/W	A2_2[23:16]								—
0x62		R/W	A2_2[15:8]								—
0x63		R/W	A2_2[7:0]								—
PLAYBACK PARAMETRIC EQUALIZER BAND 3: BIQUAD FILTER COEFFICIENT REGISTERS											
0x64	EQUALIZER BAND 3 COEFFICIENT B0	R/W	B0_3[23:16]								—
0x65		R/W	B0_3[15:8]								—
0x66		R/W	B0_3[7:0]								—
0x67	EQUALIZER BAND 3 COEFFICIENT B1	R/W	B1_3[23:16]								—
0x68		R/W	B1_3[15:8]								—
0x69		R/W	B1_3[7:0]								—
0x6A	EQUALIZER BAND 3 COEFFICIENT B2	R/W	B2_3[23:16]								—
0x6B		R/W	B2_3[15:8]								—
0x6C		R/W	B2_3[7:0]								—
0x6D	EQUALIZER BAND 3 COEFFICIENT A1	R/W	A1_3[23:16]								—
0x6E		R/W	A1_3[15:8]								—
0x6F		R/W	A1_3[7:0]								—
0x70	EQUALIZER BAND 3 COEFFICIENT A2	R/W	A2_3[23:16]								—
0x71		R/W	A2_3[15:8]								—
0x72		R/W	A2_3[7:0]								—

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
PLAYBACK PARAMETRIC EQUALIZER BAND 4: BIQUAD FILTER COEFFICIENT REGISTERS											
0x73	EQUALIZER BAND 4 COEFFICIENT B0	R/W	B0_4[23:16]								—
0x74		R/W	B0_4[15:8]								—
0x75		R/W	B0_4[7:0]								—
0x76	EQUALIZER BAND 4 COEFFICIENT B1	R/W	B1_4[23:16]								—
0x77		R/W	B1_4[15:8]								—
0x78		R/W	B1_4[7:0]								—
0x79	EQUALIZER BAND 4 COEFFICIENT B2	R/W	B2_4[23:16]								—
0x7A		R/W	B2_4[15:8]								—
0x7B		R/W	B2_4[7:0]								—
0x7C	EQUALIZER BAND 4 COEFFICIENT A1	R/W	A1_4[23:16]								—
0x7D		R/W	A1_4[15:8]								—
0x7E		R/W	A1_4[7:0]								—
0x7F	EQUALIZER BAND 4 COEFFICIENT A2	R/W	A2_4[23:16]								—
0x80		R/W	A2_4[15:8]								—
0x81		R/W	A2_4[7:0]								—
PLAYBACK PARAMETRIC EQUALIZER BAND 5: BIQUAD FILTER COEFFICIENT REGISTERS											
0x82	EQUALIZER BAND 5 COEFFICIENT B0	R/W	B0_5[23:16]								—
0x83		R/W	B0_5[15:8]								—
0x84		R/W	B0_5[7:0]								—
0x85	EQUALIZER BAND 5 COEFFICIENT B1	R/W	B1_5[23:16]								—
0x86		R/W	B1_5[15:8]								—
0x87		R/W	B1_5[7:0]								—
0x88	EQUALIZER BAND 5 COEFFICIENT B2	R/W	B2_5[23:16]								—
0x89		R/W	B2_5[15:8]								—
0x8A		R/W	B2_5[7:0]								—
0x8B	EQUALIZER BAND 5 COEFFICIENT A1	R/W	A1_5[23:16]								—
0x8C		R/W	A1_5[15:8]								—
0x8D		R/W	A1_5[7:0]								—
0x8E	EQUALIZER BAND 5 COEFFICIENT A2	R/W	A2_5[23:16]								—
0x8F		R/W	A2_5[15:8]								—
0x90		R/W	A2_5[7:0]								—

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
PLAYBACK PARAMETRIC EQUALIZER BAND 6: BIQUAD FILTER COEFFICIENT REGISTERS											
0x91	EQUALIZER BAND 6 COEFFICIENT B0	R/W	B0_6[23:16]								—
0x92		R/W	B0_6[15:8]								—
0x93		R/W	B0_6[7:0]								—
0x94	EQUALIZER BAND 6 COEFFICIENT B1	R/W	B1_6[23:16]								—
0x95		R/W	B1_6[15:8]								—
0x96		R/W	B1_6[7:0]								—
0x97	EQUALIZER BAND 6 COEFFICIENT B2	R/W	B2_6[23:16]								—
0x98		R/W	B2_6[15:8]								—
0x99		R/W	B2_6[7:0]								—
0x9A	EQUALIZER BAND 6 COEFFICIENT A1	R/W	A1_6[23:16]								—
0x9B		R/W	A1_6[15:8]								—
0x9C		R/W	A1_6[7:0]								—
0x9D	EQUALIZER BAND 6 COEFFICIENT A2	R/W	A2_6[23:16]								—
0x9E		R/W	A2_6[15:8]								—
0x9F		R/W	A2_6[7:0]								—
PLAYBACK PARAMETRIC EQUALIZER BAND 7: BIQUAD FILTER COEFFICIENT REGISTERS											
0xA0	EQUALIZER BAND 7 COEFFICIENT B0	R/W	B0_7[23:16]								—
0xA1		R/W	B0_7[15:8]								—
0xA2		R/W	B0_7[7:0]								—
0xA3	EQUALIZER BAND 7 COEFFICIENT B1	R/W	B1_7[23:16]								—
0xA4		R/W	B1_7[15:8]								—
0xA5		R/W	B1_7[7:0]								—
0xA6	EQUALIZER BAND 7 COEFFICIENT B2	R/W	B2_7[23:16]								—
0xA7		R/W	B2_7[15:8]								—
0xA8		R/W	B2_7[7:0]								—
0xA9	EQUALIZER BAND 7 COEFFICIENT A1	R/W	A1_7[23:16]								—
0xAA		R/W	A1_7[15:8]								—
0xAB		R/W	A1_7[7:0]								—
0xAC	EQUALIZER BAND 7 COEFFICIENT A2	R/W	A2_7[23:16]								—
0xAD		R/W	A2_7[15:8]								—
0xAE		R/W	A2_7[7:0]								—

Table 1. MAX98090 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
RECORD BIQUAD FILTER COEFFICIENT REGISTERS											
0xAF	RECORD BIQUAD COEFFICIENT B0	R/W	REC_B0[23:16]								—
0xB0		R/W	REC_B0[15:8]								—
0xB1		R/W	REC_B0[7:0]								—
0xB2	RECORD BIQUAD COEFFICIENT B1	R/W	REC_B1[23:16]								—
0xB3		R/W	REC_B1[15:8]								—
0xB4		R/W	REC_B1[7:0]								—
0xB5	RECORD BIQUAD COEFFICIENT B2	R/W	REC_B2[23:16]								—
0xB6		R/W	REC_B2[15:8]								—
0xB7		R/W	REC_B2[7:0]								—
0xB8	RECORD BIQUAD COEFFICIENT A1	R/W	REC_A1[23:16]								—
0xB9		R/W	REC_A1[15:8]								—
0xBA		R/W	REC_A1[7:0]								—
0xBB	RECORD BIQUAD COEFFICIENT A2	R/W	REC_A2[23:16]								—
0xBC		R/W	REC_A2[15:8]								—
0xBD		R/W	REC_A2[7:0]								—
REVISION ID REGISTER											
0xFF	REVISION ID	R	REVID[7:0]								0x43

Software Reset

The device provides a software controlled reset (Table 2) that is used to return most registers to their default (POR) states (the record biquad and playback parametric equalizer coefficients are not reset). The software reset register is a pushbutton, write only register. As a result, a read of this register always returns 0x00. Writing logic-high to SWRESET triggers a software register reset, while writing a logic-low to SWRESET has no effect.

Table 2. Software Reset Register

ADDRESS: 0x00				DESCRIPTION
BIT	NAME	TYPE	POR	
7	SWRESET	W	0	Pushbutton Software Device Reset 0: Writing a logic low to SWRESET has no effect. 1: Reset all registers to their default POR values. This excludes the record biquad and playback parametric equalizer filter coefficients (Table 30 and Table 52).
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

Power and Performance Management

The device includes comprehensive power management to allow the disabling of unused blocks to minimize supply current. In addition to this, the available power modes provide a software configurable choice between highest performance and reduced power consumption.

Device Performance Configuration

The Bias Control register (Table 3) selects the method used to derive the common-mode reference voltage. A common-mode bias created by resistive division (from the AVDD supply) facilitates lower overall power consumption by disabling the bandgap reference circuit. However, this type of BIAS reference has the disadvantage of scaling with the AVDD supply voltage (and thus also has reduced PSRR). When derived from a bandgap reference, BIAS is constant regardless of the supply voltage, but the additional circuitry increases power consumption.

The ADC, DAC, and headphone playback all have optional high-performance modes (Tables 4 and 5). In each case, these modes trade additional power consumption for enhanced performance. The ADC also has optional

Table 3. Bias Control Register

ADDRESS: 0x42				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	BIAS_MODE	R/W	0	**Select source for BIAS.** 0: BIAS derived from resistive division. 1: BIAS created by bandgap reference.

Table 4. DAC and Headphone Performance Mode Control Register

ADDRESS: 0x43				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	PERFMODE	R/W	0	**Performance Mode** Selects DAC to headphone playback performance mode: 1: Low power headphone playback mode. 0: High performance headphone playback mode.
0	DACHP	R/W	0	**DAC High-Performance Mode** 0: DAC settings optimized for lowest power consumption. 1: DAC settings optimized for best performance.

dither (recommended for the cleanest spectrum), and can be configured to two different oversampling rates. See the *Analog-to-Digital Converter (ADC)* section for additional details on ADC operation.

Device Enable Configuration

In addition to a device global shutdown control, the major input and output blocks can be independently enabled (or disabled) to optimize power consumption. The device global shutdown control is detailed in Table 6.

Table 5. ADC Performance Mode Control Register

ADDRESS: 0x44				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	OSR128	R/W	1	**ADC Oversampling Rate** 0: $f_{ADCCLK} = 64 \times f_S$ 1: $f_{ADCCLK} = 128 \times f_S$
1	ADCDITHER	R/W	1	**ADC Quantizer Dither** 0: Dither disabled. 1: Dither enabled.
0	ADCHP	R/W	0	**ADC High-Performance Mode** 0: ADC is optimized for low power operation. 1: ADC is optimized for best performance.

Table 6. Device Shutdown Register

ADDRESS: 0x45				DESCRIPTION
BIT	NAME	TYPE	POR	
7	$\overline{SHDN}$	R/W	0	**Device Active-Low Global Shutdown Control** 0: Device is in shutdown. 1: Device is active. Certain registers should not be written to while the device is active (Table 90).
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

Table 7 details the available input signal path enables (with the exception of the analog microphone inputs 1/2, which are enabled from registers 0x10 and 0x11, or Tables 9 and 10, respectively). Table 8 details the available output signal path enables.

When the device is in global shutdown, the major input and output blocks are all disabled to conserve power. However, the I2C interface remains active and all device registers can be configured. Certain registers should be programmed while in shutdown only (detailed in Table 90). Changing these registers when the device is active could result in unexpected behavior. For optimal minimized power consumption, only enable the stage blocks that are part of the intended signal path configuration.

Table 7. Input Enable Register

ADDRESS: 0x3E				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	MBEN	R/W	0	**Microphone Bias Enable** 0: Microphone bias disabled. 1: Microphone bias enabled.
3	LINEAEN	R/W	0	**Enables Line A Analog Input Block** 0: Line A input amplifier disabled. 1: Line A input amplifier enabled.
2	LINEBEN	R/W	0	**Enables Line B Analog Input Block** 0: Line B input amplifier disabled. 1: Line B input amplifier enabled.
1	ADREN	R/W	0	**Right ADC Enable** 0: Right ADC disabled. 1: Right ADC enabled.
0	ADLEN	R/W	0	**Left ADC Enable** 0: Left ADC disabled. 1: Left ADC enabled.

Table 8. Output Enable Register

ADDRESS: 0x3F				DESCRIPTION
BIT	NAME	TYPE	POR	
7	HPREN	R/W	0	**Right Headphone Output Enable** 0: Right headphone output disabled. 1: Right headphone output enabled.
6	HPLEN	R/W	0	**Left Headphone Output Enable** 0: Left headphone output disabled. 1: Left headphone output enabled.
5	SPREN	R/W	0	**Right Class D Speaker Output Enable** 0: Right speaker output disabled. 1: Right speaker output enabled.
4	SPLEN	R/W	0	**Left Class D Speaker Output Enable** 0: Left speaker output disabled. 1: Left speaker output enabled.
3	RCVLEN	R/W	0	**Receiver (Earpiece)/Left Line Output Enable** 0: Receiver/left line output disabled. 1: Receiver/left line output enabled.
2	RCVREN	R/W	0	**Right Line Output Enable** 0: Right line output disabled. 1: Right line output enabled.
1	DAREN	R/W	0	**Right DAC Digital Input Enable** 0: Right DAC input disabled. 1: Right DAC input enabled.
0	DALEN	R/W	0	**Left DAC Digital Input Enable** 0: Left DAC input disabled. 1: Left DAC input enabled.

Audio Input Configuration

The device features either six (WLP package) or four (TQFN package) flexible analog inputs. Each pair can be configured as either an analog microphone input, a single-ended or differential line input(s), or as a reduced power, full-scale differential analog input direct to the ADC mixer. The analog microphone and line inputs can either be routed to the stereo ADC mixer for recording or directly to any analog output mixer for playback.

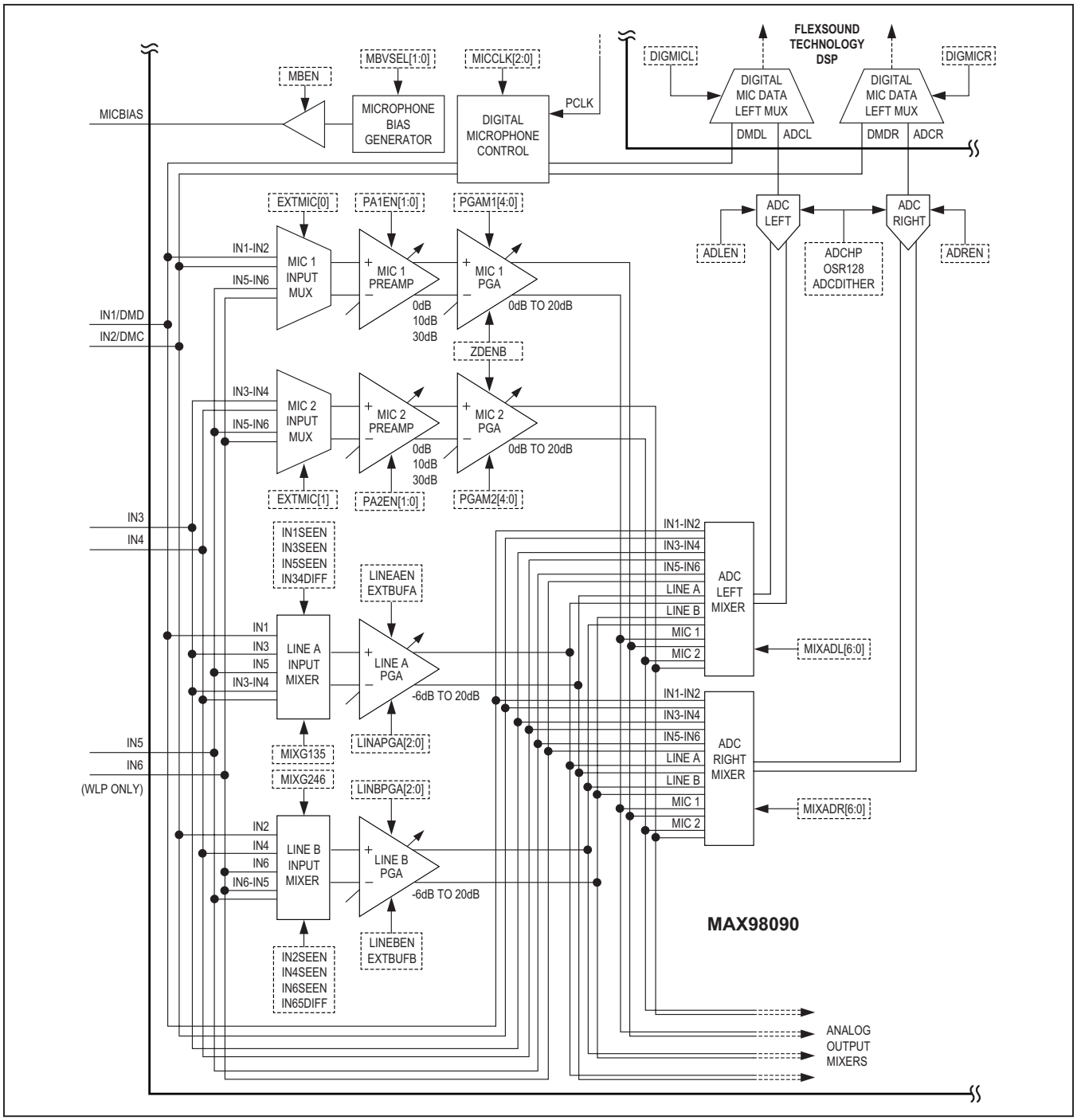


Figure 5. Analog Audio Input Functional Diagram

Analog Microphone Inputs

The device includes three differential microphone inputs (three for the WLP package and two for the TQFN package) and a programmable, low-noise microphone bias for powering a wide variety of external microphones (Figure 6). By default, analog inputs IN1 and IN2 differentially (IN1/IN2) provide the input to microphone amplifier 1, while IN3 and IN4 differentially (IN3/IN4) form the input to microphone amplifier 2. For the WLP package, the additional analog input pair (IN5 and IN6) can be configured as a differential input (IN5 - IN6) to either microphone amplifier 1 or 2 (Table 24).

In the typical application, one microphone input is used for the handset microphone and the other is used as an accessory microphone (IN1/IN2 and IN3/IN4). In systems using a background noise microphone, IN5/IN6 (WLP only) can be retasked as another microphone input.

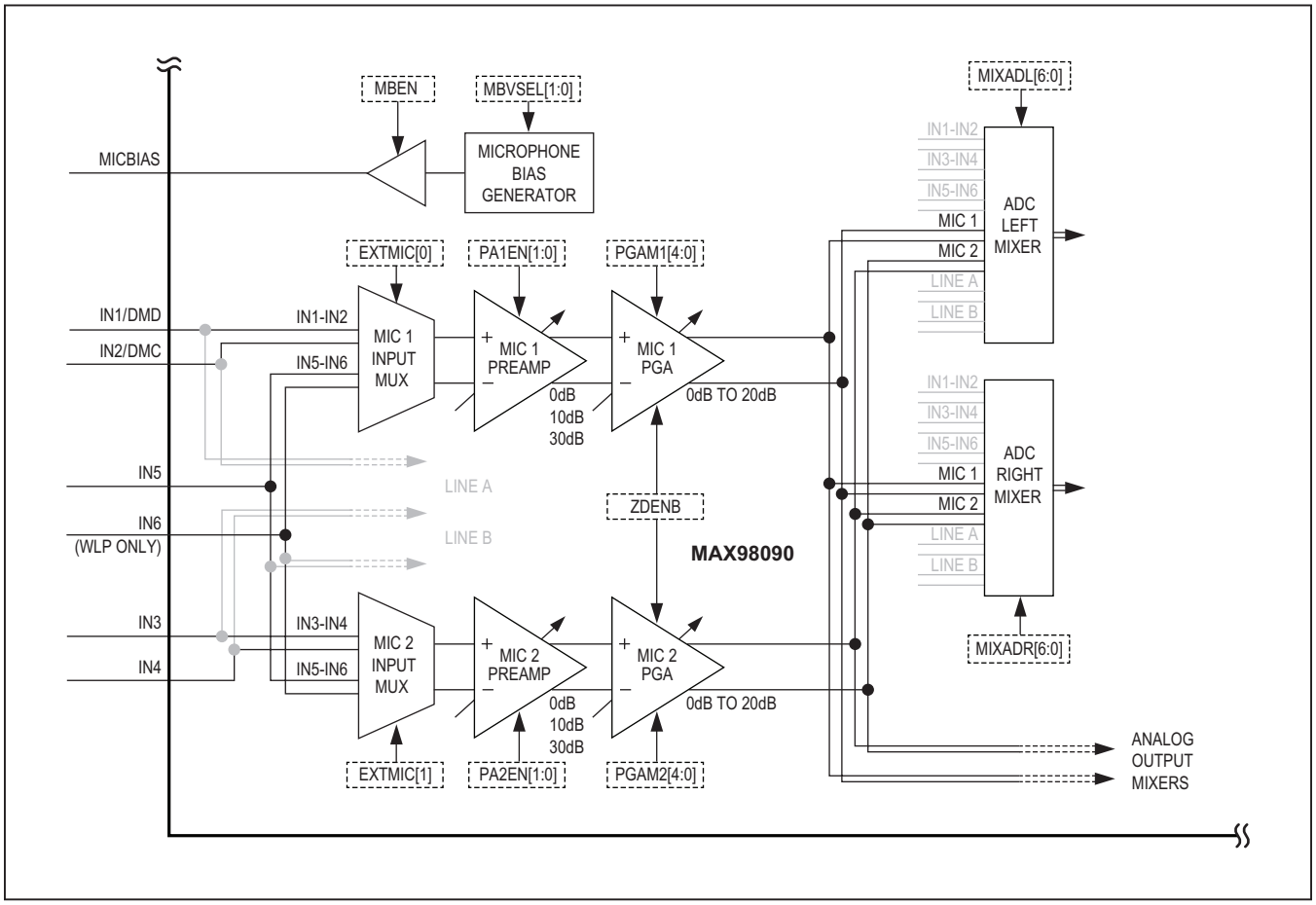


Figure 6. Analog Microphone Input Functional Diagram

Analog Microphone Preamplifier and PGA

The analog microphone inputs have two stages of programmable gain amplifiers, and are then routed to the ADC mixer (record), the analog outputs (playback), or simultaneously to both. The first, a coarse preamplifier gain stage, includes the analog microphone enable, and offers selectable 0dB, 20dB, or 30dB gain settings. The second, a fine gain stage, is a programmable-gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps (Tables 9 and 10). Together, the two stages provide up to 50dB of signal gain for the analog microphone inputs. To maximize the signal-to-noise ratio, use the coarse gain settings of the first stage whenever possible. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes.

Table 9. Microphone 1 Enable and Level Configuration Register

ADDRESS: 0x10				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	PA1EN[1:0]	R/W	0	**Microphone 1 Input Amplifier Enable and Coarse Gain Setting** 00: Disabled 10: 20dB 01: 0dB 11: 30dB
5			0	
4	PGAM1[4:0]	R/W	1	**Microphone 1 Programmable Gain Amplifier Fine Adjust Configuration** 0x1F: 0dB 0x0E: 6dB 0x06: 14dB ⋮ 0x0D: 7dB 0x05: 15dB 0x14: 0dB 0x0C: 8dB 0x04: 16dB 0x13: 1dB 0x0B: 9dB 0x03: 17dB 0x12: 2dB 0x0A: 10dB 0x02: 18dB 0x11: 3dB 0x09: 11dB 0x01: 19dB 0x10: 4dB 0x08: 12dB 0x00: 20dB 0x0F: 5dB 0x07: 13dB
3			0	
2			1	
1			0	
0			0	

Table 10. Microphone 2 Enable and Level Configuration Register

ADDRESS: 0x11				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	PA2EN[1:0]	R/W	0	**Microphone 2 Input Amplifier Enable and Coarse Gain Setting** 00: Disabled 10: 20dB 01: 0dB 11: 30dB
5			0	
4	PGAM2[4:0]	R/W	1	**Microphone 2 Programmable Gain Amplifier Fine Adjust Configuration** 0x1F: 0dB 0x0E: 6dB 0x06: 14dB ⋮ 0x0D: 7dB 0x05: 15dB 0x14: 0dB 0x0C: 8dB 0x04: 16dB 0x13: 1dB 0x0B: 9dB 0x03: 17dB 0x12: 2dB 0x0A: 10dB 0x02: 18dB 0x11: 3dB 0x09: 11dB 0x01: 19dB 0x10: 4dB 0x08: 12dB 0x00: 20dB 0x0F: 5dB 0x07: 13dB
3			0	
2			1	
1			0	
0			0	

Analog Microphone Bias Voltage

The device features a regulated, low noise microphone bias output (MICBIAS) that can be configured to power a wide range of external microphone devices. To enable the microphone bias output, set MBEN in the input enable register (Table 7). When the device is powered and the microphone bias is disabled (MBEN is low or the device is in shutdown), MICBIAS is placed in a high-impedance state. The microphone bias voltage can be set by the software to any one of 4 voltages (2.2V, 2.4V, 2.55V, or 2.8V) by programming the Microphone Bias Level Configuration register (Table 11).

Digital Microphone Inputs

One pair of microphone inputs (IN1/IN2) can also be configured to interface to up to two digital microphones (Figure 7). The record path DSP is automatically switched to accept the appropriate digital microphone data channel when enabled (Figure 13). Both channels (left and right) must be enabled to use the digital microphone interface. When both channels are enabled, the digital microphone interface provides a digital microphone clock on IN2/DMC and accepts PDM data on IN1/DMD. A single digital microphone input cannot be paired with a single analog microphone input. Left channel data is accepted on falling clock edges while the right channel data is accepted on the rising clock edges (see Figure 4 for timing requirements).

To avoid any potential clipping and distortion, always enable the record path DC blocking filters to remove any built-in DC offsets when using a digital microphone input (AHPF, Table 21). The record path biquad filter and digital gain and level control stages can also be applied to digital microphone input signals.

Digital Microphone Clock Configuration

The digital microphone clock frequency (f_{DMC}) can be configured to any one of 6 settings using MICCLK[2:0] (Table 13). The digital microphone clock is derived from a PCLK divider, with available settings ranging incrementally from $f_{PCLK}/2$ to $f_{PCLK}/8$. This wide range of available digital microphone clock frequencies is intended to support both current and next generation digital microphones. Table 12 lists the resulting clock frequencies for commonly used master clock (and resulting PCLK) frequencies.

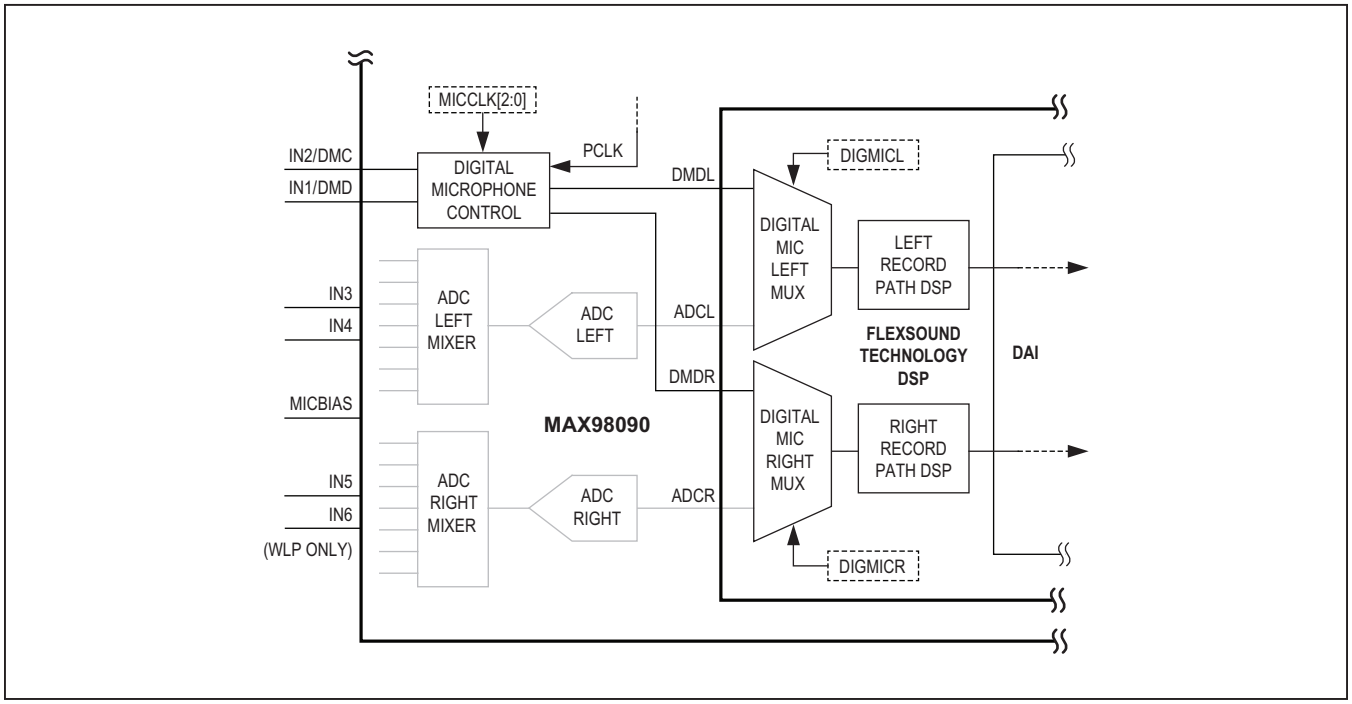


Figure 7. Digital Microphone Input Functional Diagram

Table 11. Microphone Bias Level Configuration Register

ADDRESS: 0x12				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	MBVSEL[1:0]	R/W	0	**Microphone Bias Level Configuration** 00: 2.2V 10: 2.55V 01: 2.4V 11: 2.8V
0			0	

Table 12. Digital Microphone Clocks for Commonly Used Master Clocks Settings

Master Clock Frequency (f_{MCLK})		10MHz	11.2896MHz	12MHz	12.288MHz	13/26MHz	19.2MHz
Approximate Digital Microphone Clock Frequency (f_{DMC})	$f_{PCLK}/2$	5.0MHz	5.645MHz	6.0MHz	6.144MHz	6.5MHz	—
	$f_{PCLK}/3$	3.333MHz	3.763MHz	4.0MHz	4.096MHz	4.333MHz	6.4MHz
	$f_{PCLK}/4$	2.5MHz	2.822MHz	3.0MHz	3.072MHz	3.25MHz	4.8MHz
	$f_{PCLK}/5$	2.0MHz	2.258MHz	2.4MHz	2.458MHz	2.6MHz	3.84MHz
	$f_{PCLK}/6$	1.667MHz	1.882MHz	2.0MHz	2.048MHz	2.167MHz	3.2MHz
	$f_{PCLK}/8$	1.25MHz	1.411MHz	1.5MHz	1.536MHz	1.625MHz	2.4MHz

Table 13. Digital Microphone Enable

ADDRESS: 0x13				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	DMICCLK[2:0]	R/W	0	**Digital Microphone Clock Rate Configuration** 000: $f_{DMC} = f_{PCLK}/2$ 100: $f_{DMC} = f_{PCLK}/6$ 001: $f_{DMC} = f_{PCLK}/3$ 101: $f_{DMC} = f_{PCLK}/8$ 010: $f_{DMC} = f_{PCLK}/4$ 110: Reserved 011: $f_{DMC} = f_{PCLK}/5$ 111: Reserved
5			0	
4			0	
3	—	—	—	—
2	—	—	—	—
1	DIGMICR	R/W	0	**Digital Microphone Clock and Right Channel Enable** 0: Right record channel uses on-chip ADC. 1: Right record channel uses digital microphone input. Digital microphone clock (DMC) is enabled once both data channels are enabled.
0	DIGMICL	R/W	0	**Digital Microphone Clock and Left Channel Enable** 0: Left record channel uses on-chip ADC. 1: Left record channel uses digital microphone input. Digital microphone clock (DMC) is enabled once both data channels are enabled.

Digital Microphone Frequency Compensation

The digital microphone inputs can be configured to produce a wide range of digital microphone clock frequencies. To optimize performance over the entire range of available frequencies, the device provides configurable

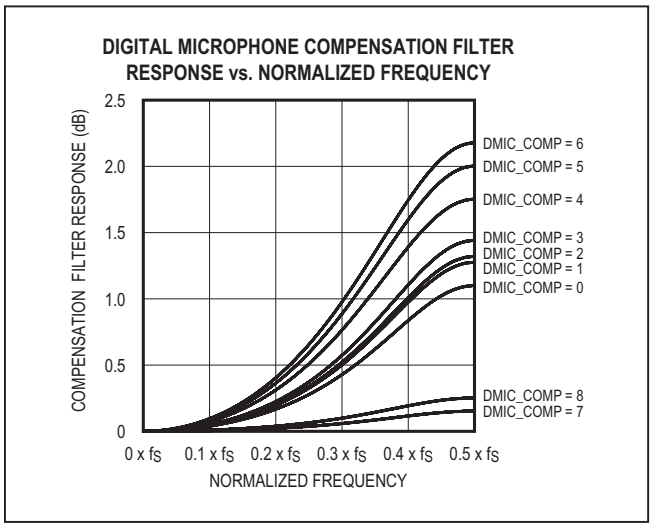


Figure 8. Digital Microphone Compensation Filter Frequency Response

frequency range and compensation settings. Once the master clock (and thus prescaled clock) frequency is decided, and the digital microphone clock divider is chosen, the digital microphone frequency range bits should be programmed to the correct range (DMIC_FREQ, Table 14). If quick configuration mode is used and a system clock bit is selected (Table 36), then the device automatically calculates and selects the correct range once the digital microphone clock divider is configured.

The digital microphone inputs also provide a configurable frequency compensation filter with 9 frequency response settings (Figure 8). Every sample rate and MCLK/PCLK frequency (and the resulting digital microphone clock frequency) combination results in a different baseline frequency response. Table 15 to Table 20 provide the recommended compensation filter settings for the most commonly used PCLK frequency and sample rate combinations. Choose the PCLK divider that results in the DMC clock frequency closest to the optimal frequency for the built-in digital MIC hardware, and then set the correct DMIC frequency range (DMIC_FREQ, Table 14). Then, based on the desired sample rate, select the appropriate compensation settings from Table 14 (DMIC_COMP).

If the system PCLK frequency does not match one of these commonly used rates, then refer to the table for the PCLK frequency that is closest (e.g., if the system PCLK frequency is 12.5MHz, see Table 17 as 12.288MHz is the closest common PCLK frequency). As before, choose the PCLK divider that results in the optimal DMC clock frequency, and set the appropriate DMIC frequency range (DMIC_FREQ, Table 14). Then choose the compensation settings based on the row that is the closest match to the configured DMC frequency. Similarly, for nonstandard sample rates choose the column with the common value closest to the actual system sample rate.

In quick configuration mode, once both the system clock and sample rate bits are selected (Table 36 and Table 37), the device automatically selects the recommended response curve once the digital microphone clock divider is configured. The digital microphone input does not support sample rates in excess of 48kHz (where DHF = 1, Table 27).

Table 14. Digital Microphone Configuration

ADDRESS: 0x14				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DMIC_COMP[3:0]	R/W	0	**Digital Microphone Compensation Filter Configuration** 0000–1000: Figure 8 details the available compensation filter configurations. 1001–1111: Configures the compensation filter to a pass through response. The compensation filter response scales with the sample rate up to the Nyquist bandwidth limit (f_S/2). Automatically decoded in quick configuration mode.
6			0	
5			0	
4			0	
3	—	—	—	—
2	—	—	—	—
1	DMIC_FREQ[1:0]	R/W	0	**Digital Microphone Frequency Range Configuration** 00: f_{DMC} < 3.5MHz 10: 4.5MHz ≤ f_{DMC} 01: 3.5MHz ≤ f_{DMC} < 4.5MHz 11: Reserved If any of the system clock quick configuration bits in register 0x04 are set, then the frequency range configuration is automatically decoded.
0		R/W	0	

Table 15. Recommended Compensation Filter Settings for f_{PCLK} = 11.2896MHz

f_{PCLK} = f_{MCLK}/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	5.6448	2	7	8	3	3	3
1	f_{PCLK}/3	3.7632	1	7	8	2	2	2
2	f_{PCLK}/4	2.8224	0	7	8	3	3	3
3	f_{PCLK}/5	2.25792	0	7	8	6	6	6
4	f_{PCLK}/6	1.8816	0	7	8	3	3	3
5	f_{PCLK}/8	1.4112	0	7	8	3	3	3

Table 16. Recommended Compensation Filter Settings for f_{PCLK} = 12MHz

f_{PCLK} = f_{MCLK}/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	6	2	7	8	3	3	3
1	f_{PCLK}/3	4	1	7	8	2	2	2
2	f_{PCLK}/4	3	0	7	8	3	3	3
3	f_{PCLK}/5	2.4	0	7	8	5	5	6
4	f_{PCLK}/6	2	0	7	8	3	3	3
5	f_{PCLK}/8	1.5	0	7	8	3	3	3

Table 17. Recommended Compensation Filter Settings for f_{PCLK} = 12.288MHz

$f_{PCLK} = f_{MCLK}$/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	6.144	2	7	8	3	3	3
1	f_{PCLK}/3	4.096	1	7	8	2	2	2
2	f_{PCLK}/4	3.072	0	7	8	3	3	3
3	f_{PCLK}/5	2.4576	0	7	8	6	6	6
4	f_{PCLK}/6	2.048	0	7	8	3	3	3
5	f_{PCLK}/8	1.536	0	7	8	3	3	3

Table 18. Recommended Compensation Filter Settings for f_{PCLK} = 13MHz

$f_{PCLK} = f_{MCLK}$/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	6.5	2	7	8	1	1	1
1	f_{PCLK}/3	4.333	1	7	8	0	0	1
2	f_{PCLK}/4	3.25	0	7	8	1	1	1
3	f_{PCLK}/5	2.6	0	7	8	4	4	5
4	f_{PCLK}/6	2.167	0	7	8	1	1	1
5	f_{PCLK}/8	1.625	0	7	8	1	1	1

Table 19. Recommended Compensation Filter Settings for f_{PCLK} = 19.2MHz

$f_{PCLK} = f_{MCLK}$/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	—	—	—	—	—	—	—
1	f_{PCLK}/3	6.4	2	7	8	1	1	1
2	f_{PCLK}/4	4.8	2	7	8	5	5	6
3	f_{PCLK}/5	3.84	1	7	8	2	2	3
4	f_{PCLK}/6	3.2	0	7	8	1	1	2
5	f_{PCLK}/8	2.4	0	7	8	5	5	6

Table 20. Recommended Compensation Filter Settings for f_{PCLK} = 256 x f_S

$f_{PCLK} = f_{MCLK}$/PSCLK (See Table 34)				RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz)				
MICCLK	DIVIDER	f_{DMC} (MHz)	DMIC_FREQ	8	16	32	44.1	48
0	f_{PCLK}/2	—	—	7	8	3	3	3
1	f_{PCLK}/3	—	—	7	8	2	2	2
2	f_{PCLK}/4	—	—	7	8	3	3	3
3	f_{PCLK}/5	—	—	7	8	6	6	6
4	f_{PCLK}/6	—	—	7	8	3	3	3
5	f_{PCLK}/8	—	—	7	8	3	3	3

Analog Line Inputs

The device includes multiple line level input options and two analog line input programmable gain amplifiers (PGAs, Figure 9). The line input structure supports multiple configurations including stereo single-ended inputs, stereo differential inputs, and stereo mixed single-ended inputs (any two per line input mixer).

Analog Line Input Mixers

The analog line input mixer allows the selection of either single-ended or differential inputs to each line input channel (Table 21). The line A input mixer can accept single-ended inputs from IN1, IN3, and IN5, or a differential input from IN3 and IN4 (IN3 - IN4). The line B input mixer can accept single-ended inputs from IN2, IN4, and IN6, or a

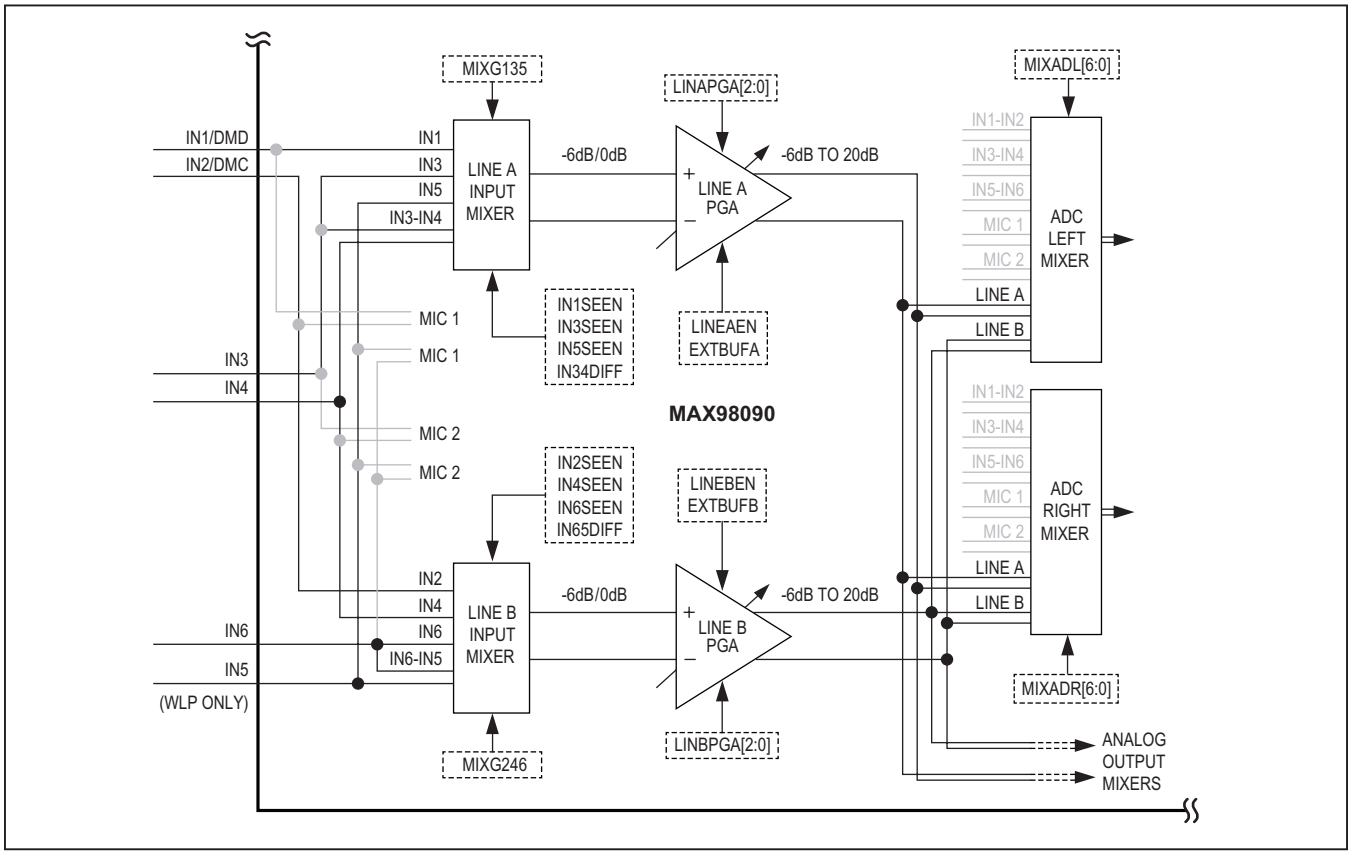


Figure 9. Analog Line Input Functional Diagram

Table 21. Line Input Mixer Configuration Register

ADDRESS: 0x0D				DESCRIPTION
BIT	NAME	TYPE	POR	
7	IN34DIFF	R/W	0	Selects IN3, IN4 differentially as an input to the line A mixer.
6	IN65DIFF	R/W	0	Selects IN6, IN5 differentially as an input to the line B mixer (WLP only).
5	IN1SEEN	R/W	0	Selects IN1 single ended as an input to the line A mixer.
4	IN2SEEN	R/W	0	Selects IN2 single ended as an input to the line B mixer.
3	IN3SEEN	R/W	0	Selects IN3 single ended as an input to the line A mixer.
2	IN4SEEN	R/W	0	Selects IN4 single ended as an input to the line B mixer.
1	IN5SEEN	R/W	0	Selects IN5 single ended as an input to the line A mixer (WLP only).
0	IN6SEEN	R/W	0	Selects IN6 single ended as an input to the line B mixer (WLP only).

differential input from IN5 and IN6 (IN6 - IN5). Internally, all analog signal paths are differential. As a result, single-ended inputs have a built in baseline gain of +6dB (from the single-ended to differential conversion) while differential inputs have 0dB of built in gain.

The line input mixer can also be set to accept and mix any two single-ended inputs. To facilitate full-scale signals, when mixing two single-ended inputs an optional -6dB of attenuation is available (MIXG135 and MIXG246, Table 23). The line input mixer attenuation setting has no effect if enabled when only a single input source is selected. If a differential input to either mixer is enabled, any single-ended inputs that are also selected are ignored, and the mixer accepts only the differential input.

Analog Line Input PGAs

To facilitate a wide range of input signal levels, each analog line input includes a coarse programmable gain amplifier (PGA) that can provide from 6dB of attenuation to 20dB of signal gain. The line inputs are then routed to either the ADC mixer (record) or analog outputs (playback).

If the line input signal exceeds full scale and requires additional attenuation, the external gain mode provides trimmed internal feedback resistors (20kΩ) for custom gain levels. Line input external gain mode is not intended to provide positive gain, and as such for optimal performance any gain of -6dB of higher should be set using the provided internal PGA gain settings.

Differentially, the external line input gain is set by using two precision (1% or better), well-matched series input resistors (Figure 10). Use the following formula to calculate the appropriate differential series input resistors:

$$A_{V_EXTLINE} = 20 \times \log (20k\Omega / R_{S_EXT})$$

For single-ended inputs, the external line input gain is set using a single precision (1% or better) series input resistor (Figure 10). However, due to the internal single-ended to differential conversion, this configuration creates an unbalanced differential amplifier configuration (configured external gain paired with a fixed internal gain of +6dB). Table 22 provides the appropriate series resistance values for common attenuation settings.

Table 22. External Gain Mode Series Resistance Values

LINE INPUT EXTERNAL GAIN (dB)	R_{S_EXT}	
	DIFFERENTIAL (kΩ)	SINGLE-ENDED (kΩ)
$A_{V_EXTLINE}$ = -9.5	60	84.5
$A_{V_EXTLINE}$ = -12.0	80	115
$A_{V_EXTLINE}$ = -15.0	112	165
$A_{V_EXTLINE}$ = -18.0	160	237

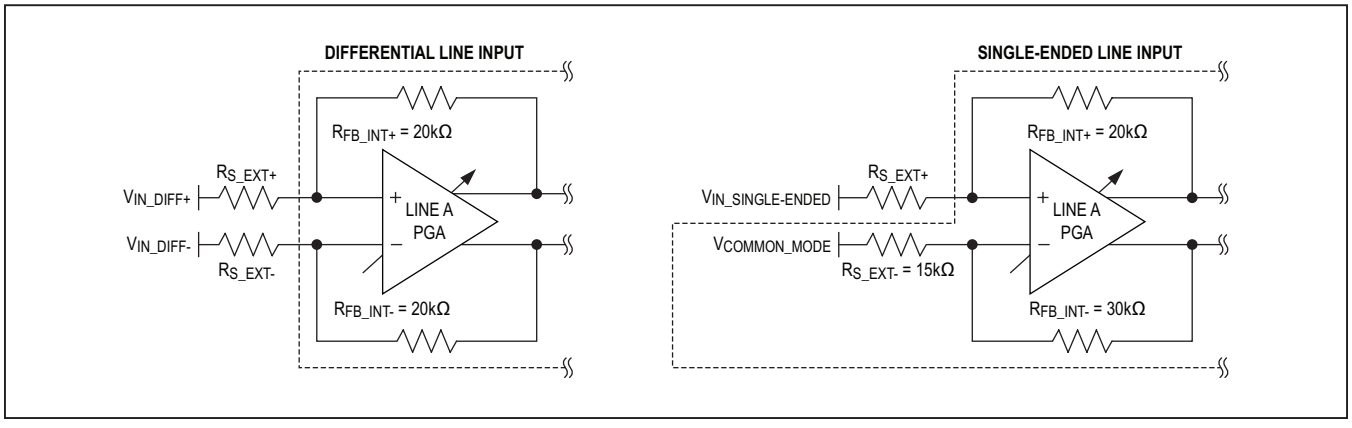


Figure 10. Analog Line Input External Gain Configurations

Table 23. Line Input Level Configuration Register

ADDRESS: 0x0E				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MIXG135	R/W	0	**Enable for a -6dB Reduction for Two Single-Ended Line A Mixer Inputs** 0: Normal line A mixer operation. 1: Gain is reduced by -6dB when two single-ended inputs are selected.
6	MIXG246	R/W	0	**Enable for a -6dB Reduction for Two Single-Ended Line B Mixer Inputs** 0: Normal line B mixer operation. 1: Gain is reduced by -6dB when two single-ended inputs are selected
5	LINAPGA[2:0]	R/W	0	**Line Input A Programmable Internal Preamp Gain Configuration** 000: 20dB 010: 3dB 100: -3dB 001: 14dB 011: 0dB 101, 110, 111: -6dB
4			1	
3			1	
2	LINBPGA[2:0]	R/W	0	**Line Input B Programmable Internal Preamp Gain Configuration** 000: 20dB 010: 3dB 100: -3dB 001: 14dB 011: 0dB 101, 110, 111: -6dB
1			1	
0			1	

Table 24. Input Mode and Source Configuration Register

ADDRESS: 0x0F				DESCRIPTION
BIT	NAME	TYPE	POR	
7	EXTBUFA	R/W	0	Selects external resistor gain mode for line input A.
6	EXTBUFB	R/W	0	Selects external resistor gain mode for line input B.
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	EXTMIC[1:0]	R/W	0	**External Analog Microphone (IN5/IN6) MUX Configuration (WLP Only)** 00: External microphone disabled: IN1/IN2 selected for MIC 1 IN3/IN4 selected for MIC 2 10: External microphone to MIC 2: IN1/IN2 selected for MIC 1 IN5/IN6 selected for MIC 2 01: External microphone to MIC 1: IN5/IN6 selected for MIC 1 IN3/IN4 selected for MIC 2 11: Reserved.
0			0	

Analog Input PGA to Analog Output Mixer

The analog line input PGA and analog microphone PGA outputs can be routed directly to any of the analog output mixers. This configuration allows the analog inputs to operate as line or microphone level input amplifiers capable of driving headphone, speaker, receiver, or line output loads. The analog inputs can also be mixed with the DAC outputs to any of the available analog output mixers. The figures in the appropriate analog input and output sections detail the signal routing.

Analog Full-Scale Direct to ADC Mixer Inputs

The analog inputs can also be configured to accept and route differential analog signals directly to the ADC mixers (record path, Figure 11). By disabling and bypassing the analog microphone and line input gain stages, this mode provides a reduced power configuration for full-scale (up to $1V_{RMS}$) analog input signals. Unlike the analog microphone and line input configurations, this mode does not allow the input signals to be routed directly to the analog output mixers (playback path, Figure 32).

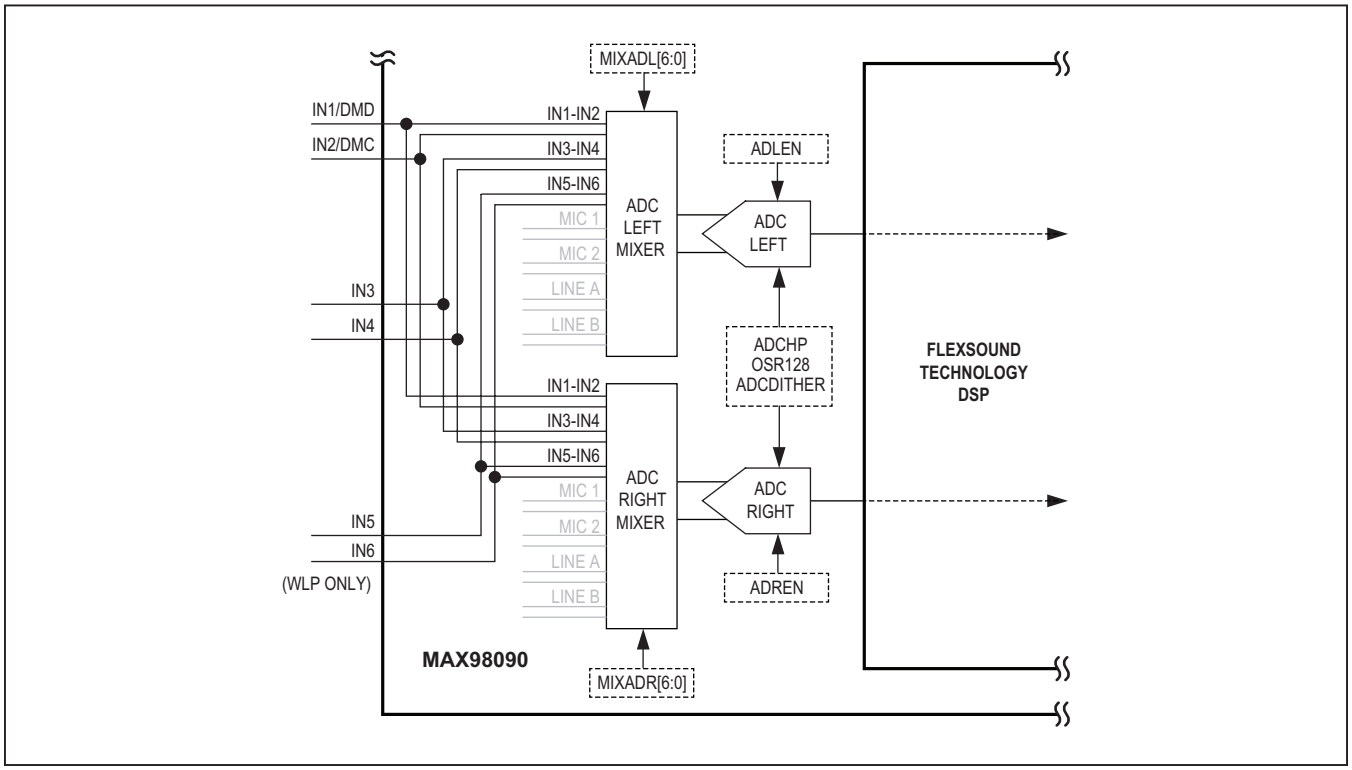


Figure 11. Analog Direct to ADC Mixer Input Functional Diagram

Audio Record Path

The device record path comprises several sequential blocks. The first block is a stereo ADC with configurable mixers that can accept input from the microphone PGAs, line input PGAs, or directly differentially from any of the analog input pairs. Internally, the digital record path has two channels (left and right), which accept a digital signal either from the appropriate digital microphone or ADC output channel. The two channels then pass through several DSP stages before being routed into the digital audio interface (DAI, Figure 12).

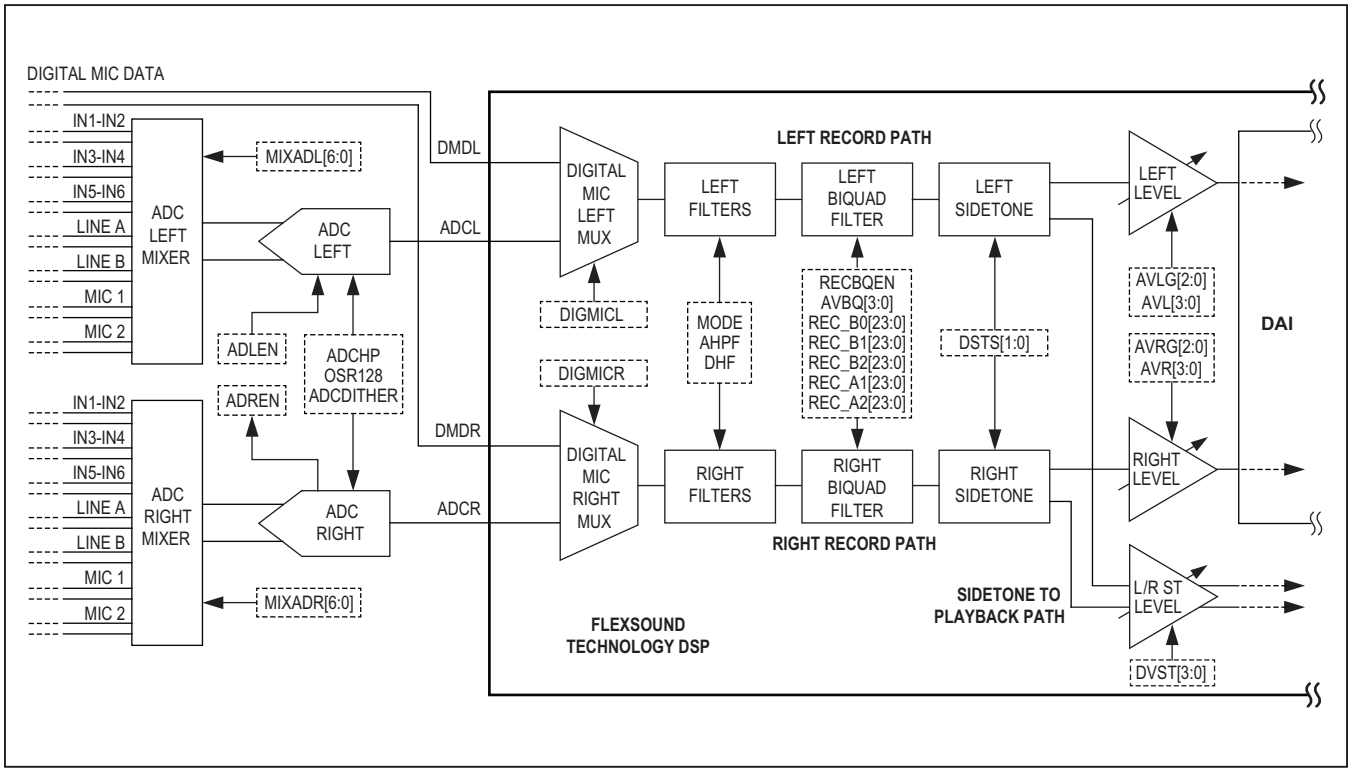


Figure 12. Record Path Block Diagram

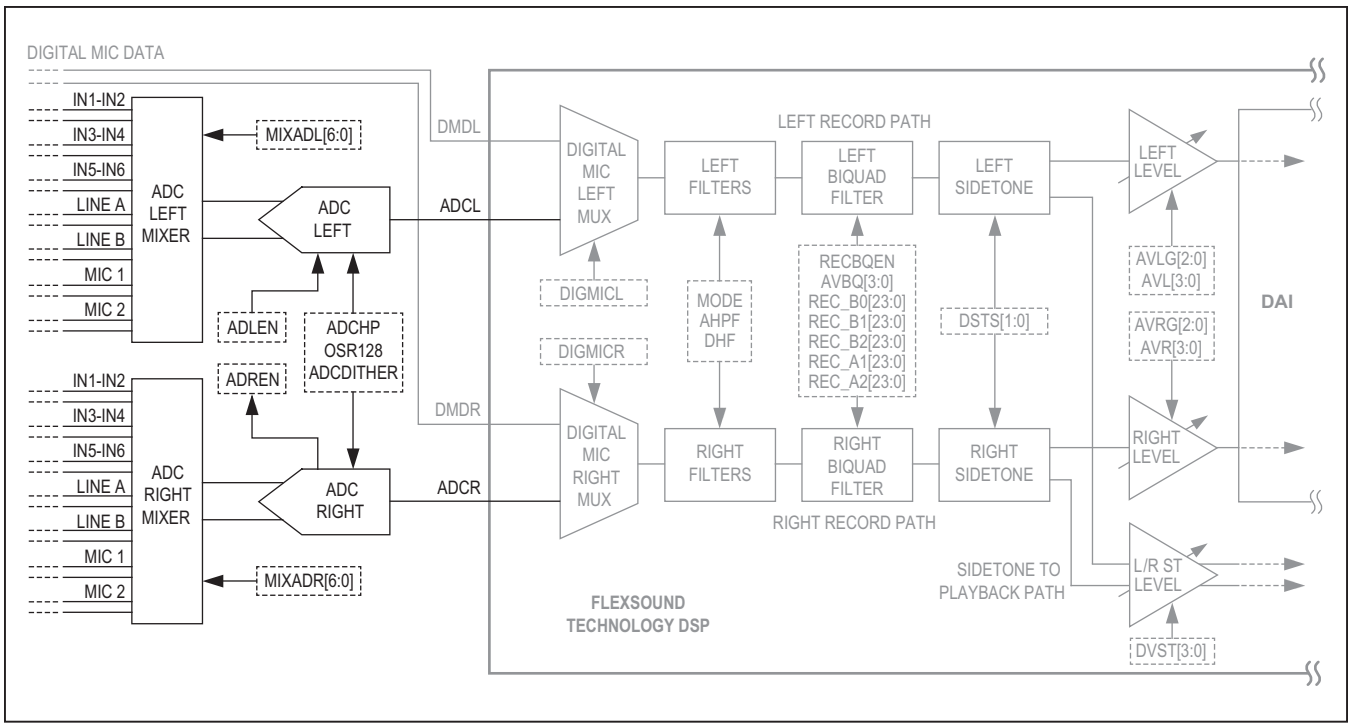


Figure 13. Record Path ADC Section

Analog-to-Digital Converter (ADC)

The stereo ADC architecture includes two independent audio paths and provides a flexible, fully configurable input mixer, two performance and power based configuration options, oversampling rate selection, and an input dither option (Figure 13). Both ADC channels can be enabled independently allowing the device to support both stereo and left or right mono configurations (Table 7).

ADC Functional Configuration

The ADC can be configured into one of two operating modes. One operating mode is optimized for maximum dynamic performance while the other is optimized for lower power consumption (Table 5). Input dither can also be added to the ADC record path. This feature consumes almost no appreciable power, but raises the RMS level of the noise floor slightly at the high end of the audio band.

The ADC supports both an over sampling rate (OSR) of 64 and 128 times the configured sampling frequency (f_S). An OSR of 128 x f_S optimizes ADC performance at the cost of slightly more power consumption than an OSR of 64 x f_S.

The DSP timing, however, places some limitations on which OSR can be used. For voice applications using standard (f_S = 8kHz) and wideband (f_S = 16kHz) sampling rates, the DSP is typically configured to utilize the voice filters (IIR). If the voice filters are enabled, the OSR is automatically configured to 128 x f_S and cannot be manually reprogrammed in order to meet timing requirements.

In most standard music/full audio range applications (where f_S = 32kHz, 44.1kHz, 48kHz, etc.) the music filters (FIR) are used. If the music filters are enabled, the OSR can be configured manually, however, the prescaled master clock (PCLK) must always be at least twice the frequency of the ADC sampling clock. To ensure this condition is met, if f_{PCLK} < 256 x f_S, then the OSR must be set to 64 x f_S. In addition, if the sampling rate exceeds 48kHz (DHF = 1, such as f_S = 96kHz), then the OSR must be configured to 64 x f_S regardless of the ratio. In any other music filter configuration, OSR = 128 can be selected as desired for optimal ADC performance.

ADC Input Mixer Configuration

The device allows for each ADC input mixer to be configured separately to accept any combination of valid input sources. The ADC mixers can accept input from the microphone PGAs (1 or 2), line input PGAs (A or B), or directly differentially from any of the analog input pairs (IN1/IN2, IN3/IN4, or IN5/IN6). The ADC input mixers then route the selected sources to the left and right ADC inputs (Tables 25 and Table 26).

Record Path FlexSound DSP

The digital record path is part of the FlexSound technology DSP and comprises multiple sequential DSP blocks. The first DSP stage contains digital filters including a voice filter (IIR), music filter (FIR), and a highpass DC-blocking filter. The next stage is a digital biquad filter with a pre-attenuation amplifier, and it is followed by a digital gain and level control stage. The record path DSP also features a digital sidetone path that is routed to and mixed into the digital playback path (Figure 14).

Record Path Digital Filters

The record path DSP includes a digital filter stage. One filter, set with the MODE bit (Table 27), offers the choice between the IIR voice filters and the FIR music filters. The IIR filters are optimized for standard (f_S = 8kHz) and wideband (f_S = 16kHz) voice applications, while the FIR filters are optimized for low power operation at higher audio/music sampling rates. For sampling rates in excess of 48kHz (f_{LRCLK} > 48kHz), use the FIR music filters and set the DHF bit. The MODE configuration selected applies to both channels of both the record and playback path DSP.

The record path DSP also features a DC-blocking filter. This filter can be used with both the IIR voice and FIR music filters, and blocks low frequency (including DC) input signals outside of the lower end of the audio band.

Table 25. Left ADC Mixer Input Configuration Register

ADDRESS: 0x15				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	MIXADL[6:0]	R/W	0	Selects microphone input 2 to left ADC mixer.
5		R/W	0	Selects microphone input 1 to left ADC mixer.
4		R/W	0	Selects line input B to left ADC mixer.
3		R/W	0	Selects line input A to left ADC mixer.
2		R/W	0	Selects IN5/IN6 differential input direct to left ADC mixer (WLP only).
1		R/W	0	Selects IN3/IN4 differential input direct to left ADC mixer.
0		R/W	0	Selects IN1/IN2 differential input direct to left ADC mixer.

Table 26. Right ADC Mixer Input Configuration Register

ADDRESS: 0x16				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	MIXADR[6:0]	R/W	0	Selects microphone input 2 to right ADC mixer.
5		R/W	0	Selects microphone input 1 to right ADC mixer.
4		R/W	0	Selects line input B to right ADC mixer.
3		R/W	0	Selects line input A to right ADC mixer.
2		R/W	0	Selects IN5/IN6 differential input direct to right ADC mixer (WLP only).
1		R/W	0	Selects IN3/IN4 differential input direct to right ADC mixer.
0		R/W	0	Selects IN1/IN2 differential input direct to right ADC mixer.

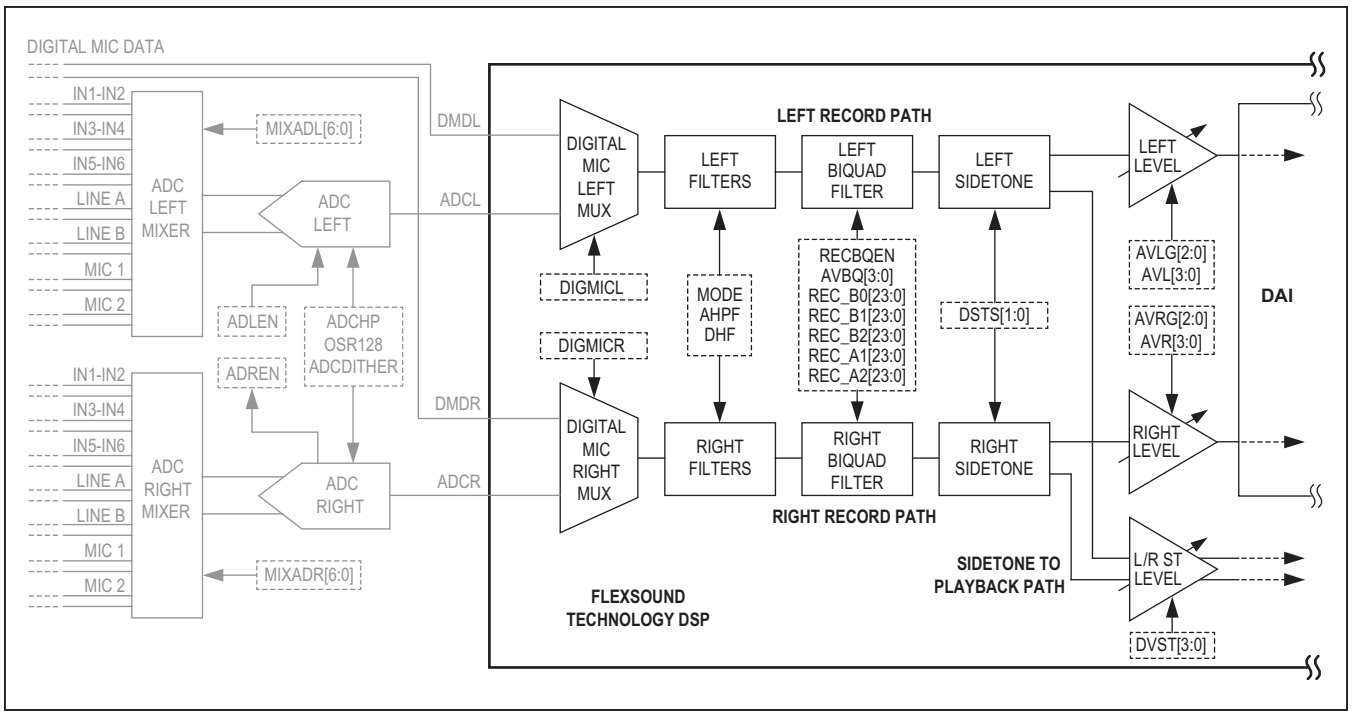


Figure 14. Record Path FlexSound Technology DSP Block

Table 27. DSP Filter Configuration Register

ADDRESS: 0x26				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MODE	R/W	1	**Enables the Codec DSP FIR Music Filters (Default IIR Voice Filters)** 0: The codec DSP filters operate in IIR voice mode with stop band frequencies below the $f_S/2$ Nyquist rate. The voice mode filters are optimized for 8kHz or 16kHz voice application use. 1: The codec DSP filters operate in a linear phase FIR audio mode optimized to maintain stereo imaging and operate at higher f_S rates while utilizing lower power.
6	AHPF	R/W	0	**Enables the Record Path DC-Blocking Filter** 0: DC-blocking filter disabled. 1: DC-blocking filter enabled.
5	DHPF	R/W	0	**Enables the Playback Path DC-Blocking Filter** 0: DC-blocking filter disabled. 1: DC-blocking filter enabled.
4	DHF	R/W	0	**Enables the DAC High Sample Rate Mode (LRCLK > 48kHz, FIR Only)** 0: LRCLK is less than 48kHz. 8x FIR interpolation filter used. 1: LRCLK is greater than 48kHz. 4x FIR interpolation filter used.
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

Record Path Biquad Filter

The record path DSP has a single stage digital biquad filter with a programmable preattenuation amplifier. The digital biquad filter configuration applies to both the left and right record channels. To enable the record path biquad filter, set RECBQEN high (Table 28). Once enabled, the level of preattenuation can be adjusted from 0dB down to -15dB (denoted A_{V_BQ}, see Table 29). The digital biquad filter cannot be set to a gain greater than ±12dB, to a Q greater than 10, or to below a minimum f_C that varies by filter type. See the Electrical Characteristics table.

The digital biquad coefficients are uninitialized at power-up, and if the filter is going to be used, the coefficients must be programmed before the device and biquad filter are enabled. The transfer function is:

$$H(z) = \frac{B_0 + B_1 \times Z^{-1} + B_2 \times Z^{-2}}{A_0 + A_1 \times Z^{-1} + A_2 \times Z^{-2}}$$

Table 28. DSP Biquad Filter Enable Register

ADDRESS: 0x41				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	RECBQEN	R/W	0	**Enable Biquad Filter in Record Path** 0: Biquad filter not used. 1: Biquad filter used in record path.
2	EQ3BANDEN	R/W	0	**Enable 3-Band EQ in Playback Path (Bands 4–7 Are Not Used)** 0: 3-band EQ disabled. 1: 3-band EQ enabled. Only valid if EQ7BANDEN = 0 and EQ5BANDEN = 0.
1	EQ5BANDEN	R/W	0	**Enable 5-Band EQ in Playback Path (Bands 6 and 7 Are Not Used)** 0: 5-band EQ disabled. 1: 5-band EQ enabled. Only valid if EQ7BANDEN = 0
0	EQ7BANDEN	R/W	0	**Enable 7-Band EQ in Playback Path** 0 : 7-band EQ disabled. 1 : 7-band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant.

Table 29. Record Path Biquad Digital Preamplifier Level Configuration Register

ADDRESS: 0x19				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	AVBQ[3:0]	R/W	0	**ADC Biquad Digital Preamplifier Gain Configuration** 0x0: +0dB 0x4: -4dB 0x8: -8dB 0xC: -12dB 0x1: -1dB 0x5: -5dB 0x9: -9dB 0xD: -13dB 0x2: -2dB 0x6: -6dB 0xA: -10dB 0xE: -14dB 0x3: -3dB 0x7: -7dB 0xB: -11dB 0xF: -15dB
2			0	
1			0	
0			0	

The digital biquad filter has five user-programmable coefficients (B_0, B_1, B_2, A_1, and A_2), and each individual coefficient is 3 bytes (24 bits) long (A_0 is fixed at 1). They occupy 15 consecutive registers (Table 30) and each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a two's complement format where the first 4 bits are the integer portion and the last 20 bits are the decimal portion (which results in an approximate +8 to -8 range for each coefficient).

Record Path Sidetone

The record path sidetone is available to allow a low-level copy of the recorded audio signal to be mixed back into the playback audio signal. When enabled, the sidetone can route the left channel, right channel, or both divided by two and then summed back into the playback path DSP. The sidetone digital gain can be programmed from -0.5dB to -60.5dB (Table 31). The digital sidetone is commonly used in telephony to allow the speaker to hear their own voice to provide a more natural user experience.

Table 30. Record Path Biquad Filter Coefficients

ADDRESS RANGE			NAME	TYPE	COEFFICIENT SEGMENT		
0xAF	0xB0	0xB1	RECORD BIQUAD COEFFICIENT B0	R/W	REC_B0[23:16]	REC_B0[15:8]	REC_B0[7:0]
0xB2	0xB3	0xB4	RECORD BIQUAD COEFFICIENT B1	R/W	REC_B1[23:16]	REC_B1[15:8]	REC_B1[7:0]
0xB5	0xB6	0xB7	RECORD BIQUAD COEFFICIENT B2	R/W	REC_B2[23:16]	REC_B2[15:8]	REC_B2[7:0]
0xB8	0xB9	0xBA	RECORD BIQUAD COEFFICIENT A1	R/W	REC_A1[23:16]	REC_A1[15:8]	REC_A1[7:0]
0xBB	0xBC	0xBD	RECORD BIQUAD COEFFICIENT A2	R/W	REC_A2[23:16]	REC_A2[15:8]	REC_A2[7:0]

Table 31. Record Path Sidetone Configuration Register

ADDRESS: 0x1A				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DSTS[1:0]		0	**Sidetone Enable and Digital Source Configuration** 00: No sidetone selected 10: Right channel 01: Left channel 11: Left + right channel
6			0	
5	—	—	—	—
4	DVST[4:0]	R/W	0	**Sidetone Digital Gain Configuration** 0x00: OFF 0x08: -14.5dB 0x10: -30.5dB 0x18: -46.5dB 0x01: -0.5dB 0x09: -16.5dB 0x11: -32.5dB 0x19: -48.5dB 0x02: -2.5dB 0x0A: -18.5dB 0x12: -34.5dB 0x1A: -50.5dB 0x03: -4.5dB 0x0B: -20.5dB 0x13: -36.5dB 0x1B: -52.5dB 0x04: -6.5dB 0x0C: -22.5dB 0x14: -38.5dB 0x1C: -54.5dB 0x05: -8.5dB 0x0D: -24.5dB 0x15: -40.5dB 0x1D: -56.5dB 0x06: -10.5dB 0x0E: -26.5dB 0x16: -42.5dB 0x1E: -58.5dB 0x07: -12.5dB 0x0F: -28.5dB 0x17: -44.5dB 0x1F: -60.5dB
3			0	
2			0	
1			0	
0			0	

Record Path Digital Gain and Level Control

The stereo record path DSP includes a digital gain and level control stage. The settings can be configured independently by channel, and are primarily used when adjusting the record level for digital microphones. The coarse digital gain adjustment can be set from 0dB to +42dB in 6dB increments, and the fine adjust level control gain can be set from -12dB to +3dB in 1dB increments (Tables 32 and 33).

Table 32. Left Record Path Digital Gain Configuration Register

ADDRESS: 0x17				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	AVLG[2:0]	R/W	0	**Left Record Path Digital Coarse Gain Configuration** 000 : 0dB 010 : +12dB 100 : +24dB 110 : +36dB 001 : +6dB 011 : +18dB 101 : +30dB 111 : +42dB
5			0	
4			0	
3	AVL[3:0]	R/W	0	**Left Record Path Digital Fine Adjust Gain Configuration** 0x0: +3dB 0x4: -1dB 0x8: -5dB 0xC: -9dB 0x1: +2dB 0x5: -2dB 0x9: -6dB 0xD: -10dB 0x2: +1dB 0x6: -3dB 0xA: -7dB 0xE: -11dB 0x3: +0dB 0x7: -4dB 0xB: -8dB 0xF: -12dB
2			0	
1			1	
0			1	

Table 33. Right Record Path Digital Gain Configuration Register

ADDRESS: 0x18				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	AVRG[2:0]	R/W	0	**Right Record Path Digital Coarse Gain Configuration** 000 : 0dB 010 : +12dB 100 : +24dB 110 : +36dB 001 : +6dB 011 : +18dB 101 : +30dB 111 : +42dB
5			0	
4			0	
3	AVR[3:0]	R/W	0	**Right Record Path Digital Fine Adjust Gain Configuration** 0x0: +3dB 0x4: -1dB 0x8: -5dB 0xC: -9dB 0x1: +2dB 0x5: -2dB 0x9: -6dB 0xD: -10dB 0x2: +1dB 0x6: -3dB 0xA: -7dB 0xE: -11dB 0x3: +0dB 0x7: -4dB 0xB: -8dB 0xF: -12dB
2			0	
1			1	
0			1	

Digital Audio Interface (DAI) Configuration

The digital audio interface (DAI) contains two primary sections (Figure 15). The first is the clock control and configuration section. The device supports both master and slave mode operation, can accept a master clock of either 256 x f_S or ranging from 10MHz to 60MHz, and can be configured for any digital audio sampling rate (f_S) from 8kHz to 96kHz. When the device is configured as the digital audio master, a variety of operating modes are available. These include a simple quick configuration mode, exact integer sampling mode, and a manual clock divider mode. When the device is configured to slave mode, the internal PLL quickly locks onto the external LRCLK frequency.

The second section is the digital audio data path control and signal routing. This section supports a variety of stereo data path configurations including serial audio input and output, audio loop through from the record to playback paths, and audio loop back from the serial data input to the serial data output. The serial data interface also supports several standard digital audio formats (PCM) including I^2S, left justified, right justified, and time division multiplexed (TDM).

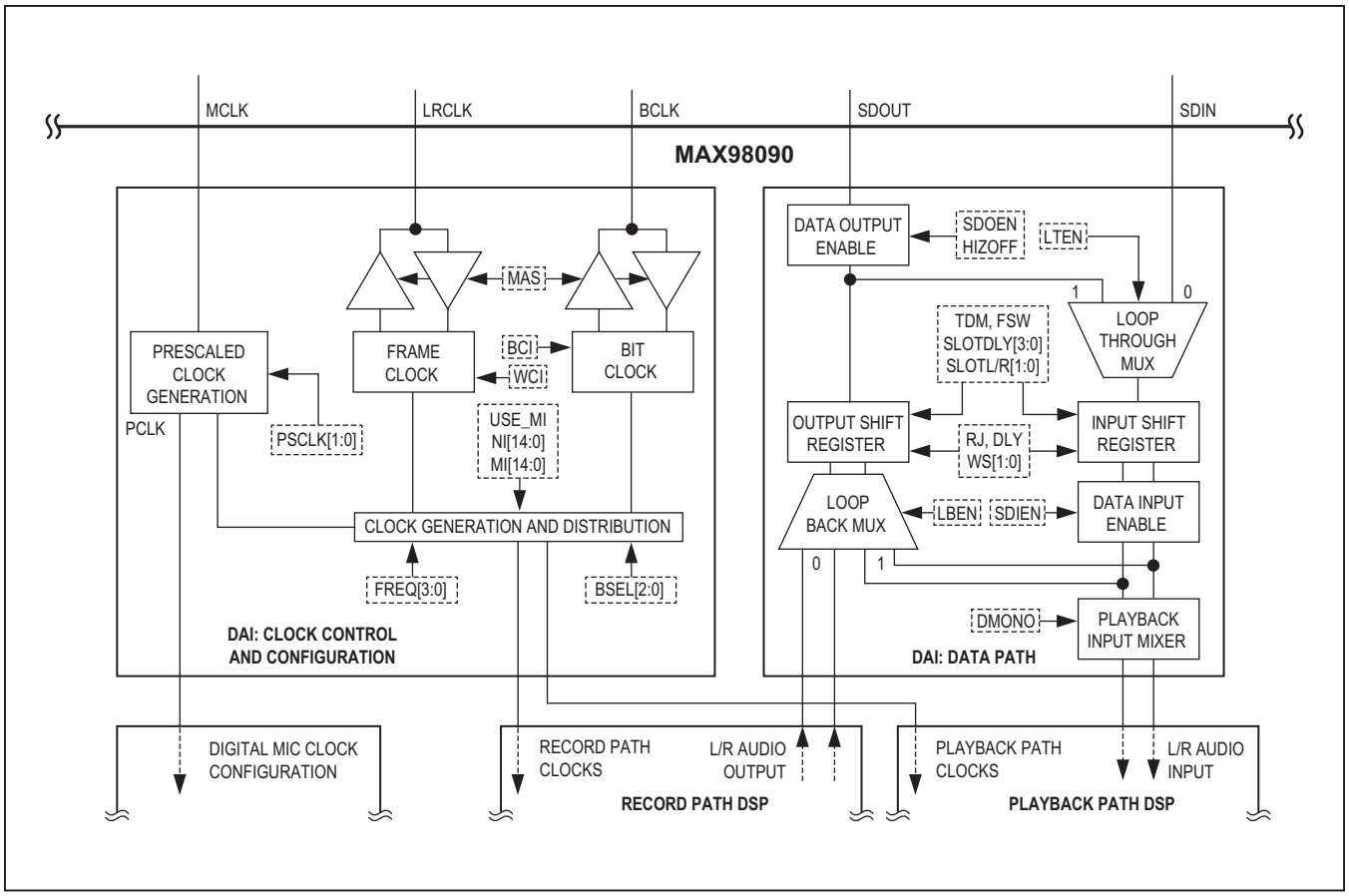


Figure 15. Simplified Digital Audio Interface Block Diagram

DAI Clock Control and Configuration

The clock control and configuration section is one of the two major blocks in the digital audio interface (Figure 16). This section is responsible for accepting and scaling the device master clock, for internal digital clock generation, and for digital audio interface data clocking and timing.

The device can accept an external master clock (MCLK) with a frequency ranging from 10MHz to 60MHz. However, for digital operation, signal processing, and data conversion the device requires an internal clock between 10MHz and 20MHz. To generate an internal master clock within this frequency range, an internal clock divider is used (Table 34). The internal clock divider can be set to frequency divide MCLK by a factor 1, 2, or 4 to create the internal prescaled master clock (PCLK). PCLK is then used, either directly or through additional divider/multiplier blocks, to clock all internal digital sections.

The digital audio interface signal paths support any sampling rate from 8kHz to 96kHz. The device has only a single DAI, and as a result both the record (output) and playback (input) digital audio paths use the same sampling rate.

The device digital audio interface supports both master and slave mode operation (Table 35). To properly time the serial data input (SDIN) and output (SDOUT), the DAI requires both a left-right frame clock (LRCLK) and a bit clock (BCLK). In master mode, the device uses one of several modes to generate both LRCLK and BCLK from the internal prescaled master clock (PCLK). In slave mode however, both LRCLK and BCLK must be externally provided.

Master Mode Clock Configuration

When the device is configured as the digital audio master, the frame clock (LRCLK) and bit clock (BCLK) are configured as outputs and the device uses the internal prescaled master clock (PCLK) to create them.

If no clock outputs or unexpected clock outputs are measured on LRCLK and/or BCLK, verify that the device is not in shutdown and that all three clocks are configured correctly. If the master clock prescale value is not selected (PSCLK[1:0]), the clock ratio is not fully configured (operating mode), or if the bit clock rate is not set (BSEL[2:0])

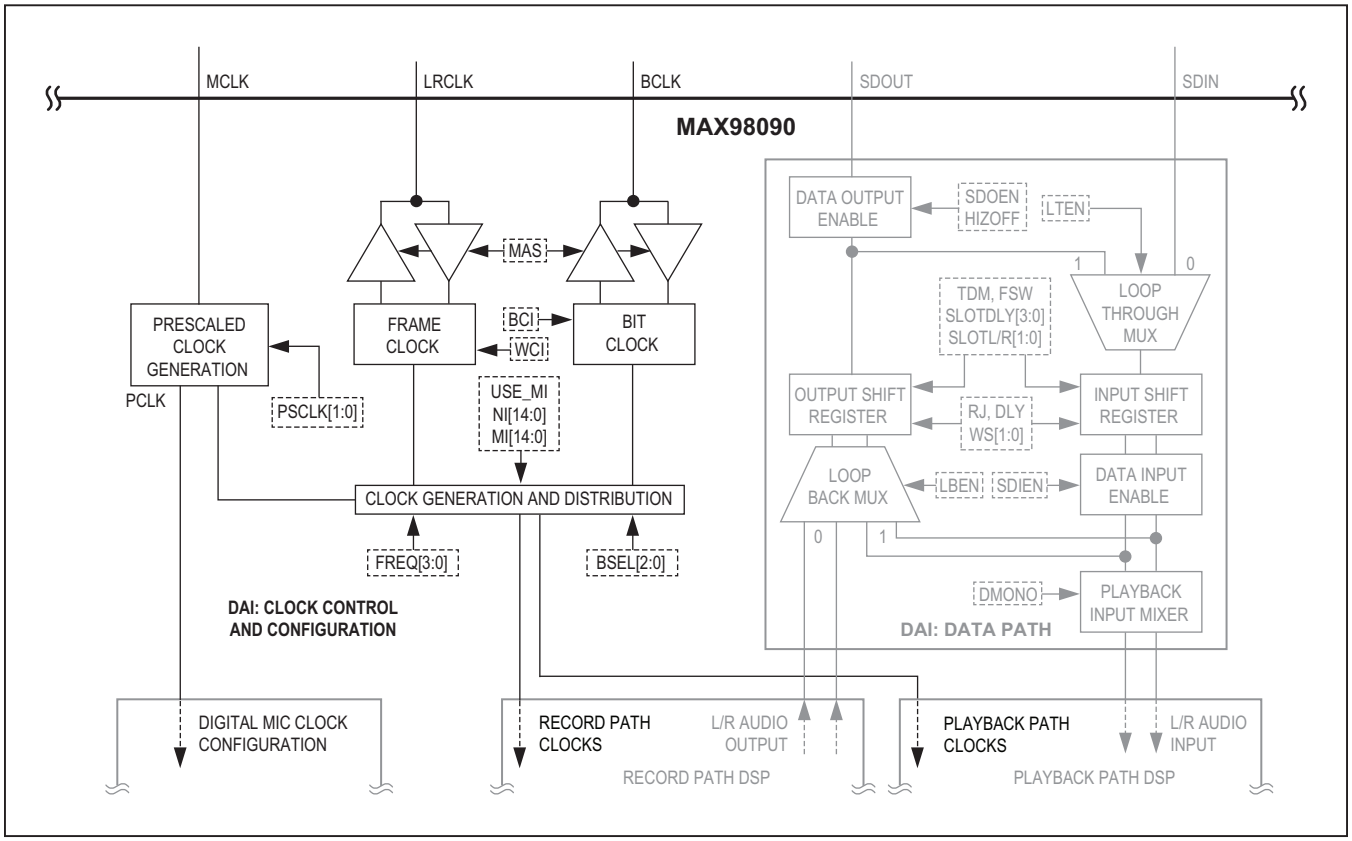


Figure 16. DAI Clock Control and Configuration Section

Table 34. System Master Clock (MCLK) Prescaler Configuration Register

ADDRESS: 0x1B				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	PSCLK[1:0]	R/W	0	**Master Clock (MCLK) Prescaler Configuration** 00: Internal master clock generation disabled 01: $f_{PCLK} = f_{MCLK}/1$, 10MHz ≤ f_{MCLK} ≤ 20MHz 10: $f_{PCLK} = f_{MCLK}/2$, 20MHz < f_{MCLK} ≤ 40MHz 11: $f_{PCLK} = f_{MCLK}/4$, 40MHz < f_{MCLK} ≤ 60MHz
4			0	
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

Table 35. Master Mode Clock Configuration Register

ADDRESS: 0x21				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MAS	R/W	0	Master Mode Enable 0: Slave mode (LRCLK/BCLK are inputs and accept external clock sources). 1: Master mode (LRCLK/BCLK are outputs and timing signals are generated internally).
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	BSEL[2:0]	R/W	0	**Bit Clock (BCLK) Configuration (Master Mode/Slave Right Justified Only)** 000: Bit clock disabled 001: $f_{BCLK} = 32 \times f_S$ 010: $f_{BCLK} = 48 \times f_S$ 011: $f_{BCLK} = 64 \times f_S$ 100: $f_{BCLK} = f_{PCLK}/2$ 101: $f_{BCLK} = f_{PCLK}/4$ 110: $f_{BCLK} = f_{PCLK}/8$ 111: $f_{BCLK} = f_{PCLK}/16$
1			0	
0			0	

then no valid clock output is present. In addition to this, the device does not generate any clocks unless at least one valid digital audio data path is enabled (ADC record, DAC playback, digital microphone input, etc.).

In master mode, the device uses two integer values (NI and MI) as a multiplier and divider (respectively) to scale PCLK into LRCLK. BCLK is then created either from a PCLK divider or from an LRCLK multiplier (Table 35). Based on the oversampling rate selected (OSR, see the *ADC Functional Configuration* section), and the configured NI/MI ratio, the output LRCLK frequency is calculated with the following relationship:

$$f_{LRCLK} = f_{PCLK} \times \frac{NI}{MI \times OSR}$$

This expression illustrates that in master mode, the relationship between LRCLK and PCLK frequency (as well as BCLK) is based on an integer ratio. As a result, any cycle to cycle jitter or absolute frequency variation in MCLK is translated first into PCLK and then into LRCLK (and BCLK) based on the selected clock ratios.

In master mode, the device provides three clock operating modes. In reality all three modes operate in exactly the same manner (using an internal MI and NI ratio to create LRCLK). However, the first two modes will internally set NI and MI automatically and are provided as configuration shortcuts for commonly used PCLK to LRCLK ratios. The three operating modes are detailed below, and are presented in order of activation priority.

Quick Configuration Mode

In quick configuration mode, the master clock frequency (Table 36) and sample rate (Table 37) are selected from a list of commonly used frequencies. Only a single bit in each quick setup register can be enabled at any given time. Quick configuration mode is activated anytime that both a master clock frequency quick setup bit and a sample rate quick setup bit are concurrently enabled. Once enabled, this mode supersedes both of the other operating modes and an internal preset ratio for NI and MI is used to create LRCLK. As a result, when Quick Configuration Mode is enabled the exact integer mode settings (Table 39), and the manual ratio mode settings (Tables 40 to 43) are preserved but ignored. If this mode is later disabled, the preserved settings of any active lower precedence modes reassert.

To ensure that the DSP is optimally configured and that all timing requirements are met, when using quick configuration mode the master clock divider (PSCLK, Table 34), digital filters (MODE, Table 27), and ADC oversampling rate (OSR128, Table 5) are automatically configured. While in quick configuration mode these registers are

Table 36. Master Clock Quick Setup Register

ADDRESS: 0x04				DESCRIPTION
BIT	NAME	TYPE	POR	
7	26M	R/W	0	Setup device for operation with a 26MHz master clock (MCLK).
6	19P2M	R/W	0	Setup device for operation with a 19.2MHz master clock (MCLK).
5	13M	R/W	0	Setup device for operation with a 13MHz master clock (MCLK).
4	12P288M	R/W	0	Setup device for operation with a 12.288MHz master clock (MCLK).
3	12M	R/W	0	Setup device for operation with a 12MHz master clock (MCLK).
2	11P2896M	R/W	0	Setup device for operation with a 11.2896MHz master clock (MCLK).
1	—	—	—	—
0	$256F_S$	R/W	0	Setup device for operation with a 256 x f_S MHz master clock (MCLK)

Table 37. Sample Rate Quick Setup Register

ADDRESS: 0x05				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	SR_96K	R/W	0	Setup clocks and filters for a 96kHz sample rate.
4	SR_32K	R/W	0	Setup clocks and filters for a 32kHz sample fate.
3	SR_48K	R/W	0	Setup clocks and filters for a 48kHz sample rate.
2	SR_44K1	R/W	0	Setup clocks and filters for a 44.1kHz sample rate.
1	SR_16K	R/W	0	Setup clocks and filters for a 16kHz sample rate.
0	SR_8K	R/W	0	Setup clocks and filters for an 8kHz sample rate.

fixed and cannot be manually changed. In this mode, when the sample rate is set to 8kHz or 16kHz, voice filters (IIR) are automatically selected and the ADC oversampling rate is fixed to 128. For any other selected sample rate, music filters (FIR) are selected and the ADC oversampling rate is configured to insure that the pre-scaled master clock frequency is greater than or equal to 256 x fS. If $f_{PCLK} \geq 256 \times f_S$ then the oversampling rate (OSR) is set to 128, otherwise OSR is set to 64. Table 38 provides a complete lookup table for the resulting quick configuration mode settings.

Exact Integer Mode

In exact integer mode, the master clock frequency and sample rate can be set to one of eight preprogrammed combinations (Table 39). There are four different available master clock frequencies (12MHz/13MHz/16MHz/19.2MHz), each of which can be selected with a sampling rate (f_S) of either 8kHz or 16kHz. Once a configuration is selected, the NI and MI bits are internally programmed to the correct ratio. These combinations are primarily intended for standard or wideband voice applications.

Table 38. Quick Configuration Mode Lookup

SELECTED MASTER CLOCK FREQUENCY			SELECTED SAMPLE RATE (kHz)					
			8	16	32	44.1	48	96
f_{MCLK}	DIVIDER	f_{PCLK}	VOICE FILTER (IIR)		MUSIC FILTER (FIR)			
26MHz	2	13Mhz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64
19.2MHz	1	19.2Mhz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64
13MHz	1	13Mhz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64
12.288MHz	1	12.288Mhz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64
12MHz	1	12MHz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64
11.2896MHz	1	11.2896MHz	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64	OSR = 64
256 x f_S	1	256 x f_S	OSR = 128	OSR = 128	OSR = 128	OSR = 128	OSR = 64	—
	2	128 x f_S	—	—	—	—	—	OSR = 64

Table 39. Clock Mode Configuration Register

ADDRESS: 0x1C				DESCRIPTION
BIT	NAME	TYPE	POR	
7	FREQ[3:0]	R/W	0	**Exact Integer Sampling Frequency (LRCLK) Configuration** Configure the DAI for specific PCLK to LRCLK ratios for f_S = 8kHz/16kHz operation (voice modes). Any setting other than 0x0 overrides manual ratio mode settings. 0000: Disabled 1XXX: Enabled Other combinations are reserved When enabled, the following PCLK to LRCLK ratios are available: 1000: f_{PCLK} = 12MHz, f_{LRCLK} = 8kHz 1001: f_{PCLK} = 12MHz, f_{LRCLK} = 16kHz 1010: f_{PCLK} = 13MHz, f_{LRCLK} = 8kHz 1011: f_{PCLK} = 13MHz, f_{LRCLK} = 16kHz 1100: f_{PCLK} = 16MHz, f_{LRCLK} = 8kHz 1101: f_{PCLK} = 16MHz, f_{LRCLK} = 16kHz 1110: f_{PCLK} = 19.2MHz, f_{LRCLK} = 8kHz 1111: f_{PCLK} = 19.2MHz, f_{LRCLK} = 16kHz
6			0	
5			0	
4			0	
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	USE_MI	R/W	0	**Use MI[15:0] in Addition to NI[14:0] to set an Accurate Frequency Ratio** 0 : MI = 65536; NI = (f_{LRCLK} / f_{PCLK}) x 65536 x 96 1 : MI is set to the value of MI[15:0] (Table 42 and Table 43).

When FREQ[3:0] register is set to 0 (FREQ[3:0] = 0000), exact integer mode is disabled. When the MSB is set to 1 (FREQ[3:0] = 1XXX) exact integer mode is enabled and the remaining bits determine which setting is selected (Table 39). If exact integer mode is enabled, the manual ratio mode settings (Tables 40 to 43) are preserved but ignored. However, if this mode is later disabled, the manual ratio mode settings reassert.

Manual Ratio Mode

In manual ratio mode, the NI and MI registers (Table 40 to Table 43) are directly programmed to set up the clock ratio. Manual ratio mode is only active when the quick Configuration and Exact Integer Modes are disabled. In manual ratio mode, if USE_MI (Table 39) is set to 0, MI is fixed at its maximum value of 0xFFFF (65536) and the programmed value has no effect. For optimal performance (especially with any noninteger PCLK to LRCLK ratio), set USE_MI to 1 and calculate both MI and NI.

To calculate the appropriate NI and MI value, use the following method:

1) Choose the over sampling rate (OSR). If $f_{PCLK} < 256 \times f_{LRCLK}$, then OSR must be set to 64. Otherwise, OSR can be set to either 128 or 64. For optimal performance, choose OSR = 128 when possible.
2) Calculate the oversampling frequency using the LRCLK frequency, and the selected oversampling rate:

$$f_{OSR} = f_{LRCLK} \times OSR.$$

3) Calculate MI using the prescaled master clock frequency, and the greatest common denominator (GCD) of the prescaled master clock frequency and the calculated oversampling frequency:

$$MI = f_{PCLK} / GCD(f_{PCLK}, f_{OSR})$$

4) Calculate NI using the calculated oversampling frequency and MI value:

$$NI = f_{OSR} \times MI / f_{PCLK}$$

Slave Mode Clock Configuration

When the device is configured as a digital audio slave, the frame clock (LRCLK) and bit clock (BCLK) are configured as external inputs. These inputs accept an externally generated frame and bit clock, and then an internal PLL determines the correct PCLK to LRCLK frequency ratio. Within a few LRCLK cycles, the internal PLL is locked onto the clock ratio and then automatically programs the internal divider ratio appropriately. The external clocks must not violate the minimum PCLK to LRCLK frequency ratio. See the Input Clock Characteristics table. If the minimum clock ratio is not satisfied, the FlexSound DSP will not have enough clock cycles to operate correctly. As a result, the audio quality and specifications are severely compromised.

In slave mode, the clock generation register settings have no effect (quick configuration, exact integer, and manual ratio mode settings have no effect). The correct MCLK to PCLK scaling factor, mode (voice/audio), and oversampling rate still need to be programmed. However, all other clock configuration settings are for master mode only. The only exception to this is when the digital audio format is set to slave mode operation with right justified data. In this configuration, the BCLK setting (BSEL[2:0], Table 35) is used to determine the number of leading padding bits (BCLK cycles) to insert (skip) before the data transmission/receiving in each frame.

Table 40. Manual Clock Ratio Configuration Register (NI MSB)

ADDRESS: 0x1D				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	NI[14:8]	R/W	0	Upper half of the PLL N value used in master mode clock generation to calculate the frequency ratio (manual ratio master mode).
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 41. Manual Clock Ratio Configuration Register (NI LSB)

ADDRESS: 0x1E				DESCRIPTION
BIT	NAME	TYPE	POR	
7	NI[7:0]	R/W	0	Lower half of the PLL N value used in master mode clock generation to calculate the frequency ratio (manual ratio master mode).
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 42. Manual Clock Ratio Configuration Register (MI MSB)

ADDRESS: 0x1F				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MI[15:8]	R/W	0	Upper half of the PLL M value used in master mode clock generation to calculate an accurate noninteger frequency ratio (manual ratio master mode).
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 43. Manual Clock Ratio Configuration Register (MI MSB)

ADDRESS: 0x20				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MI[7:0]	R/W	0	Lower half of the PLL M value used in master mode clock generation to calculate an accurate noninteger frequency ratio (manual ratio master mode).
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

DAI Digital Audio Data Path Control and Routing

The digital audio data path section supports a variety of stereo data path configurations and formats (Figure 17).

The standard configuration is to route either the record path digital audio output to the serial data output (record path to SDOUT) or to route the serial data input to the digital audio playback path (SDIN to playback path). These two primary configurations can be used either individually or together as needed by the application.

The DAI data path also supports two loop configurations. Loop back mode takes the digital audio serial data input and routes it back to the serial data output (SDIN to SDOUT). Loop through mode allows the record path audio data output to be looped through to the digital audio playback path (and can be combined with the record path to SDOUT configuration if desired). The configuration settings for all valid data path combinations are detailed in Table 44 and are illustrated in Figure 18.

SDOUT can be configured to go to either a high impedance state or to drive a valid logic level (LSB) after all data bits have been transmitted. When high impedance mode is enabled, SDOUT goes to a high-impedance state quickly after the BCLK edge for the LSB occurs to avoid potential bus contention. SDIN/loopthrough audio data can be routed through the playback path input mixer as either stereo audio data, or as a mono representation of the input audio data. By default, playback mono mode is disabled and the left/right input audio data is routed to the left/right playback channels respectively. If playback mono mode is enabled, the input audio data channels are reduced in amplitude by 6dB, mixed together (summed), and then routed to both the left and right record path channels. The full list of DAI data path configuration control bits are detailed in Table 45.

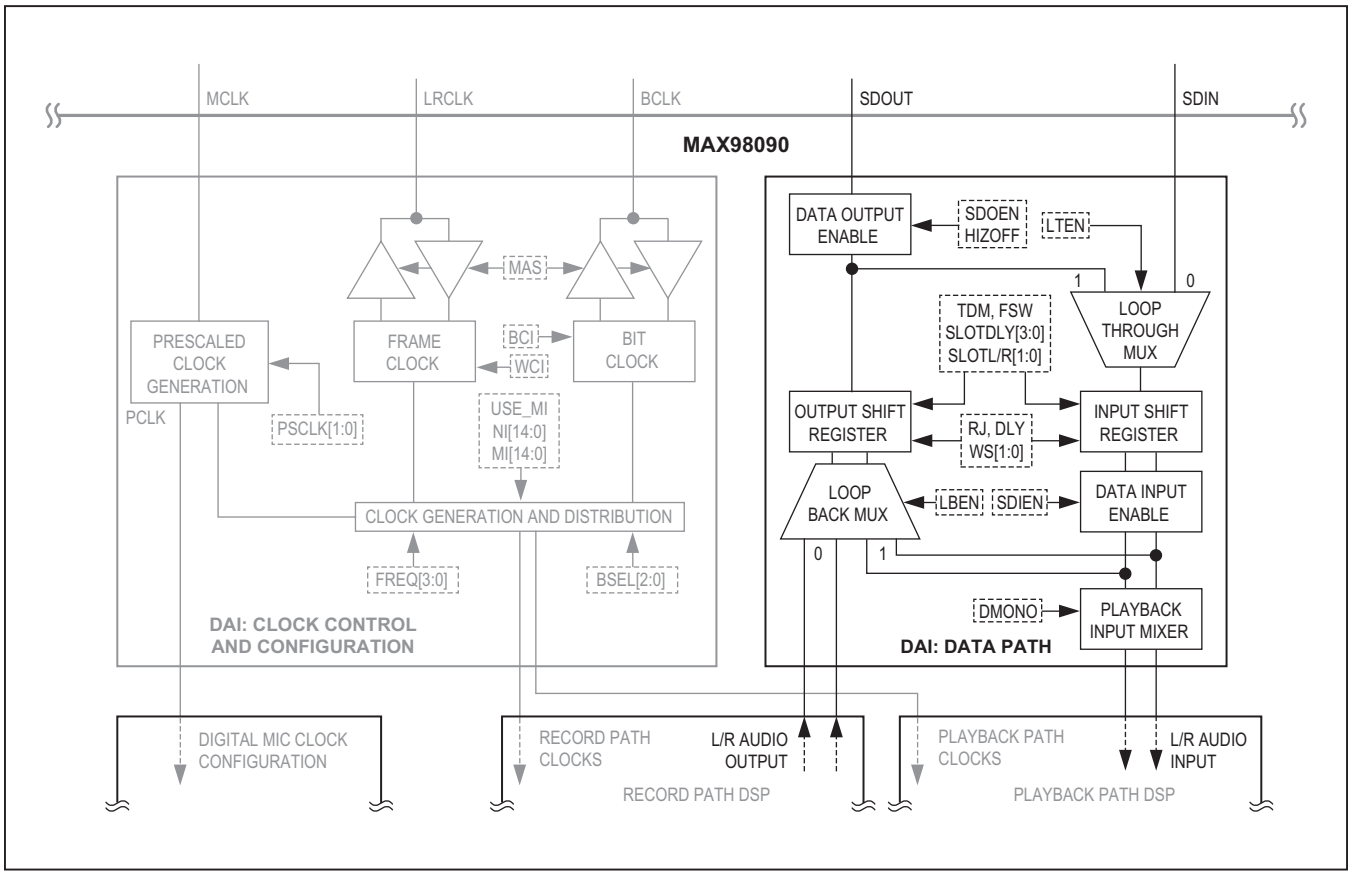


Figure 17. DAI Digital Data Path Configuration

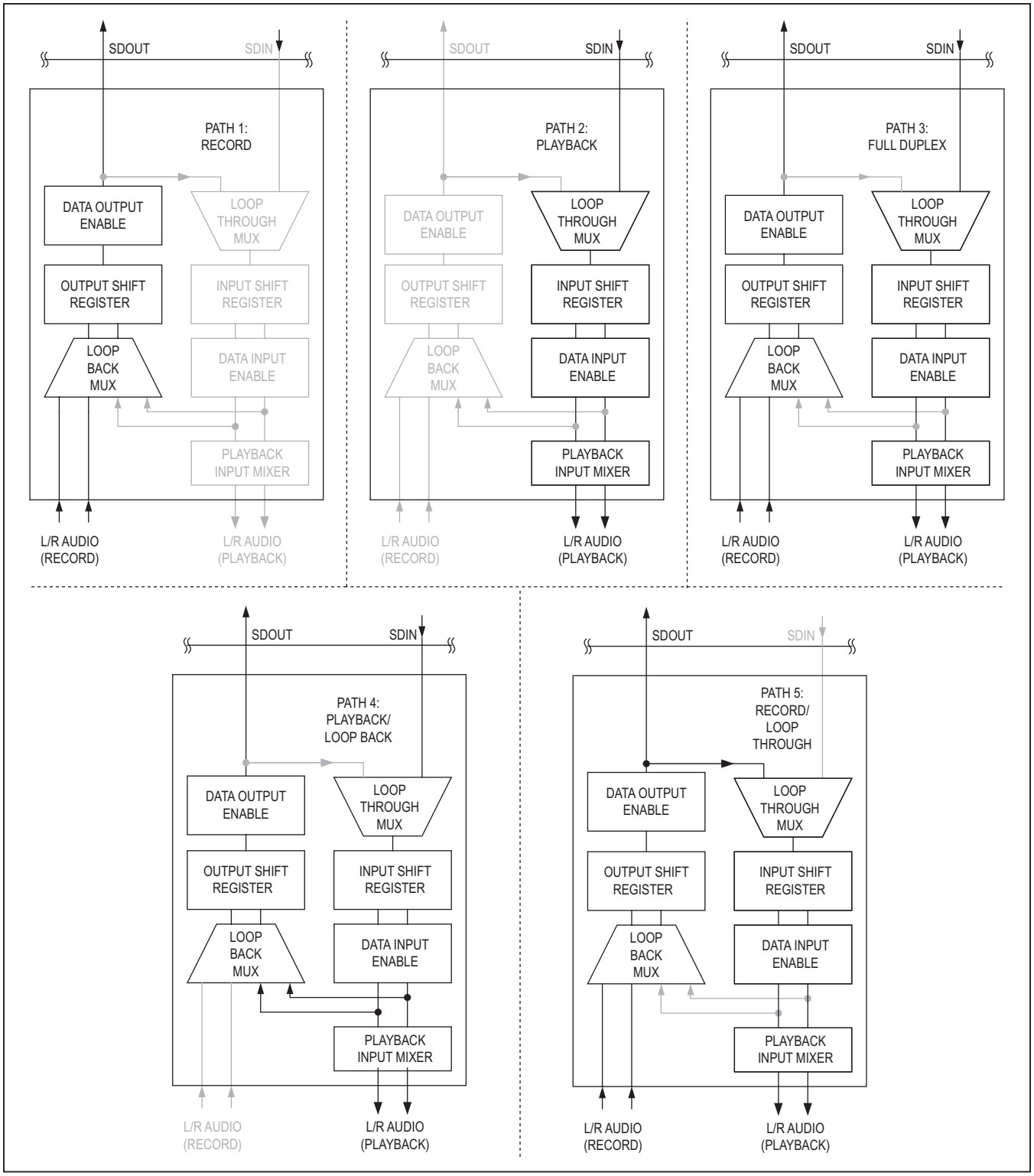


Figure 18. Digital Audio Interface (DAI) Data Path Configurations

Table 44. Digital Audio Interface (DAI) Data Path Configurations

DAI DATA PATH CONFIGURATION					
PATH	**DESCRIPTION**	**SDOEN**	**SDIEN**	**LTEN**	**LBEN**
—	DAI data path disabled	0	0	0	0
1	Record path to serial data output	1	0	0	0
2	Serial data input to playback path	0	1	0	0
3	Record path to serial data output/serial data input to playback path	1	1	0	0
4	Serial data input loop back to serial data output	1	1	0	1
5	Record path to serial data output and loop through to playback path	1	1	1	0
—	Invalid configurations	All other combinations			

Table 45. Digital Audio Interface (DAI) Input/Output Configuration Register

ADDRESS: 0x25				DESCRIPTION
BIT	**NAME**	**TYPE**	**POR**	
7	—	—	—	—
6	—	—	—	—
5	LTEN	R/W	0	**Enables Data Loop Through (Playback Path to Record Path)** 1: ADC to DAC loop-through enabled. 0: ADC to DAC loop-through disabled.
4	LBEN	R/W	0	**Enables Data Loop Back (SDIN to SDOUT)** 1: DAI SDIN used as SDOUT data source. 0: ADC used as SDOUT data source.
3	DMONO	R/W	0	**Enables Playback Mono Mode (SDIN L/2 + R/2 to Playback Path)** 1: The left- and right-channel SDIN audio input data are reduced in gain by 6dB, mixed together (summed), and routed to both the left and right record paths. 0: The left- and right-channel SDIN audio input data are routed to the left and right record path channels.
2	HIZOFF	R/W	0	**Disables Hi-Z Mode for SDOUT** 1: SDOUT drives a valid logic level after all data bits have been transmitted. 0: SDOUT goes to a high-impedance state after all data bits have been transmitted, allowing the SDOUT bus to be shared by other devices.
1	SDOEN	R/W	0	**Enables the Serial Data Output (SDOUT)** 1: Serial data output enabled. 0: Serial data output disabled.
0	SDIEN	R/W	0	**Enables the Serial Data Input (SDIN/Loop-Through)** 1: Serial data input enabled. 0: Serial data input disabled.

DAI Digital Audio Data Format

The serial data interface supports multiple pulse code modulated (PCM) digital audio formats including I²S, left justified, right justified, and time division multiplexed (TDM). If TDM mode is enabled, it takes precedence and the DAI data is in TDM format. In this case, all non-TDM digital audio data format configuration registers have no effect.

If TDM mode is disabled, then the data format is determined by the configuration selected by the control bits detailed in Table 46. These settings can be used to change the DAI data format to several supported standards such as I²S (Figure 19), left justified (Figure 20) or right justified (Figure 21). In addition, the configuration settings can be enabled or disabled independently, allowing the device to support many nonstandard data format variations.

Table 46. Digital Audio Interface (DAI) Format Configuration Register

ADDRESS: 0x22				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	RJ	R/W	0	**Configures the DAI for Right Justified Mode (No Data Delay)** 0: Left justified mode enabled with optional data delay. 1: Right justified mode enabled. DLY register is not used and BSEL[2:0] is used to determine the timing (see the *DAI Clock Control* and *Configuration* section for details). **Note:** TDM has priority over all other data formats.
4	WCI	R/W	0	**Configures the DAI for Frame Clock (LRCLK) Inversion** TDM = 0: 1: Right-channel data is transmitted while LRCLK is low. 0: Left-channel data is transmitted while LRCLK is low. TDM = 1: 0: Start of a new frame is signified by the rising edge of the LRCLK pulse. 1: Start of a new frame is signified by the falling edge of the LRCLK pulse.
3	BCI	R/W	0	**Configures the DAI for Bit Clock (BCLK) Inversion** 1: SDIN is accepted on the falling edge of BCLK. 0: SDIN is accepted on the rising edge of BCLK. Master Mode: 1: LRCLK transitions occur on the rising edge of BCLK. 0: LRCLK transitions occur on the falling edge of BCLK.
2	DLY	R/W	0	**Configures the DAI for Data Delay (I²S Standard)** 1: The most significant bit of an audio word is latched at the second BCLK edge after the LRCLK transition. 0: The most significant bit of an audio word is latched at the first BCLK edge after the LRCLK transition. Set DLY = 1 to conform to the I²S standard. DLY is only effective when TDM = 0.
1	WS[1:0]	R/W	0	**DAI Input Data Word Size (TDM = 0)** If RJ = 1: 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved If RJ = 0: 00: 16 bits 01, 10, 11: 20 bits
0			0	

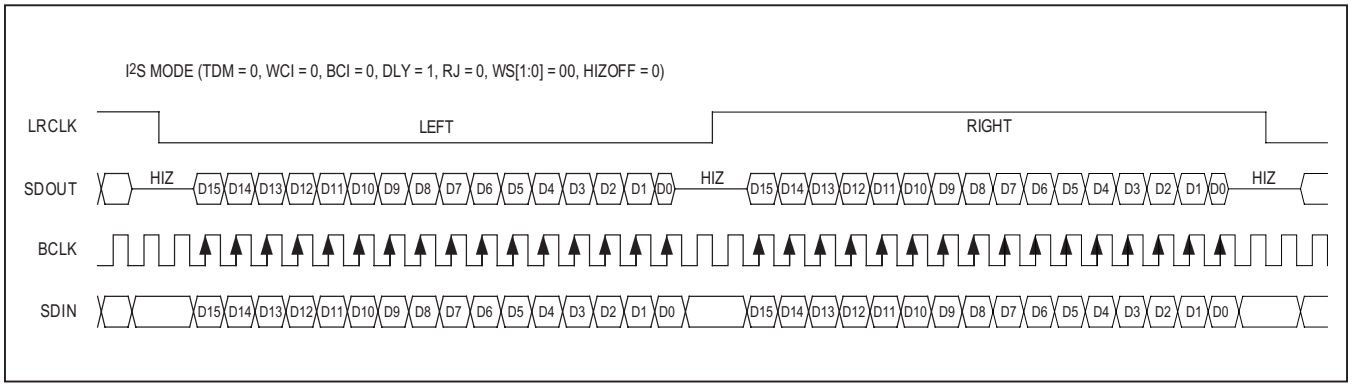


Figure 19. DAI Timing for I²S Data Format

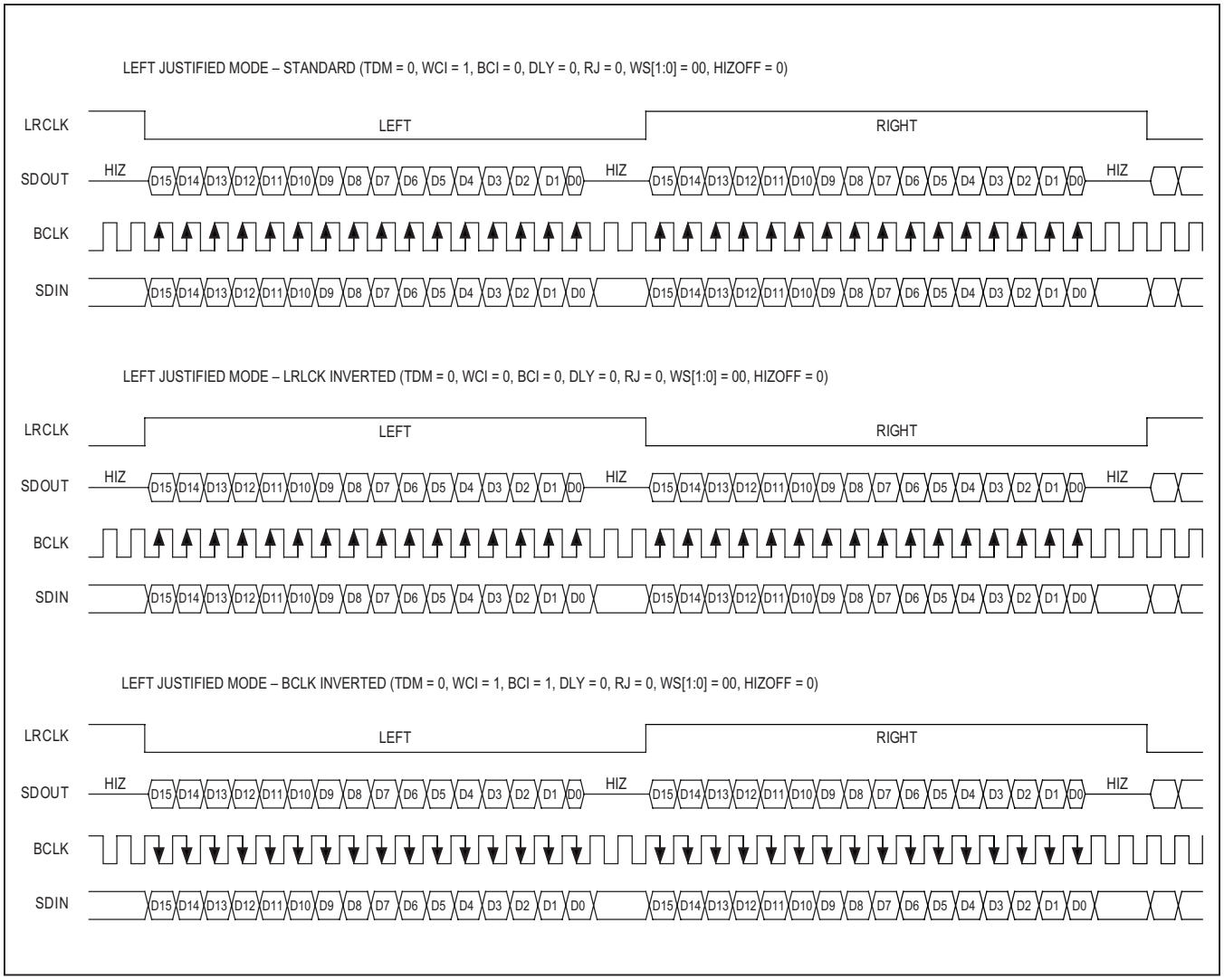


Figure 20. DAI Timing for Left Justified Data Formats

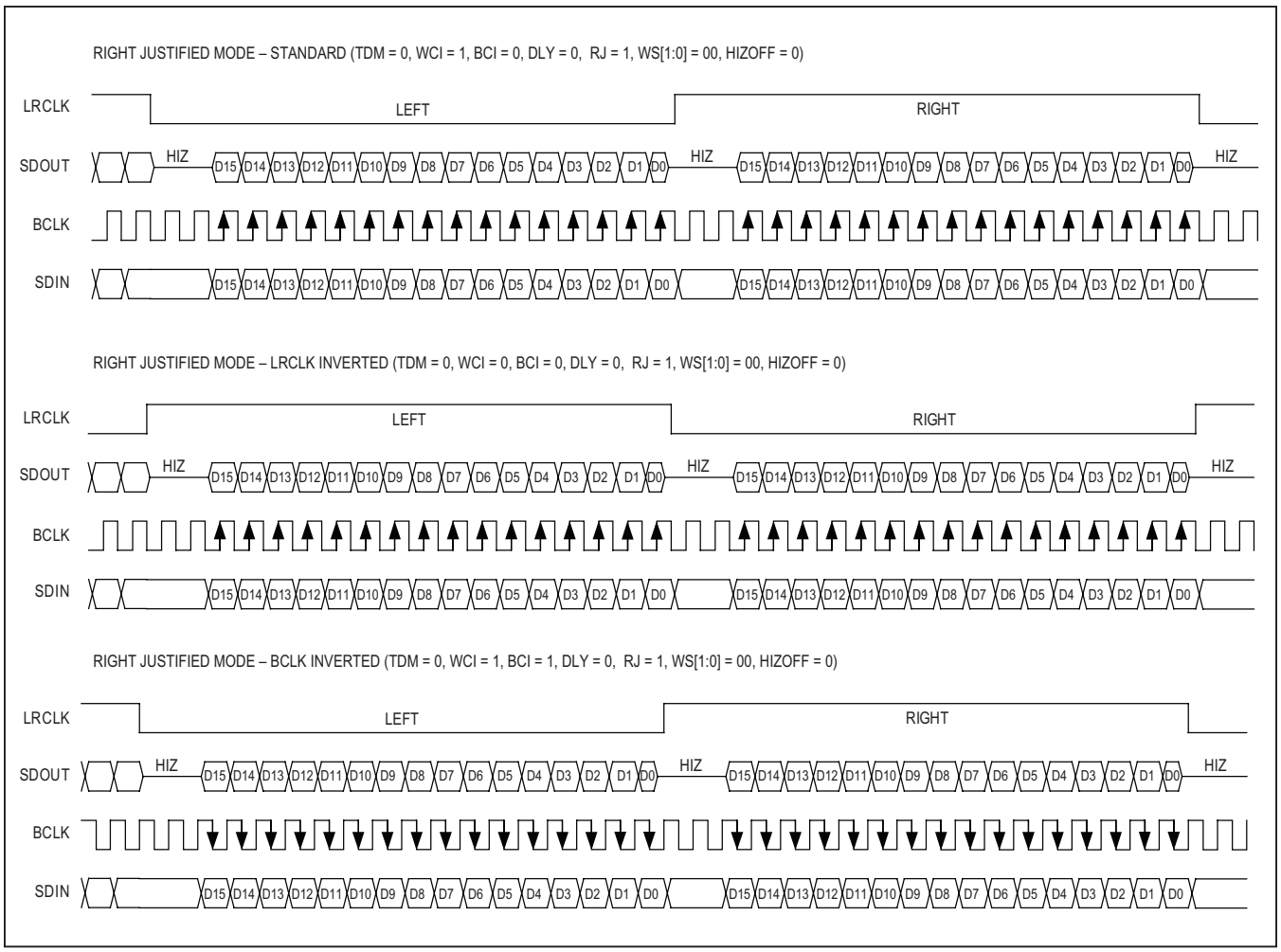


Figure 21. DAI Timing for Right Justified Data Formats

TDM Mode Data Format

If TDM mode is enabled (Table 47), the register settings in Table 39 have no effect. TDM mode supports up to four mono audio time slots in each frame. However, internally, the device only has two digital audio channels (left and right) that can be assigned to any two of the four available time frames (Table 48). The remaining two time slots remain free for another device to utilize. A data delay can be set individually for each time frame, and when operating in master mode the frame sync pulse can be set to transmit for either a single bit or an entire word in length. TDM mode timing for common configuration options is detailed in Figure 22.

Table 47. Digital Audio Interface (DAI) TDM Control Register

ADDRESS: 0x23				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	FSW	R/W	0	**Configures the DAI Frame Sync Pulse Width (TDM = 1 and MAS = 1)** 1: Frame sync pulse has a 50% duty cycle. 0: Frame sync pulse is one bit wide. **Note:** In slave mode, the device accepts a frame sync pulse width up to frame width - 1.
0	TDM	R/W	0	**Enable for Time Division Multiplex (TDM) Mode** 1: Enable TDM mode and configures the DAI to transmit and receive TDM data. 0: Disable TDM mode.

Table 48. Digital Audio Interface (DAI) TDM Format Register

ADDRESS: 0x24				DESCRIPTION
BIT	NAME	TYPE	POR	
7	SLOTL[1:0]	R/W	0	**Selects the Time Slot to use for Left-Channel Data in TDM Mode** 00: Time slot 1 10: Time slot 3 01: Time slot 2 11: Time slot 4
6			0	
5	SLOTR[1:0]	R/W	0	**Selects the Time Slot to use for Right-Channel Data in TDM Mode** 00: Time slot 1 10: Time slot 3 01: Time slot 2 11: Time slot 4
4			0	
3	SLOTDLY[3:0]	R/W	0	Enables data delay for slot 4 in TDM mode.
2			0	Enables data delay for slot 3 in TDM mode.
1			0	Enables data delay for slot 2 in TDM mode.
0			0	Enables data delay for slot 1 in TDM mode.

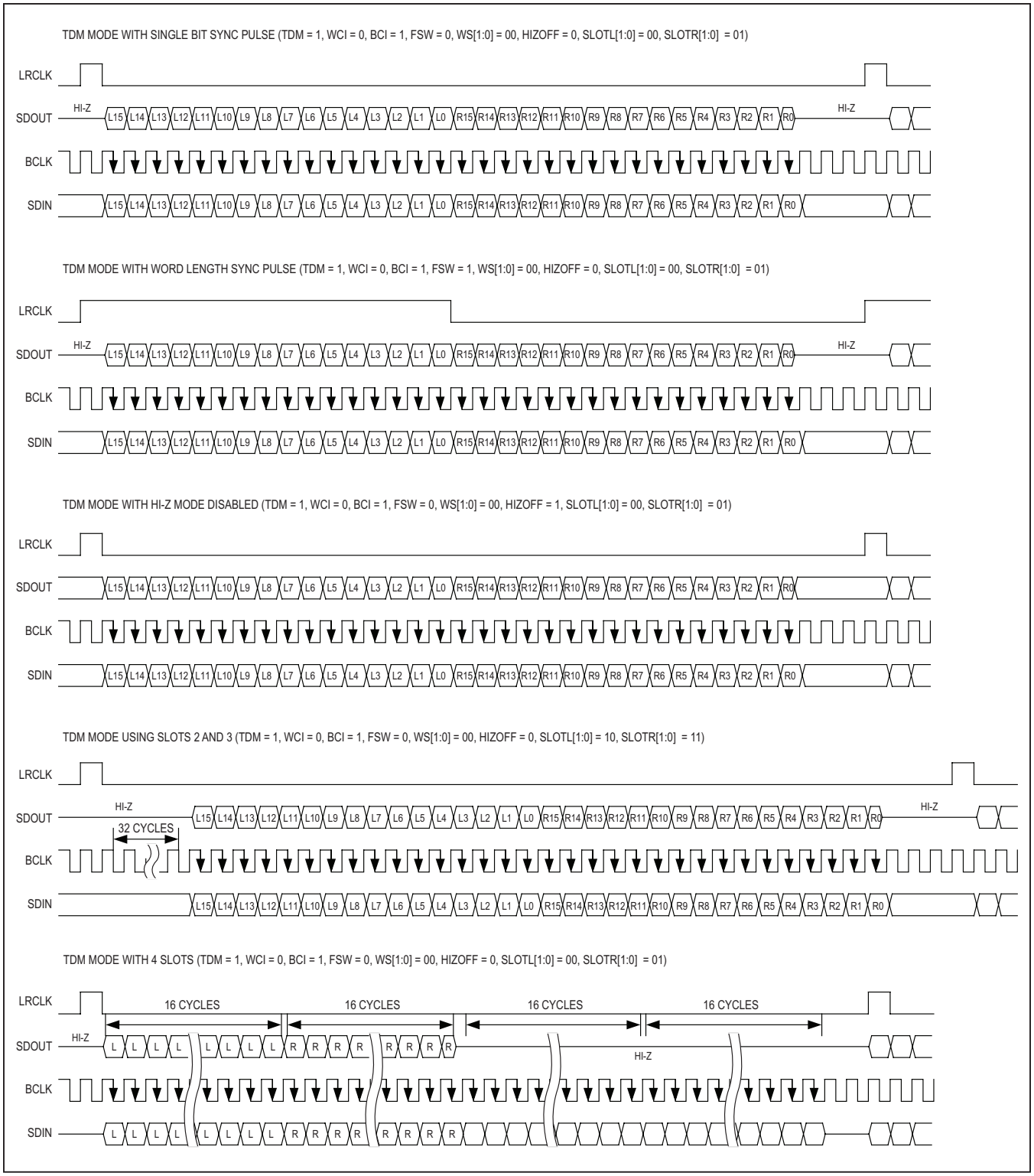


Figure 22. DAI Timing for TDM Data Format

Audio Playback Path

The device playback path has two channels (left and right) and can accept digital audio input from the DAI and/or the record path sidetone. The digital audio is then routed through several stages of FlexSound DSP followed by the digital to analog converter (Figure 23).

Playback Path FlexSound DSP

The first playback path section features the Maxim FlexSound DSP stages. The first stage accepts and mixes the DAI input with the record path sidetone (if enabled), and contains separate digital gain and digital level control stages. This stage is followed by three stereo DSP stages including a 7-band parametric equalizer, a dynamic range control section (DRC), and a digital filter stage. The playback path digital output is then routed into the DAC where it is converted back to analog before being routed to the analog output mixers.

Playback Path Digital Gain and Level Control

The stereo playback path DSP includes separate digital gain and level control stages (Figure 24). Unlike the record path, both playback path channels (left and right) share the same digital gain and level control settings. The coarse digital gain stage accepts its input from the DAI digital data output and can be set from 0dB to +18dB in 6dB increments. The fine adjust, level control stage input is the summation of the coarse gain stage output with the record path sidetone signal. It can be adjusted from -15dB to 0dB in 1dB increments (Table 49). The playback path gain and level control stage also include a mute enable.

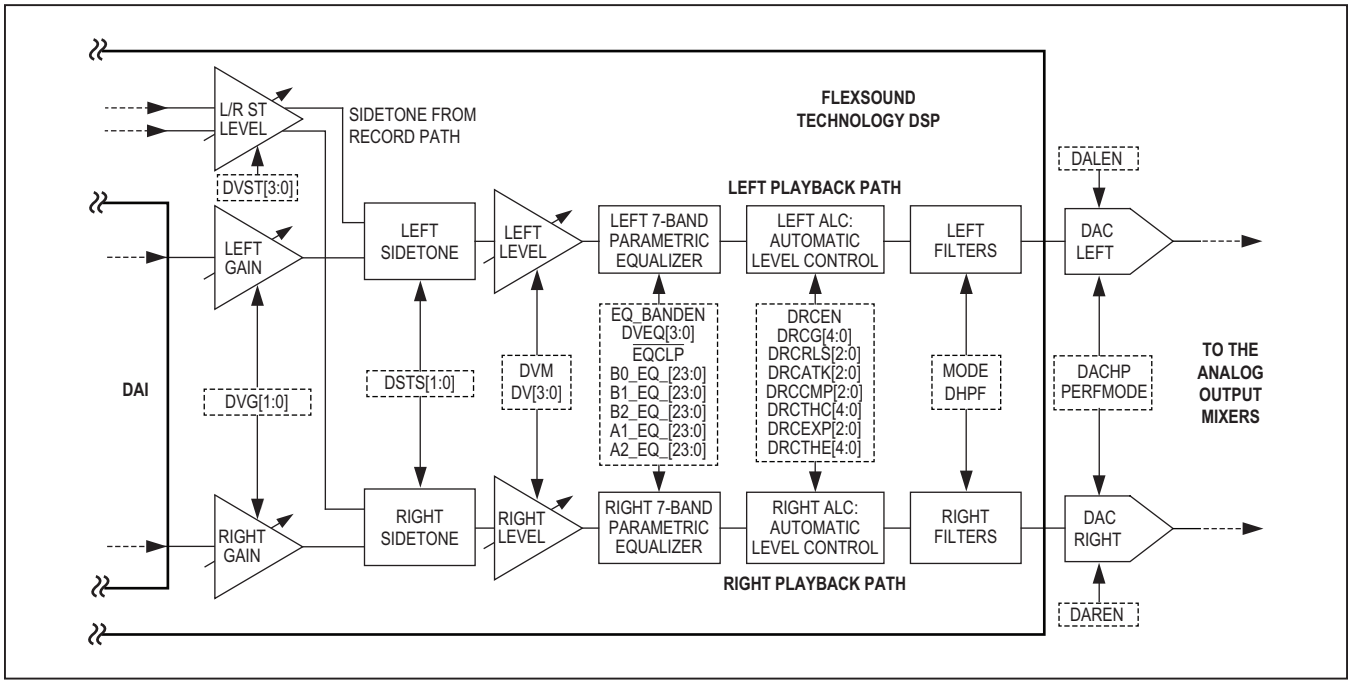


Figure 23. Playback Path Block Diagram

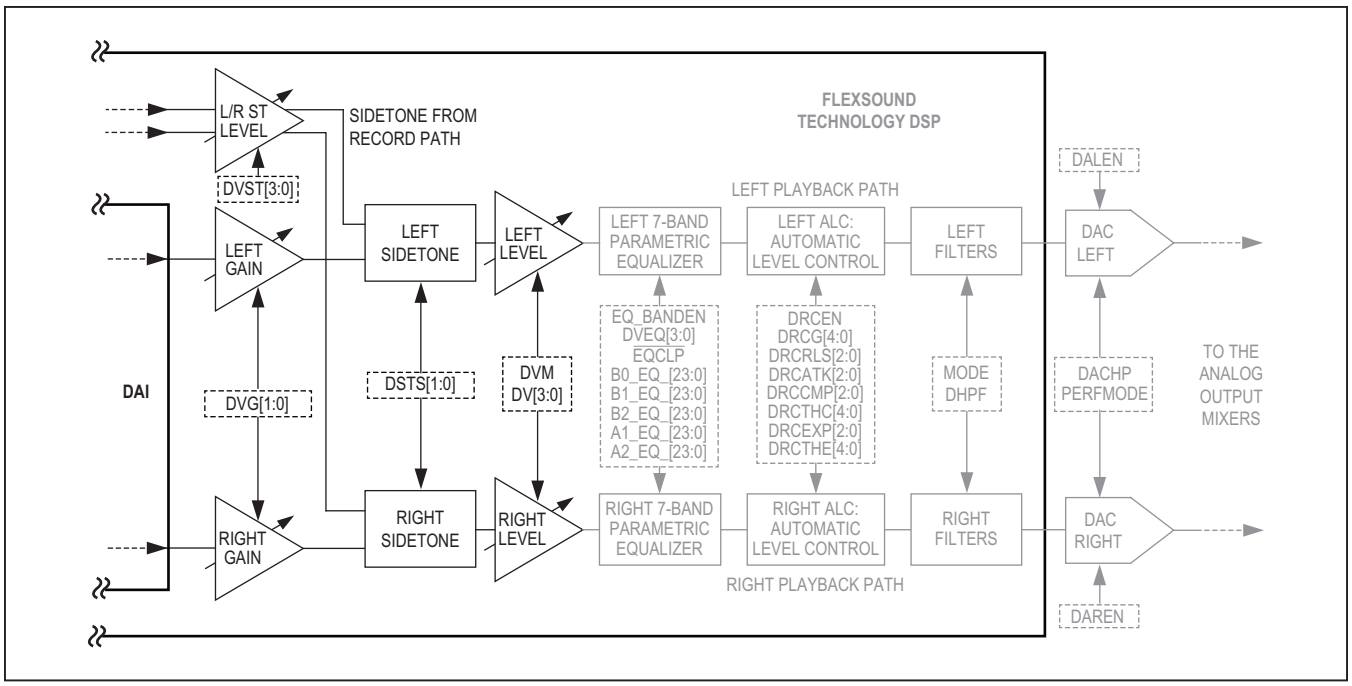


Figure 24. Playback Path Sidetone and Level Control

Table 49. Playback Gain and Level Configuration Register

ADDRESS: 0x27				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DVM	R/W	0	Enables the playback path data input mute.
6	—	—	—	—
5	DVG[1:0]	R/W	0	**Playback Path Coarse Adjust Gain Configuration** 00: 0dB 10: +12dB 01: +6dB 11: +18dB
4			0	
3	DV[3:0]	R/W	0	**Playback Path Fine Level Control Configuration** 0x0: 0dB 0x4: -4dB 0x8: -8dB 0xC: -12dB 0x1: -1dB 0x5: -5dB 0x9: -9dB 0xD: -13dB 0x2: -2dB 0x6: -6dB 0xA: -10dB 0xE: -14dB 0x3: -3dB 0x7: -7dB 0xB: -11dB 0xF: -15dB
2			0	
1			0	
0			0	

Playback Path 7-Band Parametric Equalizer

The playback path DSP features a 7-band parametric equalizer with clipping detection and a programmable pre-attenuation amplifier (Figure 25). Each of the 7 bands is a full, individually programmable digital biquad filter. The chosen configuration for any given band applies to both the left and right playback channels.

The parametric equalizer can be enabled in a 3-band, 5-band, or the full 7-band configuration (Table 50). Once the parametric equalizer is enabled, the clip detection can be set and the level of preattenuation can be adjusted from 0dB down to -15dB (denoted A_{V_EQ}, see Table 51). No single band biquad filter can be set to a gain greater than ±12dB, to a Q greater than 10, or to below a minimum f_C that varies by filter type. See the *Electrical Characteristics* table.

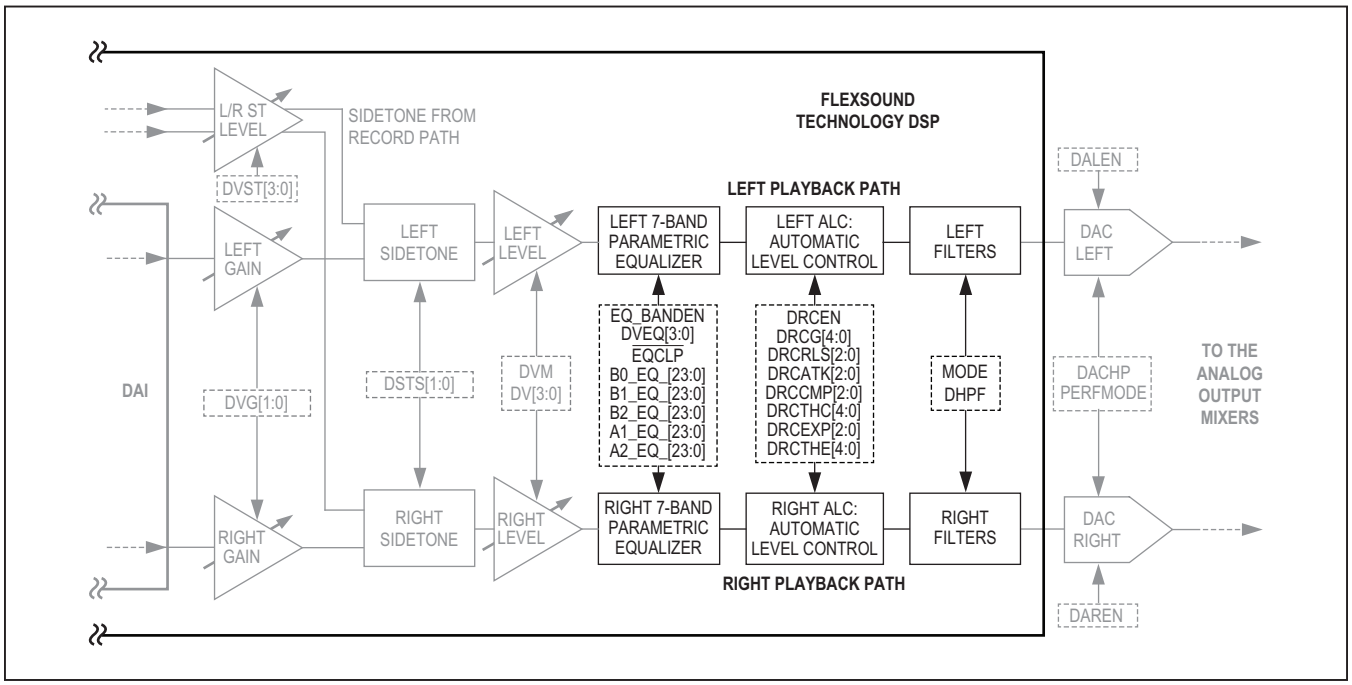


Figure 25. Playback Path DSP

Table 50. DSP Biquad Filter Enable Register

ADDRESS: 0x41				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	RECBQEN	R/W	0	**Enable Biquad Filter in Record Path** 0: Biquad filter not used. 1: Biquad filter used in ADC path.
2	EQ3BANDEN	R/W	0	**Enable 3-Band EQ in DAC Path (Bands 4–7 Are Not Used)** 0: 3-band EQ disabled. 1: 3-band EQ enabled. Only valid if EQ7BANDEN == 0 and EQ5BANDEN == 0.
1	EQ5BANDEN	R/W	0	**Enable 5-Band EQ in DAC Path (Bands 6 and 7 Are Not Used)** 0: 5-band EQ disabled. 1: 5-band EQ enabled. Only valid if EQ7BANDEN == 0
0	EQ7BANDEN	R/W	0	**Enable 7-Band EQ in DAC Path** 0: 7-band EQ disabled. 1: 7-band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant.

Table 51. Parametric Equalizer Playback Level Configuration Register

ADDRESS: 0x28				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	EQCLP	R/W	0	**Enables DAI Digital Input Equalizer Clipping Detection** 1: Equalizer clip detect disabled. 0: Equalizer clip detect enabled.
3	DVEQ[3:0]	R/W	0	**DAI Digital Input Equalizer Attenuation Level Configuration (A_{V_EQ})** 0x0: 0dB 0x4: -4dB 0x8: -8dB 0xC: -12dB 0x1: -1dB 0x5: -5dB 0x9: -9dB 0xD: -13dB 0x2: -2dB 0x6: -6dB 0xA: -10dB 0xE: -14dB 0x3: -3dB 0x7: -7dB 0xB: -11dB 0xF: -15dB
2			0	
1			0	
0			0	

The parametric equalizer coefficients are uninitialized at power-up, and when used the coefficients should be programmed before the device and equalizer are enabled. The transfer function for each band is defined as:

$$H(z) = \frac{B_0 + B_1 \times Z^{-1} + B_2 \times Z^{-2}}{A_0 + A_1 \times Z^{-1} + A_2 \times Z^{-2}}$$

The biquad filter in each band has 5 user programmable coefficients (B_0, B_1, B_2, A_1, and A_2), and each individual coefficient is 3 bytes (24 bits) long (A_0 is fixed at 1). They occupy 15 consecutive registers per band for a total of 105 consecutive registers for all 7 bands (Table 52). Each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a two's complement format where the first 4 bits are the integer portion and the last 20 bits are the decimal portion (which results in an approximate +8 to -8 range for each coefficient).

Table 52. Parametric Equalizer Band N (1–7) Biquad Filter Coefficient Registers

ADDRESS RANGE (BY BAND)							NAME	TYPE	COEFFICIENT SEGMENT
1	2	3	4	5	6	7			
0x46	0x55	0x64	0x73	0x82	0x91	0xA0	Equalizer Band N Coefficient B0	R/W	B0_N[23:16]
0x47	0x56	0x65	0x74	0x83	0x92	0xA1		R/W	B0_N[15:8]
0x48	0x57	0x66	0x75	0x84	0x93	0xA2		R/W	B0_N[7:0]
0x49	0x58	0x67	0x76	0x85	0x94	0xA3	Equalizer Band N Coefficient B1	R/W	B1_N[23:16]
0x4A	0x59	0x68	0x77	0x86	0x95	0xA4		R/W	B1_N[15:8]
0x4B	0x5A	0x69	0x78	0x87	0x96	0xA5		R/W	B1_N[7:0]
0x4C	0x5B	0x6A	0x79	0x88	0x97	0xA6	Equalizer Band N Coefficient B2	R/W	B2_N[23:16]
0x4D	0x5C	0x6B	0x7A	0x89	0x98	0xA7		R/W	B2_N[15:8]
0x4E	0x5D	0x6C	0x7B	0x8A	0x99	0xA8		R/W	B2_N[7:0]
0x4F	0x5E	0x6D	0x7C	0x8B	0x9A	0xA9	Equalizer Band N Coefficient A1	R/W	A1_N[23:16]
0x50	0x5F	0x6E	0x7D	0x8C	0x9B	0xAA		R/W	A1_N[15:8]
0x51	0x60	0x6F	0x7E	0x8D	0x9C	0xAB		R/W	A1_N[7:0]
0x52	0x61	0x70	0x7F	0x8E	0x9D	0xAC	Equalizer Band N Coefficient A2	R/W	A2_N[23:16]
0x53	0x62	0x71	0x80	0x8F	0x9E	0xAD		R/W	A2_N[15:8]
0x54	0x63	0x72	0x81	0x90	0x9F	0xAE		R/W	A2_N[7:0]

Playback Path Dynamic Range Control

The playback path includes a dynamic range control (DRC) section (Figure 25). The DRC is highly configurable and features digital make-up gain, a dynamic range compression and expansion, and programmable attack and release times.

The device dynamic range is determined by the difference between the full-scale and the RMS noise floor amplitude of the configured signal path. To avoid performance limiting, the application dynamic range is typically smaller than the dynamic range of the selected signal path. With dynamic range control disabled, the input dynamic range is equal to the output dynamic range (Figure 26). When compression is enabled, if the input signal amplitude exceeds the compression threshold the gain is reduced by the chosen compression ratio. This results in a smaller, compressed output dynamic range relative to the input dynamic range. When expansion is enabled, the gain is decreased by the chosen expansion ratio if the input signal amplitude instead falls below the expansion threshold. This results in a larger, expanded output dynamic range.

The DRC also features a digital make-up gain control section (Table 54), that can be programmed from 0dB to 12dB in 1dB increments. To avoid clipping before compression (during the attack time), the signal cannot at any time exceed the uncompressed full-scale code. Therefore, the

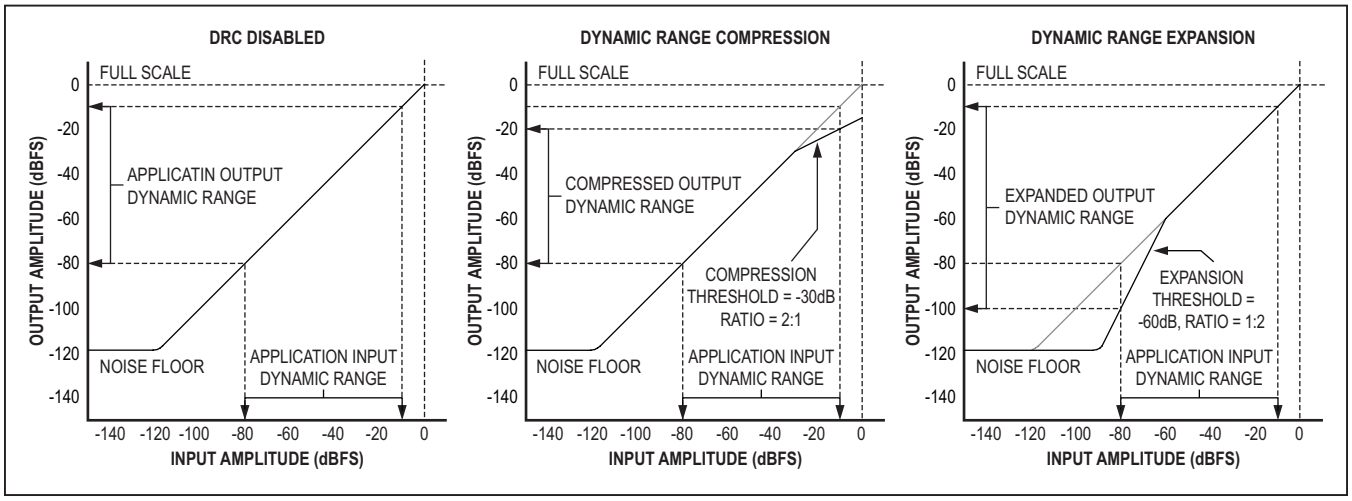


Figure 26. Dynamic Range Compression and Expansion

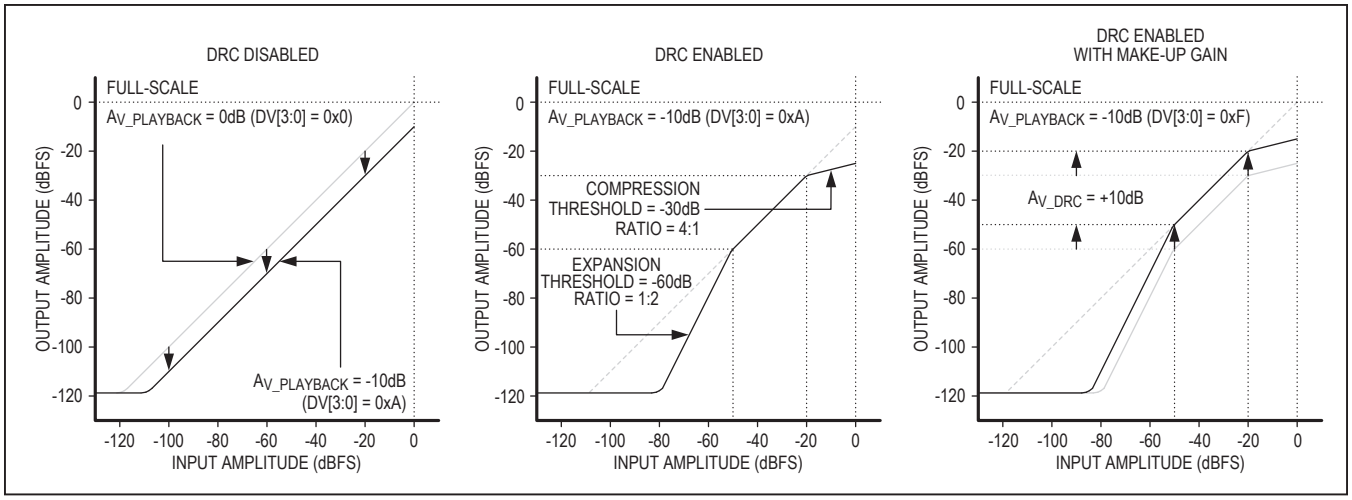


Figure 27. DRC Enable and Make-Up Gain

sum of the digital gain/level control, parametric equalizer gain, and the DRC make-up gain must not exceed 0dB total. Figure 27 shows the effect of enabling the DRC with and without digital make-up gain.

The DRC features two programmable signal thresholds. The high amplitude compression threshold is used to reduce the maximum sustained signal amplitude. The compression ratio can be set to one of five options from a 1:1 ratio to an infinite:1 ratio (or flat output amplitude as input amplitude increases). The compression threshold can be configured from -31dB to 0dB. The compression ratios and a range of thresholds are illustrated in Figure 28.

The low amplitude expansion threshold is used to prevent background noise from being amplified. When the signal level drops below the expansion threshold, the DRC reduces the gain until the signal increases above the threshold. The expansion ratio can be set to a 1:1, 1:2, or 1:3 ratio while the threshold can be configured from -35dB

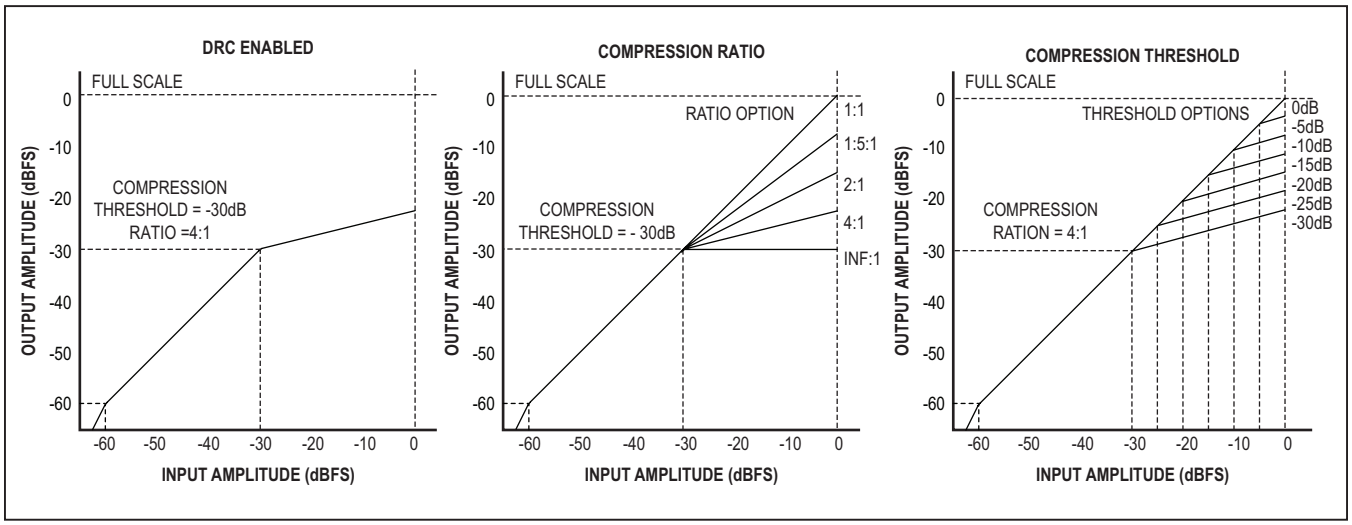


Figure 28. DRC Compression Ratio and Threshold

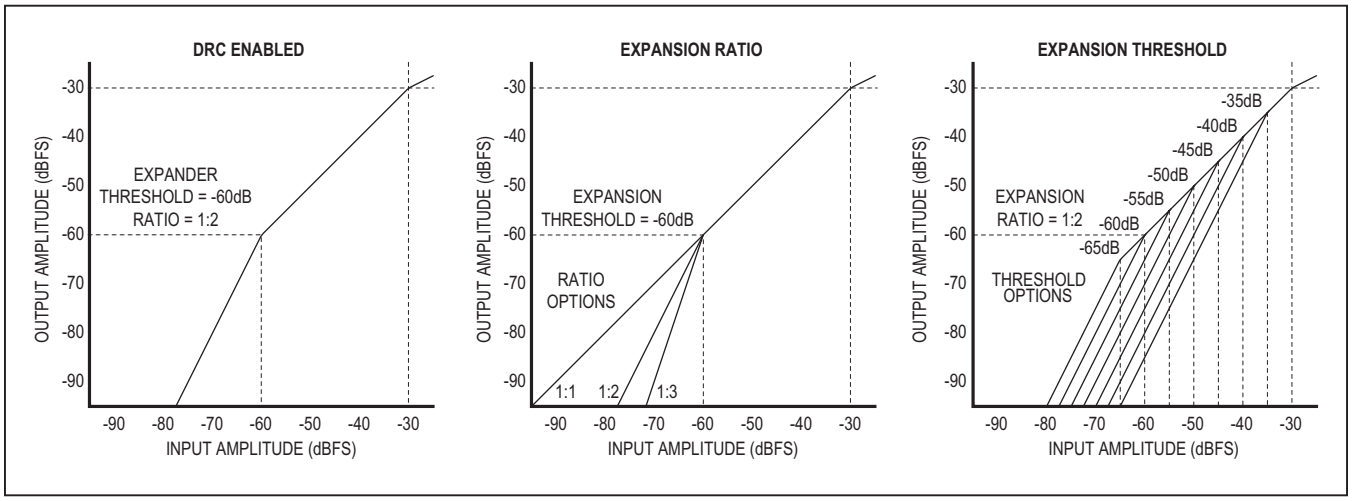


Figure 29. DRC Expansion Ratio and Threshold

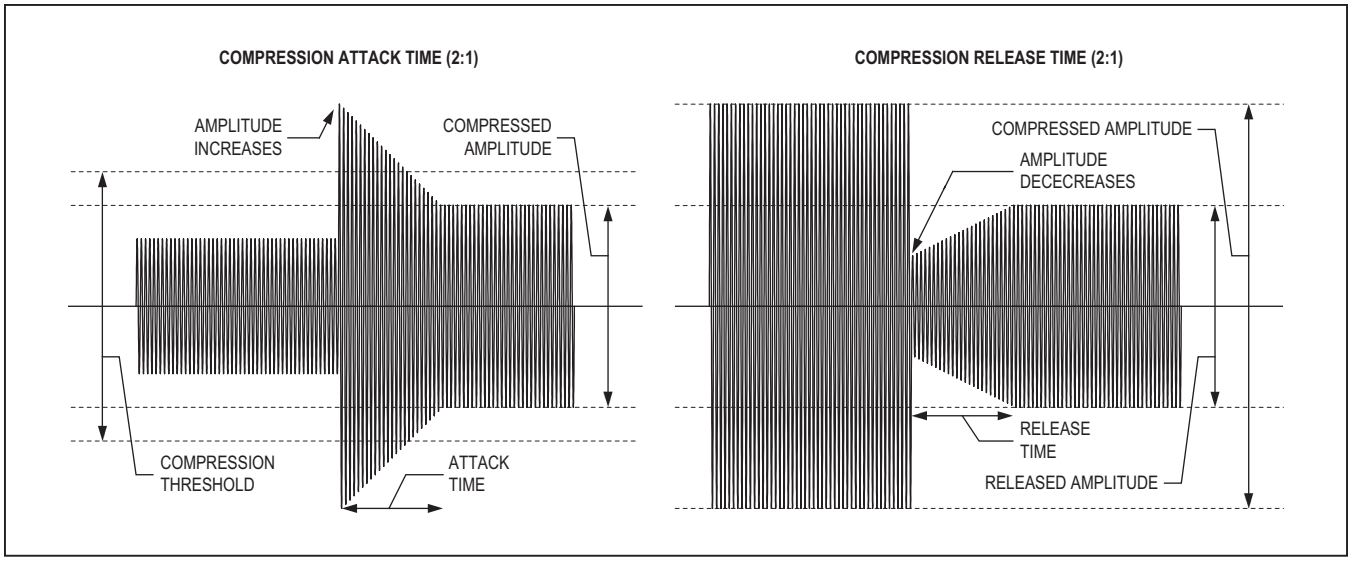


Figure 30. DRC Attack and Release Time Waveforms

to -66dB. The expansion ratios and a range of threshold are illustrated in Figure 29.

The DRC provides a wide range of programmable attack and release times (Table 53). When the compression is enabled and the signal amplitude increases until the compression threshold is exceeded, the attack time determines how quickly the selected compression ratio is applied. When the signal amplitude decreases and the compression threshold would no longer be exceeded, the release time determines how quickly the gain returns to normal (Figure 30).

When expansion is enabled and the signal amplitude decreases until it drops below the expansion threshold, the release time determines how quickly the selected expansion ratio is applied. When the signal amplitude increases and the expansion threshold would no longer be exceeded, the attack time determines how quickly the gain returns to normal.

The attack and release times are not absolute. They are instead used to set the rate at which the gain is adjusted once the signal amplitude is either above or below the appropriate threshold. Therefore the selected attack/release times are relative to the ratio of the new signal amplitude to the selected compression and expansion thresholds. The values provided in Table 53 all assume the input signal amplitude changed to exceed the appropriate threshold by a ratio of 12dB (above for compression and below for expansion). If the appropriate threshold is exceeded by a larger or smaller ratio, the attack time is increased or decreased appropriately. The change is proportional to the change in ratio in dB. For example, release time is reduced by 50% for 6dB.

For compression, if the signal amplitude exceeds the threshold by 12dB, the attack time when entering compression precisely matches the selected configuration. Likewise, when exiting compression, the release time is determined by the ratio by which the threshold was exceeded prior to the amplitude dropping.

Expansion works in exactly the same fashion except for two differences. The expansion ratio is applied when the signal amplitude drops below the expansion threshold (rather than above for compression), and the release time (rather than attack time) determines how long it takes to enter expansion (centered at 12dB below the expansion threshold). Likewise, the attack time is then used when exiting expansion. In addition, when entering expansion, the ratio of the initial input amplitude to the expansion threshold sets a delay before the expansion ratio is applied. This delay is centered at 12dB above the expansion threshold and is determined by the selected release time. There is no delay prior to the attack time when exiting expansion.

Table 53. Dynamic Range Control (DRC) Timing Register

ADDRESS: 0x33				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DRCEN	R/W	0	**PLAYBACK DRC Enable** 0: DRC disabled. 1: DRC enabled.
6	DRCRLS[2:0]	R/W	0	**PLAYBACK DRC Release Time Configuration (12dB Relative to Threshold)** 0x0: 8s 0x2: 2s 0x4: 0.5s 0x6: 0.125s 0x1: 4s 0x3: 1s 0x5: 0.25s 0x7: 0.0625s
5		R/W	0	
4		R/W	0	
3	—	—	—	—
2	DRCATK[2:0]	R/W	0	**PLAYBACK DRC Attack Time Configuration (12dB Relative to Threshold)** 0x0: 0.125ms 0x2: 1.25ms 0x4: 6.25ms 0x6: 25ms 0x1: 0.25ms 0x3: 2.5ms 0x5: 12.5ms 0x7: 50ms
1		R/W	0	
0		R/W	0	

Table 54. Dynamic Range Control (DRC) Gain Configuration Register

ADDRESS: 0x36				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	DRCG[4:0]	R/W	0	**PLAYBACK DRC Make-Up Gain Configuration** 0x0: +0dB 0x4: +4dB 0x8: +8dB 0xC: +12dB 0x1: +1dB 0x5: +5dB 0x9: +9dB 0xD: reserved 0x2: +2dB 0x6: +6dB 0xA: +10dB 0xE: reserved 0x3: +3dB 0x7: +7dB 0xB: +11dB 0xF: reserved
3			0	
2			0	
1			0	
0			0	

Table 55. Dynamic Range Control (DRC) Compressor Register

ADDRESS: 0x34				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DRCCMP[2:0]	R/W	0	**PLAYBACK DRC Compression Ratio Configuration** 0x0: 1:1 0x3: 4:1 0x1: 1.5:1 0x4: INF:1 0x2: 2:1 0x5–0x7: Reserved
6			0	
5			0	
4	DRCTHC[4:0]	R/W	0	**PLAYBACK DRC Compression Threshold Configuration** 0x00: 0 0x08: -8dB 0x10: -16dB 0x18: -24dB 0x01: -1dB 0x09: -9dB 0x11: -17dB 0x19: -25dB 0x02: -2dB 0x0A: -10dB 0x12: -18dB 0x1A: -26dB 0x03: -3dB 0x0B: -11dB 0x13: -19dB 0x1B: -27dB 0x04: -4dB 0x0C: -12dB 0x14: -20dB 0x1C: -28dB 0x05: -5dB 0x0D: -13dB 0x15: -21dB 0x1D: -29dB 0x06: -6dB 0x0E: -14dB 0x16: -22dB 0x1E: -30dB 0x07: -7dB 0x0F: -15dB 0x17: -23dB 0x1F: -31dB
3			0	
2			0	
1			0	
0			0	

Table 56. Dynamic Range Control (DRC) Expander Register

ADDRESS: 0x35				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	DRCEXP[2:0]	R/W	0	**PLAYBACK DRC Expansion Ratio Configuration** 0x0: 1:1 0x2: 1:3 0x1: 1:2 0x3–0x7: Reserved
5			0	
4	DRCTHE[4:0]	R/W	0	**PLAYBACK DRC Expansion Threshold Configuration** 0x00: -35dB 0x08: -43dB 0x10: -51dB 0x18: -59dB 0x01: -36dB 0x09: -44dB 0x11: -52dB 0x19: -60dB 0x02: -37dB 0x0A: -45dB 0x12: -53dB 0x1A: -61dB 0x03: -38dB 0x0B: -46dB 0x13: -54dB 0x1B: -62dB 0x04: -39dB 0x0C: -47dB 0x14: -55dB 0x1C: -63dB 0x05: -40dB 0x0D: -48dB 0x15: -56dB 0x1D: -64dB 0x06: -41dB 0x0E: -49dB 0x16: -57dB 0x1E: -65dB 0x07: -42dB 0x0F: -50dB 0x17: -58dB 0x1F: -66dB
3			0	
2			0	
1			0	
0			0	

Playback Path Digital Filters

The playback path DSP includes a digital filter stage. One filter, set with the MODE bit (Table 57), offers the choice between the IIR voice filters and the FIR music filters. The IIR filters are optimized for standard (f_S = 8kHz) and wideband (f_S = 16kHz) voice applications, while the FIR filters are optimized for low power operation at higher audio/music sampling rates. For sampling rates in excess of 50kHz (f_{LRCLK} > 50kHz), the FIR audio filters must be used, and the DHF bit should be set to appropriately scale the FIR interpolation filter. The MODE configuration selected applies to both channels of both the record and playback path DSP.

The playback path DSP also features a DC-blocking filter. This filter can be used with both the IIR voice and FIR music filters, and blocks low-frequency (including DC) input signals outside of the lower end of the audio band.

Digital-to-Analog Converter (DAC) Configuration

The stereo DAC architecture includes two independent audio paths, analog outputs that can be routed to any of the analog output mixers, and two operating modes (Table 4). One operating mode is optimized for maximum dynamic performance while the other is optimized for lower power consumption. Both DAC channels can be enabled independently, allowing the device to support both stereo and left or right mono configurations (Table 8).

Table 57. DSP Filter Configuration Register

ADDRESS: 0x26				DESCRIPTION
BIT	NAME	TYPE	POR	
7	MODE	R/W	1	**Enables the CODEC DSP FIR Music Filters (Default IIR Voice Filters)** 0: The codec DSP filters operate in IIR voice mode with stop band frequencies below the $f_S/2$ Nyquist rate. The voice mode filters are optimized for 8kHz or 16kHz voice application use. 1: The codec DSP filters operate in a linear phase FIR audio mode optimized to maintain stereo imaging and operate at higher f_S rates while utilizing lower power.
6	AHPF	R/W	0	**Enables the Record Path DC-Blocking Filter** 0: DC-blocking filter disabled. 1: DC-blocking filter enabled.
5	DHPF	R/W	0	**Enables the Playback Path DC-Blocking Filter** 0: DC-blocking filter disabled. 1: DC-blocking filter enabled.
4	DHF	R/W	0	**Enables the DAC High Sample Rate Mode (LRCLK > 50kHz, FIR Only)** 0: LRCLK is less than 50kHz. 8x FIR interpolation filter used. 1: LRCLK is greater than 50kHz. 4x FIR interpolation filter used.
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

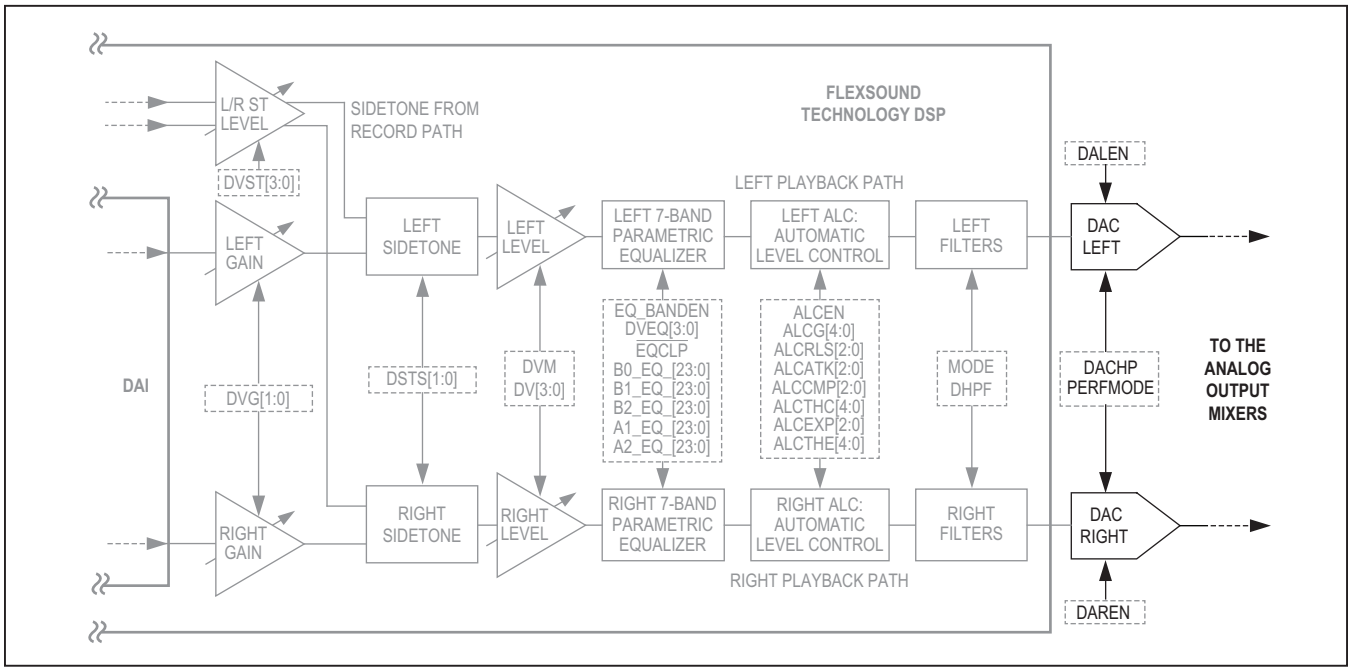


Figure 31. Playback Path Digital-to-Analog Converter

Analog Audio Output Configuration

The device features three independent integrated analog audio output drivers (Figure 32). The receiver/line output driver can be configured either as a differential receiver/earpiece output or as a stereo single-ended line output driver. The stereo speaker output drivers are filterless Class D differential amplifiers capable of driving both 4Ω and 8Ω speakers. The headphone output drivers utilize Maxim's DirectDrive architecture with an integrated charge pump, and provide configurable headphone and headset jack detection. Each analog audio output driver has a programmable gain input mixer and output amplifier. Each mixer accepts any combination of signals from the playback DAC, the analog microphone amplifier, and the line input drivers.

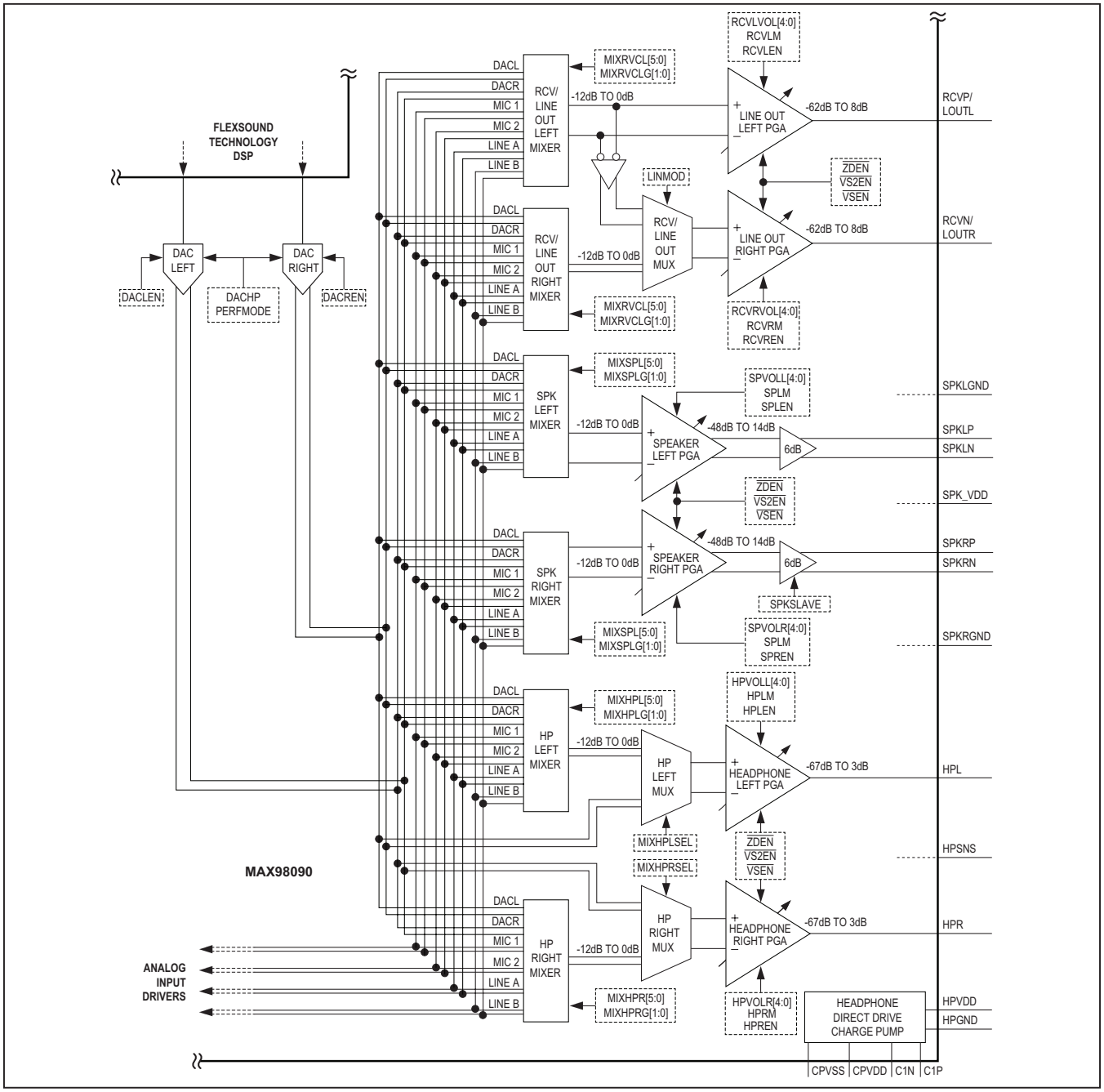


Figure 32. Analog Audio Output Functional Diagram

Analog Class AB Configurable Receiver/Line Output

The device features a configurable analog Class AB programmable gain amplifier output that can be configured to act either a mono differential output or as a stereo single-ended output. When configured as a differential analog output (LINEMOD = 0, Table 61), the driver is an ideal receiver driver capable of driving both 16Ω and 32Ω differential loads (such as an earpiece speaker). In the receiver configuration, the mono output of the left receiver/line output mixer is routed to both the left and right output drivers in a bridge tied load (BTL) configuration (Figure 33). In this configuration, the mixer input signal source(s) and both the mixer and output amplifier gain settings are determined by the left channel registers. All right output channel register settings have no effect in receiver/earpiece mode.

When configured as a stereo single-ended analog output (LINEMOD = 1, Table 61), the driver is optimized for standard ground referenced, high impedance line outputs. In the line output configuration, the output of the left and right line output mixers are individually routed to the left and right output drivers (respectively, Figure 34). In this configuration, both channels are configured individually by the left and right channel registers.

Receiver/Earpiece Mixer and Gain Control

When configured as a differential receiver output, only the left output configuration registers are used. The receiver mixer can be configured to accept any combination of signals from the playback DAC, the analog microphone amplifiers, and the line input drivers (Table 58). The receiver input mixer also provides several attenuation options (Table 59). The mixer attenuation options of -6dB, -9.5dB, and -12dB are sized to prevent clipping when several full-scale input sources are selected.

The receiver output is a programmable gain amplifier (PGA) capable of driving a wide range of differential loads (including standard 16Ω and 32Ω earpiece speakers). The receiver PGA has a wide volume adjustment range from -62dB to +8dB, provides a high attenuation mute control (Table 60), and features programmable click and pop reduction options. See the *Click-and-Pop Reduction* section for details. The receiver PGA output common-mode voltage is either half of V_{AVDD} (in resistive divider BIAS mode) or about 0.78V (in bandgap BIAS mode).

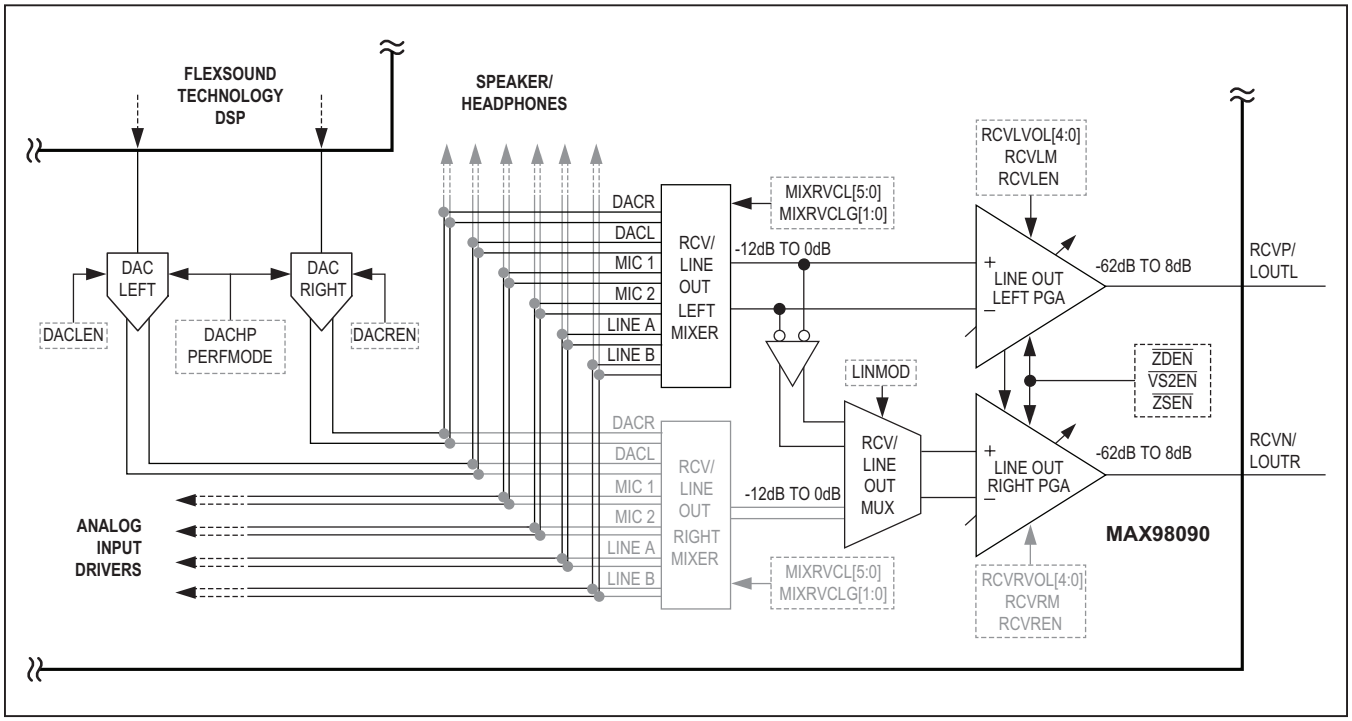


Figure 33. Receiver Output Functional Diagram

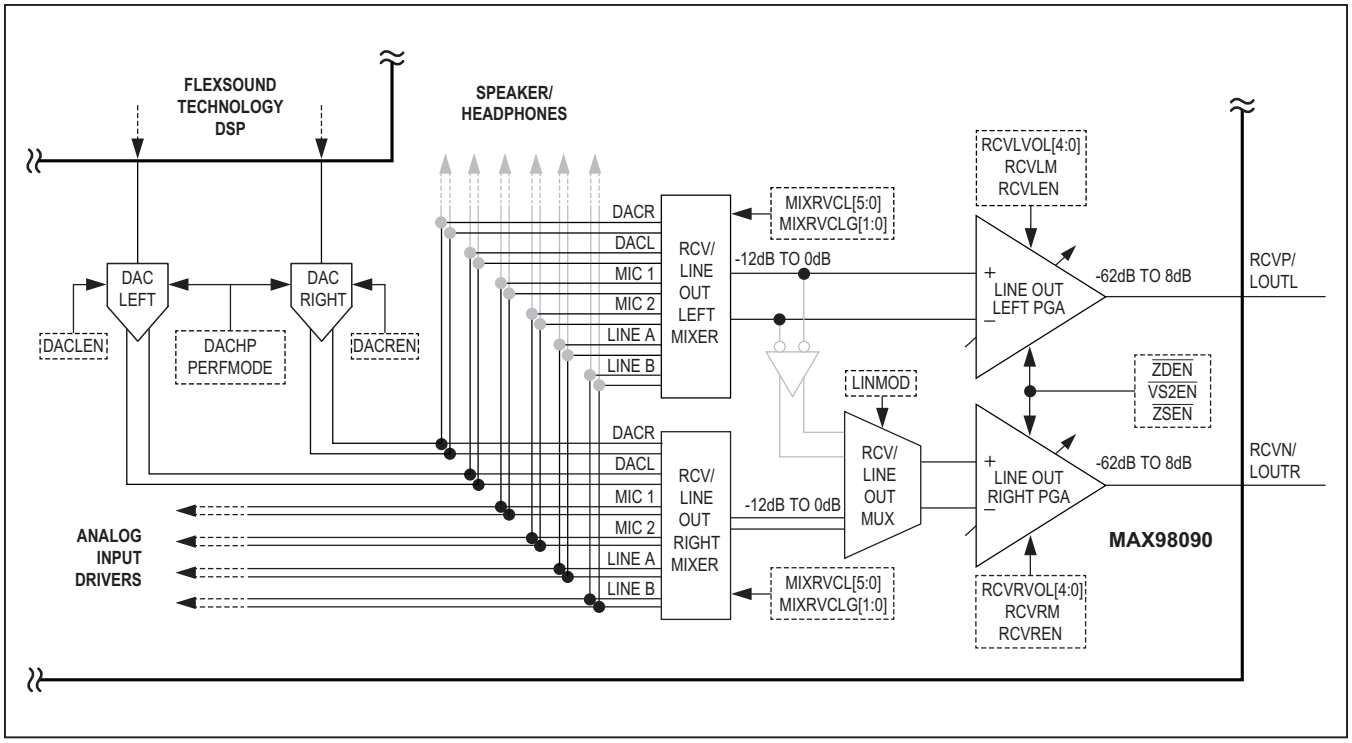


Figure 34. Stereo Single-Ended Line Output Functional Diagram

Table 58. Receiver and Left Line Output Mixer Source Configuration Register

ADDRESS: 0x37				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	MIXRCVL[5:0]	R/W	0	Selects MIC 2 as the input to the receiver/line out left mixer.
4			0	Selects MIC 1 as the input to the receiver/line out left mixer.
3			0	Selects line B as the input to the receiver/line out left mixer.
2			0	Selects line A as the input to the receiver/line out left mixer.
1			0	Selects DAC right as the input to the receiver/line out left mixer.
0			0	Selects DAC left as the input to the receiver/line out left mixer.

Line Output Mixer and Gain Control

When configured as a stereo single-ended line output, the left and right configuration registers can be programmed independently. Each channel mixer can be configured to accept any combination of signals from the playback DAC, the analog microphone amplifiers, and the line input drivers (Tables 58 and 61). The input mixers also provide several attenuation options (Tables 59 and 62). The mixer attenuation options of -6dB, -9.5dB, and -12dB are sized to prevent clipping when several full-scale input sources are selected.

The left and right line output drivers are independent programmable gain amplifiers (PGAs) capable of driving high impedance ground referenced loads. The line output PGAs have a wide volume adjustment range from -62dB to +8dB, provide a high attenuation mute control (Tables 60 and 63), and feature programmable click and pop reduction options. See the *Click-and-Pop Reduction* section for details. The output common-mode voltage is either half of V_{AVDD} (in resistive divider BIAS mode) or about 0.78V (in bandgap BIAS mode). As a result of the internal architecture, the left and right channel each have a built in baseline gain of -3dB (when all programmable gain options are set to 0dB).

Table 59. Receiver and Left Line Output Mixer Gain Control Register

ADDRESS: 0x38				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	MIXRCVLG[1:0]	R/W	0	**Receiver/Line Output Left Mixer Gain Configuration** 00: 0dB 10: -9.5dB 01: -6dB 11: -12dB
0			0	

Table 60. Receiver and Left Line Output Volume Control Register

ADDRESS: 0x39				DESCRIPTION
BIT	NAME	TYPE	POR	
7	RCVLM	R/W	0	**Left Receiver/Line Output Mute** 0: Left output amplifier not muted. 1: Left output amplifier is muted.
6	—	—	—	—
5	—	—	—	—
4	RCVLVOL[4:0]	R/W	1	**Receiver/Line Output Left PGA Volume Configuration** 0x1F: +8dB 0x17: +2dB 0x0F: -12dB 0x07: -35dB 0x1E: +7.5dB 0x16: +1dB 0x0E: -14dB 0x06: -38dB 0x1D: +7dB 0x15: +0dB 0x0D: -17dB 0x05: -42dB 0x1C: +6.5dB 0x14: -2dB 0x0C: -20dB 0x04: -46dB 0x1B: +6dB 0x13: -4dB 0x0B: -23dB 0x03: -50dB 0x1A: +5dB 0x12: -6dB 0x0A: -26dB 0x02: -54dB 0x19: +4dB 0x11: -8dB 0x09: -29dB 0x01: -58dB 0x18: +3dB 0x10: -10dB 0x08: -32dB 0x00: -62dB
3			0	
2			1	
1			0	
0			1	

Table 61. Right Line Output Mixer Source Configuration Register

ADDRESS: 0x3A				DESCRIPTION
BIT	NAME	TYPE	POR	
7	LINMOD	R/W	0	**Selects Between Receiver BTL Mode and Line Output mode** 0: Receiver BTL mode. All control of the output is from the left-channel registers. 1: Line Output mode. Left and right channels are programmed independently.
6	—	—	—	—
5	MIXRCVR[5:0]	R/W	0	Selects MIC 2 as the input to the line out right mixer
4			0	Selects MIC 1 as the input to the line out right mixer
3			0	Selects Line B as the input to the line out right mixer
2			0	Selects Line A as the input to the line out right mixer
1			0	Selects DAC Right as the input to the line out right mixer
0			0	Selects DAC Left as the input to the line out right mixer

Table 62. Right Line Output Mixer Gain Control Register

ADDRESS: 0x3B				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	MIXRCVRG[1:0]	R/W	0	**Line Output Right Mixer Gain Configuration** 00: 0dB 10: -9.5dB 01: -6dB 11: -12dB
0			0	

Table 63. Right Line Output Volume Control Register

ADDRESS: 0x3C				DESCRIPTION
BIT	NAME	TYPE	POR	
7	RCVRM	R/W	0	**Right Receiver/Line Output Mute** 0: Right output amplifier not muted. 1: Right output amplifier is muted.
6	—	—	—	—
5	—	—	—	—
4	RCVRVOL[4:0]	R/W	1	**Line Output Right PGA Volume Configuration** 0x1F: +8dB 0x17: +2dB 0x0F: -12dB 0x07: -35dB 0x1E: +7.5dB 0x16: +1dB 0x0E: -14dB 0x06: -38dB 0x1D: +7dB 0x15: +0dB 0x0D: -17dB 0x05: -42dB 0x1C: +6.5dB 0x14: -2dB 0x0C: -20dB 0x04: -46dB 0x1B: +6dB 0x13: -4dB 0x0B: -23dB 0x03: -50dB 0x1A: +5dB 0x12: -6dB 0x0A: -26dB 0x02: -54dB 0x19: +4dB 0x11: -8dB 0x09: -29dB 0x01: -58dB 0x18: +3dB 0x10: -10dB 0x08: -32dB 0x00: -62dB
3			0	
2			1	
1			0	
0			1	

Analog Class D Speaker Output

The device features an integrated stereo differential speaker amplifier. The analog stereo speaker output has three series sections comprising a flexible input mixer, a programmable gain amplifier, and a differential Class D output driver (Figure 35). The speaker output is capable of driving both 4Ω and 8Ω loads, utilizes a highly efficient Class D architecture, and meets EMI emission standards while driving a filterless speaker load.

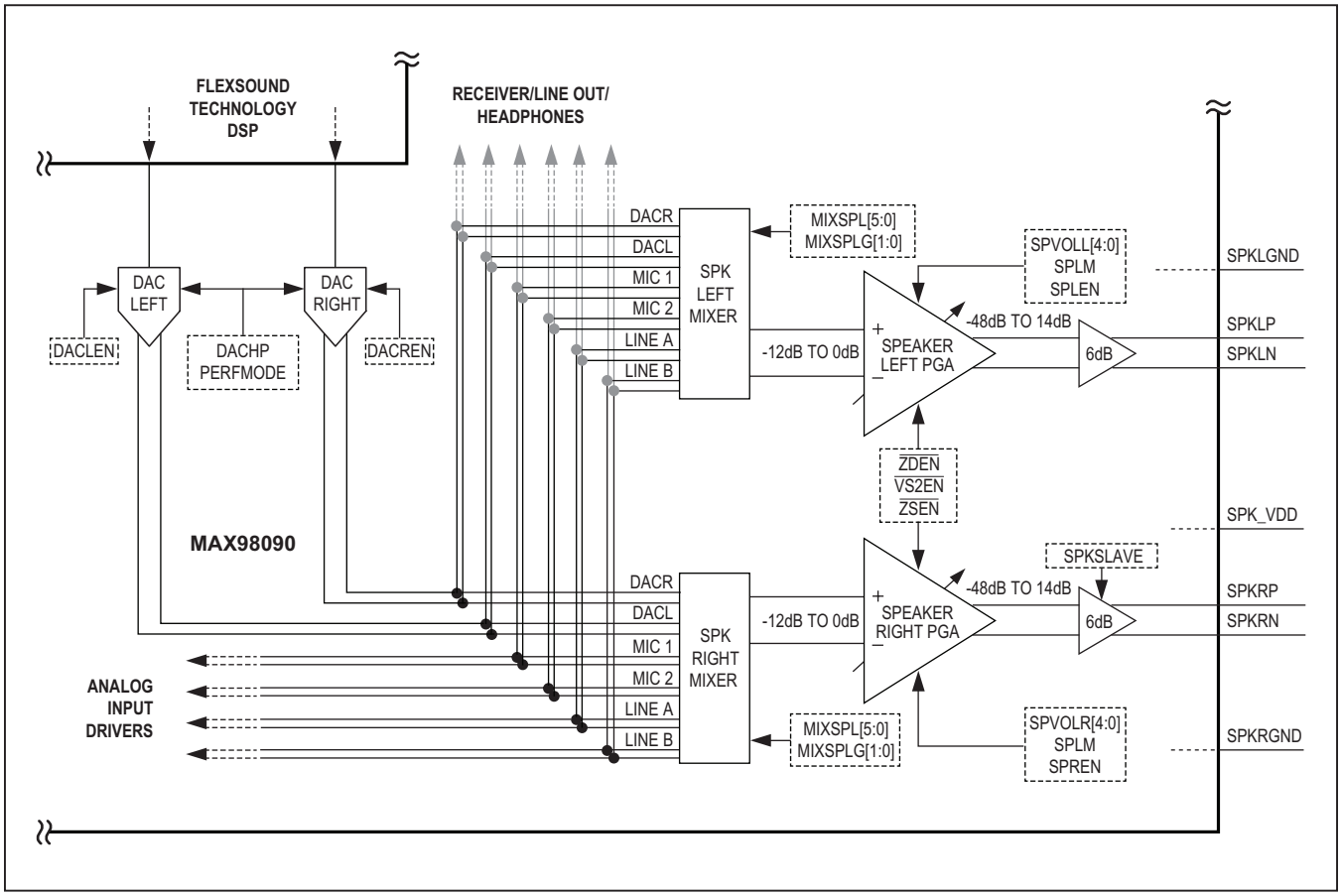


Figure 35. Class D Speaker Output Functional Diagram

Speaker Output Mixer and Gain Control

The speaker mixers can be configured to accept any combination of signals from the playback DAC, the analog microphone amplifiers, and the line input drivers (Tables 64 and 65). The input mixers also provide several attenuation options (Table 66). The mixer attenuation options of -6dB, -9.5dB, and -12dB are sized to prevent clipping when several full-scale input sources are selected.

Table 64. Left Speaker Mixer Configuration Register

ADDRESS: 0x2E				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	MIXSPL[5:0]	R/W	0	Selects microphone input 2 to left speaker mixer
4			0	Selects microphone Input 1 to left speaker mixer
3			0	Selects line input B to left speaker mixer
2			0	Selects line input A to left speaker mixer
1			0	Selects right DAC output to left speaker mixer
0			0	Selects left DAC output to left speaker mixer

Table 65. Right Speaker Mixer Configuration Register

ADDRESS: 0x2F				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	SPK_SLAVE	—	—	**Speaker Slave Mode Enable** 0: Right-channel clock always generated independently. 1: Right channel uses left-channel clock if both channels are enabled.
5	MIXSPR[5:0]	R/W	0	Selects microphone input 2 to right speaker mixer.
4			0	Selects microphone input 1 to right speaker mixer.
3			0	Selects line input B to Right speaker mixer.
2			0	Selects line input A to right speaker mixer.
1			0	Selects right DAC output to right speaker mixer.
0			0	Selects left DAC output to right speaker mixer.

Table 66 Speaker Mixer Gain Control Register

ADDRESS: 0x30				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	MIXSPRG[1:0]	R/W	0	**Right-Speaker Mixer Gain Configuration** 00: +0dB 10: -9.5dB 01: -6dB 11: -12dB
2			0	
1	MIXSPLG[1:0]	R/W	0	**Left-Speaker Mixer Gain Configuration** 00: +0dB 10: -9.5dB 01: -6dB 11: -12dB
0			0	

The speaker output programmable gain amplifiers (PGAs) have a wide volume adjustment range from -48dB to +14dB, provide a high attenuation mute control (Table 67 and Table 68), and feature programmable click and pop reduction options. See *Click-and-Pop Reduction* section for details. In addition to the programmable gain range, the Class D output driver also provides another 6dB of built-in gain.

Table 67. Left Speaker Amplifier Volume Control Register

ADDRESS: 0x31				DESCRIPTION			
BIT	NAME	TYPE	POR				
7	SPLM	R/W	0	**Left Speaker Output Mute Enable** 0 : Speaker output volume set by the volume control bits. 1 : Left speaker output muted.			
6	—	—	—	—			
5	SPVOLL[5:0]	R/W	1	**Left Speaker Output Amplifier Volume Control Configuration**			
4			0	0x3F: +14dB	0x35: +9dB	0x2B: -1dB	0x21: -17dB
				0x3E: +13.5dB	0x34: +8dB	0x2A: -2dB	0x20: -20dB
3			1	0x3D: +13dB	0x33: +7dB	0x29: -3dB	0x1F: -23dB
				0x3C: +12.5dB	0x32: +6dB	0x28: -4dB	0x1E: -26dB
2			1	0x3B: +12dB	0x31: +5dB	0x27: -5dB	0x1D: -29dB
				0x3A: +11.5dB	0x30: +4dB	0x26: -6dB	0x1C: -32dB
1			0	0x39: +11dB	0x2F: +3dB	0x25: -8dB	0x1B: -36dB
				0x38: +10.5dB	0x2E: +2dB	0x24: -10dB	0x1A: -40dB
0			0	0x37: +10dB	0x2D: +1dB	0x23: -12dB	0x19: -44dB
				0x36: +9.5dB	0x2C: +0dB	0x22: -14dB	0x18: -48dB

Table 68. Right Speaker Amplifier Volume Control Register

ADDRESS: 0x32				DESCRIPTION			
BIT	NAME	TYPE	POR				
7	SPRM	R/W	0	**Right Speaker Output Mute Enable** 0 : Speaker output volume set by the volume control bits. 1 : Right-speaker output muted.			
6	—	—	—	—			
5	SPVOLR[5:0]	R/W	1	**Right Speaker Output Amplifier Volume Control Configuration**			
4			0	0x3F: +14dB	0x35: +9dB	0x2B: -1dB	0x21: -17dB
				0x3E: +13.5dB	0x34: +8dB	0x2A: -2dB	0x20: -20dB
3			1	0x3D: +13dB	0x33: +7dB	0x29: -3dB	0x1F: -23dB
				0x3C: +12.5dB	0x32: +6dB	0x28: -4dB	0x1E: -26dB
2			1	0x3B: +12dB	0x31: +5dB	0x27: -5dB	0x1D: -29dB
				0x3A: +11.5dB	0x30: +4dB	0x26: -6dB	0x1C: -32dB
1			0	0x39: +11dB	0x2F: +3dB	0x25: -8dB	0x1B: -36dB
				0x38: +10.5dB	0x2E: +2dB	0x24: -10dB	0x1A: -40dB
0			0	0x37: +10dB	0x2D: +1dB	0x23: -12dB	0x19: -44dB
				0x36: +9.5dB	0x2C: +0dB	0x22: -14dB	0x18: -48dB

Efficient Class D Speaker Output Driver

A Class D amplifier offers much higher efficiency than a Class AB amplifier. The high efficiency is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current steering switches and consume negligible additional power. Any power loss associated with a Class D output stage is primarily due to the loss in the MOSFET on-resistance, and the baseline quiescent current overhead.

For comparison, the theoretical best-case efficiency of a linear amplifier is 78%. However, that efficiency is only possible at peak output power conditions. Under normal operating levels (typical music reproduction levels), efficiency often falls below 30%. Under the same conditions, the device's differential Class D speaker output amplifier still exhibits 80% efficiency.

By default, the Class D output switching clocks are independently generated for the left and right channels. With slave mode enabled, the right channel becomes a slave to the left channel and uses the same clock (Table 65). In slave mode, the switching scheme is synchronous. As a result, slave mode operation eliminates potential beat tones that can occur with asynchronous stereo Class D switching.

Traditional Class D amplifiers often require the use of external LC filters and/or shielding to meet EN55022B and FCC electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions limiting edge-rate control circuitry reduces EMI emissions. This allows the device to drive both 4Ω and 8Ω without any additional output filtering. The filterless Class D outputs are designed for typical applications where the trace length to the speakers is short and has a low series resistance. See the *Filterless Class D Speaker Operation* section for application level details.

Analog Class-H Headphone Output

The stereo headphone output driver has a flexible input mixer, programmable gain stage, an integrated charge pump, and a ground referenced DirectDrive Class H output amplifier (Figure 36). The headphone output amplifier is capable of driving both 16Ω and 32Ω ground-referenced headphone loads.

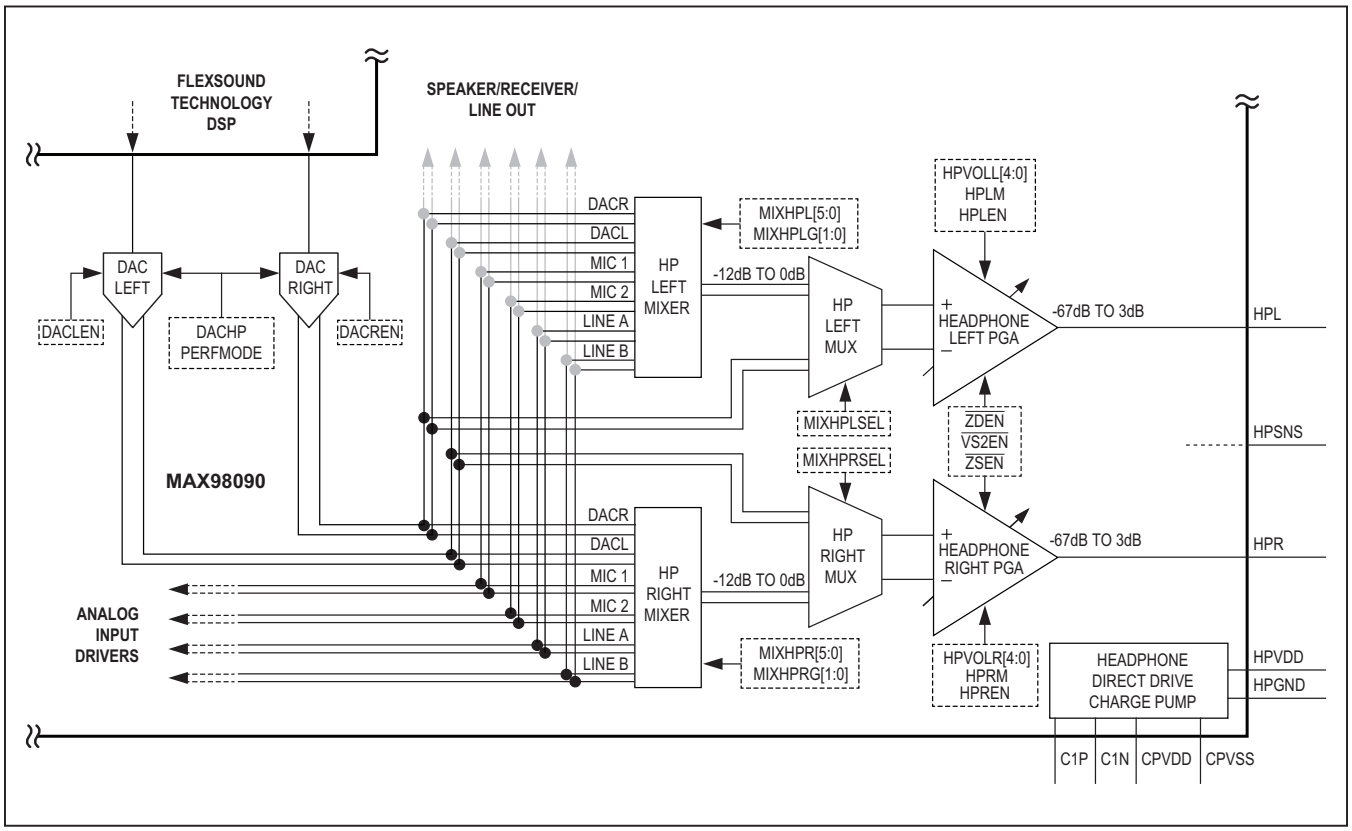


Figure 36. DirectDrive Headphone Output Functional Diagram

Headphone Output Mixer and Gain Control

The headphone mixers can be configured to accept any combination of signals from the playback DAC, the analog microphone amplifiers, and the line input drivers (Table 69 and Table 70). The input mixers also provide several attenuation options (Table 71). The mixer attenuation options of -6dB, -9.5dB, and -12dB are sized to prevent clipping when several full-scale input sources are selected.

Table 69. Left Headphone Mixer Configuration Register

ADDRESS: 0x29				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	MIXHPL[5:0]	R/W	0	Selects microphone input 2 to left headphone mixer.
4			0	Selects microphone input 1 to left headphone mixer.
3			0	Selects line input B to left headphone mixer.
2			0	Selects line input A to left headphone mixer.
1			0	Selects right DAC output to left headphone mixer.
0			0	Selects left DAC output to left headphone mixer.

Table 70. Right Headphone Mixer Configuration Register

ADDRESS: 0x2A				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	MIXHPR[5:0]	R/W	0	Selects microphone input 2 to right headphone mixer.
4			0	Selects microphone input 1 to right headphone mixer.
3			0	Selects line input B to right headphone mixer.
2			0	Selects line input A to right headphone mixer.
1			0	Selects right DAC output to right headphone mixer.
0			0	Selects left DAC output to right headphone mixer.

Table 71. Headphone Mixer Control and Gain Register

ADDRESS: 0x2B				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	MIXHPRSEL	R/W	0	**Select Headphone Mixer as Right Input Source (Default DAC Right Direct)** 0: DAC only source (best dynamic range and power consumption) 1: Headphone mixer source
4	MIXHPLSEL	R/W	0	**Select Headphone Mixer as Left Input Source (Default DAC Left Direct)** 0: DAC only source (best dynamic range and power consumption) 1: Headphone mixer source
3	MIXHPRG[1:0]	R/W	0	**Right-Headphone Mixer Gain Configuration** 00: +0dB 10: -9.5dB 01: -6dB 11: -12dB
2			0	
1	MIXHPLG[1:0]	R/W	0	**Left-Headphone Mixer Gain Configuration** 00: +0dB 10: -9.5dB 01: -6dB 11: -12dB
0			0	

Additionally, the headphone output has a reduced power direct from DAC playback mode (Figure 37). In this configuration, the stereo DAC outputs from the playback path are routed around the headphone mixer directly to the headphone output amplifiers. When paired with the low power headphone playback mode (Table 4), this combination is the lowest power digital to analog playback configuration available.

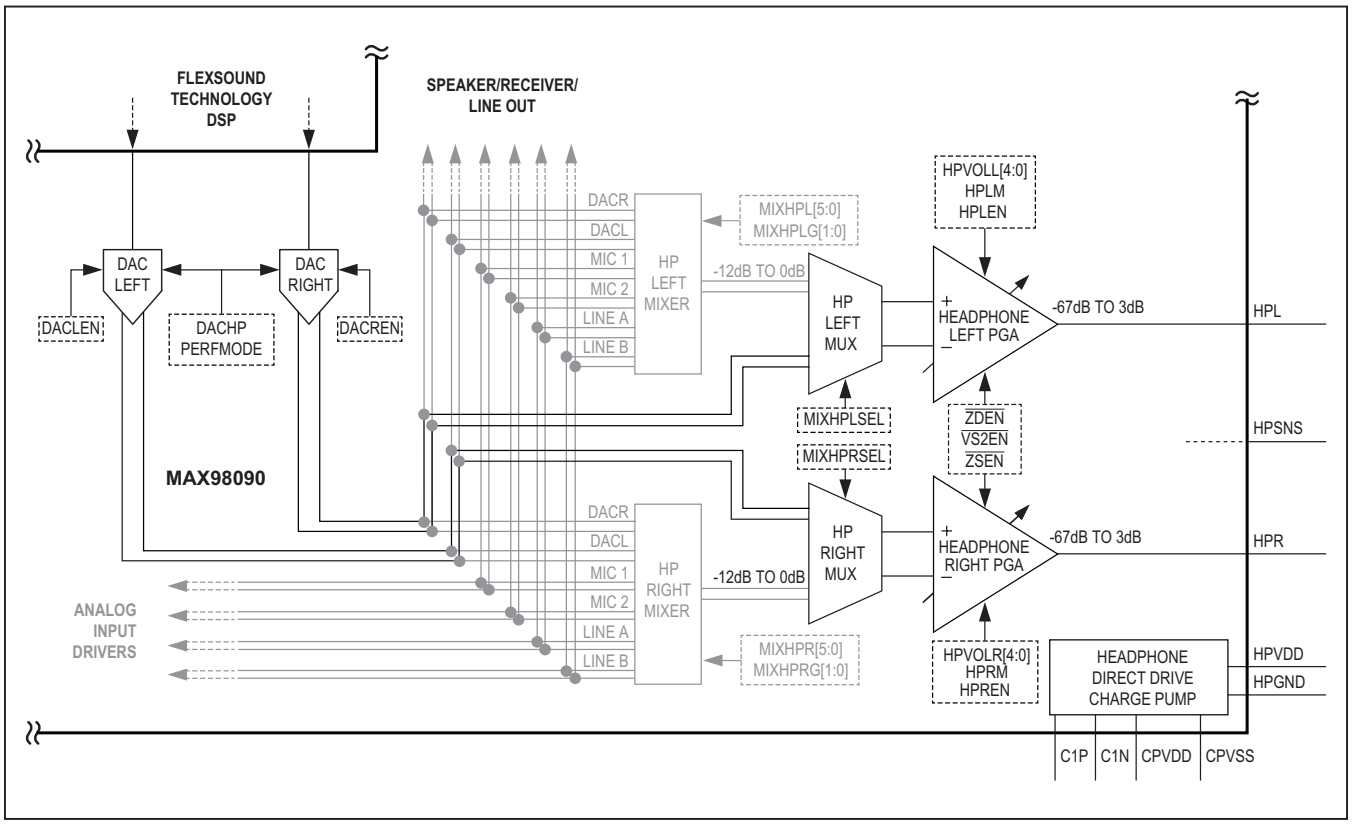


Figure 37. Reduced Power DAC Playback to Headphone Output Configuration

The headphone output programmable gain amplifiers (PGAs) have a wide volume adjustment range from -67dB to +3dB, provide a high attenuation mute control (Table 72 and Table 73), and feature programmable click-and-pop reduction options. See the *Click-and-Pop Reduction* section for details.

Table 72. Left Headphone Amplifier Volume Control Register

ADDRESS: 0x2C				DESCRIPTION
BIT	NAME	TYPE	POR	
7	HPLM	R/W	0	**Left Headphone Output Mute Enable** 0 : Headphone output volume set by the volume control bits. 1 : Headphone output muted.
6	—	—	—	—
5	—	—	—	—
4	HPVOLL[4:0]	R/W	1	**Left Headphone Output Amplifier Volume Control Configuration** 0x1F: +3dB 0x17: -3dB 0x0F: -17dB 0x07: -40dB 0x1E: +2.5dB 0x16: -4dB 0x0E: -19dB 0x06: -43dB 0x1D: +2dB 0x15: -5dB 0x0D: -22dB 0x06: -47dB 0x1C: +1.5dB 0x14: -7dB 0x0C: -25dB 0x04: -51dB 0x1B: +1dB 0x13: -9dB 0x0B: -28dB 0x03: -55dB 0x1A: +0dB 0x12: -11dB 0x0A: -31dB 0x02: -59dB 0x19: -1dB 0x11: -13dB 0x09: -34dB 0x01: -63dB 0x18: -2dB 0x10: -15d 0x08: -37dB 0x00: -67dB
3			1	
2			0	
1			1	
0			0	

Table 73. Right Headphone Amplifier Volume Control Register

ADDRESS: 0x2D				DESCRIPTION
BIT	NAME	TYPE	POR	
7	HPRM	R/W	0	**Right Headphone Output Mute Enable** 0 : Headphone output volume set by the volume control bits. 1 : Headphone output muted.
6	—	—	—	—
5	—	—	—	—
4	HPVOLR[4:0]	R/W	1	**Right Headphone Output Amplifier Volume Control Configuration** 0x1F: +3dB 0x17: -3dB 0x0F: -17dB 0x07: -40dB 0x1E: +2.5dB 0x16: -4dB 0x0E: -19dB 0x06: -43dB 0x1D: +2dB 0x15: -5dB 0x0D: -22dB 0x06: -47dB 0x1C: +1.5dB 0x14: -7dB 0x0C: -25dB 0x04: -51dB 0x1B: +1dB 0x13: -9dB 0x0B: -28dB 0x03: -55dB 0x1A: +0dB 0x12: -11dB 0x0A: -31dB 0x02: -59dB 0x19: -1dB 0x11: -13dB 0x09: -34dB 0x01: -63dB 0x18: -2dB 0x10: -15dB 0x08: -37dB 0x00: -67dB
3			1	
2			0	
1			1	
0			0	

Headphone Ground Sense

To improve channel isolation, the device has a low-side headphone sense (HPSNS) that senses the ground return of the headphone load. For optimal performance, connect the headphone sense line through an isolated trace to a point as close as possible to the ground pole of the headphone jack (Figure 38). If this is not possible, or if headphone sense is not used, connect it to the analog ground plane. In this configuration, channel isolation can be degraded, resulting in increased channel-to-channel crosstalk.

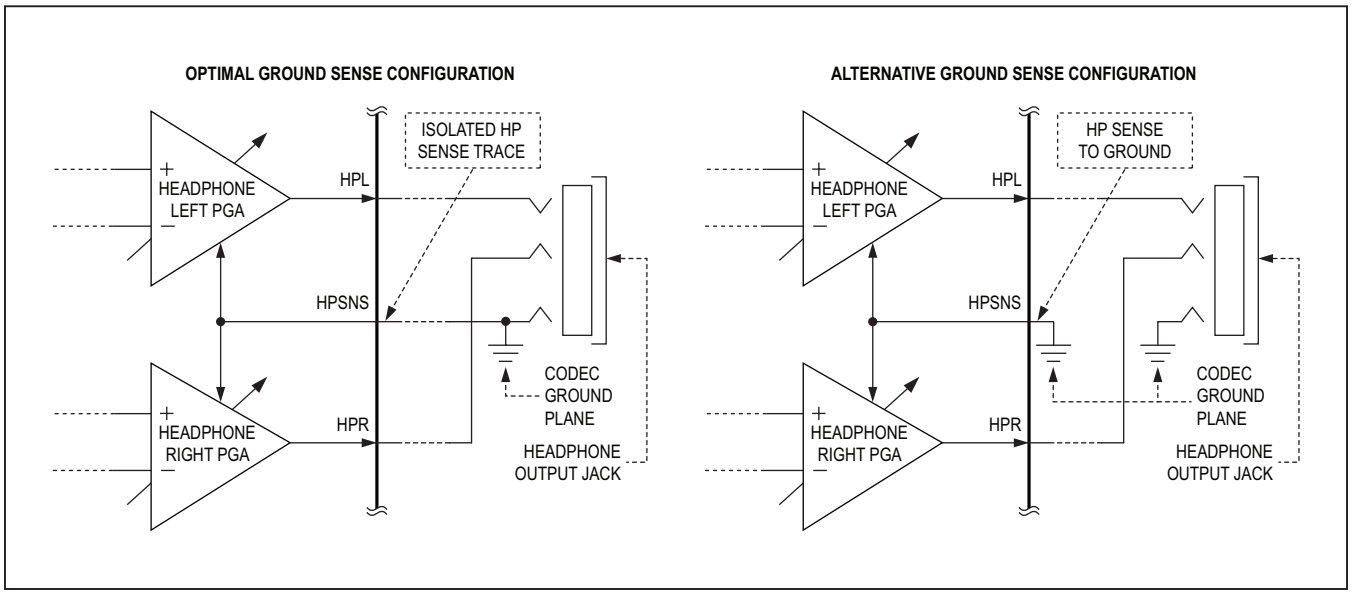


Figure 38. Headphone Output Ground Sense Connections

DirectDrive Headphone Output Amplifier

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically at either half the high-side supply, or at a bandgap referenced common mode level). As a result, large coupling capacitors are needed to block this DC bias and AC-couple the audio output to the headphone load. Without these capacitors, a significant DC current would flow through the ground referenced headphone load. The result is both unnecessary power dissipation, and potential damage to both the headphone load and amplifier.

Maxim's second-generation DirectDrive architecture solves this problem by using a charge pump to create an internal negative supply voltage. This increases the overall output signal swing while at the same time, allowing the headphone outputs to be biased at GND even while operating from a single supply (Figure 39). Without a DC bias component, there is no need for the large AC-coupling capacitors. Instead of two large (typically 220µF) capacitors, the charge pump only requires three small ceramic capacitors. This conserves board space, reduces cost, and improves the frequency response of the headphone amplifier.

Class H Amplifier Charge Pump

A Class H amplifier has the same output architecture as a Class AB amplifier. However, in a Class H amplifier the power supplies are modulated by the output signal. The integrated headphone charge pump generates both the positive and negative power supply for the headphone output amplifier. To maximize efficiency, both the charge pump's switching frequency and output voltage level and format change based on the headphone output signal level.

The charge pump has three different operating ranges each with a different switching frequency. The two lower power ranges use a three-level switching scheme to generate half supply rails at $\pm V_{HPVDD}/2$ while the high power range uses a standard two-level switching scheme to generate full supply rails at $\pm V_{HPVDD}$. The switching frequency and voltage levels of each range are optimized to maintain high efficiency while meeting the different output power requirements (Table 74).

Table 74. Charge-Pump Operating Ranges

RANGE	HEADPHONE OUTPUT LEVEL (% of V_{HPVDD})	CHARGE PUMP CONFIGURATION		
		FREQUENCY (kHz)	$V_{CPVDD/CPVSS}$	WAVEFORM
1	< 10	~82	$\pm V_{HPVDD}/2$	Range 1
2	10 to 25	~660	$\pm V_{HPVDD}/2$	Range 2
3	> 25	~500	$\pm V_{HPVDD}$	Range 3

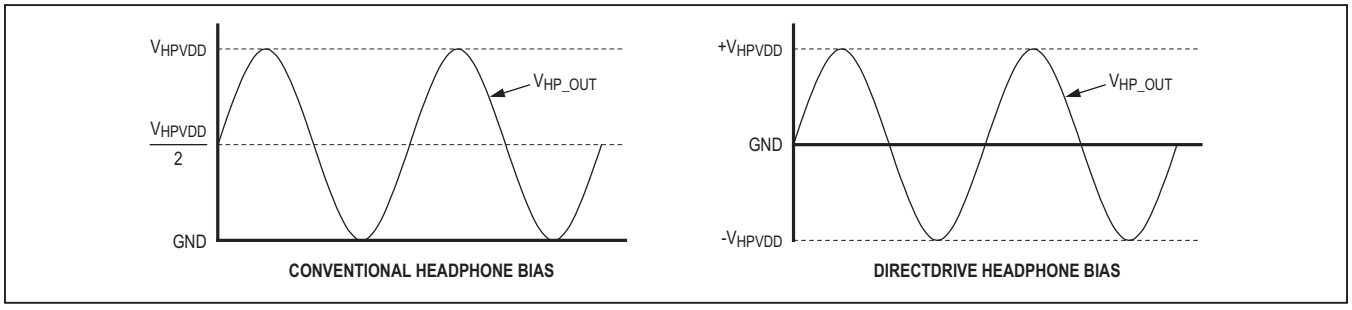


Figure 39. Conventional vs. DirectDrive Headphone Output Bias

Range 1 (V_{HP_OUT} < 10% of V_{HPVDD}): When the output signal level is less than 10% of HPVDD, the output signal swing is low and the power consumption for driving the headphone load is small relative to the charge pump quiescent consumption and switching losses. Therefore, to minimize switching losses, the charge-pump frequency is reduced to its lowest rate (~82kHz) and the bipolar output supply rails are set to half of HPVDD or $\pm V_{HPVDD}/2$ (Figure 40, Range 1).

Range 2 (10% of V_{HPVDD} ≤ V_{HP_OUT} < 25% of V_{HPVDD}): When the output signal level is between 10% and 25% of HPVDD, the output signal swing is still less than half of HPVDD. However, the load power consumption requirements are now much higher than the charge-pump quiescent consumption and switching losses. To meet the increased load power requirements, the charge-pump switching frequency increases (~660kHz) while the bipolar output supply rails remain at half of HPVDD or $\pm V_{HPVDD}/2$ (Figure 40, Range 2).

Range 3 (25% of V_{HPVDD} ≤ V_{HP_OUT}): When the output signal level exceeds 25% of HPVDD, the output signal swing is much wider. As a result, the charge pump now generates bipolar full HPVDD output supply rails ($\pm V_{HPVDD}$). The switching frequency in this range is slightly lower (~500kHz). However, the increased voltage differential allows the headphone output driver to reach its maximum voltage swing and load driving capability (Figure 40, Range 3).

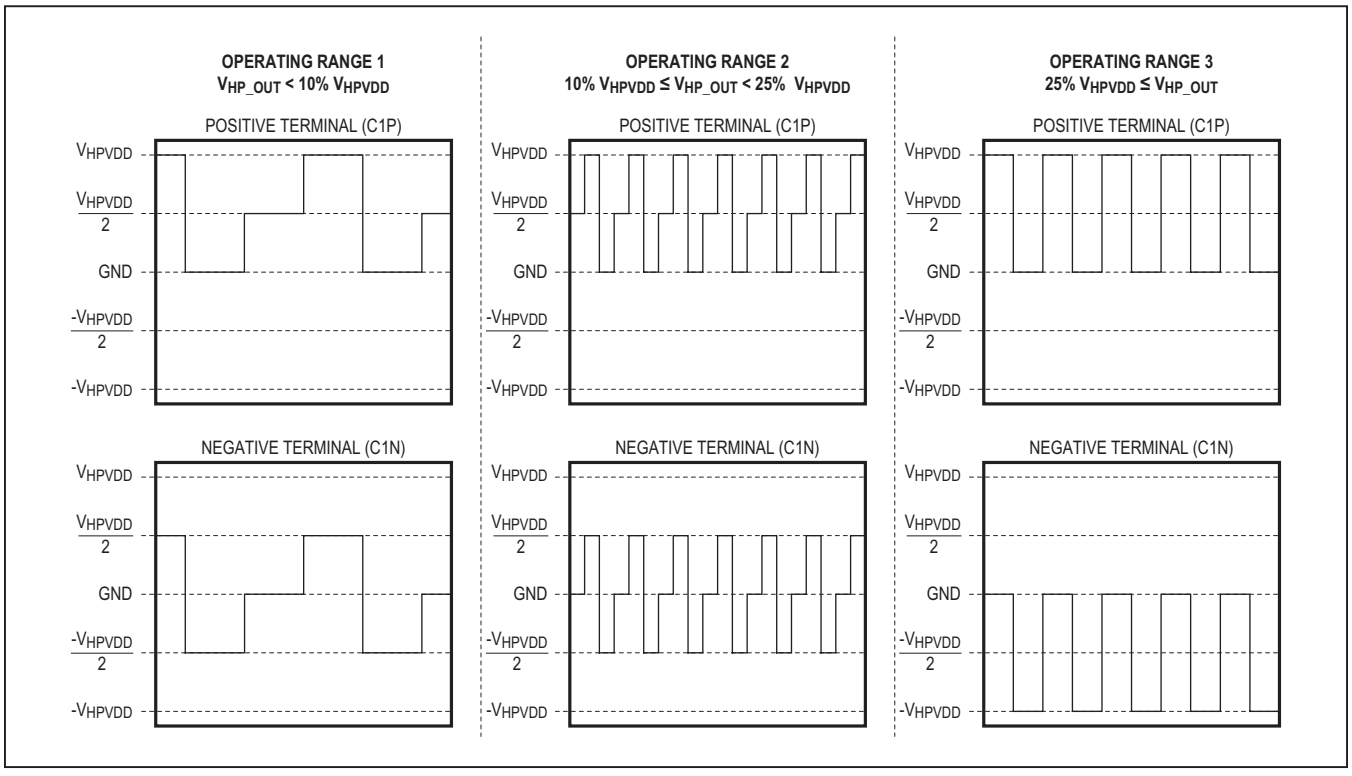


Figure 40. Class H Amplifier Charge Pump Operating Ranges

To prevent audible crosstalk, the switching frequency in all three charge pump ranges is well outside of the audio band. In addition, to prevent audible distortion during supply range changes, the charge pump transitions from one output power range to another very quickly. When changing from the half supply range ($\pm V_{HPVDD}/2$) to the full supply range ($\pm V_{HPVDD}/2$), the transition occurs immediately if the threshold is exceeded (to avoid clipping for a rapidly increasing audio output). When moving back down, there is a 32ms delay between the threshold detection and the supply range transition. The quick supply level transitions draw a significant transient current from HPVDD. To prevent a droop/glitch on HPVDD, the bypass capacitance must be appropriate to supply the required transient current (Figures 53 and 54).

Click-and-Pop Reduction

The device includes extensive click-and-pop reduction circuitry designed to minimizes audible clicks and pops at turn-on, turn-off, and during volume changes. These features include zero-crossing detection, volume change smoothing, and volume change stepping (Table 75).

Zero-crossing detection is available on the analog microphone input PGAs and all analog output PGAs and volume controls to prevent large glitches when volume changes are made. Instead of making a volume change immediately, the change is made when the audio signal crosses the midpoint (Figure 42). If no zero crossing occurs within the timeout window (100ms), the volume change occurs regardless of signal level.

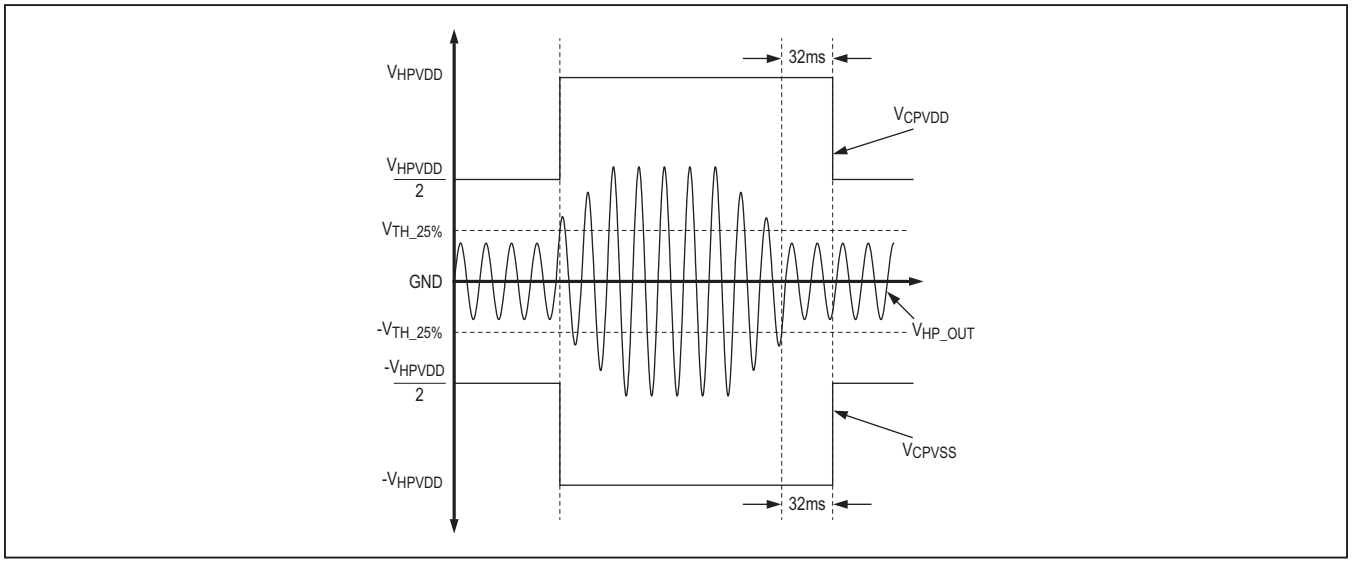


Figure 41. Class H Amplifier Supply Range Transitions

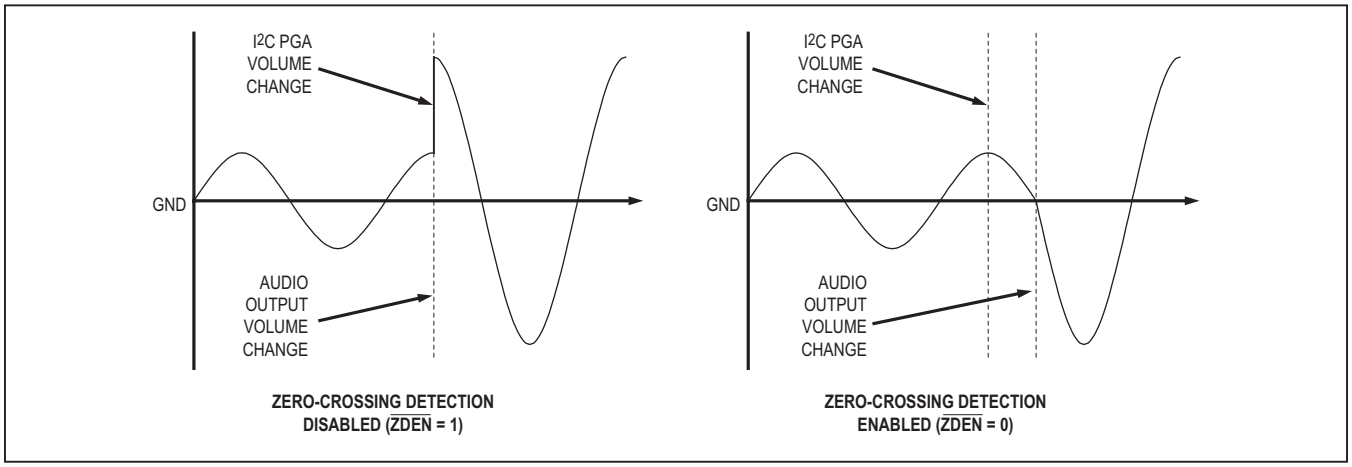


Figure 42. Zero-Crossing Detection

Table 75. Zero-Crossing Detection and Volume Smoothing Configuration Register

ADDRESS: 0x40				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	$\overline{ZDEN}$	R/W	0	**Zero-Crossing Detection** 0: Volume changes made only at zero crossings or after approximately 100ms. 1: Volume changes made immediately upon request.
1	$\overline{VS2EN}$	R/W	0	**Enhanced Volume Smoothing** Only valid is volume adjustment smoothing is enabled ($\overline{VSEN}$ = 0). 0: Each volume change waits until the previous volume step has been applied to the output. Allows volume smoothing to function with zero-crossing timeout. 1: Volume smoothing enhancement is disabled.
0	$\overline{VSEN}$	R/W	0	**Volume Adjustment Smoothing** 0: Volume changes are smoothed by stepping through intermediate levels. 1: Volume changes are made directly in a single step.

Volume smoothing is available on all analog output PGAs. When enabled, all volume changes are broken into the smallest available step size. The volume is then ramped through each step between the initial and final volume setting at a rate of one step every 1ms. Volume smoothing also occurs at device turn-on and turn-off. During turn-on, the volume is first set to mute before the output is enabled. Once enabled, mute is first disabled and then the volume is ramped to the programmed level. At turn-off, the volume is ramped down to the minimum gain, and then muted, before the outputs are disabled. If zero-crossing detection is enabled, each volume step occurs at a zero crossing.

When no audio signal is present, zero-crossing detection can timeout and prevent volume smoothing from occurring. Enable enhanced volume smoothing to prevent the volume controller from requesting another volume step until the previous step has been set. Each step in the volume ramp then occurs either after a zero crossing has occurred in the audio signal or after the timeout window has expired.

During PGA turn-off, volume smoothing ramps the volume down to the minimum setting, if enabled. However, to prevent long turn off times enhanced volume smoothing and zero-crossing detection is not applied at PGA mute or turn-off. If volume smoothing is too slow or is not used, the zero-crossing detection can still be used to minimize click and pop when disabling an output PGA. First ramp the PGA volume down to (in one step or multiple steps) its minimum volume setting. Zero-crossing detection is applied to each step of the volume change. Then, once at the minimum volume, either enable mute or disable the output PGA.

Jack Detection

The device features a flexible, software configurable jack detection interface. Once enabled, the jack detection interface uses two internal comparators to sense the insertion/removal of a jack and identify the type of jack inserted (headphones or headset). When the device is in shutdown or the microphone bias is disabled, the comparator thresholds are referenced to $V_{SPKLVDD}$. When the device is active and microphone bias is enabled, the comparator thresholds are referenced to $V_{MICBIAS}$.

Jack detection operation relies on a pullup resistance to set the bias when no jack is inserted. When the device is in shutdown mode or the microphone bias is disabled (MICBIAS is high impedance), an internal pullup is enabled on JACKSNS, and is referenced to the SPKLVDD supply. When the device is not in shutdown and the microphone bias is enabled, the internal pullup is disabled (JACKSNS is high impedance). In this state, successful jack detection requires an external pullup on JACKSNS to MICBIAS. The jack detection internal interface structure and typical external application circuit is shown in Figure 43.

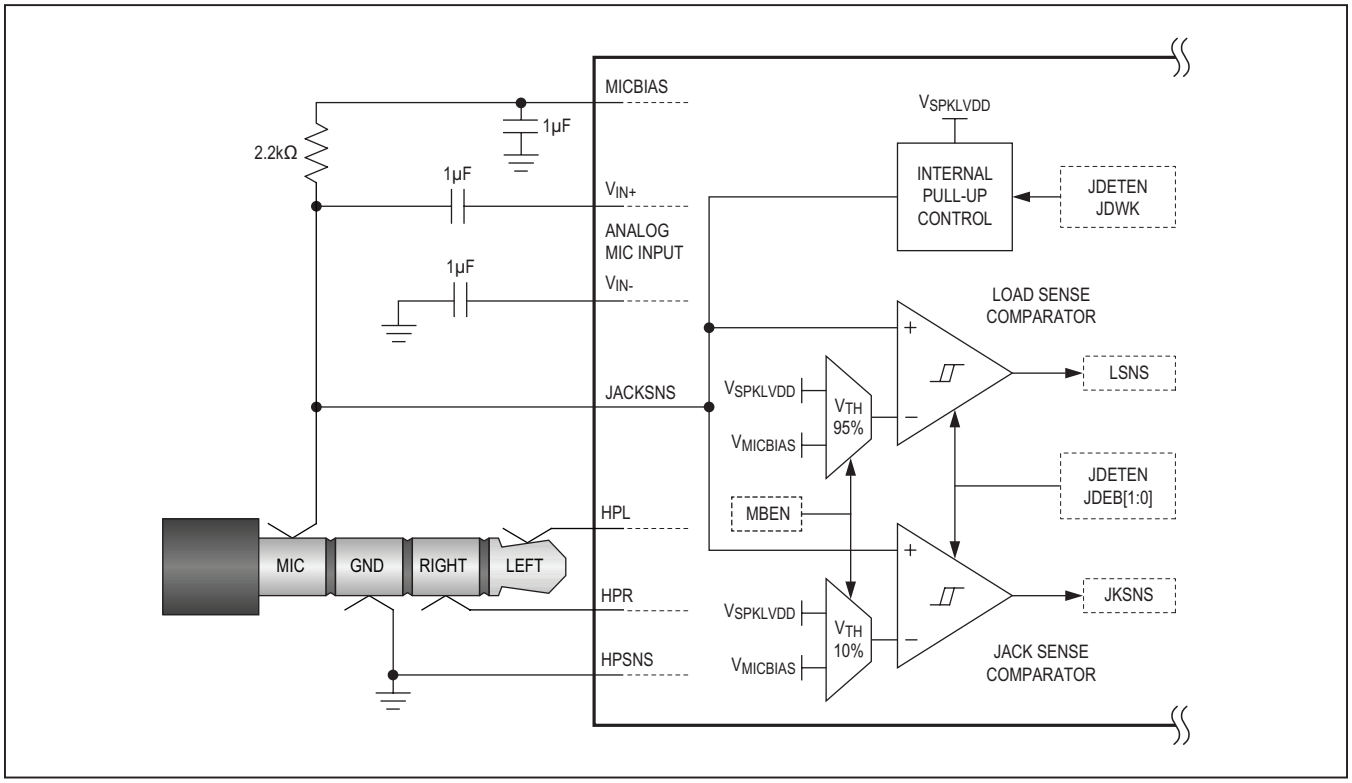


Figure 43. Block Diagram and Typical Application Circuit for Jack Detection

Table 76. Jack Detection Status Results

JACKSNS VOLTAGE	JACK DETECTION RESULTS		
	LSNS	JKSNS	STATE
$V_{TH_95\%} \le V_{JACKSNS}$	1	1	No jack detected
$V_{TH_10\%} \le V_{JACKSNS} < V_{TH_95\%}$	0	1	Headset detected
$V_{JACKSNS} < V_{TH_10\%}$	0	0	Headphones detected
No condition	1	0	Not possible/reserved

Jack Detection Internal Comparators

When enabled, the device detects jack insertion and removal by monitoring the voltage on JACKSNS with two internal comparators. The load sense comparator has a 95% threshold of the reference supply and is used to determine whether or not a jack has been inserted or removed. The jack sense comparator has a threshold of 10% of the reference supply, and is used to identify the type of jack (headphones/headset) inserted (Table 78).

When a jack is not inserted (open), the pullup resistance conducts high. In this state, $V_{JACKSNS}$ is above the load sense comparator threshold and LSNS is set high to indicate that no jack is inserted. When a jack is inserted it loads JACKSNS and pulls the voltage below the load sense comparator threshold. LSNS is then set low to indicate that a jack is now inserted. When the jack is removed, the pullup resistance once again conducts high and LSNS is set high to indicate that the jack was removed.

When a jack is inserted, the loading on JACKSNS pulls the voltage below the load sense comparator threshold. However, depending on the type of jack connected the voltage may or may not be pulled below the jack sense comparator threshold. If a headphone jack is inserted (3 pole), JACKSNS is shorted to ground. This pulls the voltage below the jack sense comparator threshold (10% of the reference supply) and JKSNS is set low to indicate headphones are inserted. If instead, a headset jack is inserted (4 pole, as shown in Figure 44), instead JACKSNS is biased to a voltage somewhere between the referenced supply and ground. In this case, $V_{JACKSNS}$ is above the jack sense comparator threshold but below the load sense comparator threshold. This state indicates that a headset is inserted. Table 76 details the three possible jack detection status results.

These comparators are only active when the JDETEN is set high. When jack detection is disabled, JACKSNS is in a high impedance state and the interface is completely shut down. When the device is in shutdown and JDETEN is low, LSNS and JKSNS retain their previous state regardless of the jack status.

Jack Detection Programmable Debounce

The load sense and jack sense comparators also have a programmable debounce timeout. The debounce timeout ensures that the jack detection status doesn't change unless the new state is persistent for longer than the timeout. This prevents rapid changes on LSNS and JKSNS during jack insertion/removal transients, and ensures that false jack detection interrupts are not generated. The debounce timeout can be programmed to one of four settings from 25ms to 200ms (Table 77).

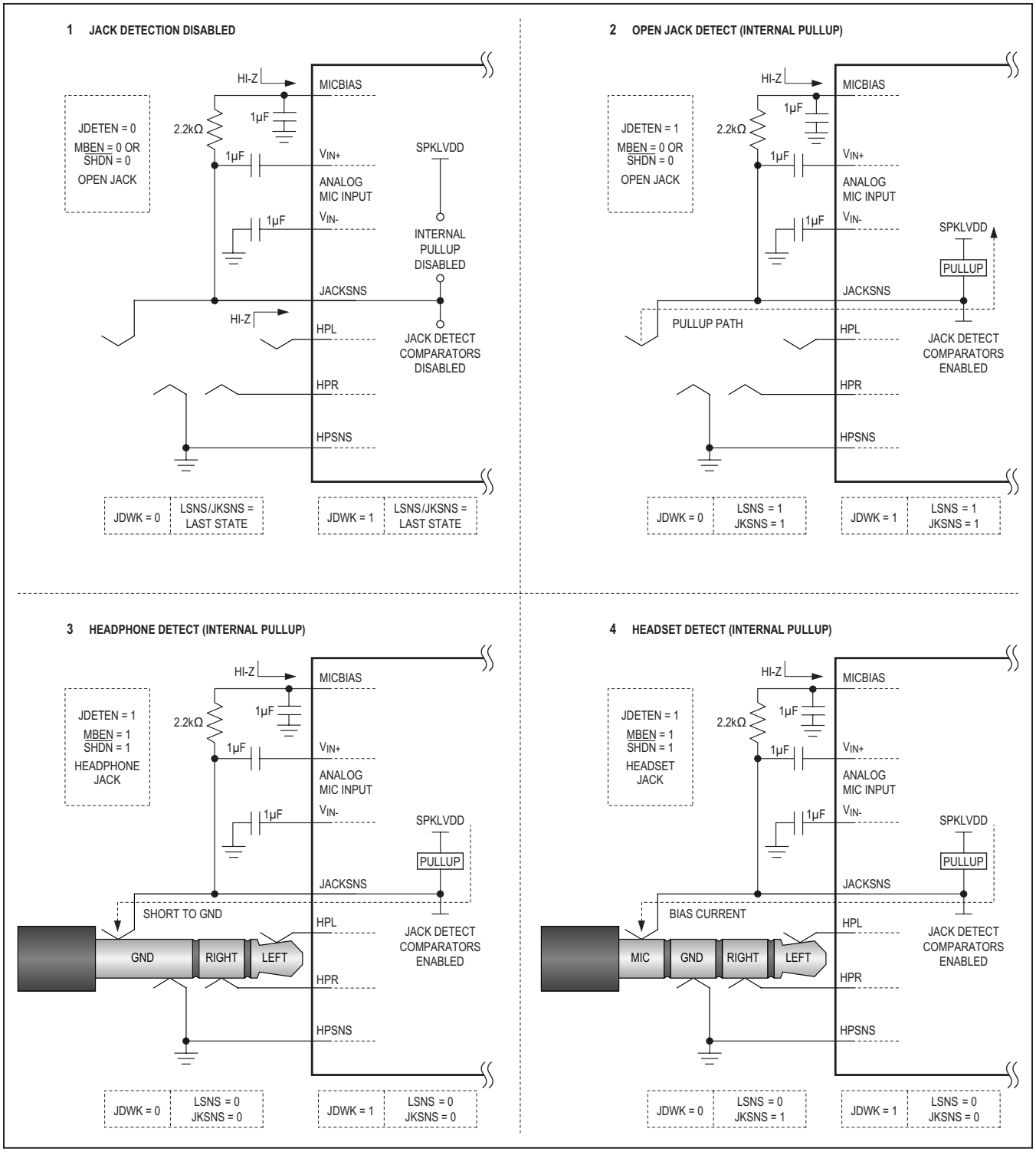


Figure 44. Jack Detection Cases with Internal Pullup Resistance

Jack Detection Interrupt Generation

Whenever a jack is inserted or removed and the state of either LSNS or JKSNS changes, a jack detection event is indicated with the jack configuration change flag (JDET, Table 85). If the jack detection event is not masked (IJDET, Table 86), it also generates an interrupt on $\overline{IRQ}$. The jack detection event bit (JDET) is clear on read. An I^2C read clears both the JDET bit status and the interrupt assertion on $\overline{IRQ}$ (if present). Unless a read occurs after each jack detection event, both the JDET bit and the $\overline{IRQ}$ interrupt will remain asserted and no new events or interrupts can be detected.

A change in state from LSNS = 1 to LSNS = 0 indicates that a jack has been inserted, while a change in state from LSNS = 0 to LSNS = 1 indicates that a jack has been removed. When an insertion occurs, if JKSNS does not change and remains at JKSNS = 1, a headset insertion is indicated, while a change in state from JKSNS = 1 to JKSNS = 0 indicates headphones have been inserted. The state transitions, and the interrupt events generated, are ideally used for state machine control in any jack detection software drivers.

Operation with an Internal Pullup Resistance

The device has both a strong and weak internal pullup option. The internal pullup resistors are only active if the device is in shutdown ($\overline{SHDN}$ = 0,Table 6) or when MICBIAS is disabled (MBEN = 0, Table 7), and they allow jack detection and identification to function in those states. This functionality is ideal for cases where the device is put into a sleep or shutdown state, but needs to trigger a device or system level interrupt signal for wake on insertion operation.

When JDWK is low (default, Table 77), the strong internal pullup is used (approximately 2.4kΩ referenced to SPKLVDD). This configuration is capable of detecting and identifying both headphone and headset insertion. When JDWK is high, the weak internal pullup (approximately 5µA to SPKLVDD) is used. The weak internal pullup minimizes the supply current after jack insertion and is ideal for wake on insertion cases where the system might not immediately power up. The weak internal pullup cannot bias a microphone load, and therefore, cannot identify headset insertion or accessory button presses.

Figure 44 details how jack detection works with the internal pullup resistance. In case 1, jack detection is disabled and both MICBIAS and JACKSNS are high impedance. In this state, LSNS and JKSNS retain the last valid jack detection result. In case 2, no jack is inserted and the internal pullup resistance to SPKLVDD conducts JACKSNS up above both the load and jack sense comparator thresholds. In this case, with an open circuit jack, both the strong and weak internal pullups produce the correct jack detection result and the only power consumption is that required to bias the internal comparators. In case 3, a headphone jack is inserted shorting JACKSNS to ground, well below both the load and jack sense comparator thresholds. In this state, both the strong and weak internal pullups produce the correct jack detection result but the strong internal pullup consumes significantly more current than the weak internal pullup. In case 4, a headset jack is inserted. In this state, the strong and weak internal pullups produce different jack detection results. The strong internal pullup biases the headset MIC (and JACKSNS) to a level between the load sense and jack sense comparator thresholds that produces the correct jack detection result. The weak internal pullup, however, is not strong enough to bias a headset MIC and as a result it falsely reports that a headphones jack is present.

Operation with an External Pullup Resistance

The internal pullup resistance is sufficient for wake on interrupt or basic jack detection and identification, but an external pullup resistance to MICBIAS is required to properly bias and current limit a headset microphone (Figure 43). When jack detect is enabled and the device is active ($\overline{SHDN}$ = 1, Table 6) with MICBIAS enabled (MBEN = 1, Table 7), JACKSNS is placed into a high-impedance state and the internal pullup resistor is disabled. In this state, the external pullup resistor then determines the bias voltage level at JACKSNS.

Figure 45 details the operation of jack detection with an external pullup resistance. In Case 1, jack detection is disabled. As a result, the internal jack detect comparators are disabled and LSNS/JKSNS retain their last valid jack detection result. In case 2, no jack is inserted and the external pullup resistance to MICBIAS conducts JACKSNS up above both the load and jack sense comparator thresholds. In case 3, a headphone jack is inserted shorting JACKSNS to ground, well below both the load and jack sense comparator thresholds. In case 4, a headset jack is inserted and the external pullup biases the headset MIC (and JACKSNS) to a level between the load sense and jack sense comparator thresholds.

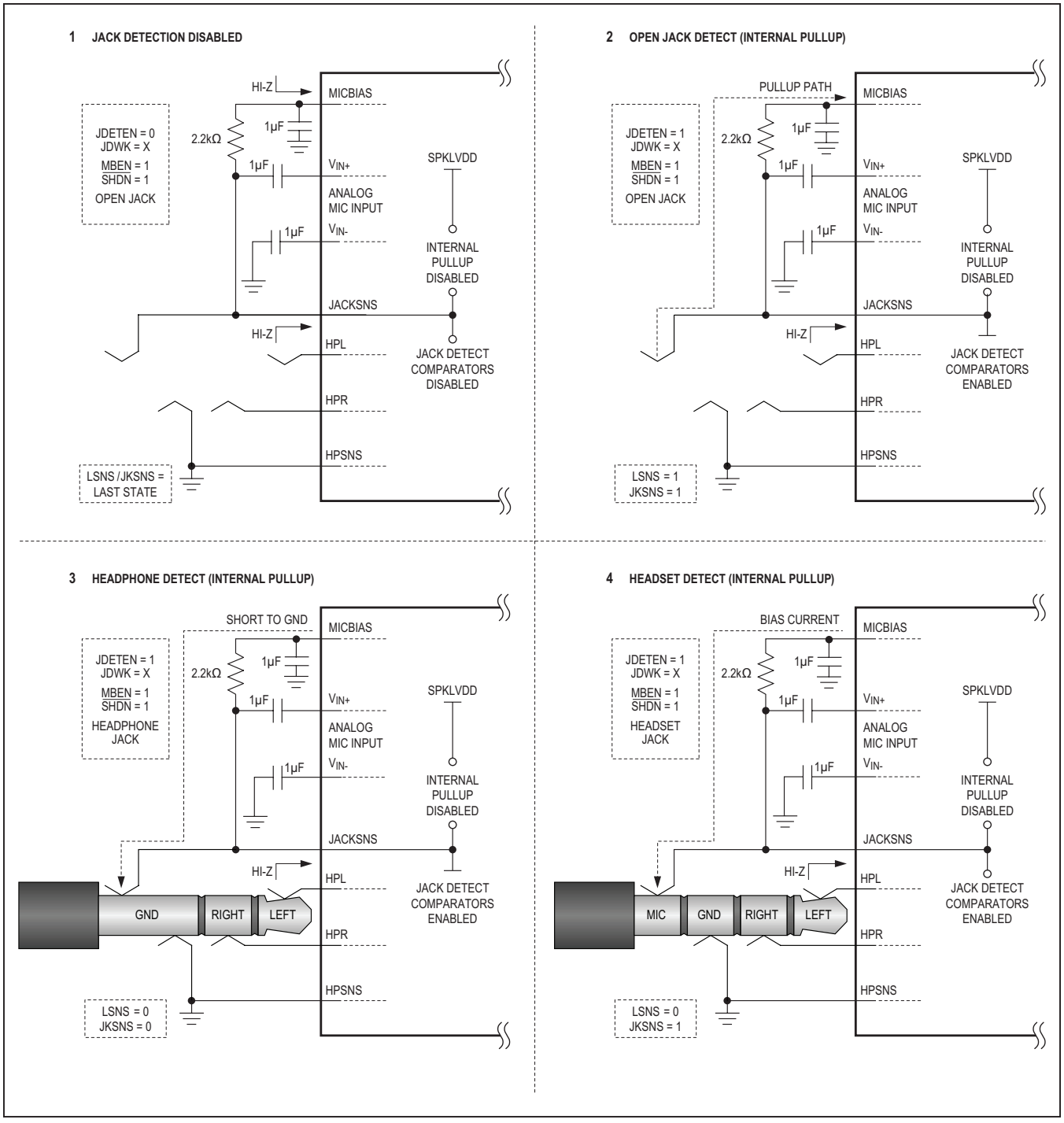


Figure 45. Jack Detection Operation with External Pullup Resistance

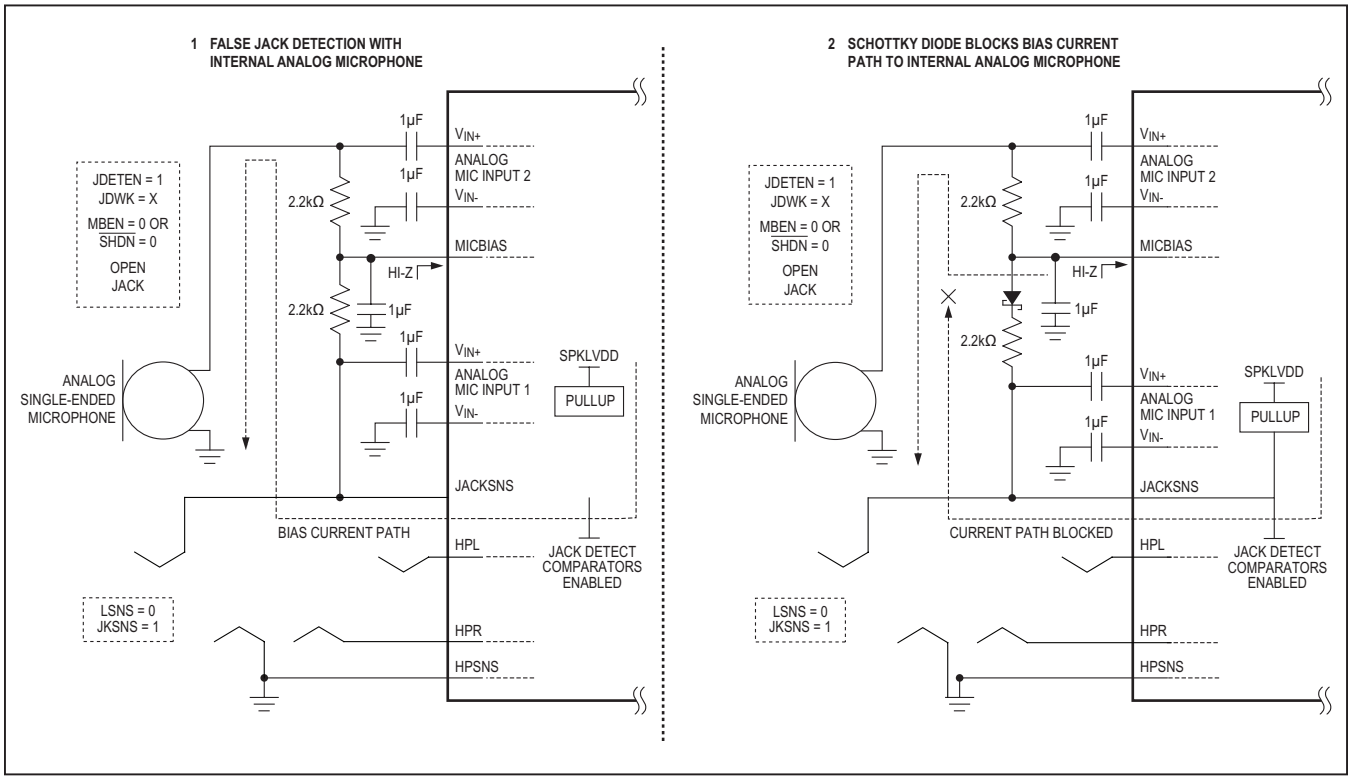


Figure 46. Jack Detection with Internal Analog Microphones

Accessory Button Detection

After jack insertion, the device can detect button presses on any accessories that include a microphone and a switch that shorts the microphone ring to ground. Button presses can be detected either when MICBIAS is enabled or if it is disabled and the strong internal pullup is used (JDWK = 0). A button press changes the state of JKSNS from 1 to 0 until the button is released, and this change in state generates an event on the jack detection change flag (JDET). This event is used to trigger the appropriate action associated with the key press.

Jack Detection with Internal Analog Microphones

If the application requires fixed internal analog microphone(s), and must also detect, identify, and operate with a headset microphone, the general jack detecaion application circuit (Figure 43) does not operate as expected. The complication introduced by an internal analog microphone is detailed in Figure 46.

When no jack is inserted (case 1) the internal pullup resistance attempts to pull JACKSNS above the load sense comparator threshold. However, the external pullup to MICBIAS creates an unintended current path through the internal analog microphone pullup. As a result, the voltage at JACKSNS is biased to a level between the jack sense and load sense comparator thresholds, resulting in a false headset jack detection. When a headset jack is inserted, there is a parallel load on JACKSNS between the inserted headset jack and the internal analog microphone. This could potentially result in a headset being reported as headphones.

A Schottky diode with a very low forward drop (case 2) can be inserted in series with the external pullup resistance. When MICBIAS is disabled, the Schottky diode is reverse biased and the current path is blocked. When MICBIAS is enabled, the diode is forward biased and the external pullup to mic bias functions as detailed in Figure 45. The diode does introduce a series voltage drop, and the MICBIAS voltage and/or the series resistance value might need to be adjusted to compensate and ensure that the headset MIC is properly biased. Alternatively, a switch can be used in series either above or below the internal analog microphone to break the bias current path when MICBIAS is disabled.

Table 77. Jack Detect Configuration Register

ADDRESS: 0x3D				DESCRIPTION
BIT	NAME	TYPE	POR	
7	JDETEN	R/W	0	**Jack Detect Enable** 0: Jack detect circuitry disabled 1: Jack detect circuitry enabled
6	JDWK	R/W	0	**JACKSNS Pullup Configuration** 0: 2.4kΩ resistor to SPKLVDD (allows microphone detection) 1: 5µA to SPKLVDD (minimizes supply current) Valid when MICBIAS = 0 or $\overline{SHDN}$ = 0.
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	—	—	—	—
1	JDEB[1:0]	R/W	0	**Jack Detect Debounce** Configures the jack detect debounce time: 00: 25ms 10: 100ms 01: 50ms 11: 200ms
0			0	

Table 78. Jack Status Register

ADDRESS: 0x02				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	—	—	—	—
4	—	—	—	—
3	—	—	—	—
2	LSNS	R	0	**Microphone Load Sense (Valid Only if JDETEN = 1)** 0: $V_{JACKSNS} \le 0.95V \times V_{SUPPLY}$ 1: $V_{JACKSNS} > 0.95V \times V_{SUPPLY}$ V_{SUPPLY} is determined by the state of MBEN and $\overline{SHDN}$ so that: MBEN = 0 or $\overline{SHDN}$ = 0: $V_{SUPPLY} = V_{SPKLVDD}$ (internal pullup) MBEN = 1 and $\overline{SHDN}$ = 1: $V_{SUPPLY} = V_{MICBIAS}$ (external pullup)
1	JKSNS	R	0	**Jack Connection Sense (Valid Only if JDETEN = 1)** 0: $V_{JACKSNS} < 0.1V \times V_{SUPPLY}$ 1: $V_{JACKSNS} \ge 0.1V \times V_{SUPPLY}$ V_{SUPPLY} is determined by the state of MBEN and $\overline{SHDN}$ so that: MBEN = 0 or $\overline{SHDN}$ = 0: $V_{SUPPLY} = V_{SPKLVDD}$ (internal pullup) MBEN = 1 and $\overline{SHDN}$ = 1: $V_{SUPPLY} = V_{MICBIAS}$ (external pullup)
0	—	—	—	—

Quick Setup Configuration

The quick setup configuration registers provide simple device configuration options for commonly used signal paths and settings. Each quick setup register contains write only, push-button configuration bits. When written high, a quick configuration bit will internally set all other appropriate register bits to program the device to the selected configuration. Writing a logical low to a quick configuration bit has no effect, and when read back all quick configuration bits always show a logic-low.

Quick setup bits change the state of registers appropriate to the selected configuration only. As such, they do not remove or reset existing device settings that do not share the same configuration registers. This allows complementary selections from several different quick configuration registers to be used together in a logical sequence to configure the device. Do not combine multiple quick setup bits that configure either the same section or any shared data path as part of a single sequence. This type of sequence might not produce the desired results as later quick setup bits may overwrite registers programmed by earlier selections.

The digital audio interface (DAI) quick setup register (Table 79) is used to select the DAI data format. The configurations in this register program the master mode clock configuration register (Table 34), the DAI format configuration register (Table 46), and the DAI TDM control register (Table 47).

The playback path quick setup register (Table 80) is used to configure the digital playback path and to select and program an analog output. The configuration bits in this register program the DAI I/O configuration register (Table 45), the output enable register (Table 8), and the selected analog output mixer, volume, and control registers (headphones, receiver, speaker, or line output).

Table 79. Digital Audio Interface (DAI) Quick Setup Register

ADDRESS: 0x06				DESCRIPTION
BIT	NAME	TYPE	POR	
7	—	—	—	—
6	—	—	—	—
5	RJ_M	W	0	Sets up DAI for right-justified master mode operation.
4	RJ_S	W	0	Sets up DAI for right-justified slave mode operation.
3	LJ_M	W	0	Sets up DAI for left-justified master mode operation.
2	LJ_S	W	0	Sets up DAI for left-justified slave mode operation.
1	I2S_M	W	0	Sets up DAI for I²S master mode operation.
0	I2S_S	W	0	Sets up DAI for I²S slave mode operation.

Table 80. Playback Path Quick Setup Register

ADDRESS: 0x07				DESCRIPTION
BIT	NAME	TYPE	POR	
7	DIG2_HP	W	0	Sets up the DAC to headphone path.
6	DIG2_EAR	W	0	Sets up the DAC to receiver path.
5	DIG2_SPK	W	0	Sets up the DAC to speaker path
4	DIG2_LOUT	W	0	Sets up the DAC to line out path.
3	—	—	—	—
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

The analog microphone/direct input to record path quick setup register (Table 81) is used to select and program an analog input and to configure the digital record path. The configuration bits in this register program the DAI I/O configuration register (Table 45), the input enable register (Table 7), and the appropriate input mixer, volume, and control registers (analog microphone or direct to ADC mixer).

The line input to record path quick setup register (Table 82) is used to program the analog input and to configure the digital record path. The configuration bits in this register program the DAI I/O configuration register (Table 45), the input enable register (Table 7), and the appropriate input mixer, volume, and control registers (single-ended or differential line input).

Table 81. Analog Microphone/Direct Input to Record Path Quick Setup Register

ADDRESS: 0x08				DESCRIPTION
BIT	NAME	TYPE	POR	
7	IN12_MIC1	W	0	Sets up the IN1/IN2 to microphone 1 to ADCL path
6	IN34_MIC2	W	0	Sets up the IN3/IN4 to microphone 2 to ADCR path
5	—	—	—	—
4	—	—	—	—
3	IN12_DADC	W	0	Sets up the IN1/IN2 direct to ADCL path
2	IN34_DADC	W	0	Sets up the IN3/IN4 direct to ADCR path
1	IN56_DADC	W	0	Sets up the IN5/IN6 direct to ADCL path (WLP only)
0	—	—	—	—

Table 82. Line Input to Record Path Quick Setup Register

ADDRESS: 0x09				DESCRIPTION
BIT	NAME	TYPE	POR	
7	IN12S_AB	W	0	Sets up stereo single-ended record: IN1/IN2 to line in A/B to ADCL/R
6	IN34S_AB	W	0	Sets up stereo single-ended record: IN3/IN4 to line in A/B to ADCL/R
5	IN56S_AB	W	0	Sets up stereo single-ended record: IN5/IN6 to line in A/B to ADCL/R (WLP only)
4	IN34D_A	W	0	Sets up mono differential record: IN3/IN4 to line in A to ADCL
3	IN65D_B	W	0	Sets up mono differential record: IN6/IN5 to line in B to ADCR (WLP only)
2	—	—	—	—
1	—	—	—	—
0	—	—	—	—

The analog microphone input to analog output quick setup register (Table 83) is used to configure the analog input and to select and program an analog output. The configuration bits in this register program the input enable register (Table 7), the output enable register (Table 8), and the appropriate input and output mixer, volume, and control registers (analog microphone and either the headphones, speaker, receiver, or line output).

The line input to analog output quick setup register (Table 84) is used to configure the analog input and to select and program an analog output. The configuration bits in this register program the input enable register (Table 7), the output enable register (Table 8), and the appropriate input and output mixer, volume, and control registers (line input and either the headphones, speaker, receiver, or line output).

Table 83. Analog Microphone Input to Analog Output Quick Setup Register

ADDRESS: 0x0A				DESCRIPTION
BIT	NAME	TYPE	POR	
7	IN12_M1HPL	W	0	Sets up the IN1/IN2 differential to microphone 1 to headphone left path
6	IN12_M1SPKL	W	0	Sets up the IN1/IN2 differential to microphone 1 to speaker left path
5	IN12_M1EAR	W	0	Sets up the IN1/IN2 differential to microphone 1 to receiver path
4	IN12_M1LOUTL	W	0	Sets up the IN1/IN2 differential to microphone 1 to lineout left path
3	IN34_M2HPR	W	0	Sets up the IN3/IN4 differential to microphone 2 to headphone right path
2	IN34_M2SPKR	W	0	Sets up the IN3/IN4 differential to microphone 2 to speaker right path
1	IN34_M2EAR	W	0	Sets up the IN3/IN4 differential to microphone 2 to receiver path
0	IN34_M2LOUTR	W	0	Sets up the IN3/IN4 differential to microphone 2 to lineout right path

Table 84. Line Input to Analog Output Quick Setup Register

ADDRESS: 0x0B				DESCRIPTION
BIT	NAME	TYPE	POR	
7	IN12S_ABHP	W	0	Sets up the IN1/IN2 single ended to line In A/B to headphone L/R path
6	IN34D_ASPKL	W	0	Sets up the IN3/IN4 differential to line in A to speaker left path
5	IN34D_AEAR	W	0	Sets up the IN3/IN4 differential to line in A to receiver path
4	IN12S_ABLOUT	W	0	Sets up the IN1/IN2 single ended to line in A/B to lineout L/R path
3	IN34S_ABHP	W	0	Sets up the IN3/IN4 single ended to line in A/B to headphone L/R path
2	IN65D_BSPKR	W	0	Sets up the IN6/IN5 differential to line in B to speaker right path (WLP only)
1	IN65D_BEAR	W	0	Sets up the IN6/IN5 differential to line in B to receiver path (WLP only)
0	IN34S_ABLOUT	W	0	Sets up the IN3/IN4 single ended to line in A/B to lineout L/R path

Device Status Flags

The device uses register 0x01 (Table 85) and $\overline{IRQ}$ to report the status of various device functions. The status register bits are set when their respective events occur, and cleared upon reading the register. Device status can be determined either by polling register 0x01, or by configuring $\overline{IRQ}$ to pull low when specific events occur. $\overline{IRQ}$ is an open-drain output that requires a pullup resistor (10kΩ nominal) for proper operation. When first exiting shutdown (into normal operation), other status flags may assert based on the device settings, register sequencing, and clock sequencing.

Status Flag Masking

Register 0x03, the device status interrupt mask register (Table 86) determines which bits in the device status interrupt register (Table 85) can trigger a hardware interrupt

Table 85. Device Status Interrupt Register

ADDRESS: 0x01				DESCRIPTION
BIT	NAME	TYPE	POR	
7	CLD	CoR	0	**Clipping Detect Flag** 0: No clipping has occurred. 1: Digital record / playback clipping has occurred. CLD asserts when the digital record or playback path is clipping due to signal amplitude exceeding full-scale. This condition is detected at the record path gain control output (AVLG/AVRG), the playback path gain control output (DVG), and the parametric equalizer output. To resolve, adjust the gain settings near these detection points.
6	SLD	CoR	0	**Slew Level Detect Flag** 0: No volume slewing sequences have completed. 1: All volume / level slewing complete. SLD asserts when any one (or more) of the programmable-gain analog output volume controllers or digital level control arrays has completed slewing from a previous setting to a new programmed setting. If multiple settings are changed at the same time, in either the analog or digital domain, the SLD flag will assert only after the last slew is completed. SLD also asserts when the serial interface soft-start or soft-stop process has completed.
5	ULK	CoR	0	**Digital Audio Interface (DAI) Phase Locked Loop (PLL) Unlock Flag** 0: PLL is locked (if enabled and operating properly). 1: PLL is not locked (if enabled and operating properly). ULK reports that the digital audio phase-locked loop for DAI is not locked. This condition only occurs in slave mode when the deviation on LRCLK relative to PCLK exceeds the lock on range (approximately 4 PCLK periods). This condition can also occur if PCLK is running and LRCLK has been stopped outside of shutdown. Deviation in BCLK (or shutting it down) will never trigger a ULK assertion. DAI input and output data may not be processed / clocked correctly if a ULK event occurs.
4	—	—	—	—
3	—	—	—	—
2	JDET	CoR	0	**Jack Configuration Change Flag** 0: No change in jack configuration. 1: Jack configuration has changed. JDET asserts anytime jack detection is enabled, and either LSNS or JKSNS changes state (Table 78). If jack detection is enabled, JDET will assert correctly even while the device is in the shutdown state. This allows JDET to generate wake on insert interrupts.
1	DRCACT	CoR	0	**DRC Compression Flag** 0: The DRC is either disabled or not in the compression region. 1: The DRC is operating in the compression region.
0	DRCCLP	CoR	0	**DRC Clipping Flag** 0: The DRC is either disabled or no clipping has occurred. 1: DRC clipping has occurred.

on $\overline{IRQ}$ (assert low). By default, all of the device status interrupts (except JDET) only set the corresponding status bit and do not generate a hardware interrupt. Set the corresponding bit high in the mask register to enable hardware interrupts.

Device Revision Identification

The device provides a Revision ID Number register to allow the software to identify the current version of the device. The current device revision ID value is 0x43.

Table 86. Device Status Interrupt Mask Register

ADDRESS: 0x03				DESCRIPTION
BIT	NAME	TYPE	POR	
7	ICLD	R/W	0	**Clipping Detect Interrupt Enable** 0: Clipping detection only sets CLD (0x01[7]). 1: Clipping detection triggers $\overline{IRQ}$ and sets CLD (0x02[7]).
6	ISLD	R/W	0	**Slew Level Detect Interrupt Enable** 0: Slew level detection only sets SLD (0x01[6]). 1: Slew level detection triggers $\overline{IRQ}$ and sets SLD (0x02[6]).
5	IULK	R/W	0	**Digital PLL Unlock Interrupt Enable** 0: PLL Unlock Condition only sets ULK (0x01[5]). 1: PLL Unlock Condition triggers $\overline{IRQ}$ and sets ULK (0x02[5]).
4	—	—	—	—
3	—	—	—	—
2	IJDET	R/W	1	**Jack Configuration Change Interrupt Enable** 0: Changes in headset configuration only sets JDET (0x01[2]). 1: Changes in headset configuration triggers $\overline{IRQ}$ and sets JDET (0x01[2]).
1	IDRCACT	R/W	0	**DRC Compression Interrupt Enable** 0: DRC compression only sets DRCACT (0x01[1]). 1: DRC compression triggers $\overline{IRQ}$ and sets DRCACT (0x01[1]).
0	IDRCCLP	R/W	0	**DRC Clipping Interrupt Enable** 0: DRC clipping only sets DRCCLP (0x01[0]). 1: DRC clipping triggers $\overline{IRQ}$ and sets DRCCLP (0x01[0]).

Table 87. Revision ID Number Register

ADDRESS: 0xFF				DESCRIPTION
BIT	NAME	TYPE	POR	
7	REV_ID[7:0]	R	0	**Read Back the Revision ID of the Device** The current revision ID is 0x43.
6			1	
5			0	
4			0	
3			0	
2			0	
1			1	
0			1	

I²C Serial Interface

The MAX98090 features an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX98090 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX98090 by transmitting the proper slave address followed by the register address and then the data word.

Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX98090 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX98090 transmits the proper slave address followed by a series of nine SCL pulses. The MAX98090 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX98090 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Table 88. Device I²C Slave Address

PART NUMBER	READ ADDRESS	WRITE ADDRESS
MAX98090A	0x21	0x20
MAX98090B	0x23	0x22

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the MAX98090. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX98090 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX98090A, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the MAX98090A for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the MAX98090A for write mode. The address is the first byte of information sent to the MAX98090 after the START condition. Similarly, for the MAX98090B, the seven most significant bits are 0010001. Setting the read/write bit to 1 (slave address = 0x23) configures the MAX98090B for read mode. Setting the read/write bit to 0 (slave address = 0x22) configures the MAX98090B for write mode. The slave address are summarized in Table 88.

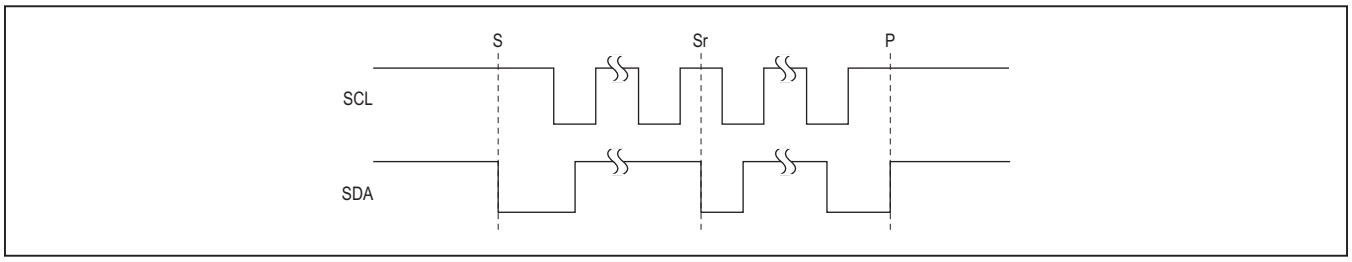


Figure 47. START, STOP, and REPEATED START Conditions

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX98090 uses to handshake receipt each byte of data when in write mode. The MAX98090 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX98090 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX98090, followed by a STOP condition.

Write Data Format

A write to the MAX98090 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 49 illustrates the proper frame format for writing one byte of data to the MAX98090. Figure 50 illustrates the frame format for writing n-bytes of data to the MAX98090.

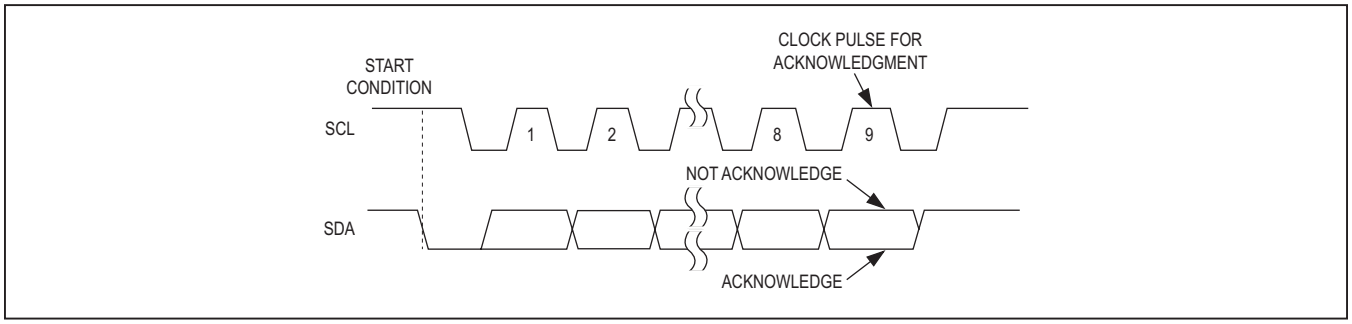


Figure 48. Acknowledge Timing

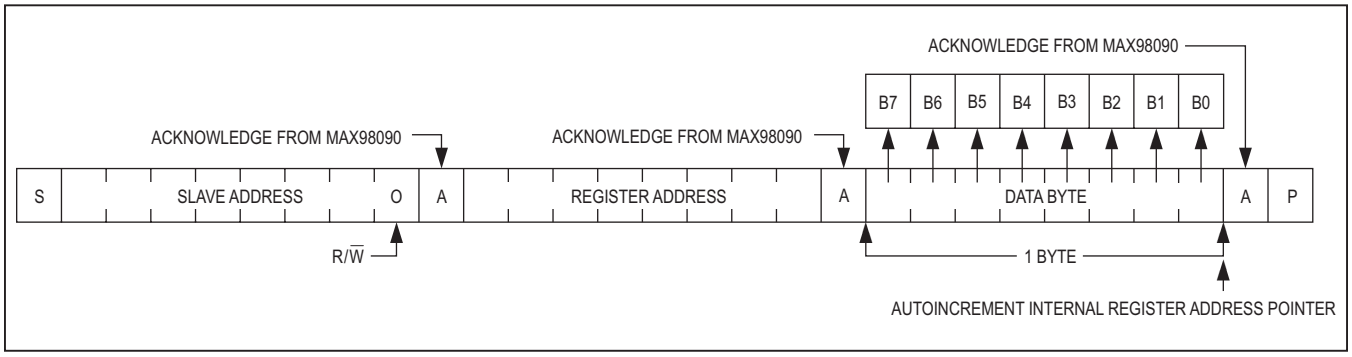


Figure 49. Writing One Byte of Data to the MAX98090

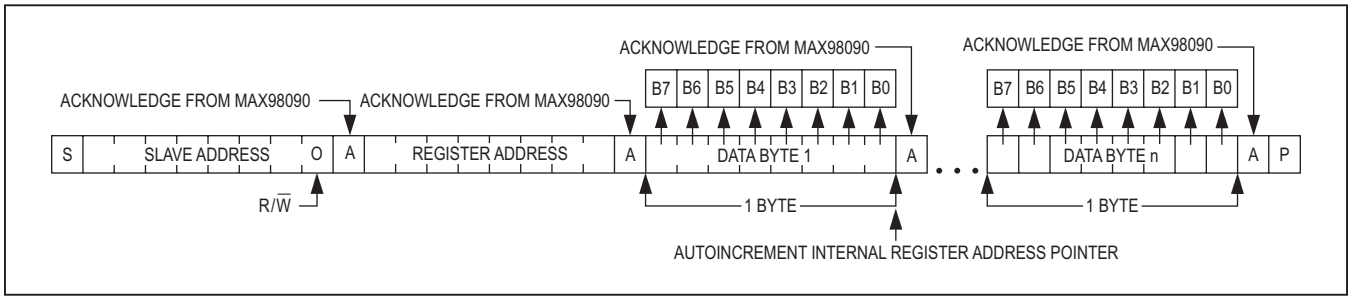


Figure 50. Writing n-Bytes of Data to the MAX98090

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX98090. The MAX98090 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX98090's internal register address pointer. The pointer tells the MAX98090 where to write the next byte of data. An acknowledge pulse is sent by the MAX98090 upon receipt of the address pointer data.

The third byte sent to the MAX98090 contains the data that is written to the chosen register. An acknowledge pulse from the MAX98090 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0xE7 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX98090 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX98090 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX98090's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX98090 then transmits the contents of the specified register, and the address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 51 illustrates the frame format for reading one byte from the MAX98090. Figure 52 illustrates the frame format for reading multiple bytes from the MAX98090.

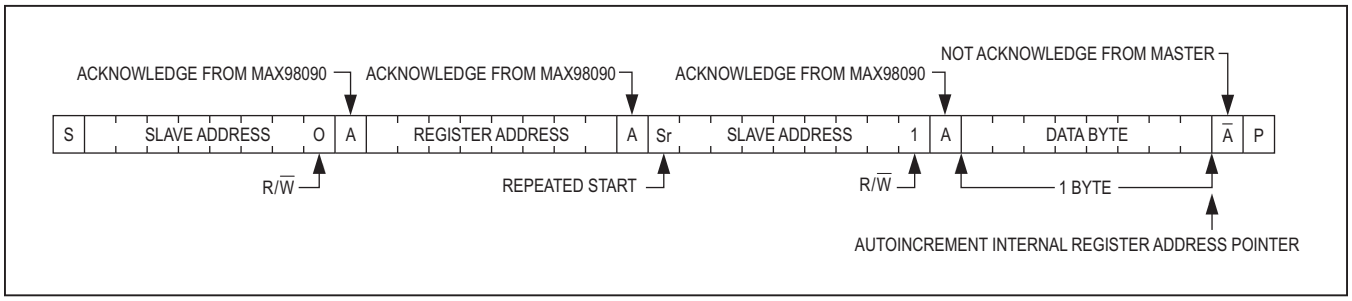


Figure 51. Reading One Byte of Data from the MAX98090

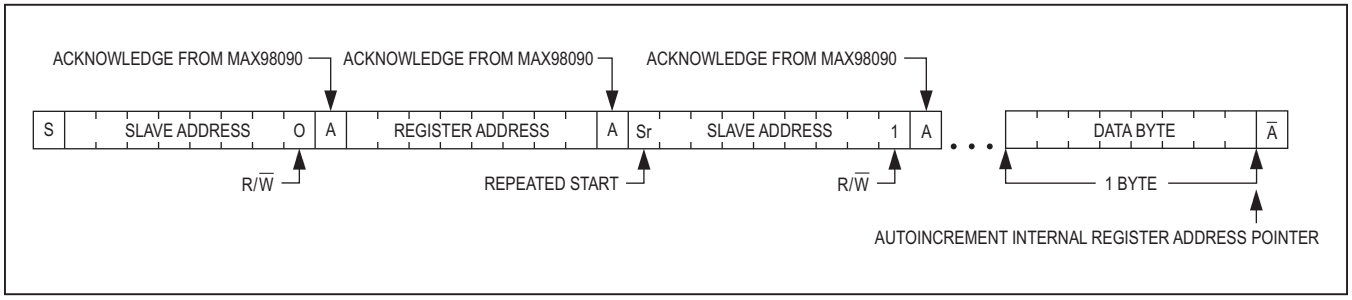


Figure 52. Reading n-Bytes of Data from the MAX98090

Applications Information

Typical Application Circuits

Figures 53 and 54 are two example application circuits for the device. The external components shown are the minimum required for the device to operate. Additional application specific components might be required.

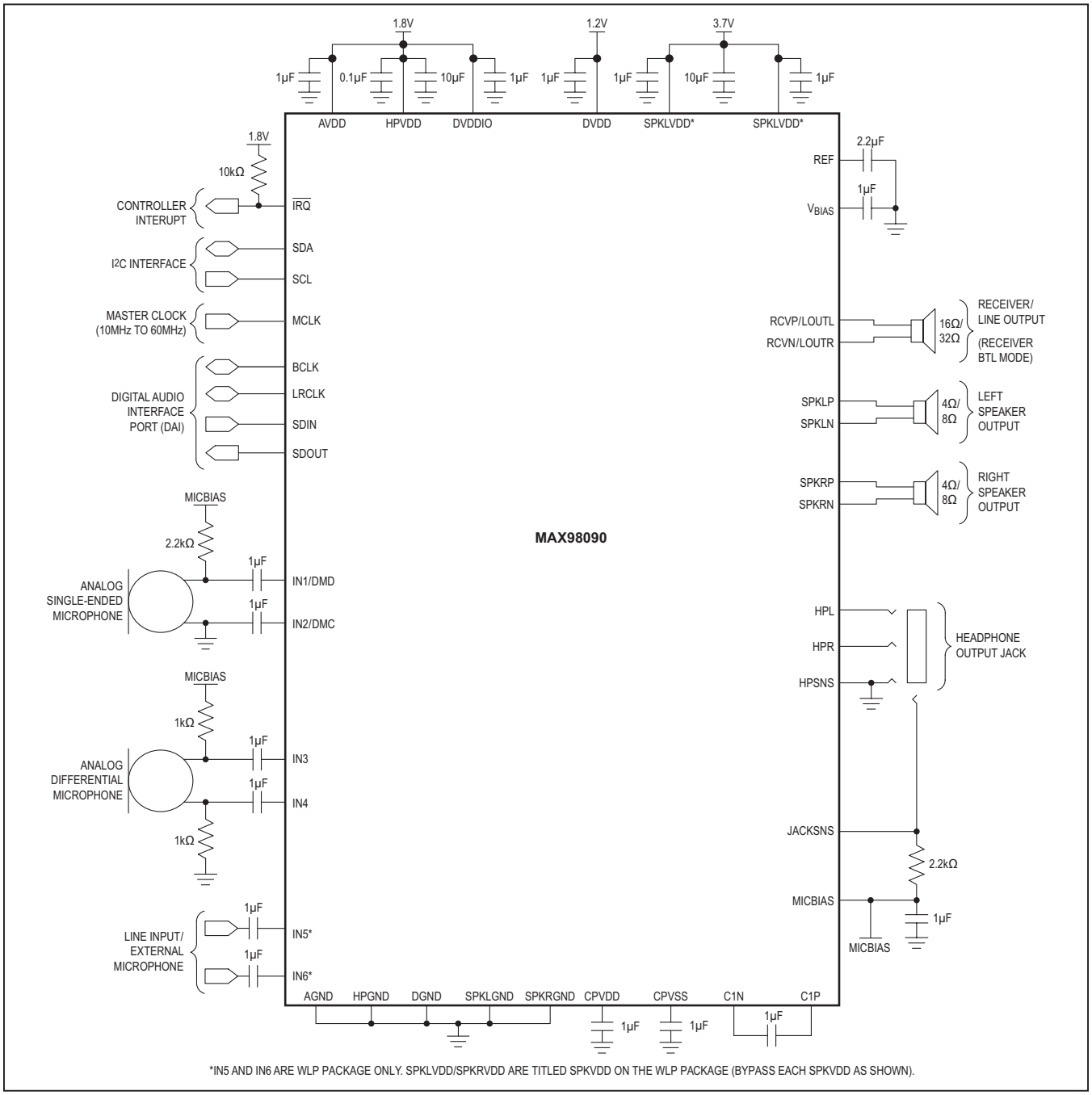
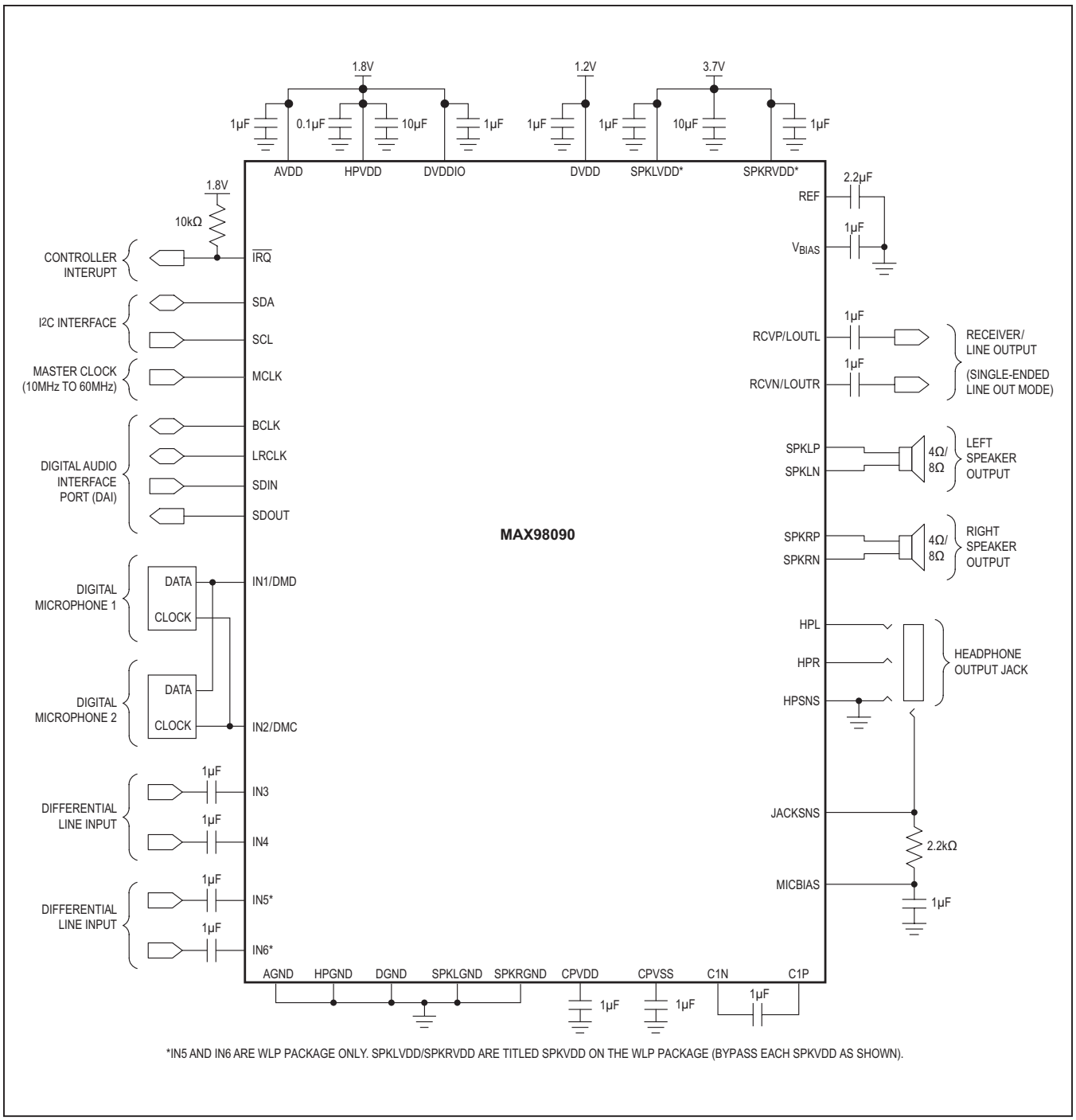


Figure 53. Typical Application Circuit with Analog Microphone Inputs and Receiver Output



*IN5 AND IN6 ARE WLP PACKAGE ONLY. SPKLVDD/SPKRVDD ARE TITLED SPKVDD ON THE WLP PACKAGE (BYPASS EACH SPKVDD AS SHOWN).

Figure 54. Typical Application Circuit with Digital Microphone Input and Stereo Line Outputs

Startup/Shutdown Register Sequencing

To ensure proper device initialization and minimal click-and-pop, program the devices control registers in the correct order. To shut down the device, simply set $\overline{SHDN}$ = 0. Table 89 details an example startup sequence for the device. To minimize click and pop on the analog output drivers (headphones, speakers, receiver, and line outputs), the output drivers should be powered using the following sequence:

1) Prior to powering the device ($\overline{SHDN}$ = 0) and before enabling the outputs, the output driver mute(s) should be enabled and the PGA gain(s) should be set to their lowest setting.
2) After all configuration settings are complete, power up the device ($\overline{SHDN}$ = 1).
3) Enable any analog outputs that are part of the desired configuration.
4) Disable the mute on each respective analog output.
5) If volume smoothing is disabled (Table 75), ramp the volume up, one register step at a time, from the minimum setting until the desired volume (gain) is reached (this sequence is part of the example in Table 89). If volume smoothing is enabled, this sequence is automatically implemented and the desired volume (gain) can be programmed in a single step.

While many configuration options and settings can be changed while the device is operating ($\overline{SHDN}$ = 1), some settings should only be adjusted with the device in shutdown ($\overline{SHDN}$ = 0). Table 90 lists the registers and bits that should not be changed during active operation. Changing these settings during normal operation ($\overline{SHDN}$ = 1) can compromise device stability and performance specifications. All external clocks (MCLK in master mode and MCLK, LRCLK, and BCLK in slave mode) must be running and stable before the device is taken out of shutdown. If the clocks are enabled or changed while the device is active (not in shutdown) phase errors and audible glitches may be introduced.

Table 89. Detailed Device Startup Sequence

SEQUENCE	DESCRIPTION	REGISTERS
1	Set $\overline{SHDN}$ = 0	0x45 (Default POR State)
2	Configure Clocks (also enable all external clocks)	0x1B to 0x21
3	Configure Digital Audio Interface (DAI)	0x22 to 0x25
4	Configure Digital Signal processing (DSP)	0x17 to 0x1A, 0x26 to 0x28, 0x33 to 0x36, 0x41
5	Load Coefficients	0x46 to 0xBD
6	Configure Power and Bias Mode	0x42 to 0x44
7	Configure Analog Mixers	0x0D, 0x15, 0x16, 0x29, 0x2A, 0x2B, 0x2E, 0x2F, 0x37, 0x3A
8	Configure Analog Gain and Volume Controls. To Minimize Click and Pop for Analog Outputs, Enable Mute and Set the Output PGAs to the minimum gain setting.	0x0E to 0x11, 0x2B to 0x2D, 0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C
9	Configure Miscellaneous Functions	0x03, 0x12, 0x13, 0x14, 0x40
11	Set $\overline{SHDN}$ = 1 (Power Up)	0x45
10	Enable Desired Functions	0x3D to 0x3F
11	Disable Mute on Analog Output Drivers	0x2C, 0x2D, 0x31, 0x32, 0x39, 0x3C
12	For all Analog Output Drivers, if Gain Smoothing is Disabled Ramp the Gain up One Volume Step per Write until the Desired Gain is Reached. If it is Enabled, Program the Desired Gain in a Single Step.	0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C

Table 90. Register Changes that Require $\overline{SHDN}$ = 0

DESCRIPTION	REGISTER
Clock Control and Quick Configuration Registers	0x04 to 0x0B, 0x1B to 0x26
DAC/ADC Enables (only these bits)	0x3E, 0x3F
Bias/DAC/ADC Control	0x42 to 0x44
Digital Signal Processing Enables and Coefficients	0x33 to 0x35, 0x41, 0x46 to 0xBD
Digital Microphone Configuration	0x13, 0x14

External Supply Sequencing

When powering-up the device, there is no requirement for the sequence with which each supply is applied. All supplies must be brought to their nominal voltage before the part can be configured for proper operation. The part should be placed into software shutdown before any supplies are removed to avoid audible artifacts. Register settings are retained as long as supply voltages are kept above the power-on-reset voltages listed in Table 91.

Table 91. Power-On Reset Voltage

SUPPLY	POR VOLTAGE
AVDD	1.0V
HPVDD	NO POR
DVDD	1.0V
DVDDIO	NO POR
SPKVDD	1.2V

Component Selection

AC-Coupling Capacitors

An input capacitor, C_{IN}, in conjunction with the input impedance of the device line inputs forms a highpass filter that removes the DC bias from an incoming analog signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming very low source impedance (comparatively), the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies. If needed, line output AC-coupling capacitor values can be calculated in similar fashion by using the input resistance of the next stage connected to the line output drivers.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the internal switches and the ESR of external charge pump capacitors dominate.

The holding capacitor (bypassing HPVSS) value and ESR directly affect the ripple at HPVSS. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* section for more information.

Filterless Class D Speaker Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x SPK_VDD peak to peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

For typical applications (such as handsets, tablets, etc.) where the trace length from driver the speaker is short and low impedance, the device does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the Class D output filter results in a smaller, less costly, and more efficient solution. In cases where the trace/wire length is long, and/or series resistance/inductance is high, an output LC filter might be required. In such a case, if the nominal impedance of the load is not constant over the entire audio band, a Zobel (impedance matching) circuit might be required.

Because the frequency of the IC's output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

EMI Considerations and Optional Ferrite Bead Filter

Reducing trace length minimizes radiated EMI. On the PCB, route SPKLP/SPKLN and SPKRP/SPKRN as differential pairs with the shortest trace lengths possible. This minimizes trace loop area, and thereby, the inductance of the circuit. If filter components are used on the speaker outputs, minimize the trace length from any ground tied passive components to SPK_GND to further minimize radiated EMI.

In applications where speaker leads/wires are long (exceeding approximately 12in), additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground (Figure 55). Use a ferrite bead with low DC resistance, high frequency (> 600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF with the value based upon optimizing EMI performance.

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers. The device is designed specifically to reject RF signals; however, PCB layout has a large impact on the susceptibility of the end product.

In RF applications, improvements to both layout and component selection decreases the susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the device. The wavelength (λ) in meters is given by: $\lambda = c/f$, where $c = 3 \times 10^8$ m/s, and f = the RF frequency of interest.

Route audio signals on inner layers of the PCB to allow ground planes above and below to shield them from RF interference. Ideally the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

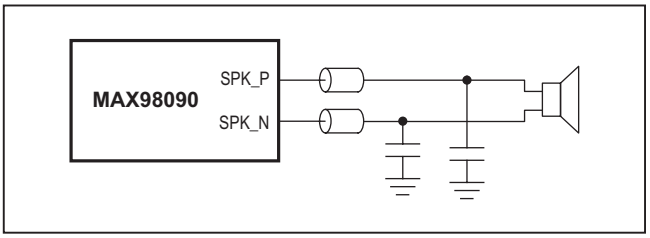


Figure 55. Optional Class D Ferrite Bead EMI Filter

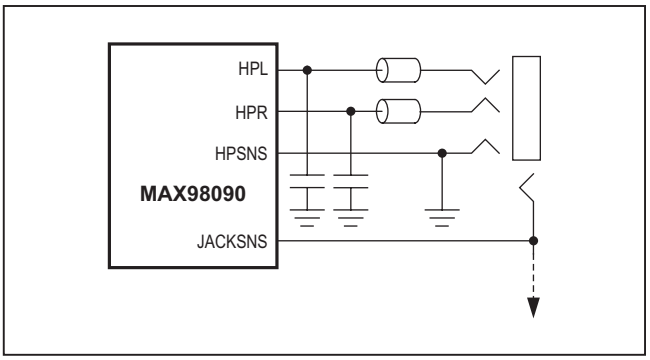


Figure 56. Optional Class H Output RFI Filter

Additional RF immunity can also be obtained by relying on the self-resonant frequency of capacitors, as it exhibits a frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self-resonance at RF (high) frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the device. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Avoid using micro vias to connect to the ground plane as these vias do not conduct well at RF frequencies. At the Headphone outputs, additional RFI can be achieved by using series ferrite beads with the parallel capacitors to ground (Figure 56).

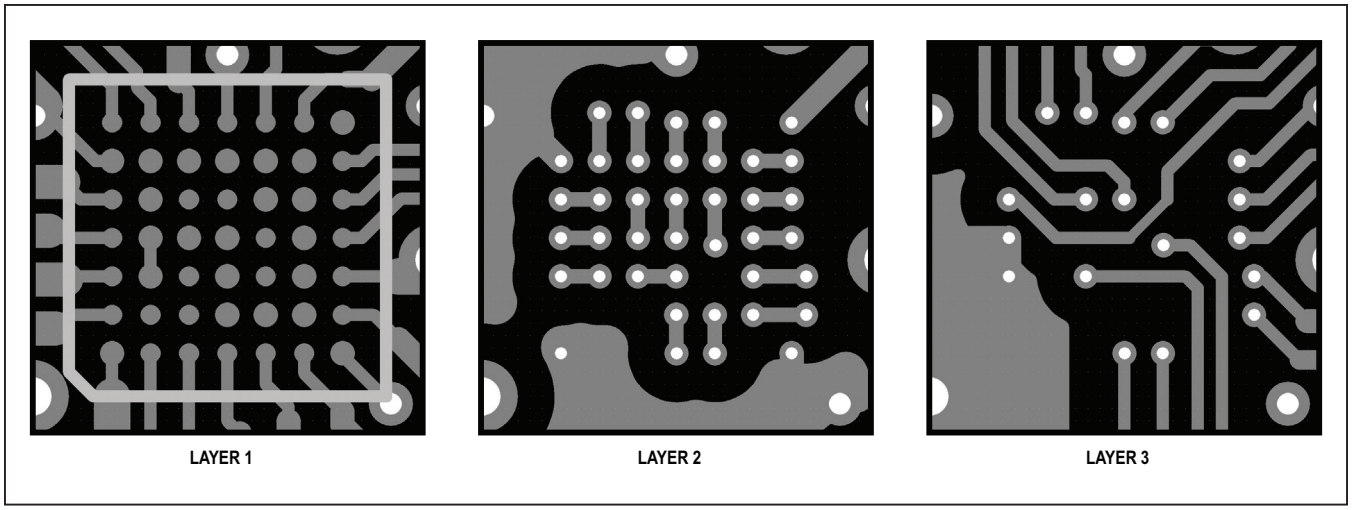


Figure 57. PCB Breakout Routing Example for WLP Package

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. When designing a PCB layout, partition the circuitry so that the analog sections of the device are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, and HPGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS, BIAS and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND, and bypass AVDD directly to AGND. Connect all digital I/O termination to the ground plane with minimum path length to DGND, and bypass DVDD and DVDDIO directly to DGND.

Place the capacitor between C1P and C1N as close as possible to the device to minimize trace length from C1P to C1N. Inductance and resistance added between C1P and C1N reduce the output power of the headphone amplifier. Bypass HPVDD, CPVDD and CPVSS with capacitors located close to the pin with short trace lengths to HPGND. Close decoupling of CPVDD and CPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

HPSNS senses ground noise on the headphone jack and adds the same noise to the output audio signal, thereby making the output (headphone output, ground) noise free. Connect HPSNS to the headphone jack shield to ensure accurate pickup of headphone ground noise.

Bypass SPK_VDD to SPK_GND with the shortest trace length possible and connect SPKLP, SPKLN, SPKRP, and SPKRN to the stereo speakers using the shortest traces possible. If filter components are used on the speaker outputs, be sure to locate them as close as possible to the device to ensure maximum effectiveness.

Route microphone signals from the microphone to the device as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, ground the negative microphone input as near to the audio source as possible and then treat the positive and negative traces as differential pairs.

An evaluation kit (EV Kit) is available to provide an example layout. The EV Kit allows quick setup of the device and includes easy-to-use software allowing all internal registers to be controlled.

Recommended PCB Routing

The IC uses a 49-bump WLP package. Figure 57 provides an example of how to connect to all active bumps using 3 layers of the PCB. To ensure uninterrupted ground returns, use layer 2 as a connecting or dog-bone layer between layer 1 and layer 3, and flood the remaining area with a copper ground plane.

Unused Pins

Table 92 shows how to connect the devices unused pins when circuit blocks are disabled. If the system is extremely noisy or there is a concern that unused analog inputs might be enabled, then alternatively unused analog audio inputs can be AC coupled to AGND (if component cost and area allow it).

Table 92. Unused Pin Connections

PIN NAME	CONNECTION	PIN NAME	CONNECTION
SUPPLY PLANES		**ANALOG AUDIO OUTPUTS**	
AVDD	Always connect	HPL	Unconnected
AGND	Always connect	HPR	Unconnected
HPVDD	Always connect	HPSNS	AGND
HPGND	Always connect	SPKLP	Unconnected
DVDD	Always connect	SPKLN	Unconnected
DVDDIO	Always connect	SPKRP	Unconnected
DGND	Always connect	SPKRN	Unconnected
SPKVDD	Always connect	RCVP / LOUTL	Unconnected
SPKLVDD	Always connect	RCVN / LOUTR	Unconnected
SPKRVDD	Always connect	**DIGITAL AUDIO INTERFACE**	
SPKLGND	Always connect	SDIN	DGND
SPKRGND	Always connect	SDOUT	Unconnected
CHARGE PUMP		MCLK	Always connect
CPVDD	Unconnected	LRCLK	DGND
CPVSS	Unconnected	BCLK	DGND
C1P	Unconnected	**I²C INTERFACE**	
C1N	Unconnected	SCL	Always connect
ANALOG AUDIO INPUTS		SDA	Always connect
IN1/DMD	Unconnected	$\overline{IRQ}$	Unconnected
IN2/DMC	Unconnected	**OTHER**	
IN3	Unconnected	MICBIAS	Unconnected
IN4	Unconnected	JACKSNS	Unconnected
IN5	Unconnected	BIAS	Always connect
IN6	Unconnected	REF	Always connect

Ordering Information

PART	ADDRESS	TEMP RANGE	PIN-PACKAGE
MAX98090AEWJ+T	0x20	-40°C to +85°C	49 WLP
MAX98090AETL+T	0x20	-40°C to +85°C	40 TQFN
MAX98090BEWJ+T	0x22	-40°C to +85°C	49 WLP
MAX98090BETL+T	0x22	-40°C to +85°C	40 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
49 WLP	W493B3+2	**21-0443**	Refer to **Application Note 1891**
40 TQFN	T4055+1	**21-0140**	**90-0121**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	—
1	8/13	Corrected various errors	1, 9, 11, 15–17, 20–26, 30, 37–48, 50–54, 56–63, 66–68, 72, 78, 79, 82, 84–88, 91, 92, 94–96, 98, 103–105, 110, 113, 120, 121, 129, 141, 142, 146, 149, 150, 151, 158–162, 164
2	8/14	Corrected various errors and made various updates	10, 11, 15, 16, 28, 38–66, 70, 89–92, 100, 111–113, 118, 124, 146, 147, 149, 151, 152, 165, 168

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