External Memory Interfaces Intel Agilex® 7 M-Series FPGA IP Core Release Notes

Updated for Intel® Quartus® Prime Design Suite: **23.2**

IP Version: **4.0.0**

Online Version
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1. External Memory Interfaces Intel Agilex® 7 M-Series FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- External Memory Interfaces Intel Agilex 7 M-Series FPGA IP User Guide
- External Memory Interfaces Intel Agilex 7 M-Series FPGA IP Design Example User Guide

1.1. External Memory Interfaces Intel Agilex® 7 M-Series FPGA IP v4.0.0

Table 1. v4.0.0 2023.06.26

Description	Impact
Verified in the Intel Quartus Prime software v23.2.	Provides external memory interface IP for DDR4, DDR5, and LPDDR5 external memory for Intel Agilex® 7 M-Series devices. The tables that follow summarize speed and feature support.

Note: This documentation is preliminary and subject to change.

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Table 2. Intel Agilex 7 M-Series Fabric EMIF IP Speed Support Summary

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	**Category**	**Subcategory**	**-1**	**-2**	**-3**	**Support Detail**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**
DDR4	Memory Format	Component	3200/1600 (1R)	3200/1600 (1R)	2666/1333 (1R)						X [1]	X	X [3]		X [1]	X	X [3]	
			2666/1333 (2R)	2666/1333 (2R)	2400/1200 (2R)						X [1]	X	X [3]		X [1]	X	X [3]	
DDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		UDIMM	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		SODIMM	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		RDIMM	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
LPDDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

continued...

Protocol	Category	Subcategory	Max Rate (Mbps/MHz)				Support Detail	-1				-2				-3			
			-1	-2	-3			S	C	T	H	S	C	T	H	S	C	T	H

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.
- **1** = Supports VCS and QuestaSim.
- **2** = Current performance in the Intel Quartus Prime software. Check the External Memory Interface Spec Estimator for production performance.
- **3** = Timing is currently preliminary. It will be necessary to recompile designs in future releases.

Note: Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

Table 3. Intel Agilex 7 M-Series Fabric EMIF IP Feature Support Summary

Protocol	Category	Sub-Category	Supported?	S	C	T	H
DDR4	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM					
		RDIMM					
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi-rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF Toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
DDR5	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM	X	X	X	X	
		RDIMM	X	X	X	X	

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
LPDDR5	Interface Width	32	X	X	X	X	
		16	X	X	X	X	
	Controller	Hard controller	X	X	X	X	
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

- X = supported feature.
- [1] = VHDL is not supported.

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Table 4. Intel Agilex 7 M-Series HPS EMIF IP Speed Support Summary

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	**Category**	**Subcategory**	**-1**	**-2**	**-3**	**Support Detail**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**
DDR4	Memory Format	Component	3200/1600 (1R)	3200/1600 (1R)	2666/1333 (1R)						X [1]	X	X [3]		X [1]	X	X [3]	
			2666/1333 (2R)	2666/1333 (2R)	2400/1200 (2R)						X [1]	X	X [3]		X [1]	X	X [3]	
DDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		UDIMM																
		SODIMM																
		RDIMM																
LPDDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	

Support level key:

- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.
- [1] = Supports VCS and QuestaSim.
- [2] = Current performance in the Intel Quartus Prime software. Check the External Memory Interface Spec Estimator for production performance.
- [3] = Timing is currently preliminary. It will be necessary to recompile designs in future releases.

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Table 5. Intel Agilex 7 M-Series HPS EMIF IP Feature Support Summary

Protocol	Category	Sub-Category	Supported?	S	C	T	H
DDR4	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM					
		RDIMM					
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi-rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode					
		Fabric async mode					
		NoC	X	X	X	X	
	Debug	EMIF Toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
DDR5	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM					
		RDIMM					

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode					
		Fabric async mode					
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
LPDDR5	Interface Width	32	X	X	X	X	
		16	X	X	X	X	
	Controller	Hard controller	X	X	X	X	
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	AXI access mode	Fabric sync mode					
		Fabric async mode					
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					

Support level key:
- S = simulation support
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- H = hardware support

- X = supported feature.
- [1] = VHDL is not supported.

1.2. External Memory Interfaces Intel Agilex 7 M-Series FPGA IP v3.0.0

Table 6. v3.0.0 2023.04.03

Description	Impact
Verified in the Intel Quartus Prime software v23.1.	Provides external memory interface IP for DDR4, DDR5, and LPDDR5 external memory for Intel Agilex 7 M-Series devices. The tables that follow summarize speed and feature support.

Note: This documentation is preliminary and subject to change.

Notice: Device support for Intel Agilex 7 M-series FPGAs and SoCs in the Intel Quartus Prime Pro Edition software version 23.1 is restricted. To enable M-series device support in your instance of the Intel Quartus Prime Pro Edition software, contact your regional Intel FPGA sales representative.

Table 7. Intel Agilex 7 M-Series Fabric EMIF IP Speed Support Summary

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	**Category**	**Subcategory**	**-1**	**-2**	**-3**	**Support Detail**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**
DDR4	Memory Format	Component	3200/1600 (1R)	3200/1600 (1R)	2666/1333 (1R)						X [1]	X	X [3]		X [1]	X	X [3]	
			2666/1333 (2R)	2666/1333 (2R)	2400/1200 (2R)						X [1]	X	X [3]		X [1]	X	X [3]	
DDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		UDIMM	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
		SODIMM	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]	3200/1600 (1DPC 1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]	3200/1600 (1DPC 2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
LPDDR5	Memory Format	Component	3200/1600 (1R) [2]	3200/1600 (1R) [2]	3200/1600 (1R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	
			3200/1600 (2R) [2]	3200/1600 (2R) [2]	3200/1600 (2R) [2]						X [1]	X	X [3]		X [1]	X	X [3]	

Support level key:

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- C = compilation support
- T = timing support
- H = hardware support

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.
- [1] = Supports VCS and QuestaSim.
- [2] = Current performance in the Intel Quartus Prime software. Check the External Memory Interface Spec Estimator for production performance.
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Table 8. Intel Agilex 7 M-Series Fabric EMIF IP Feature Support Summary

Protocol	Category	Sub-Category	Supported?	S	C	T	H
DDR4	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM					
		RDIMM					
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi-rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF Toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
DDR5	Interface Width	16, 16+ECC, 32, 32+ECC	X	X	X	X	
		SODIMM, UDIMM	X	X	X	X	
		RDIMM					

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	Controller	Hard controller	X	X	X	X	
	3DS	3DS					
	Design Example		X	X	X	X	
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					
LPDDR5	Interface Width	32	X	X	X	X	
		16	X	X	X	X	
	Controller	Hard controller	X	X	X	X	
	Design Example		X	X	X	X	
	DBI	Read DBI					
		Write DBI	X	X	X	X	
	Mirroring	Address mirroring for odd ranks for multi rank DIMMs					
	DM	DM pins	X	X	X	X	
	Preamble	Read preamble settings					
		Write preamble settings					

continued...

Protocol	Category	Sub-Category	Supported?	S	C	T	H
	AXI access mode	Fabric sync mode	X	X	X	X	
		Fabric async mode	X	X	X	X	
		NoC	X	X	X	X	
	Debug	EMIF toolkit					
	Simulation	Abstract PHY					
	Simulators [1]	VCS	X	X			
		VCS-MX	X	X			
		ModelSim SE	X	X			
		Xcellium					
		Aldec					

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- S = simulation support
- C = compilation support
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- H = hardware support

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