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APPLICATION BULLETIN
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USING THE ADS1201 EVALUATION BOARD

By Saeid Jannesari

FEATURES

- **EASY INSTALLATION AND USE**
- **ON BOARD *SINC*³ DIGITAL FILTER WITH PROGRAMMABLE MODULATOR CLOCK AND DECIMATION RATIO**
- **RETRIEVES FILTER OUTPUT DATA INTO PC FOR ANALYSIS AND DISPLAY**
- **PERFORMS FOURIER TRANSFORMS ON COLLECTED DATA**
- **DISPLAYS DATA IN BOTH FREQUENCY AND TIME DOMAIN**
- **USER-FRIENDLY VISUAL BASIC™ GRAPHICAL INTERFACE**

This application bulletin provides information on the operation and usage of the ADS1201U evaluation fixture and provides detailed description of the digital filter design implemented into Xilinx XC4010E Field Programmable Gate Array (FPGA). The latest information, along with the FPGA files can be found on the Burr-Brown web site. The ADS1201U evaluation board communicates to a PC via a bi-directional parallel port. It is capable of collecting up to 8192 data words at a maximum data rate of 1000Hz. The user interface software is written in Visual Basic and controls the filter configuration and data retrieval, as well as graphical display and analysis. Data can be displayed in time and frequency domain. Optionally, retrieved data can be saved to a file for transport to other graphical and mathematical software applications. In addition, a hard copy of the displayed graphics in time or frequency domain can be obtained. In this bulletin, a complete description of the hardware and software features of the ADS1201U evaluation kit will be given.

ADS1201U

Since the information in this bulletin concerns the ADS1201U, the following is a brief description of the part. ADS1201U is a single channel precision, wide dynamic range, second-order Delta-Sigma (ΔΣ) modulator operating from a single +5V supply (see Figure 1 for device pinout). The ΔΣ modulator converts an analog signal into a 1-bit digital data stream of ones and zeros. The ones density of the output data stream is proportional to the input analog signal. Oversampling and noise shaping are used to reduce the quantization noise in the frequency band of interest. A ΔΣ modulator can be used with a digital filter for wide dynamic range A/D conversion of 24 bits of resolution or better. Filtering the noise is the primary purpose of the digital filter. Its secondary purpose is to convert the 1-bit data stream at high sample rate into a higher bit data stream at lower rate (decimation). The output data from the ADS1201U modulator is read via the MOUT pin. The modulator outputs data at the rising edge of MCLK with a short time delay, t_d. It is recommended to synchronize the reading of the output data with the falling edge of MCLK (Figure 2). The collected output of the modulator is then passed through a digital low-pass filter and the resulting output word is decimated and truncated to the desired data rate and effective resolution, respectively. The combination of the ΔΣ modulator and the digital decimation filter forms a ΔΣ A/D converter. For more detailed information and specifications concerning the ADS1201U modulator, refer to the ADS1201 data sheet.

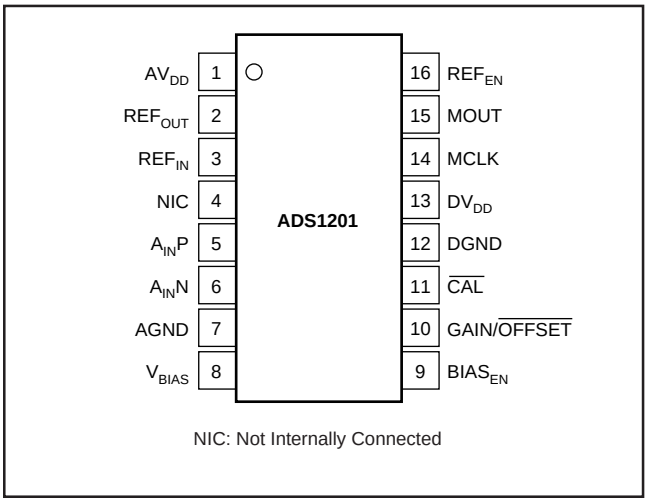

FIGURE 1. ADS1201U Device Pinout.

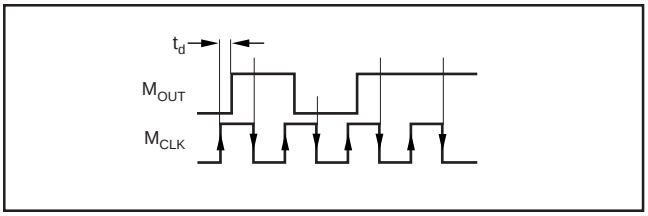

FIGURE 2. ADS1201U Output Read Operation.

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INSTALLATION

The ADS1201U evaluation kit contains the following items:

- A completely assembled and tested ADS1201U Evaluation Board
- 25-pin ribbon cable with connectors (PC Parallel Port Interface Cable)
- A 3 1/2" setup diskette containing all software components needed to install and run the ADS1201U demonstration software
- ADS1201U Application Bulletin
- ADS1201U Product Data Sheet

The following system requirements are needed in order to install and run the ADS1201U evaluation software:

- IBM-compatible PC with a 486/66MHz processor or better, Super VGA graphics, bi-directional parallel port and Microsoft Windows 3.1 or higher operating system
- Triple DC power supply (+5V, ±15V)
- A clean signal source

To install the ADS1201U demonstration board, first verify that the power supply is set to +5V and ±15V DC. Make sure that the ADS1201 modulator is properly inserted in the socket with correct orientation (see component layout in Figure 18). Connect the power cables to the board and turn the power on. The LED close to the Xilinx FPGA should turn on for a short period and then go off. This will indicate that the Xilinx is configured properly. Next, connect the 25-pin ribbon cable between the board and the PC parallel port. Connect the input signal via a coaxial cable to the BNC connector on the board marked as J1. Make sure that the input signal does not exceed the maximum input range of the ADS1201 modulator.

The ADS1201 evaluation software is written in Visual Basic. To install the ADS1201 evaluation software, insert the 3 1/2" diskette supplied with the demo kit into the PC floppy drive A and run the SETUP.EXE program from drive A. This will automatically install all the necessary software components in appropriate locations on drive C. It also creates a directory on drive C called "ADS1201demo" and installs the ADS1201DEMO.EXE in that directory. The user can create a shortcut to this program, or run the program directly from this directory.

HARDWARE DESCRIPTION

Figure 15 shows the schematic of the evaluation board. Figure 16 and 17 shows the digital filter and control circuitry inside the Xilinx FPGA. The modulator clock and decimation ratio can be programmed by setting appropriate registers inside the FPGA. The 4MHz master oscillator is divided down by the value in the configuration register to produce modulator clock (MCLK). The ADS1201U evaluation board is made up of the following five sections:

1) Xilinx XC4010E FPGA containing the digital filter, PC interface and control circuitry
2) Analog input buffers
3) Input reference voltage source
4) An easy-to-use socket for ADS1201U evaluation
5) Power supply circuits

The main purpose of the analog input buffer is to convert a single-ended signal into a differential signal with common-mode voltage fixed at 2.5V. Jumpers JMP1 through JMP4 will allow the users to either use the on-board input buffer or to connect an external signal directly to the input of ADS1201U. Optionally, the users can design their own analog input buffer in the analog breadboard area of the board. Figure 3 shows the schematic of the analog input buffer.

An on-board 2.5V reference voltage source is provided that can be connected to the ADS1201U REF_{IN} pin via JMP6. Optionally, the ADS1201U can be operated from the internal reference voltage. To use the ADS1201U internal reference voltage, set jumper JMP8 to +5V and install JMP5.

The ADS1201U socket has been selected specially to allow for easy insertion and removal of the parts under evaluation. A low profile socket can also be used to minimize the noise pickup at the inputs. **No power should be applied to the DUT board while inserting new parts for evaluation.**

DIGITAL FILTER DESIGN

The digital filter structure chosen to decode the output of the ΔΣ modulator is a *SINC*^{3} digital filter. The function of the *SINC*^{3} digital filter is to output after each *N* input samples a word which represents a weighted average of the last *3(N-1)+1* input samples. This filter can be implemented in software using straight linear convolution as:

$$y(k) = \sum_{n=0}^{3N-1} h(n)x(n-k) \tag{1}$$

where, *x(i)* denotes the input data stream made up of ones and zeros, *h(n)* are the filter coefficients, *y(k)* represents the decimated output data words and *N* is the decimation ratio. The coefficients of the digital filter, *h(n)*, are calculated based on the desired decimation ratio as follows:

$$h(n) = \frac{n(n+1)}{2} \quad 1 \le n \le N \tag{2}$$

$$h(n) = \frac{N(N+1)}{2} + (n+N)(2N-1-n) \quad N \le n \le 2N \tag{3}$$

$$h(n) = \frac{(3N-n-1)(3N-n)}{2} \quad 2N \le n \le 3N \tag{4}$$

The transfer function of a *SINC*^{3} digital filter can be expressed as:

$$H(Z) = \left(\frac{1}{N}\sum_{i=0}^{N-1} Z^{-i}\right)^3 = \left(\frac{1}{N}\frac{1-Z^{-N}}{1-Z^{-1}}\right)^3 \tag{5}$$

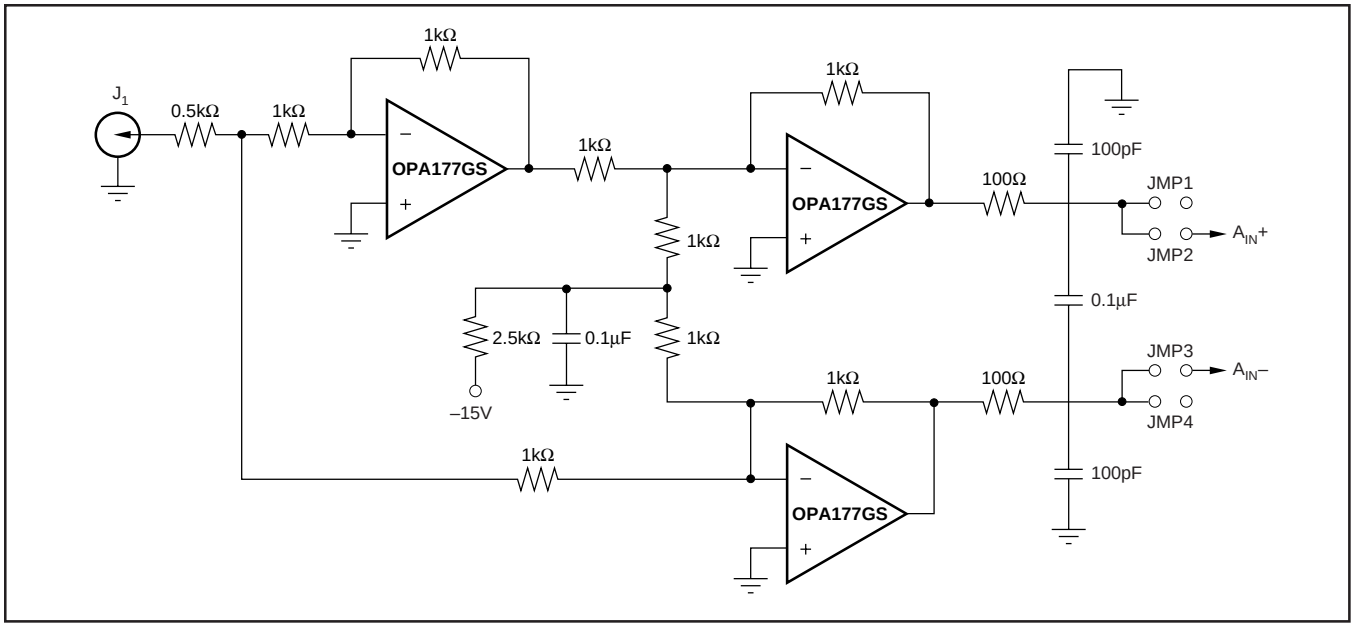

FIGURE 3. Analog Input Buffers.

Substituting Z by $e^{-j\omega T}$, the frequency response obtained is as follows:

$$H(j\omega) = \left(\frac{\sin(N\omega T)}{N \sin(\omega T)} \right)^3 \quad (6)$$

Where N is the decimation ratio. It is easy to see from the above frequency response that the location of the first notch occurs at f_S/N, where f_S is the sampling frequency (MCLK) and N is the decimation ratio. At the most basic level, the digital filter simply performs a moving average of the modulator output. Figure 4 shows the normalized frequency response of the digital filter.

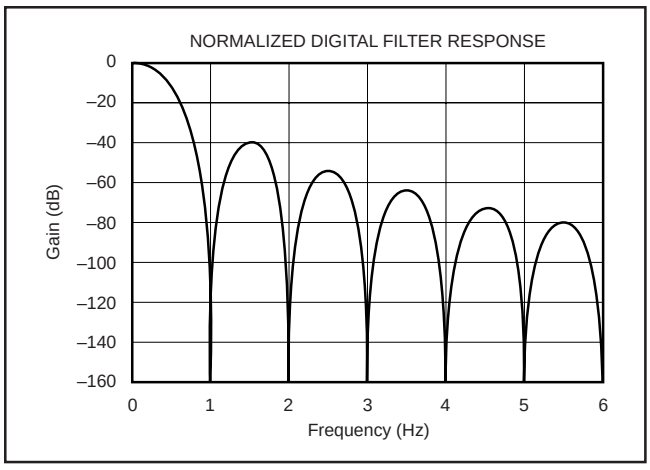

FIGURE 4. Normalized Digital Filter Response.

The relationship betwen modulator clock (f_S), output data rate and decimation ratio (N) is given by:

$$\text{Data rate} = \frac{f_S}{N} \quad (7)$$

therefore, data rate can be used to place a specific notch frequency in the digital filter response. For a *SINC*^{3} filter response, the –3dB point is 0.262 times the data rate.

FILTER IMPLEMENTATION

For small decimation ratios and low clock rates, the linear convolution of *x(n)* and *h(n)* in Equation 1 can be efficiently implemented in software using the FFT algorithm. To do this, one can make use of a property of DFT transform which says convolution in time domain is identical to multiplication in frequency domain:

$$y(n) = h(n) \bullet x(n) \Leftrightarrow Y(k) = H(k)X(k) \quad (8)$$

therefore, the DFTs of *x(n)* and *h(n)* are multiplied point by point and the inverse DFT of the result is the desired linear convolution. To make this technique work with the FFT algorithm, one must make sure that the two sequences *x(n)* and *h(n)* have the same length and are powers of 2. For large decimation ratios and high output data rates, a hardware implementation of the *SINC*^{3} filter is more efficient. The filter transfer function in Equation 5 can be implemented using a series cascade of three integrators and three differentiators as shown in Figure 5. The three integrators

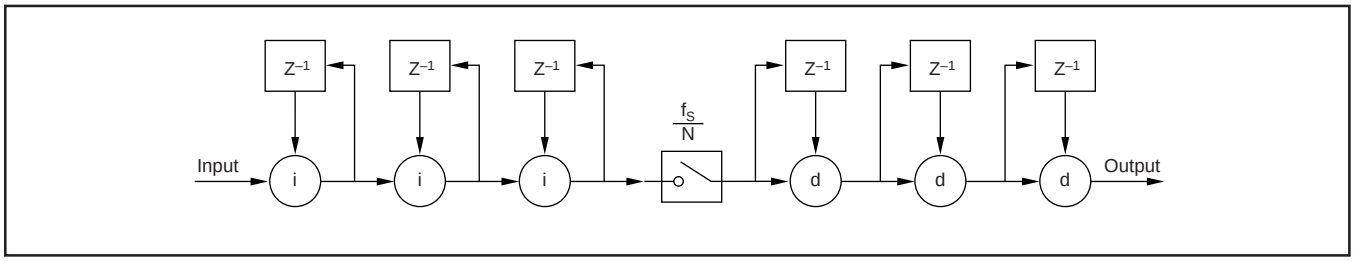

FIGURE 5. SINC^3 Digital Filter Topology.

operate at the high modulator clock frequency f_S. The output from the third integrator is decimated down by N and fed to the input of the first differentiator. The three differentiators operate at the low clock frequency of f_S/N, where N is the decimation ratio. Figures 16 and 17 shows the detailed schematic of the $SINC^3$ digital filter, as implemented in Xilinx FPGA. The 40-bit filter output is latched onto the output data register where it can be transferred into the PC via the parallel port one byte at a time. Calibration and scaling is performed in software once the raw data is loaded into the PC memory.

Figure 6 shows the implementation of a single integrator in Xilinx FPGA. The 40-bit wide incoming data is continuously added to the previously accumulated result.

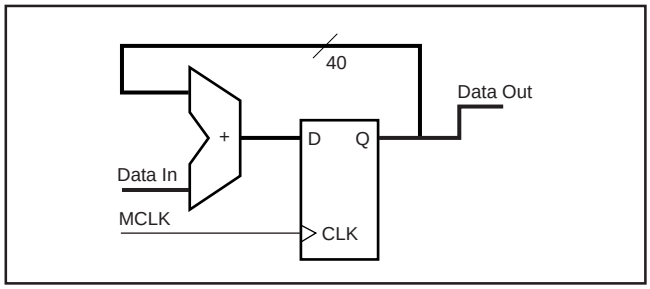

FIGURE 6. Xilinx Integrator Implementation.

Figure 7 shows the implementation of a single differentiator. The 40-bit wide incoming data is latched onto the D flip-flop array while being subtracted from the previously latched result.

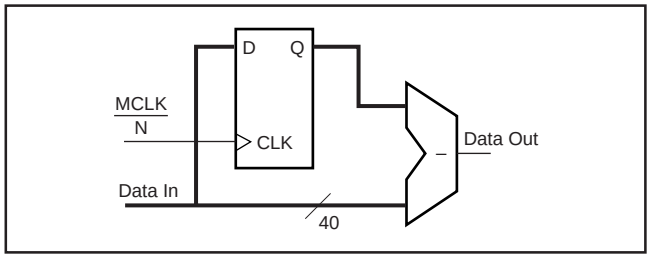

FIGURE 7. Xilinx Differentiator Implementation.

The 8-bit configuration register inside the FPGA is used to program the modulator clock frequency (MCLK), which runs the filter as well as the modulator. Decimation ratio can be programmed by setting the appropriate bits of the two 8-bit decimation registers designated as “dr_low” and “dr_hi” in Figure 16. The ADS1201U evaluation software allows the user to simply select from eight possible clock frequencies and type in the desired decimation ratio. After this, the output data rate is calculated and the appropriate values are programmed into the configuration and decimation registers inside the FPGA. The eight allowable modulator frequencies are: 1M, 512, 256, 128, 64, 32, and 16kHz. The maximum decimation ratio allowed is 8192. The minimum decimation ratio is dependent on the selection of the modulator clock frequency and is limited so the output data rate never exceeds 1000Hz.

ADS1201 GAIN/OFFSET CALIBRATION

In an ideal ADC transfer function, if one connects the midpoints of each quantization code with a straight line, the line will pass through the origin with a 45° angle. Any deviation from this ideal condition indicates the existence of some type of error. If the line does not pass through the origin, the converter has an offset error.

If the line is at a slope other than 45°, the converter has a gain error. In addition to offset and gain errors, a typical A/D converter will also have a complex nonlinearity profile. In the ADS1201U, two pins are dedicated to control offset and gain calibration, $\overline{CAL}_{ENB}$ and GAIN/$\overline{OFFSET}$. The user normally performs offset and gain calibration after each filter configuration. For offset calibration, pins $\overline{CAL}_{ENB}$ and GAIN/$\overline{OFFSET}$ are set to LOW and HIGH, respectively. As a result, internal switches S_1 and S_2 are disconnected from the device inputs (A_{IN}+, A_{IN}–), and S_3 and S_4 are connected to reference voltage, V_{REF} (Figure 8). With these conditions, the output of the modulator is passed through the digital filter. The filter output word is saved as the offset error. For gain calibration, the internal switches, S_5 and S_6, connect the inputs to V_{REF} and ground, respectively. Under these conditions, the output of the filter is saved as the gain error. The output values obtained from offset and gain calibration are used to calculate a gain calibration coefficient *gc* as follows:

$$g_C = \frac{V_{REF}}{(\text{gain error} - \text{offset error})} \quad (9)$$

V_{REF} = 2.5V

offset error = data when inputs are shorted

gain error = data when inputs are at V_{REF} and ground

The normalized filter output is then calibrated as:

calibrated_output = (output – offset error) • gc

where, *output* refers to uncalibrated output.

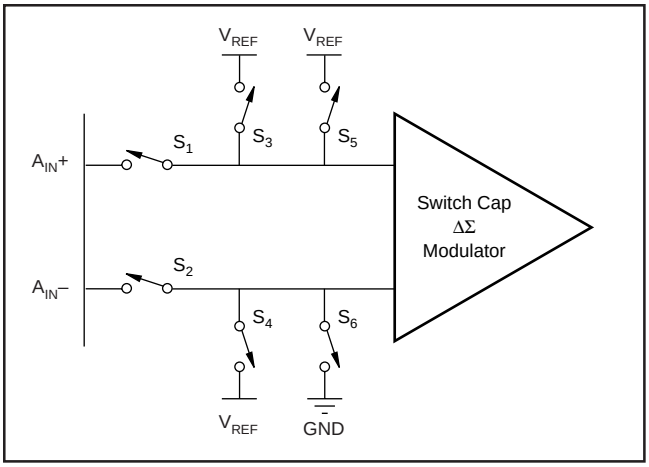

FIGURE 8. ADS1201U Internal Connections for Gain/Offset Calibration.

CIRCUIT LAYOUT CONSIDERATIONS

Good circuit design and board layout is very important in any test fixture. This becomes even more important when designing with mixed-signal components such as data converters. For the ADS1201U evaluation board, it was necessary to have separate ground planes for analog and digital components. Since ADS1201U analog pins are located on one side (Figure 1, pins 1-8) and all digital pins are located on the other side (pins 9-16), it was easily possible to separate the analog and digital ground planes on the demonstration board, (shown in Figure 19) with analog pins on the analog ground plane area and digital pins on the digital ground plane area. Every attempt was made to place and route the analog input buffers and reference circuits on the analog circuit area as close to the DUT pins as possible. The Xilinx FPGA and all digital support logic circuits were placed on the digital side of the board. The two partitioned ground planes were connected together at one point close to the power supply filters. The following layout guidelines were used in designing the ADS1201U evaluation board:

- Use separate power supplies for analog and digital power lines. Place the power supply bypass capacitors as close to the device pins as possible and place the smallest capacitors closest to IC power supply pins.
- Separate the analog and digital ground planes. Keep the same partition for all layers. Analog and digital ground planes will eventually be connected at one point (in most cases, this is a point close to the board power source).
- Mixed-signal components such as data converters should bridge the ground partition with analog and digital pins over their respective ground planes.
- Make sure that the regions between signal traces are filled with copper that is attached to the ground plane. This is specially important to reduce crosstalk and coupling between adjacent signal lines.
- Place and route all analog and digital circuit components and signal traces over their respective ground planes. This includes analog and digital power line traces, regulators, and filters.
- Place any analog input buffers and filters as close to the input pins of the DUT as possible and keep all noisy lines and high frequency signals, such as clock, away from the inputs of the device under test, as well as input reference pins.
- Use surface-mount components if possible.

SOFTWARE FEATURES

The ADS1201U demonstration software is written in Visual Basic and is designed to allow evaluation of the part using a PC. It is both mouse and keyboard compatible. The pull-down menus and different control buttons can be selected by a mouse click or typing the highlighted letters while holding down the TAB key. For example, to access the filter configuration window, the user can click on the Configure menu item with a mouse or by typing the letter C while holding the TAB key down. The main window contains a graph for displaying data. The graph automatically scales the vertical axis based on the input data. The user can also select manual scaling of the vertical axis by typing appropriate values in the Max and Min boxes.

MAIN WINDOW

When the ADS1201U evaluation program is executed, the main window appears on the screen as shown in Figure 11. The pull-down menus in the main window are, File, Configuration, Debug and Help. The File menu allows the user to copy the previously collected data to a file, print a hard copy of the graph, display the data and or exit the program. The Configuration menu allows the user to perform two functions. The first is to access the filter configuration window and the second is to select various windowing functions for the FFT analysis. The Debug menu allows access to the debug window and the DC voltmeter window. Finally, the Help menu gives some information about the software and version. The command button designated as Capture on the main window is used to capture data after the filter is configured. The text box in front of the Capture button displays the number of data points to capture. The user can type in a new number or use the up/down arrows to change this value.

Below the Capture button is the Display Data List button. Pressing this button will display the previously collected data on the screen. The mean and standard deviation is also calculated and displayed. The display options are Normalized, Voltage, and Continuous. If Normalized is selected, the displayed data is a number between zero and one, which represents the modulator output density of ones. If Voltage is selected, each output is calibrated and scaled to represent the differential voltage at the modulator inputs. Selecting Continuous will continuously capture and display data.

The FFT options are FFT Plot and Time Plot. The default is Time Plot. By selecting FFT option, the fourier transform of the collected data is displayed on the graph. This mode works only if the number of captured data is a power of 2. A continuous display of time or frequency plot is possible by selecting Continuous from the display options and selecting either Time or FFT Plot from the FFT options. The speed by which data is collected and displayed has to do with the selected output data rate.

The Calibration options are: Offset_Cal, Gain_Cal and Normal. Usually, after each filter configuration, the user should perform an offset and then a gain calibration. The default values for offset and gain calibrations are zero and one, which means no offset or gain calibration. Selecting the Offset_Cal and capturing new data will cause an offset calibration to be performed, as described in the Calibration section. Selecting the Gain_Cal and capturing new data will perform a gain calibration on the device. The values of the

resulting offset and gain calibrations are then displayed in the adjacent text boxes. After performing the offset and gain calibrations, the user will select Normal mode. From this point on, every new data that is captured is calibrated using these offset and gain calibration values.

The information regarding the previously selected modulator clock frequency, decimation ratio, output data rate and FFT window function is displayed in the lower right hand corner of the main window.

CONFIGURATION WINDOW

Usually, the first thing that the user does after running the program is to access the filter configuration window. In this window (see Figure 12), the user can select from one of eight different modulator clock frequencies (MCLK) and type in a decimation ratio. Decimation ratio can also be entered by scrolling the horizontal scroll bar. The output data rate is automatically calculated and displayed in a text box. When the OK button is pressed, the configuration registers inside the FPGA are programmed for the selected MCLK and decimation ratio. After configuring the digital filter, the user can activate the main window and perform offset and gain calibration or capture new data. The information regarding the previously selected modulator clock frequency, decimation ratio and output data rate is displayed continuously in the main window at the lower right hand corner.

DEBUG WINDOW

In the Debug window, the user can read and write to the filter configuration registers, read from the output data register, and set/change the parallel port base address (see Figure 13).

DC VOLTMETER WINDOW

In this window, the output of the filter is continuously scaled and displayed as voltage on a DVM-like display. In addition, a measurement history of up to 1000 points are kept (see Figure 14). The measurement interval and the number of averages for each measurement can be changed by the user. This will allow the user to collect from several minutes up to several hours of measurement history. In this window, an EKG-type display is provided to keep a graphical history of the measurement data. The graph moves from right to left as new data comes in. The horizontal scrollbar allows the user to review the previously collected data while new measurements are being made. This window also has a pull-down menu that allows the user to copy the measurement data to a file, display data on the screen, or quit the window.

DATA COLLECTION AND DISPLAY

Normally, after the filter configuration is done, the user should perform offset and gain calibration before collecting new data. Offset calibration must be done first. To do this, in the main window, click on the Offset_Cal radio button and press the Capture button. After this is done, the value of the offset calibration is displayed in a text box in front of the Offset_Cal radio button. Next, to perform gain calibration, click on the Gain_Cal radio button and press the capture button. After calibration is finished, the value of the gain calibration coefficient is calculated and displayed in a text box in front of the Gain_Cal radio button. From this point on, the user can collect new data by clicking on the Normal_Mode radio button, selecting the number of data points to be collected and pressing the Capture button. The collected data is automatically adjusted to account for the offset and gain calibration coefficients. The graph is set to auto scale by default, which displays an optimum fit of data on the graph. The user can optionally change the maximum and minimum vertical scale values manually. The user can also zoom in on a portion of the graph by holding down the left mouse button and dragging on the rectangular area to be zoomed. After zooming is performed, a horizontal scroll bar appears that allows the user to pan left and right on the graph. To unzoom, click the right mouse button and select Undo Zoom from the popup menu. There are many more features associated with the graph. The user can explore these features by moving the mouse cursor onto the graph area and clicking the right mouse button. A popup menu appears from which different selections can be made.

After collecting new data, the user can click on the FFT radio button to display the FFT of the data just collected. For the FFT to work, the number of data collected must be a power of two. An example of time and frequency plot is shown in Figures 9 and 10, respectively.

A list of collected data can be displayed by clicking the Display Data List button or by selecting the Display Data option from the File menu. Either way, the data is displayed in a list box. The user can scroll up and down through the data. The form containing the list box can be resized to display more of the data on the screen at one time. The average and standard deviation of collected data is calculated and displayed on top of this form.

Collected data can be copied to a file for future analysis and display using other mathematical and graphical applications. To copy data to a file, select the Copy option from the File menu and enter the desired file name and path. Data is saved as ASCII format.

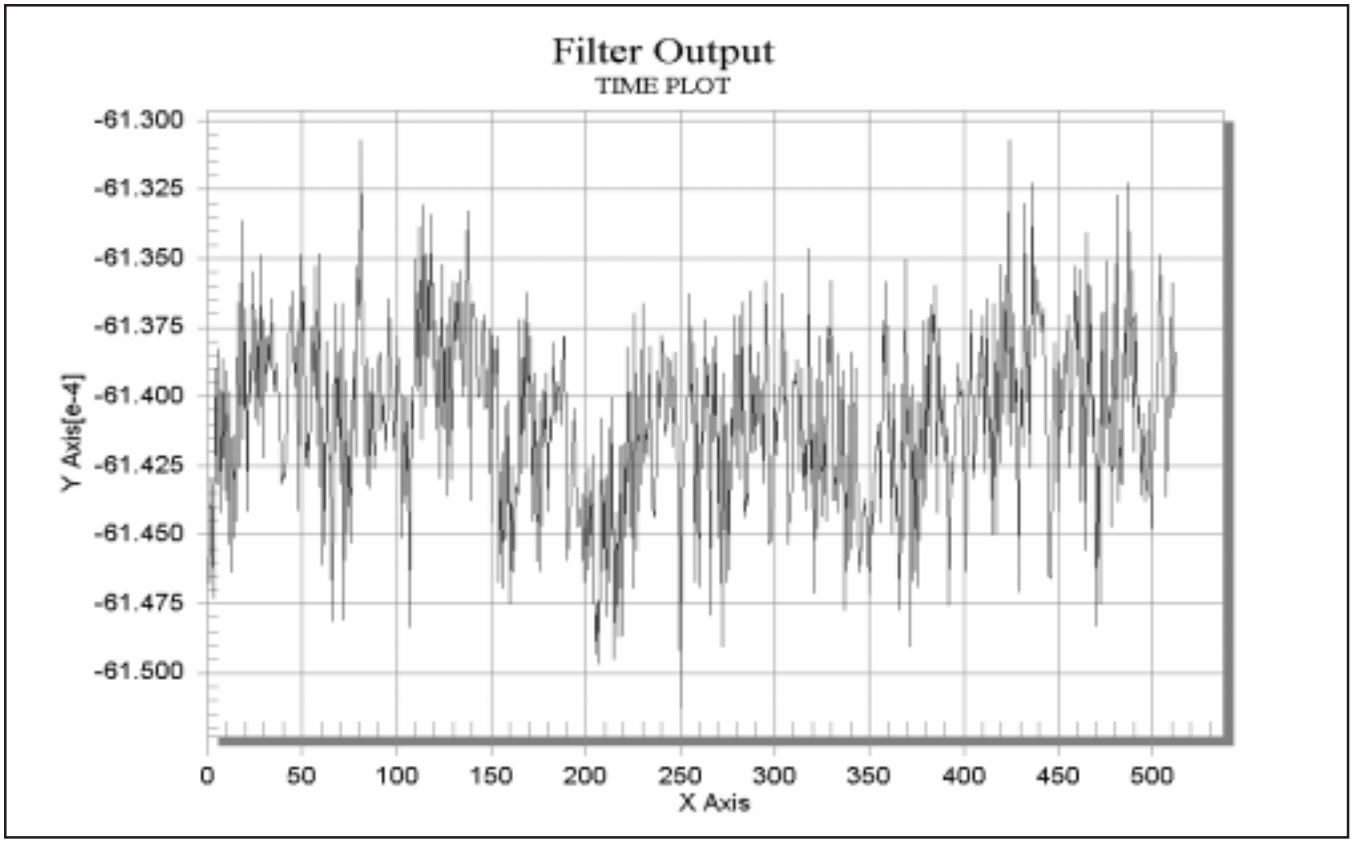

FIGURE 9. Time Domain Plot. X-Axis Represents Sample Number, Y-Axis is Voltage.

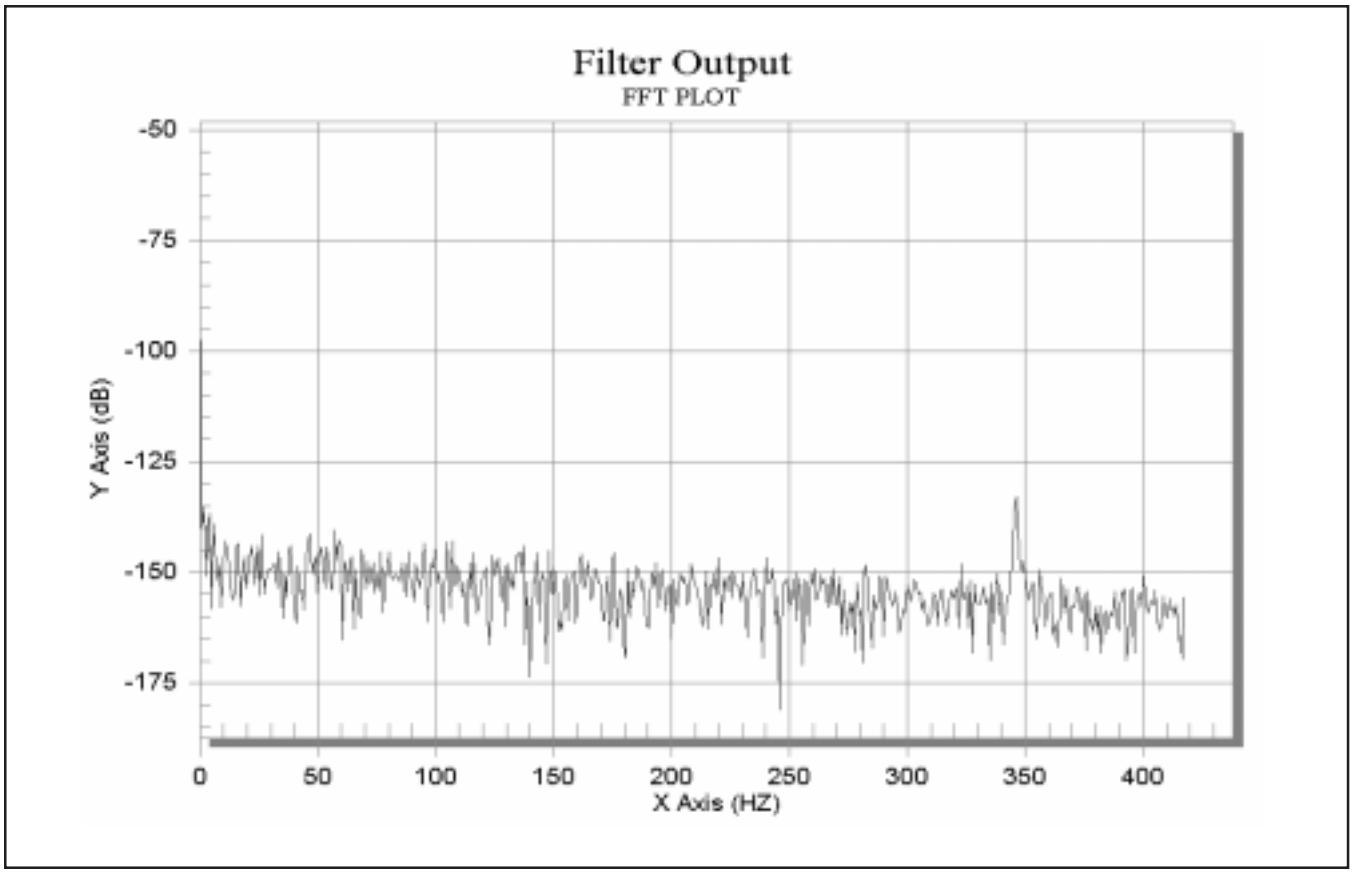

FIGURE 10. FFT Plot of Data Shown in Figure 9. X-Axis Represents Frequency in Hz, Y-Axis is dB.

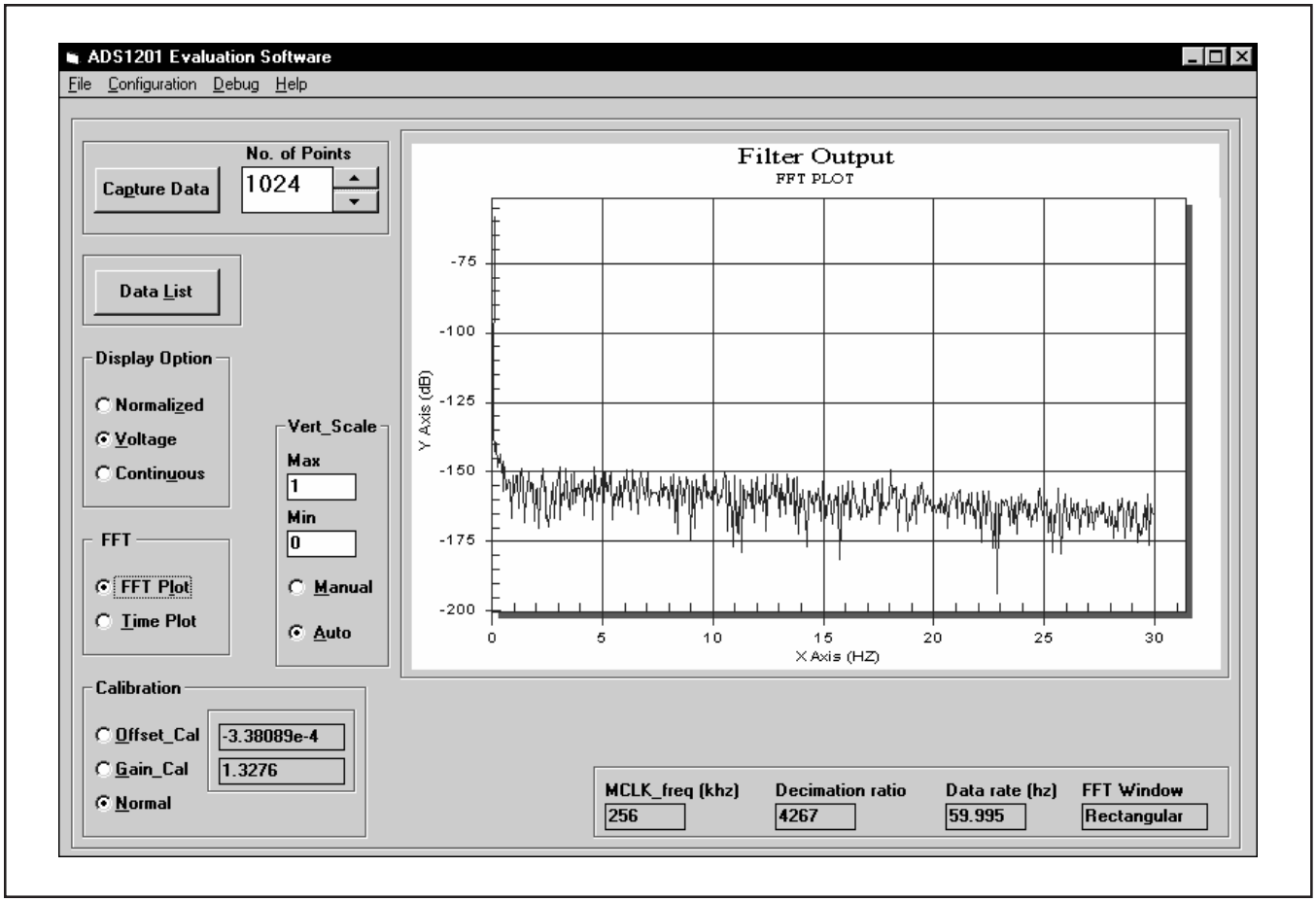

FIGURE 11. ADS1201 Evaluation Software Main Window.

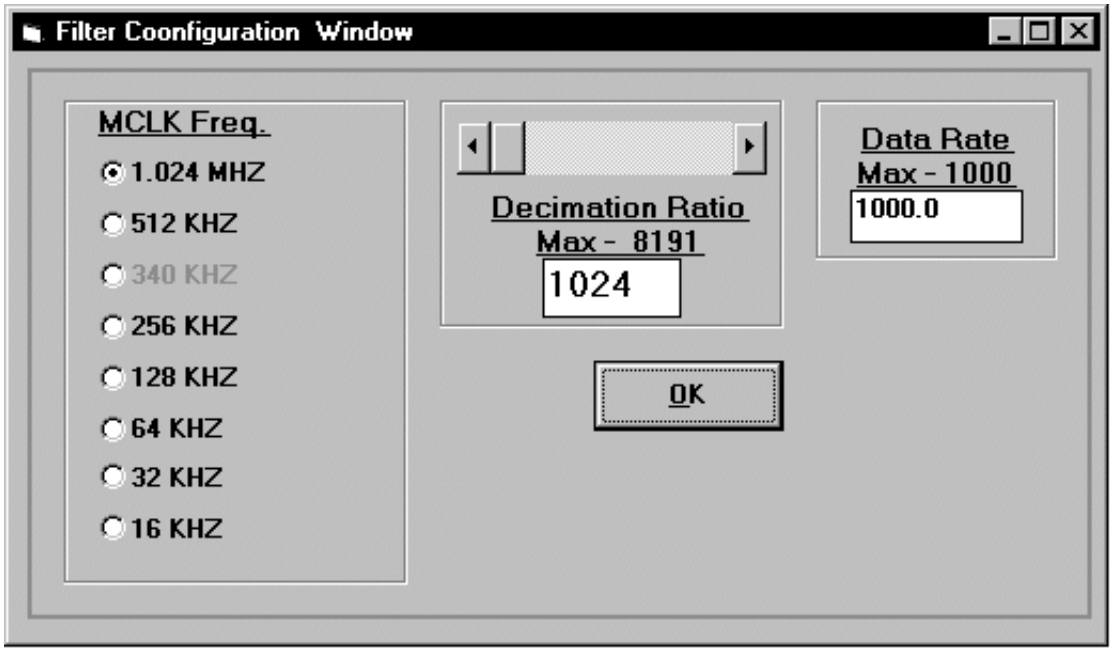

FIGURE 12. ADS1201 Evaluation Software Configuration Window.

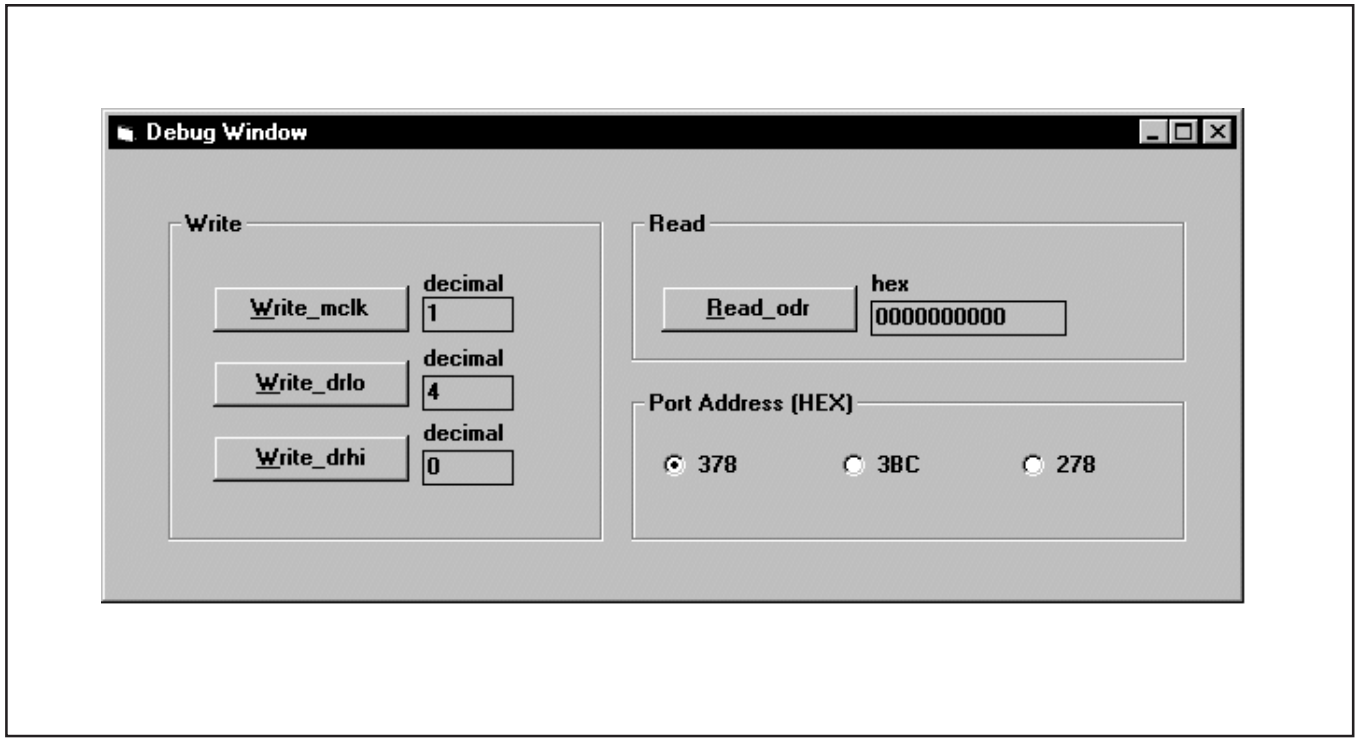

FIGURE 13. ADS1201 Evaluation Software Debug Window.

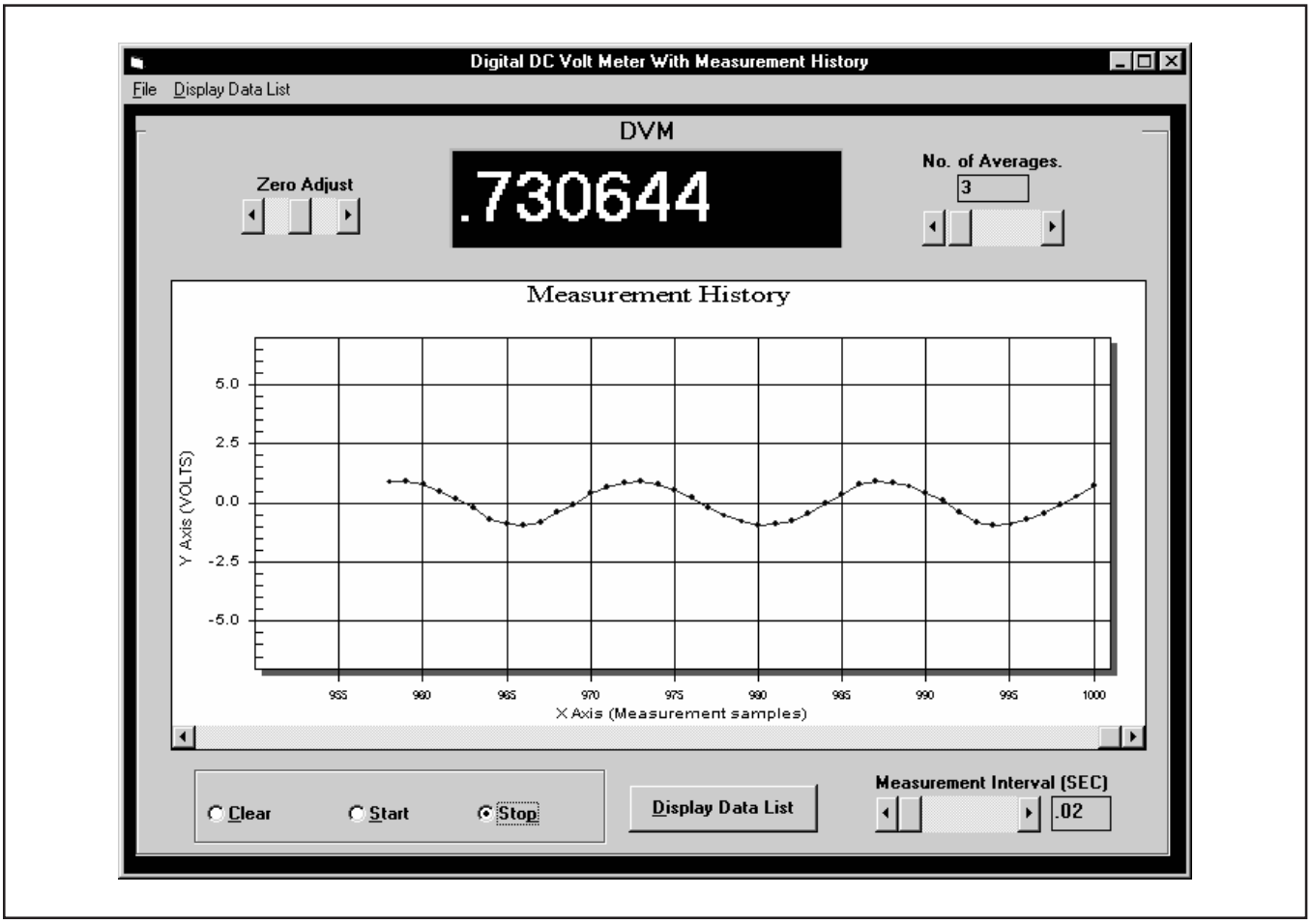

FIGURE 14. ADS1201 Evaluation Software DC Voltmeter Window.

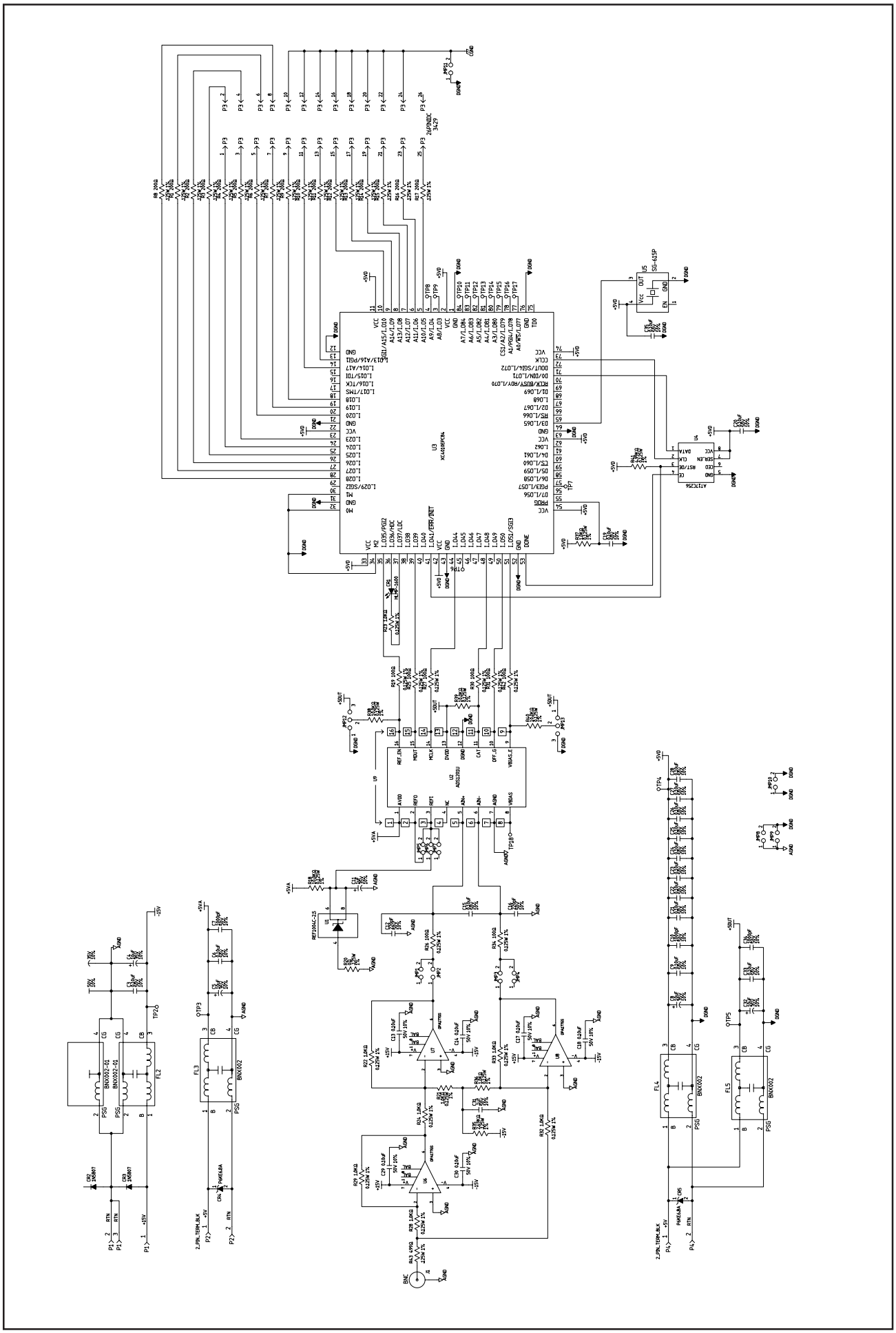

FIGURE 15. ADS1201U Demonstration Board.

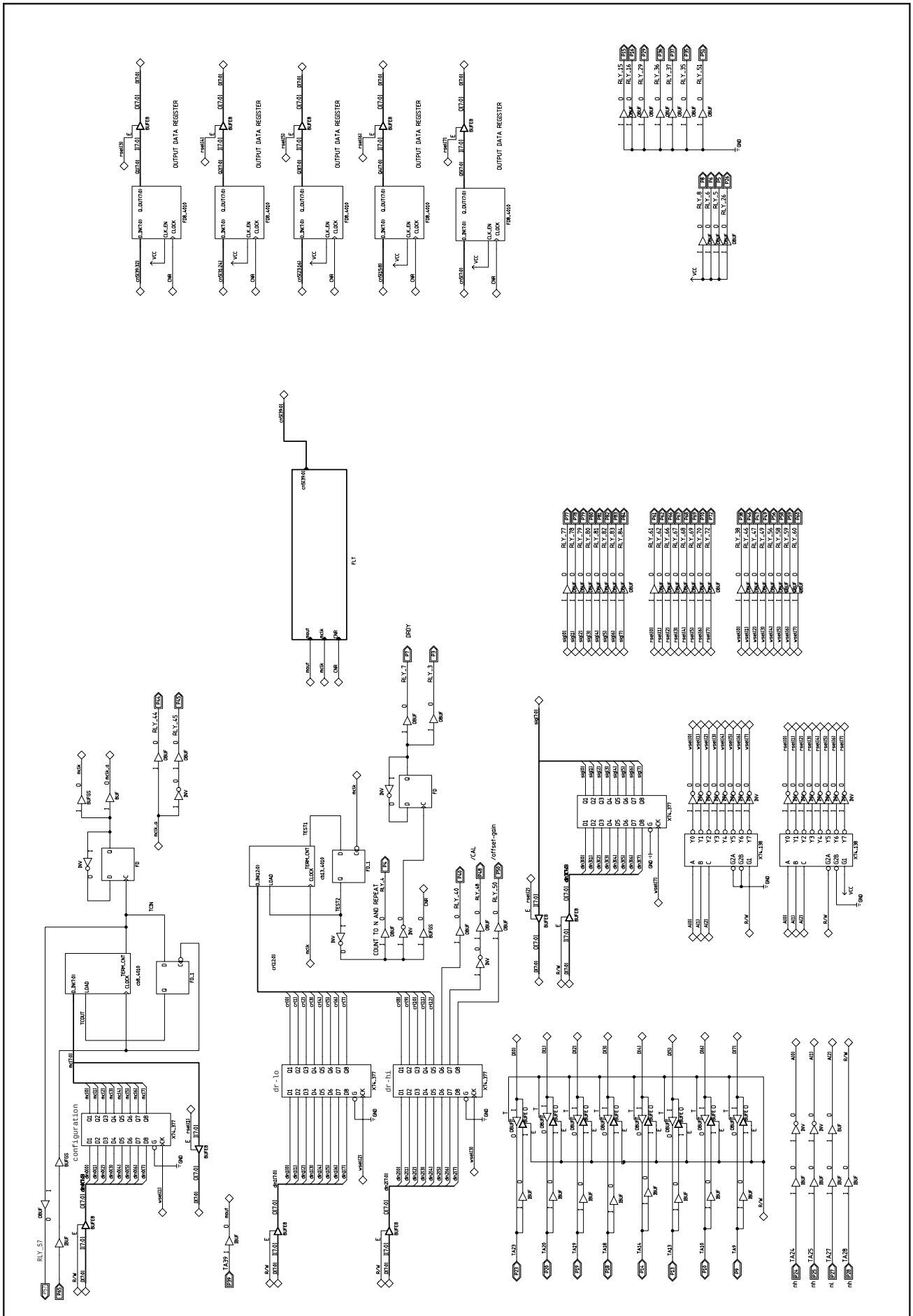

FIGURE 16. Xilinx FPGA Implementation PC Interface and Control.

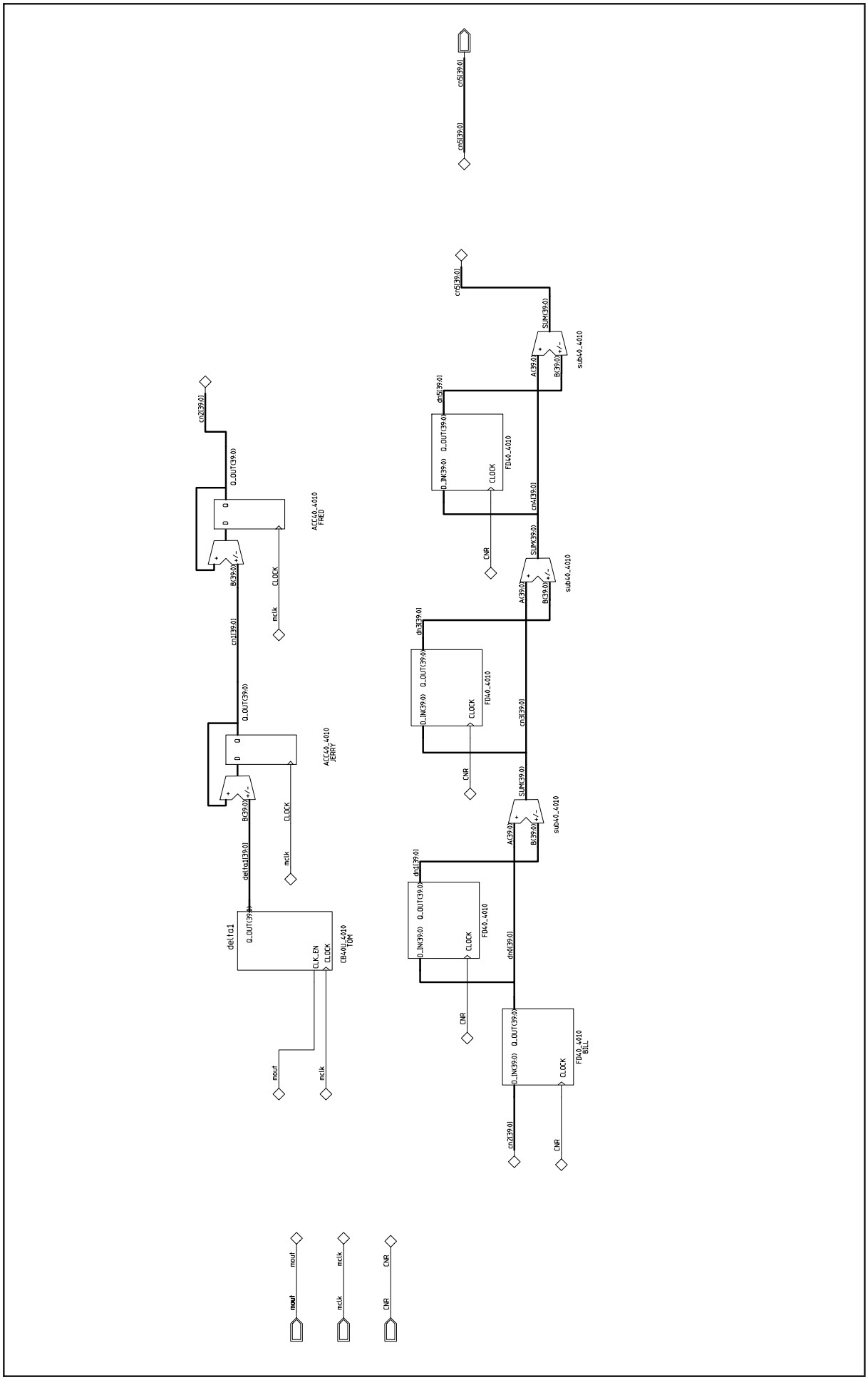

FIGURE 17. Xilinx FPGA Implementation Digital Filter (FLT).

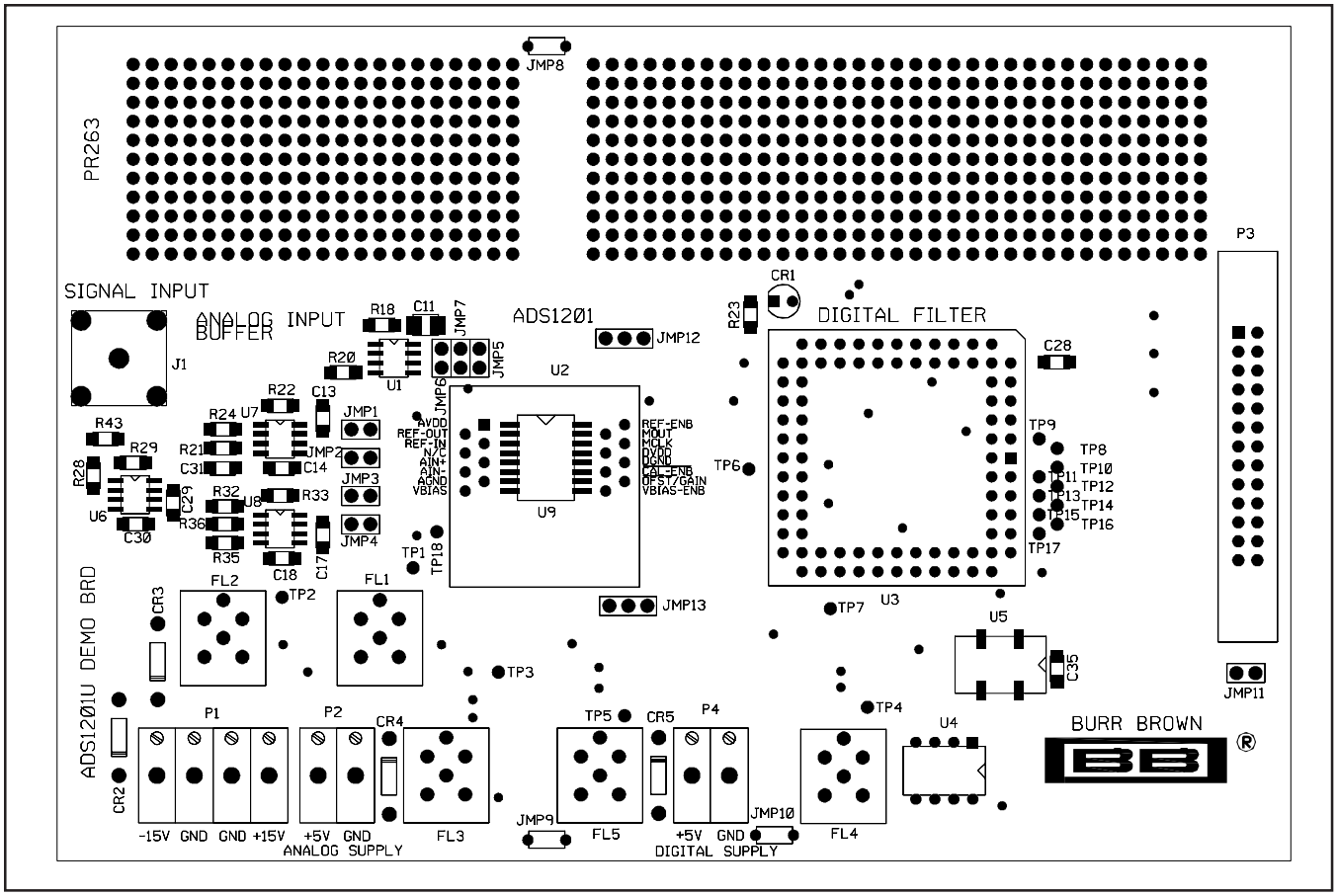

FIGURE 18. Board Outline (top silkscreen).

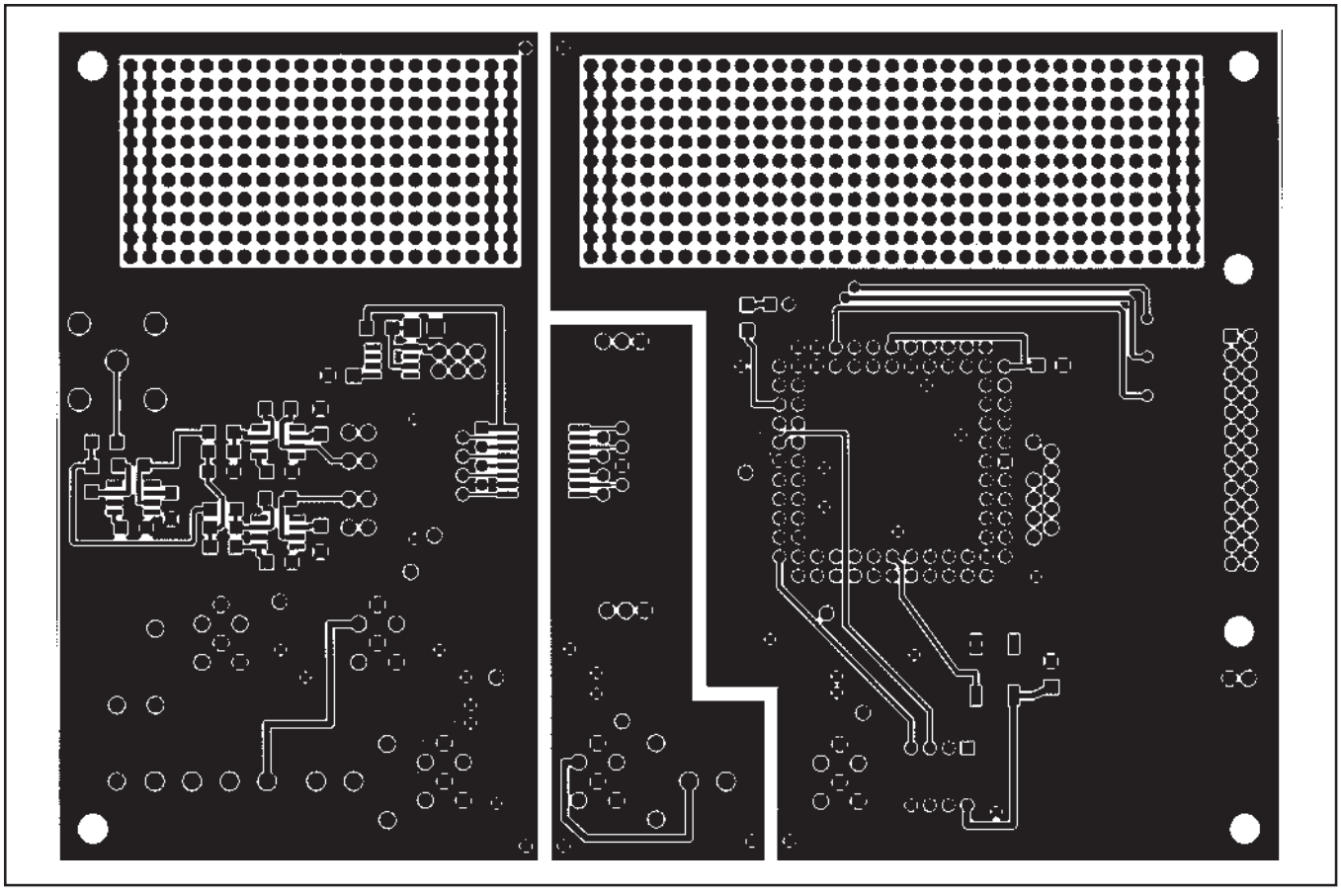

FIGURE 19. Board Outline (top view).

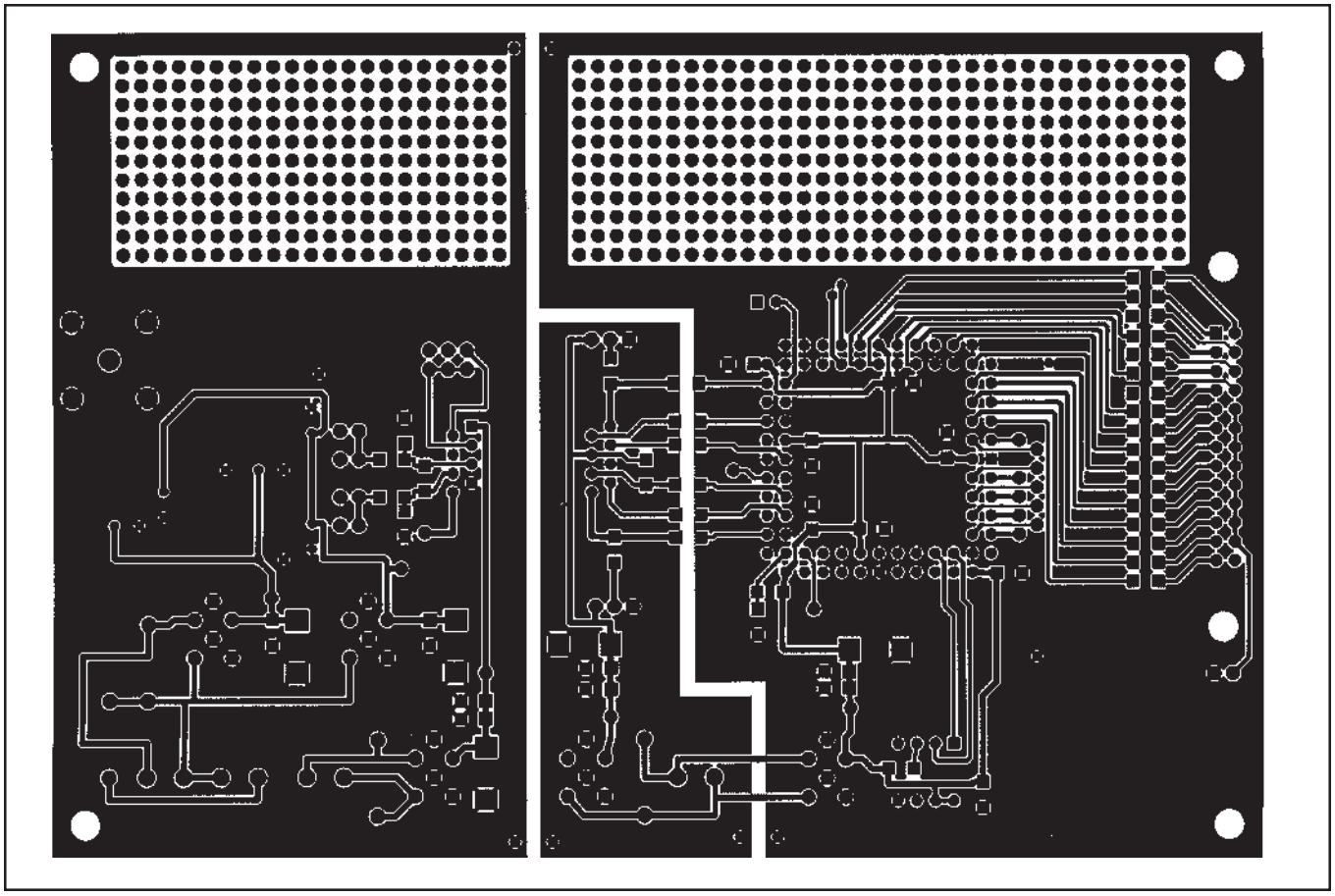

FIGURE 20. Board Outline (bottom view).

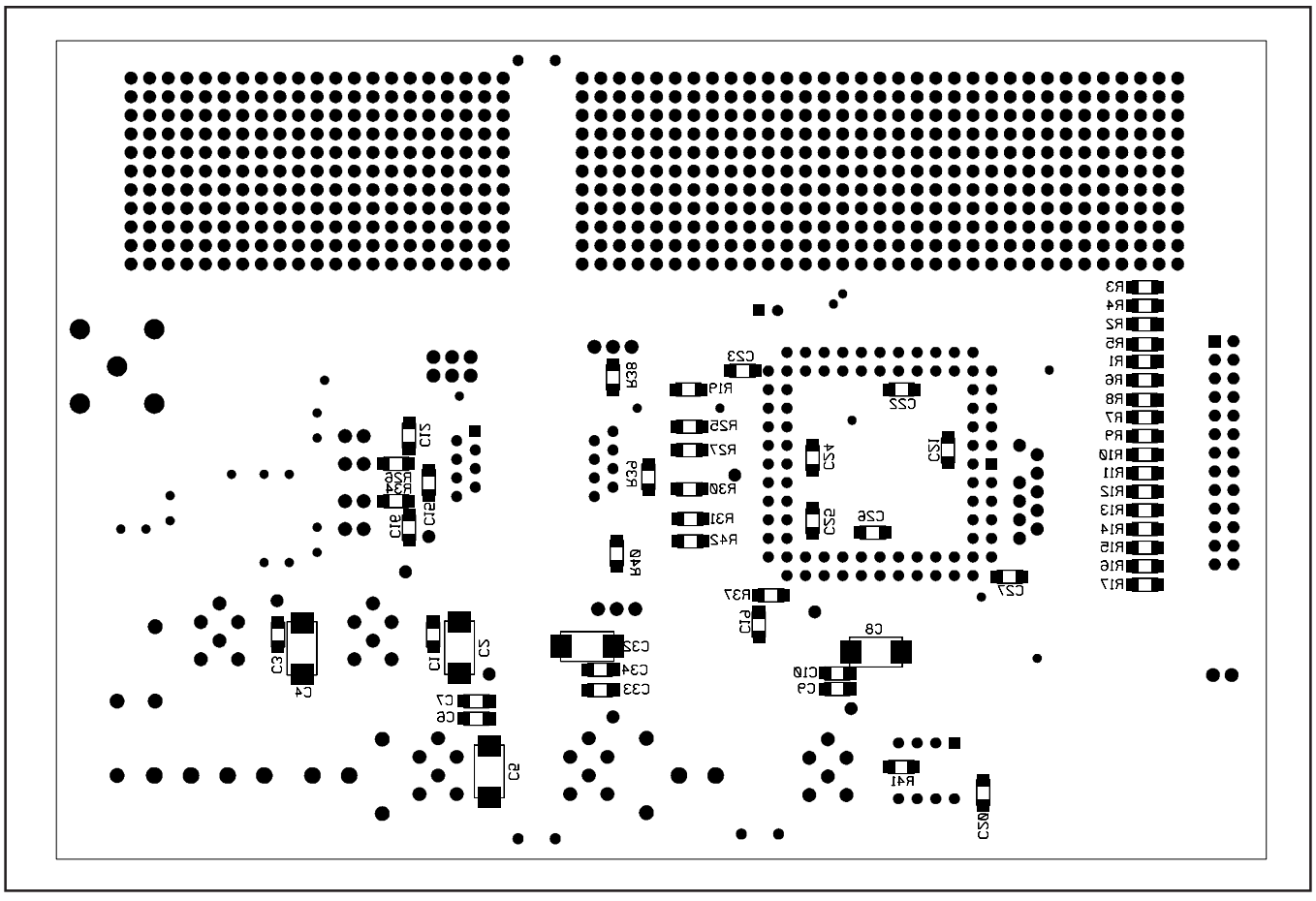

FIGURE 21. Board Outline (bottom silkscreen).