# SPA-2318

# SPA-2318Z

RoHS Compliant & Green Package

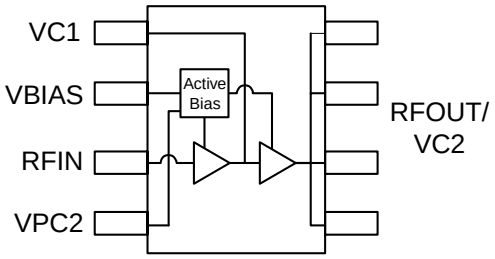
## 1700-2200 MHz 1 Watt Power Amp with Active Bias

## Product Description

Sirenza Microdevices' SPA-2318 is a high efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot.

This product is specifically designed for use as a driver amplifier for infrastructure equipment in the 1960 and 2140 MHz bands. Its high linearity makes it an ideal choice for multi-carrier and digital applications.

The matte tin finish on Sirenza's lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.




## Product Features

- **Now available in Lead Free, RoHS Compliant, & Green Packaging**
- **High Linearity Performance:**
  **+21 dBm IS-95 Channel Pwr at -55 dBc ACP**
  **+20.7 dBm W-CDMA Channel Pwr at -50dBc ACP**
  **+47 dBm Typ. OIP3**
- **On-chip Active Bias Control**
- **High Gain: 24 dB Typ. at 1960 MHz**
- **Patented High Reliability GaAsHBT Technology**
- **Surface-Mountable Plastic Package**

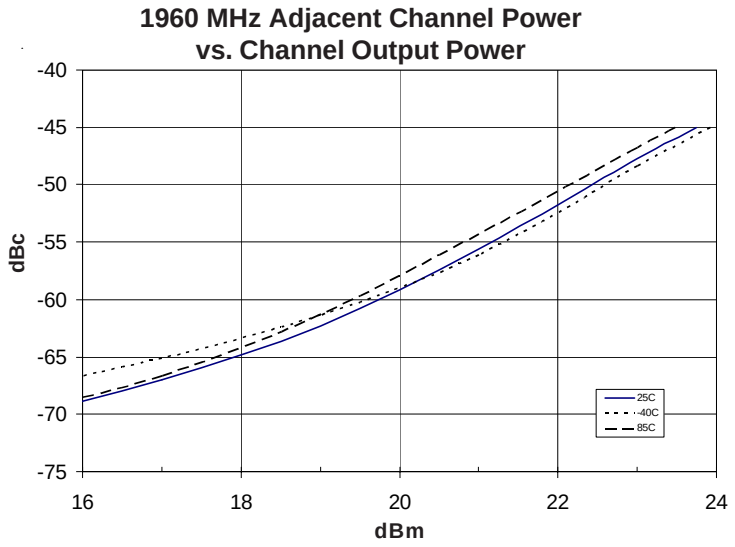
## Applications

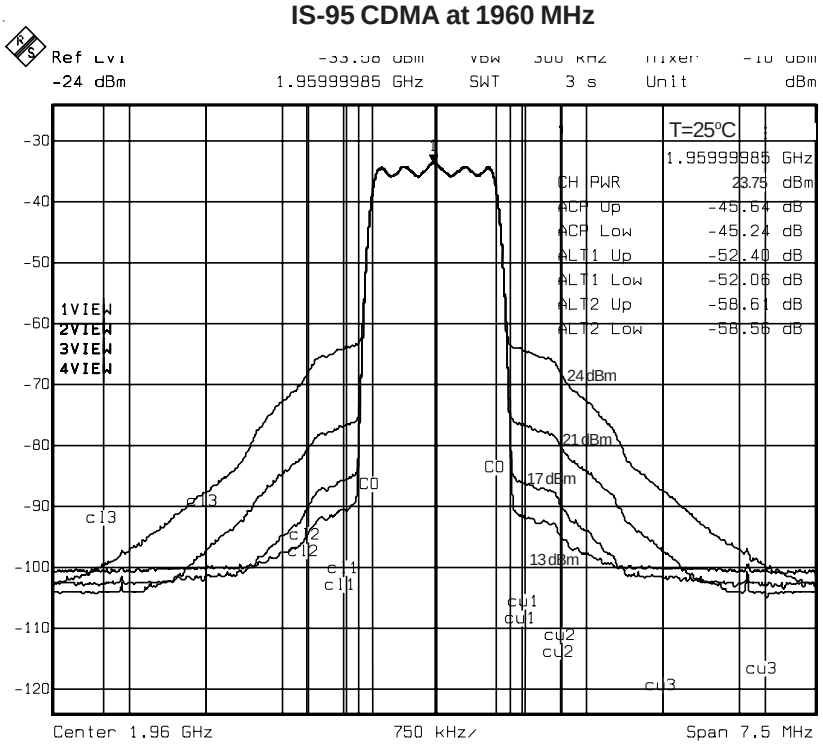
- **W-CDMA Systems**
- **PCS Systems**
- **Multi-Carrier Applications**

| Symbol | Parameters: Test Conditions: $Z_0$ = 50 Ohms Temp = 25°C, Vcc = 5.0V | | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|
| $f_0$ | Frequency of Operation | | MHz | 1700 | | 2200 |
| $P_{1dB}$ | Output Power at 1dB Compression[1] | f = 1960 MHz<br>f = 2140 MHz | dBm | | 29.5<br>29.5 | |
| ACP | Adjacent Channel Power [1]<br>IS-95 @ $P_{OUT}$ = 21.0 dBm<br>W-CDMA @ $P_{OUT}$ = 20.7 dBm | <br>f = 1960 MHz<br>f = 2140 MHz | dBc | | <br>-55.0<br>-50.0 | <br><br>-47.0 |
| $S_{21}$ | Small Signal Gain [1,2] | f = 1960 MHz<br>f = 2140 MHz | dB | 22.5 | 24.0<br>23.5 | 25.0 |
| VSWR | Input VSWR [1,2] | f = 1960 MHz<br>f = 2140 MHz | -<br>- | | 1.6:1<br>1.6:1 | |
| $OIP_3$ | Output Third Order Intercept Point [2]<br>Power out per tone = +14dBm | f = 1960 MHz<br>f = 2140 MHz | dBm | | 46.5<br>47.0 | |
| NF | Noise Figure [1,2] | f = 1960 MHz<br>f = 2140 MHz | dB | | 5.5<br>5.5 | |
| $I_{CC}$ | Device Current [1,2] | Ibias = 10 mA<br>Ic1 = 70 mA<br>Ic2 = 320 mA | mA | 360 | 400 | 425 |
| $V_{CC}$ | Device Voltage [1,2] | | V | 4.75 | 5.0 | 5.25 |
| $R_{th\ j-l}$ | Thermal Resistance (junction - lead), $T_L$ = 85°C | | °C/W | | 31 | |

[1] Optimal ACP tune [2] Optimal IP3 tune

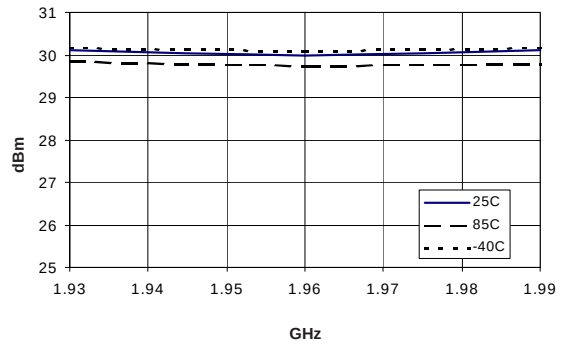
## ACP Optimized 1960 MHz Application Circuit Data, Icc=400mA, Vcc=5V
## IS-95, 9 Channels Forward



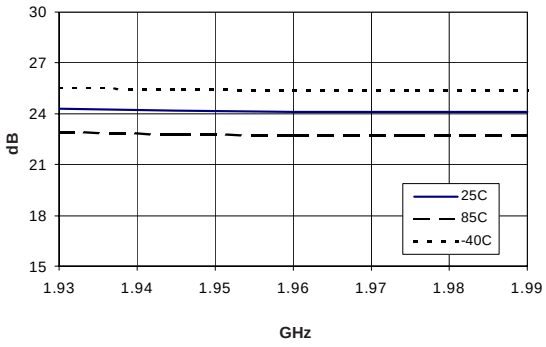



## ACP Optimized 1960 MHz Application Circuit Data, Icc=400mA, Vcc=5V

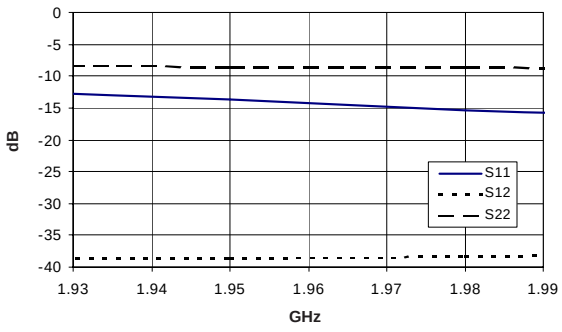
P1dB vs Frequency



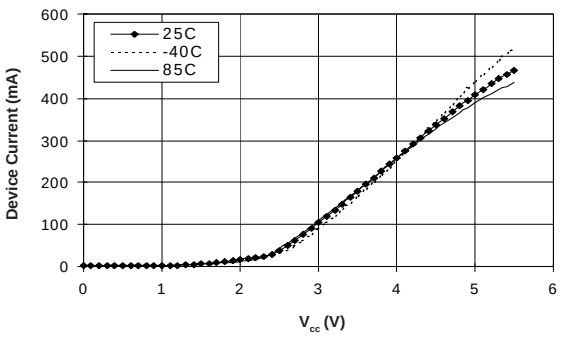

Gain vs. Frequency



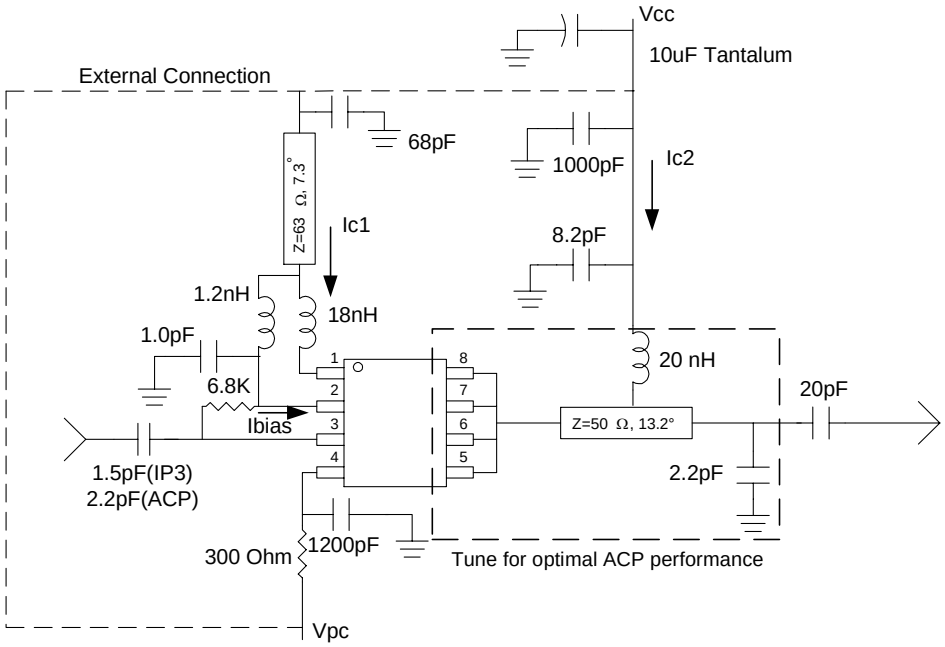

Input/Output Return Loss, Isolation vs Frequency, T=25°C



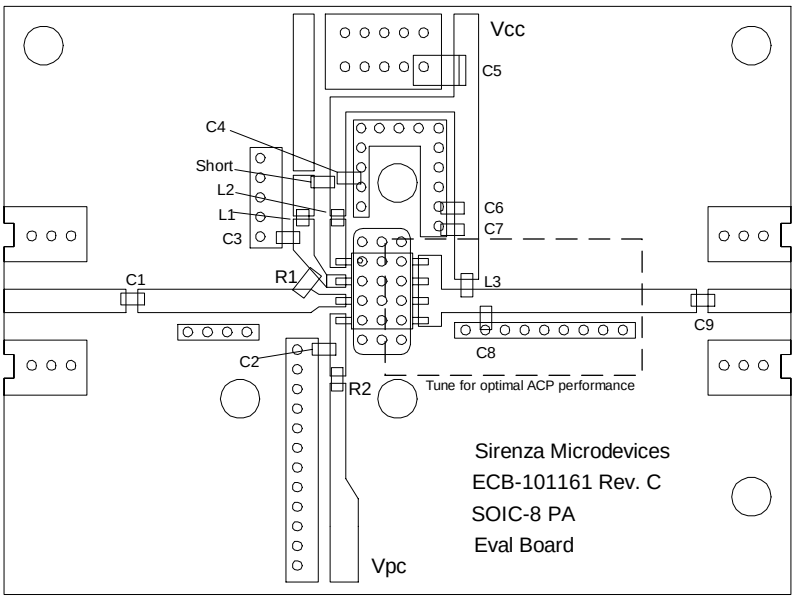

Device Current vs. Source Voltage



## 1930 - 1990 MHz Schematic




## 1930 - 1990 MHz Evaluation Board Layout

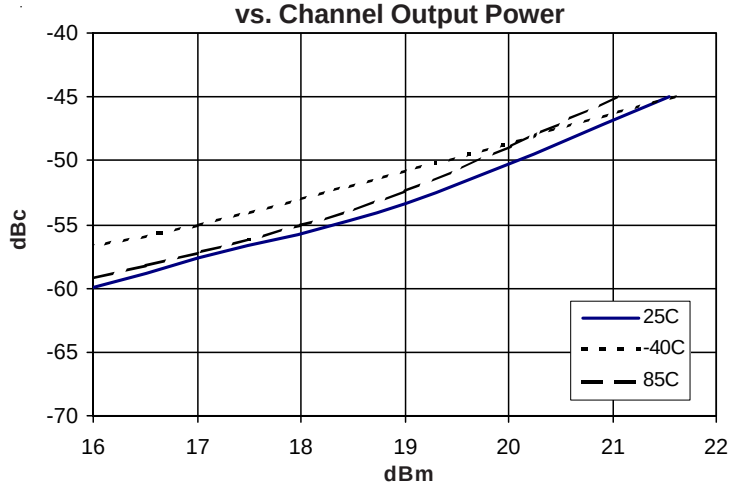



| Ref. Des. | Value | Part Number |
|---|---|---|
| C1 | 1.5pF, ±0.25pF (IP3)<br>2.2pF, ±0.25pF (ACP) | Rohm MCH18 series |
| C2 | 1200pF, 5% | Rohm MCH18 series |
| C3 | 1.0pF, ±0.25pF | Rohm MCH18 series |
| C4 | 68pF, 5% | Rohm MCH18 series |
| C5 | 10uF, 10% | AVX TAJB106K020R |
| C6 | 1000pF, 5% | Rohm MCH18 series |
| C7 | 8.2pF, ±0.5pF | Rohm MCH18 series |
| C8 | 2.2pF, ±0.25pF | Rohm MCH18 series |
| C9 | 20pF, 5% | Rohm MCH18 series |
| L1 | 1.2nH, ±0.3nH | Toko LL1608-FS series |
| L2 | 18nH, 5% | Toko LL1608-FS series |
| L3 | 20nH, 5% | Coilcraft HQ 0805 series |
| R1 | 6.8K Ohm, 5% | Rohm MCR03 series |
| R2 | 300 Ohm, 5% | Rohm MCR03 series |

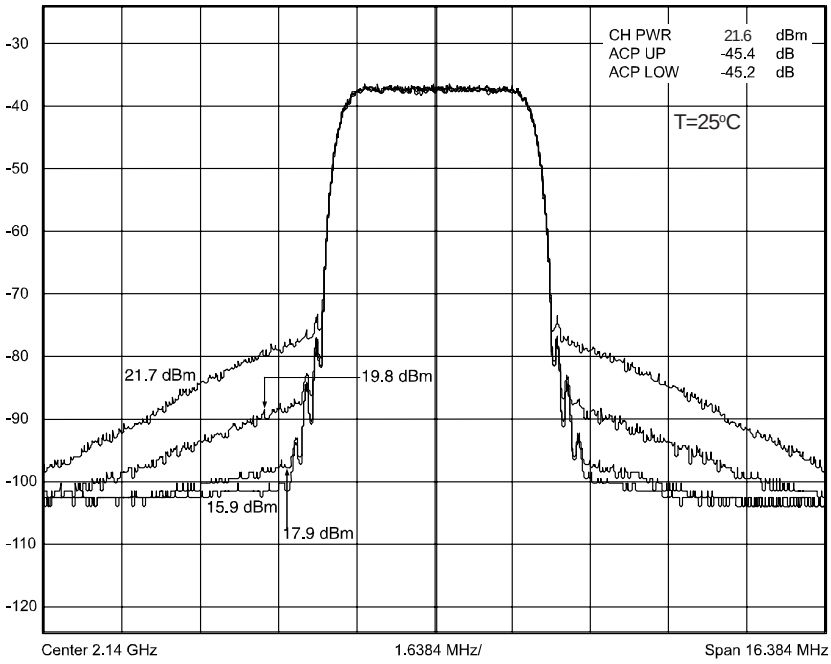
## ACP Optimized 2140 MHz Application Circuit Data, Icc=400mA, Vcc=5V

**W-CDMA setup is PCCPCH+PSCH+SSCH+CPICH+PICH+64 DPCH,**
**10.5 dB peak to average @ 0.001% probability**

**W-CDMA at 2.14 GHz Adjacent Channel Power vs. Channel Output Power**

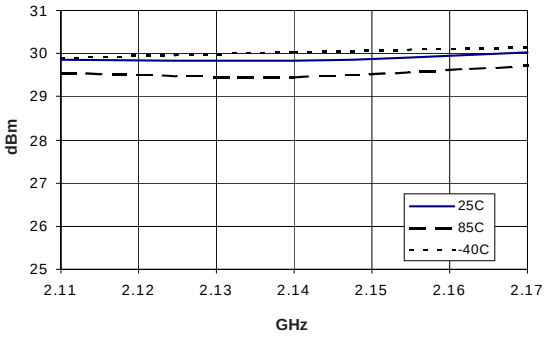



**W-CDMA at 2.14 GHz**

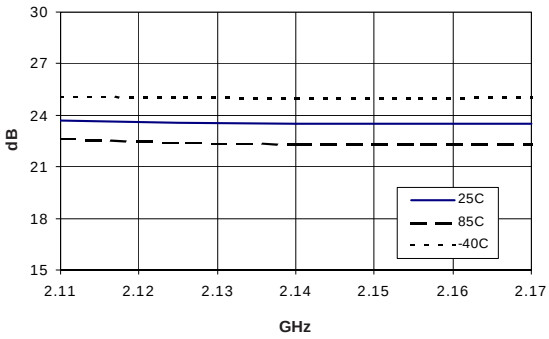


## ACP Optimized 2140 MHz Application Circuit Data, Icc=400mA, Vcc=5V

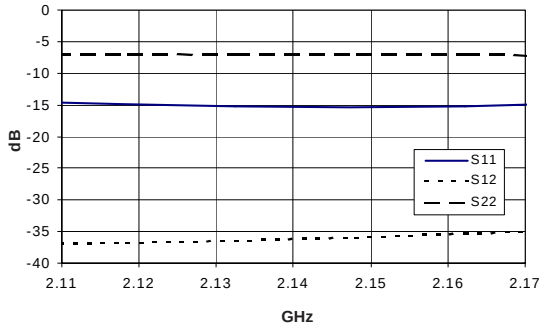
P1dB vs Frequency



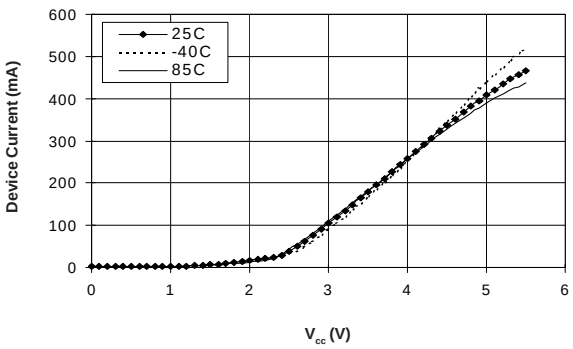

Gain vs. Frequency



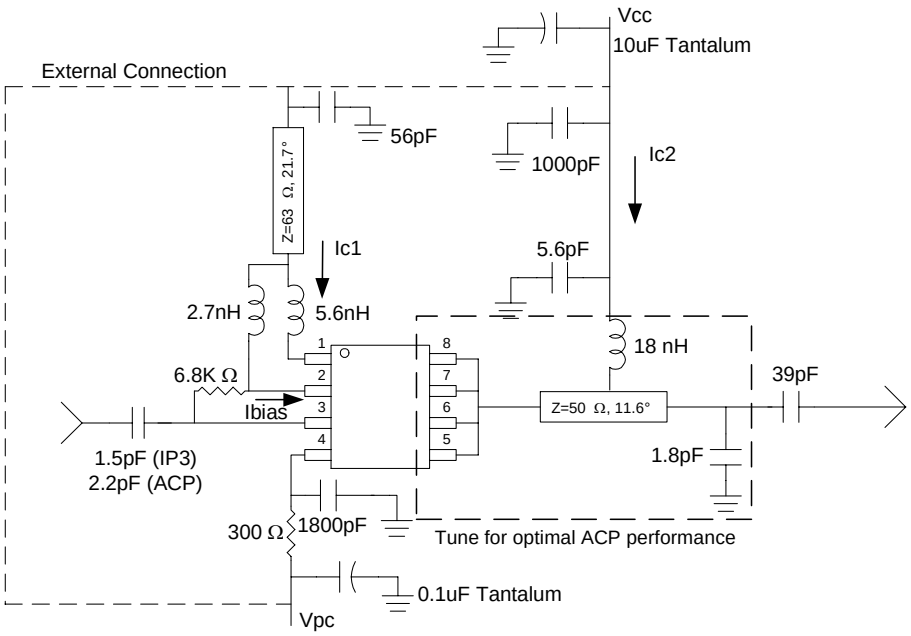

Input/Output Return Loss, Isolation vs Frequency, T=25°C



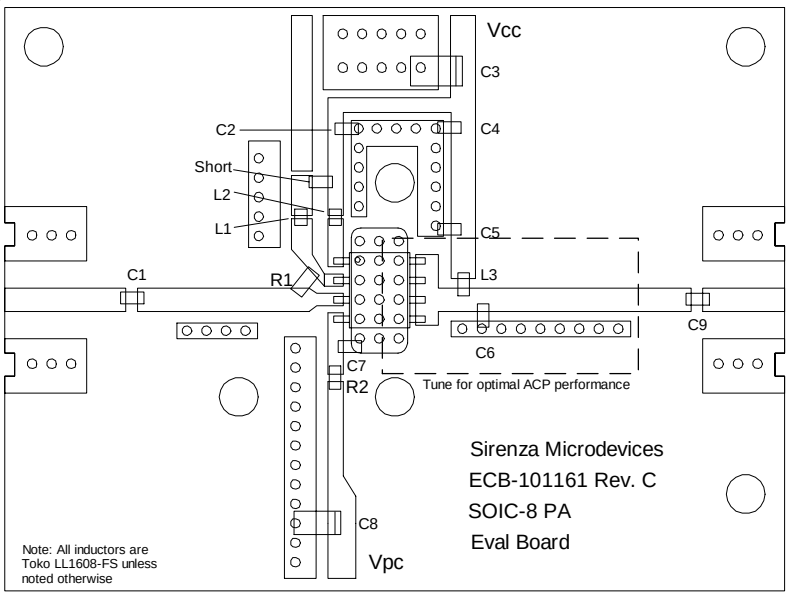

Device Current vs. Source Voltage



## 2110 - 2170 MHz Schematic



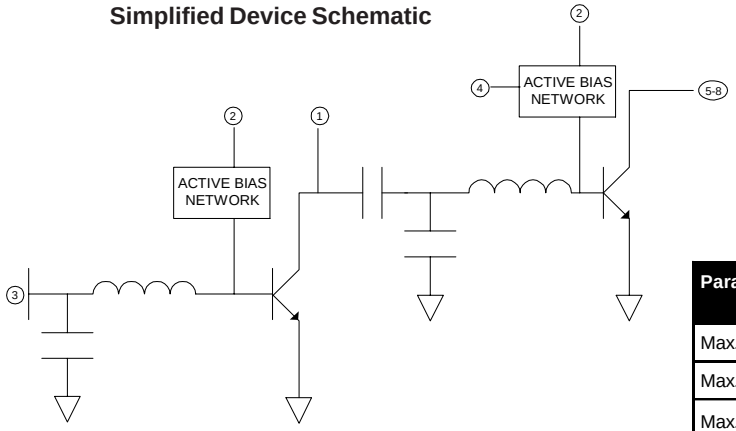

## 2110 - 2170 MHz Evaluation Board Layout




| Ref. Des. | Value | Part Number |
|---|---|---|
| C1 | 1.5pF, ±0.25pF (IP3)<br>2.2pF, ±0.25pF (ACP) | Rohm MCH18 series |
| C2 | 56pF, 5% | Rohm MCH18 series |
| C3 | 10uF, 10% | AVX TAJB106K020R |
| C4 | 1000pF, 5% | Rohm MCH18 series |
| C5 | 5.6pF, ±0.5pF | Rohm MCH18 series |
| C6 | 1.8pF, ±0.25pF | Rohm MCH18 series |
| C7 | 1800pF, 5% | Rohm MCH18 series |
| C8 | 0.1uF, 10% | Matsuo 267M3502104K |
| C9 | 39pF, 5% | Rohm MCH18 series |
| L1 | 2.7nH, ±0.3nH | Toko LL1608-FS series |
| L2 | 5.6nH, ±0.3nH | Toko LL1608-FS series |
| L3 | 18nH, 5% | Toko LL1608-FS series |
| R1 | 6.8K Ohm, 5% | Rohm MCR03 series |
| R2 | 300 Ohm, 5% | Rohm MCR03 series |

| Pin # | Function | Description |
|---|---|---|
| **1** | VC1 | VC1 is the supply voltage for the first stage transistor. The configuration as shown on application schematic is required for optimum RF performance. |
| **2** | Vbias | Vbias is the bias control pin for the active bias network. Recommended configuration is shown in the Application Schematic. |
| **3** | RF In | RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the Application Schematic. |
| **4** | VPC2 | VPC2 is the bias control pin for the active bias network for the second stage. The recommended configuration is shown in the Application Schematic. |
| **5, 6, 7, 8** | RF Out/VC2 | RF output and bias pins. Bias should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed. An output matching network is necessary for optimum performance. |
| **EPAD** | Gnd | Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 9). |

### Simplified Device Schematic




### Absolute Maximum Ratings

| Parameter (Ta = 25ºC) | Absolute Limit |
|---|---|
| Max. Supply Current ($I_{c1}$) at $V_{CC}$ typ. | 150 mA |
| Max. Supply Current ($I_{c2}$) at $V_{CC}$ typ. | 750 mA |
| Max. Device Voltage ($V_{CC}$) at $I_{cc}$ typ. | 6.0 V |
| Max. RF Input Power | 16 dBm |
| Max. Junction Temp. ($T_J$) | +160 ºC |
| Max. Storage Temp. | +150 ºC |

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

$$I_{CC}V_{CC}\ (max) < (T_J - T_L)/R_{th,j\text{-}l}$$

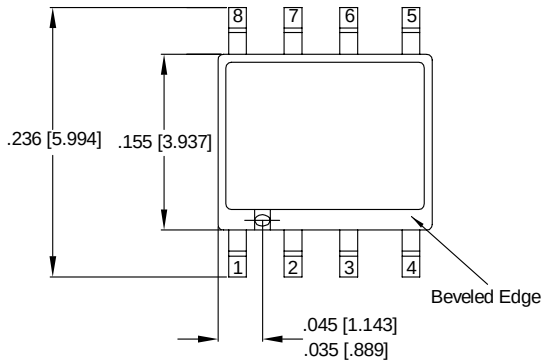
**Caution: ESD sensitive**

Appropriate precautions in handling, packaging and testing devices must be observed.

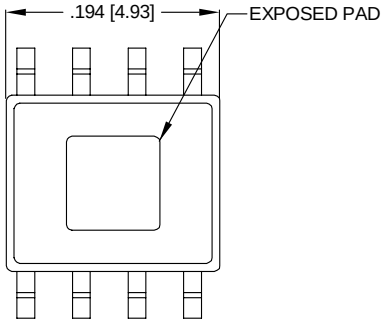
The Moisture Sensitivity Level rating for this device is level 1 (**MSL-1**) based on the JEDEC 22-A113 standard classification. No special moisture packaging/handling is required during storage, shipment, or installation of the devices.

## Package Outline Drawing

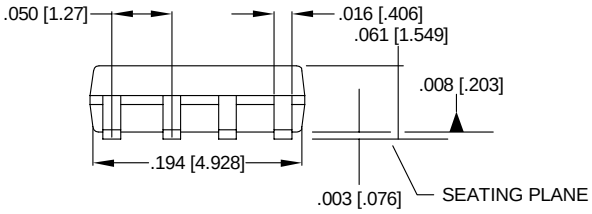
(See SMDI MPO-101644 for tolerances, available on our website)



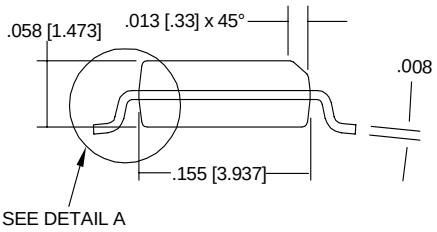

TOP VIEW



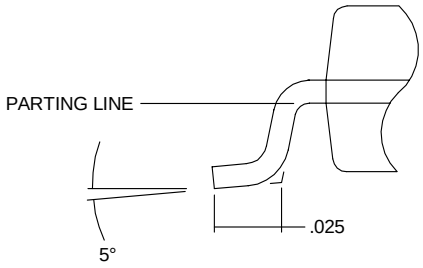

BOTTOM VIEW




SIDE VIEW




END VIEW



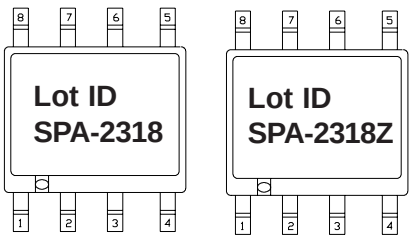

DETAIL A

**Note:** DIMENSIONS ARE IN INCHES [MM]

## Part Number Ordering Information

| Part Number | Reel Size | Devices/Reel |
|---|---|---|
| SPA-2318 | 7" | 500 |
| SPA-2318Z | 7" | 500 |

## Part Identification Marking




## Recommended Land Pattern