Order this document
by MC68322/D

MOTOROLA

Microprocessor and Memory Technologies Group

MC68322

Product Brief

Integrated Printer Processor

The MC68322 is a high-performance integrated printer processor, which combines an MC68000 compatible EC000 Core processor, a RISC graphics processor (RGP) and a print engine video controller (PVC) with numerous system integration features on a single integrated circuit. It is the first of Motorola's M68000 family designed specifically for laser printers. The MC68322 provides a unique solution for new designs as well as an excellent migration path for existing M68000-powered printers. Additionally, the new chip will find ready application to the inkjet printer and multifunction-peripheral (Fax/Modem/Printer) markets and other embedded control applications, which require very fast bit manipulations. The MC68322 provides outstanding performance at an extremely affordable price.

Historically, printer applications have been solved using a single general purpose processor and external application specific circuitry. The MC68322 employs a highly specialized, multi-processor architecture, which enables the user to take advantage of memory reduction techniques. This design implementation provides a technically superior and more cost effective system solution. Specialized display list banding techniques executed by the dedicated RISC graphics processor enable system memory requirements to be significantly reduced.

The use of software memory reduction techniques alone, an approach taken by conventional controllers, lack the power needed to handle complex pages, causing the controller to fall back to lower resolution or reduced page throughput. By integrating an EC000 Core, RGP, and PVC using a unique dual bus architecture, the MC68322 optimizes overall system performance. The dual bus architecture eliminates bus contention between processing units creating a true parallel processing environment. The additional bandwidth allows each processing unit to operate at peak performance. Working in conjunction with an on-chip, programmable, bursting DRAM controller, the processing units are capable of achieving outstanding throughput. These dedicated processing units enable the MC68322 to produce 600 dot per inch images using substantially less memory than conventional controllers. The MC68322 extends these benefits to low-cost 4–8 page per minute printers.

The MC68322 significantly reduces component count, board space, power consumption and their inherent costs while yielding higher reliability and shorter design time. The MC68322 provides support for toner conservation, enabling the print controller to conserve toner when printing in draft mode. The MC68322 provides the perfect printing environment for users of complex page description languages (such as PCL and PostScript) and less scaleable graphics imaging models such as Windows Printing System and QuickDraw). Complete code compatibility with the M68000 Family provides the designer access to a broad base of established real-time kernels, operating systems, languages, applications and development tools, many of which are optimized for embedded processing and printing applications. Figure 1 shows a block diagram of the MC68322.

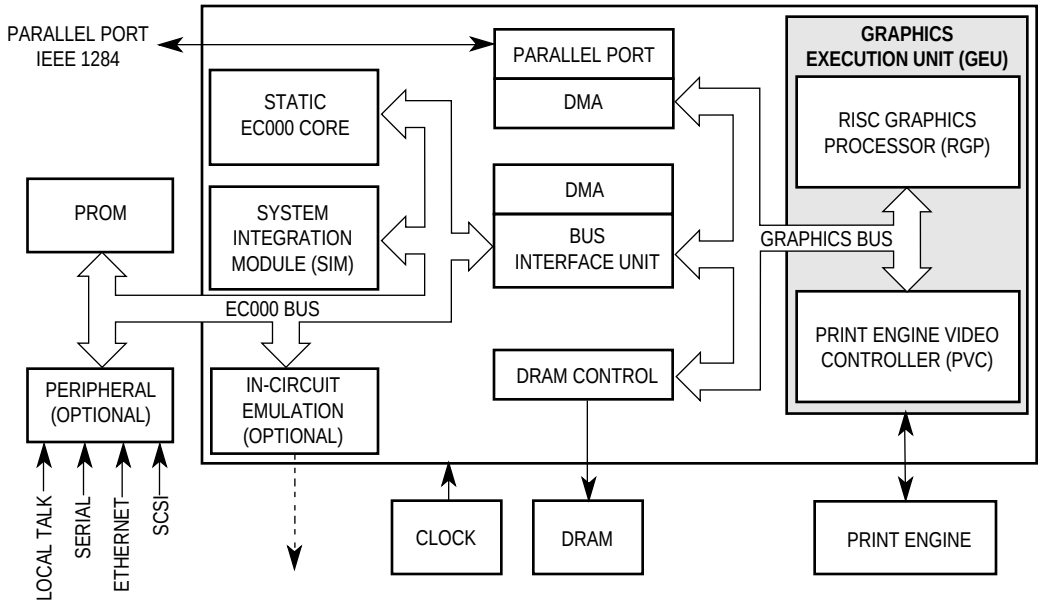

Figure 1. System Block Diagram

FEATURES

- Static EC000 Core Processor
  - – Complete Code Compatibility with M68000 Family
  - – Glueless Interface to Peripherals
  - – 256 Mbyte Address Range
- Graphics Execution Unit (GEU)
  - – Memory Reduction Techniques
    - - Run Length Encoded Scan Line Tables
  - – RISC Graphics Processor (RGP)
    - - Processes Multi-Operation Graphics Orders from Display List
    - - Produces Compressed Bit Map Image using Hardware Banding
    - - Dedicated Graphics Bus Allows up to 8 PPM Performance at 600 DPI Resolution
  - – Print Engine Video Controller (PVC)
    - - Converts Bit Map Image to Serial Data Stream and Feeds Print Engine
    - - Generic, Programmable, Non-Impact Printer Communications Interface
    - - Toner Conservation Technique
  - – Dedicated High-Performance DMA Controller for GEU Operations
- Bus Interface Unit (BIU)
  - – Dual Bus Architecture Allows Separate Buses to Function Independently
  - – Distributed Processing Optimizes System Performance
- System Integration Module (SIM)
  - – 8 Programmable Chip Selects
  - – 256 Kbytes to 512 Mbytes of PROM Address Space
  - – Independently Programmable Timing Parameters for each ROM Bank
  - – Integrated System Timer
- DRAM System Integration Module (DSIM)
  - – Supports 512 Kbyte, 2 Mbyte, and 8 Mbyte DRAM Bank Sizes
  - – Directly Controls up to 6 Banks of DRAM; Supports up to 48 Mbytes of DRAM
  - – Programmable Transparent Refresh of DRAM Banks
  - – Bursting DRAM Interface
- General-Purpose DMA Controller Module
  - – Provides High Speed Downloads Without Impact to Core Processor Performance
- IEEE 1284 Parallel Port Controller Module
  - – DMA Controller Supports 2 Mbyte/sec Bidirectional Communication Transfers
- 16MHz or 20MHz Operation
- 160 Pin Plastic Quad Flat Pack (QFP)

MC68322 SIGNAL DESCRIPTION

Figure 2 illustrates the MC68322 input and output signals within their functional groups. Table 1 lists the signal names, mnemonics, and functional descriptions of the MC68322 signals.

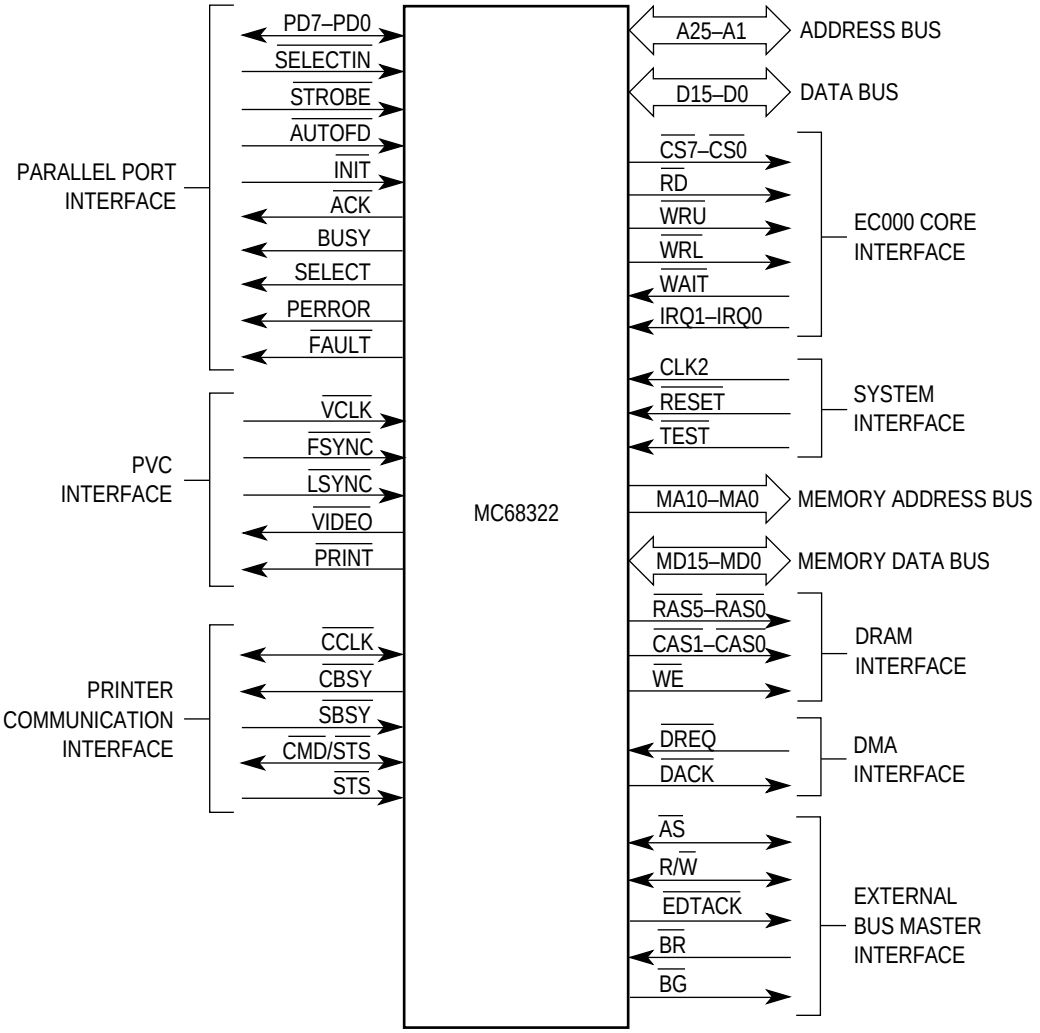

Figure 2. MC68322 Functional Signal Groups

Table 1. Signal Index

Signal Name	Mnemonic	Function
Address Bus	A25–A1	25-bit external address bus.
Address Strobe	$\overline{AS}$	Indicates a valid address is on the bus.
Auto Feed Control	$\overline{AUTOFD}$	Parallel port control signal.
Bus Grant	$\overline{BG}$	Asserted to grant bus mastership to an external device.
Bus Request	$\overline{BR}$	Asserted by an external device to request bus master ship.
Chip Select	$\overline{CS7}$–$\overline{CS0}$	PROM and I/O chip selects.
Clock	CLK2	2× system clock.
Column Address Strobe	$\overline{CAS1}$, $\overline{CAS0}$	DRAM column address strobes.
Command Busy	$\overline{CBSY}$	Command busy indicates that a command will be sent to the printer.
Command Clock	$\overline{CCLK}$	Command clock is the command/status clock to/from the printer.
Command/Status Data	$\overline{CMD}$ /$\overline{STS}$	Command/status data is the synchronous communications and data out to the printer, or the bidirectional command/status data to or from the printer.
Data Bus	D15–D0	16-bit data bus used for byte or word transfers.
DMA Acknowledge	$\overline{DACK}$	Output that indicates data transfer is complete.
DMA Request	$\overline{DREQ}$	Input that starts a DMA transfer.
DRAM Address Bus	MA10–MA0	Multiplexed DRAM address bus.
DRAM Data Bus	MD15–MD0	16-bit DRAM data bus.
External Master DTACK	$\overline{EDTACK}$	External master support signal.
Frame Sync	$\overline{FSYNC}$	Indicates the top of the page in response to a print request.
Initialization Input	$\overline{INIT}$	Parallel port initialize control.
Interrupt Request	$\overline{IRQ1}$, $\overline{IRQ0}$	Interrupt request input.
Line Sync	$\overline{LSYNC}$	Indicates the left edge of the page.
PPI Data Bus	PD7–PD0	Parallel port interface bidirectional data bus.
Print Request	$\overline{PRINT}$	Print request requests a page to be printed.
Printer Busy	BUSY	Parallel port printer busy.
Printer Data Strobe	$\overline{STROBE}$	Parallel port signal that latches incoming data.
Printer Error	$\overline{FAULT}$	Parallel port printer error.
Printer Paper Path Error	PERROR	Parallel port paper error.
Printer Select	$\overline{SELECTIN}$	Parallel port request for "on-line" status.
Printer Selected	SELECT	Printer "on-line".
Read Enable	$\overline{RD}$	PROM and I/O read enable strobe.
Read/Write	R/$\overline{W}$	Identifies the transfer as a read or write.
Reset	$\overline{RESET}$	Processor reset.
Row Address Strobe	$\overline{RAS5}$–$\overline{RAS0}$	DRAM row address strobe.
Status Busy	$\overline{SBSY}$	Indicates a status wants to be received from the printer.
Status Data	$\overline{STS}$	Status data is the synchronous status data from the printer.

Table 1. Signal Index (Continued)

Signal Name	Mnemonic	Function
Test	$\overline{\text{TEST}}$	Test mode pin.
Transfer Acknowledge	$\overline{\text{ACK}}$	Parallel port transfer acknowledge.
Video	$\overline{\text{VIDEO}}$	Video is the digital serial video image.
Video Clock	$\overline{\text{VCLK}}$	Video clock is used to shift the video image.
Wait	$\overline{\text{WAIT}}$	PROM and I/O wait.
Write Enable	$\overline{\text{WE}}$	DRAM write enable strobe.
Write Enable – Lower	$\overline{\text{WRL}}$	PROM and I/O write enable strobe indicates valid data on D7–D0.
Write Enable – Upper	$\overline{\text{WRU}}$	PROM and I/O write enable strobe indicates valid data on D15–D8.

TERMS AND DEFINITIONS

BANDING

Banding is the process of building an image out of strips called bands. These bands, which describe the graphics operations necessary to construct the bit-mapped image for the page, are represented in an intermediate form called a display list. The printer display language (PDL) emulator firmware running on the EC000 Core generates the display list before the print engine begins the actual printing process. Generally, band $n + 1$ is being composed while band n is being output to the print engine.

Banding is desirable in printer controllers because the resulting system cost can be greatly reduced due to the significant memory savings associated with this technique. For banding to be viable, the display list must meet two requirements: it must fit in considerably less memory than the full-page image would require and the commands required to generate a band (called graphic orders) must be executable within the time it takes to print the previous band.

RUN-LENGTH ENCODING (RLE)

The scanline graphics orders contained within the display list reference a set of associated tables located in memory. These scanline tables contain bitstring specifiers that are run-length encoded in order to characterize an extremely compact representation of a bit-mapped image. The combination of run length compressed graphics data and the elimination of redundant information in the display list enables the display list to be significantly smaller than the actual bit-mapped image.

EC000 CORE PROCESSOR UNIT

The EC000 Core is a static, low-power, 32-bit general purpose microprocessor. It has a 28-bit address range for internal register decoding of chip selects and DRAM controller functions. This address range allows for full code compatibility with existing M68000 family based designs and future upward compatibility to higher performance designs. The EC000 Core is register and memory map compatible with the industry standard MC68000 and MC68HC000 processors.

The EC000 Core performs general purpose computing, I/O handling, exception handling, and display list rendering. For more information about the EC000 Core, refer to the *MC68322 User's Manual*.

The MC68322 was designed to support EC000 Core in-circuit emulation so that new hardware and software designs, which are being ported to the MC68322, can be tested rapidly. This is accomplished by providing additional signals in a 208-pin pin grid array (PGA) package that are not available in the 160-pin quad flat pack (QFP) package.

GRAPHICS EXECUTION UNIT (GEU)

The GEU is comprised of two independent processing units, the RGP and the PVC. The GEU performs all graphics functions required by complex PDLs. One of these functions is the bit-block transfer (BitBLT). The MC68322 performs extremely fast BitBLT operations. One, two, and three operand BitBLT operations are supported yielding 256 logical BitBLT operation combinations. The MC68322 also provides flexibility, through control registers, to provide many configurations. These control registers provide printer video characteristics (such as margins, width, and height), system memory timing, wait states, access auto termination, DRAM control, and external device access control.

GEU OPERATION

The RGP and PVC perform burst read and write accesses to DRAM through the DRAM controller. The RGP interprets a display list, which the EC000 Core or host application generates, to render a banded bit map page image. After a page image (or band image) is rendered by the RGP, the PVC converts the bitmap image into a serial data stream and transfers the rendered page image through the video interface to the print engine. The software interfaces to the RGP and PVC employ a combination of resources, including MC68322 registers and interrupts. The RGP and PVC require only a minimal amount of initialization and intervention by the EC000 Core to produce a banded page image and to transfer the image to the print engine. A functional block diagram depicting the GEU operations of the MC68322 is illustrated in Figure 3.

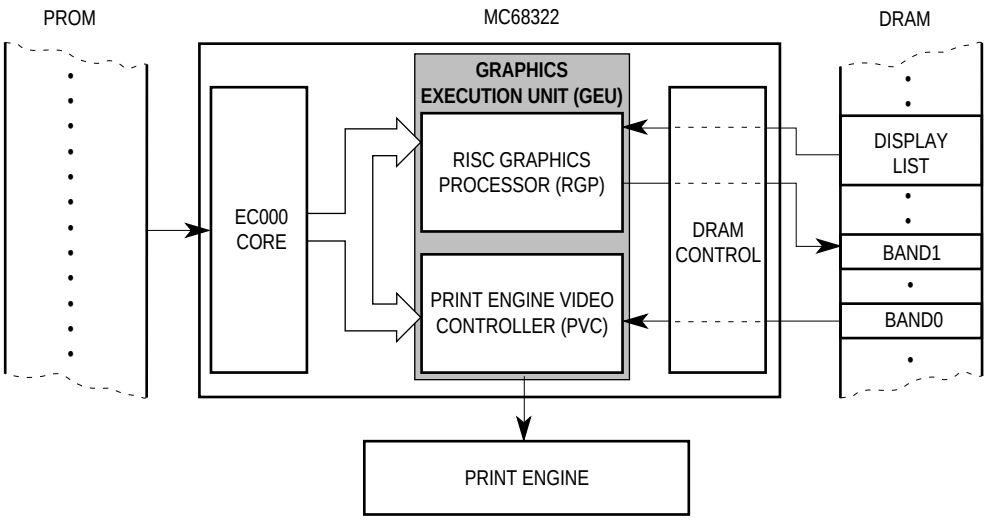

Figure 3. MC68322 Functional Block Diagram

RISC GRAPHICS PROCESSOR (RGP)

The RGP is a high-performance bit-image processor optimized for the 16-bit DRAM interface on the MC68322. The RGP achieves performance levels that enable the MC68322 to be used effectively in banding applications or in other high-speed or high-density bit-mapped graphics products. The RGP is comprised of several major blocks: graphic order parser, graphic order execution unit, write back logic and band control registers. The software interface to the RGP consists of three registers: RGP start register (RSR), RGP diagnostic register (RDR), and the RGP interrupt event register (RIER).

The RGP is activated when the EC000 Core writes the starting address of a display list into the RSR. A display list is a list of special instructions called graphic orders. The RGP executes these graphic orders to

render a page or band image. When the end of the display list is reached, the RGP generates an interrupt and waits for another display list address. The RSR is double buffered so a second display list address can be loaded while the RGP is working on the first display list. Upon completion of the first display list, an interrupt is generated and the second display list begins executing immediately.

The RGP can render an entire page from a display list or multiple bands from a single banded display list. A banded display list contains band information near the beginning of the display list. This band information includes the address and size of the band as well as the band number that is to be processed. The RGP uses this information to determine which orders from the display list to process and where in memory to create the bit map image for this specific band. The write back logic of the RGP automatically updates any graphic orders that cross band boundaries in order to prepare them for execution during rendering of the following band. This is done without any intervention from software running on the EC000 Core. After one band is fully rendered and the RGP generates an interrupt, software simply adjusts the display list to reflect the next band information and then restarts the RGP.

PRINT ENGINE VIDEO CONTROLLER (PVC)

The PVC is started by loading a set of registers, known as the printer control block (PCB) with the dimensions and location of the print image. When the last register is loaded, the PVC fetches the first page band image data from memory and waits for the print engine to signal start-of-page via frame synchronize ($\overline{\text{FSYNC}}$). When $\overline{\text{FSYNC}}$ is detected, the PVC generates a band begin interrupt and transmits the page image video data to the print engine. When the entire page band image is transmitted, a page end interrupt is generated allowing software to reclaim the image memory space.

The MC68322 contains a generic non-impact printer video interface, suitable for virtually all printers currently on the market. The video interface supports most laser printer and various inkjet interfaces. The PVC moves rasterized data from DRAM to the video port automatically. A digital phase locked loop is provided for those printers that do not supply a video clock source. The generic video interface consists of the I/O signals defined in Table 4.

Table 4. MC68322 PVC I/O Signals

Signal	I/O	Description
$\overline{\text{PRINT}}$	O	Print Request requests a page to be printed.
$\overline{\text{FSYNC}}$	I	Frame Sync indicates the top of the page in response to a print request.
$\overline{\text{LSYNC}}$	I	Line Sync indicates the left edge of the page.
$\overline{\text{VIDEO}}$	O	Video is the digital serial video image.
$\overline{\text{VCLK}}$	I	Video Clock is used to shift the video image (either from the printer, or an 8x clock used for the digital phase locked loop).

PRINTER COMMUNICATION INTERFACE

The MC68322 provides signals for printer communications interfacing to 8-bit synchronous full duplex interface printers. Interrupts, if enabled, indicate when a serial command has been sent or a serial status has been received. For synchronous operation, the signals are defined in Table 5.

Table 5. MC68322 Printer Communications Interface I/O Signals

Signal	I/O	Description
$\overline{\text{CBSY}}$	O	Command busy indicates that a command will be sent to the printer.
$\overline{\text{SBSY}}$	I	Status busy indicates the printer is ready to receive status.
$\overline{\text{CMD}}/\overline{\text{STS}}$	I/O	Command/Status Data is the synchronous command data out to the printer, or the bi-directional command/status data to/from the printer.
$\overline{\text{STS}}$	I	Status Data is the synchronous status data from the printer.
$\overline{\text{CCLK}}$	I/O	Command Clock is the command/status clock to/from the printer.

The MC68322 contains two 8-bit registers for synchronous communications, a command register and a status register. When the command register is written, the $\overline{\text{CBSY}}$ signal is brought active and the command data is sent as a serial stream on the $\overline{\text{CMD}}$ line with $\overline{\text{CCLK}}$ toggling high-to-low and low-to-high once per command bit. When the print engine is ready to respond with status, it does so by activating the $\overline{\text{SBSY}}$ signal. This causes the MC68322 to toggle $\overline{\text{CCLK}}$ high-to-low and low-to-high eight times (once per status bit) and assemble serial data from the $\overline{\text{STS}}$ line into the status register.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules and typical glue logic. The MC68322 has five modules to assist the EC000 Core and GEU. These five modules are the bus interface unit (BIU), system integration module (SIM), DRAM system integration module (DSIM), general purpose direct memory access (DMA) controller, and parallel port interface (PPI).

BUS INTERFACE UNIT (BIU)

The dual bus architecture of the MC68322 allows the printing workload to be distributed among processing units and executed in parallel. Because studies have shown that 70% of all MC68000 bus accesses are instruction fetches, the MC68322 has been designed so that the EC000 Core bus traffic to DRAM is less than 30% of all EC000 bus accesses.

The BIU allows the EC000 Core and GEU, which reside on separate bus structures, to function independently by handling general purpose DMA, and EC000 Core accesses to DRAM. The EC000 Core can perform instruction and PROM data fetches without impacting GEU bus operations. However, the GEU has a higher priority than the EC000 Core for DRAM accesses in order to print pages correctly.

The BIU, in conjunction with the SIM, also allows SRAM to be added to the EC000 Core bus for system stack space, temporary data storage, or as a buffer for peripheral data.

SYSTEM INTEGRATION MODULE

The SIM provides the ROM, PROM, and I/O chip selects. It contains eight chip selects that can be programmed to decode the address and internally supply the $\overline{\text{DTACK}}$ after the appropriate number of wait states. Each chip select can be programmed to support up to 64 Mbytes of address space.

CHIP-SELECT BANKS AND REGISTERS

The eight chip-selects directly support ROM, PROM and I/O chip-select banks. Each ROM or I/O bank is pointed to by a corresponding chip-select register through the base address field. These eight chip-select

banks are individually programmable for an address range of 256 Kbytes to 64 Mbytes.

Each ROM or I/O bank can be a different size or disabled. On reset, chip-select bank 0 is set to 8 Mbytes and chip-select banks 7 through 1 are disabled. They can also be individually located anywhere within the 256 Mbyte memory map and can be contiguous or disjoint, as required by the operating environment.

The chip-selects for each bank can be selected to provide a wide range of timing parameters. The timing parameters that can be programmed are set up time, access time, hold time, and recovery time for both reads and writes. The SIM on the MC68322 provides internal bus cycle auto-acknowledge and wait states, which can be inserted as required.

DRAM SYSTEM INTEGRATION MODULE (DSIM)

A fully integrated bursting DRAM controller is on-chip to provide a cost-effective and efficient DRAM interface to the MC68322. The DRAM controller has six $\overline{RAS}$ signals to provide for multiple DRAM banks of different sizes. With six $\overline{RAS}$ signals, multiple banks of DRAM can be supported to allow end users to add DRAM SIMM modules for more expandability. The DRAM controller also has upper and lower $\overline{CAS}$ signals to perform DRAM byte selects. A CAS before RAS refresh is programmable along with bank sizes and access timer. The DRAM controller multiplexes addresses to provide up to 8 Mbytes of DRAM address space per bank. Additionally, the DRAM controller provides a separate 16-bit DRAM data path and a write enable signal for a glueless DRAM interface.

DRAM BANKS AND REGISTERS

The MC68322 directly supports up to six DRAM banks with a bursting read and write interface. Each DRAM bank is pointed to by a corresponding DRAM register through the base address field. Each DRAM register contains a base address field containing the internal address bits A27–A19 in the DRAM bank's starting address. These six DRAM banks can be contiguous or disjoint as required by the operating environment.

DRAM sizes are programmed through encoding the size fields of each DRAM register. The MC68322 allows for up to 8 Mbytes of DRAM in each of the eight banks. The timing parameters for each DRAM bank are preprogrammed to provide a 2, 3, or 4 clock access. On reset, all DRAM banks are disabled.

DRAM REFRESH

Refresh cycles are carried out with CAS before RAS refresh cycles. DRAMs that support CAS before RAS refresh contain an internal row address counter, which is automatically selected and incremented when the $\overline{CAS}$ signal is asserted, and followed by asserting the $\overline{RAS}$ signal. The DRAM refresh rate is fully programmable. The DRAM controller performs refreshes from system reset until the DRAM controller is initialized.

GENERAL PURPOSE DMA CONTROLLER

The MC68322 has a single-ended general purpose DMA controller integrated on-chip. The DMA can be programmed to transfer data from a high-speed I/O peripheral to DRAM with minimal intervention from the EC000 Core.

PARALLEL PORT INTERFACE (PPI)

The MC68322 contains a direct, IEEE 1284 Level 2 compliant, bi-directional 8-bit PPI. The PPI supports four IEEE 1284 communications modes: compatibility (Centronics), nibble, byte, and enhanced capabilities port (ECP). It also fully supports all variants of these modes, including device ID requests and run-length encoded data compression.

The PPI contains specialized hardware to provide automatic handshaking during forward data transfers. When hardware handshaking is used in conjunction with the parallel port's dedicated DMA controller, transfer rates as high as 2 Mbytes/sec can be achieved in the ECP forward mode. The hardware handshaking can also be completely disabled to allow software to directly control the parallel port interface signals and to support new protocols. Control and data signals are brought out to provide a glueless interface to the parallel port.

The following table identifies the operating frequency, voltage, and available package type for the MC68322.

MC68322 Package/Frequency Availability

Package	16 MHz –5 V	20 MHz–5 V
Plastic Quad Flat Pack (FT)		

The documents listed in the following table contain detailed information on the MC68322. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Title	Order Number
M68000 Family Programmer's Reference Manual	M68000PM/AD
The 68K Source	BR729/D
MC68322 User's Manual	MC68322UM/AD

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.