hmp

32K x 32 EEPROM MODULE

PUMA 2E1000-70/90/12

HMP Ltd, West Chirton, North Shields, Tyne & Wear NE29 8SE England
Tel. (+44) 191 293 0500 Fax. (+44) 191 259 0997

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Description

The PUMA 2E1000 is a 1Mbit High Speed EEPROM module user configurable as 32Kx32, 64Kx16 or 128Kx8.

Available with access times of 70, 90 & 120ns the device has an industry standard ceramic 66 pin P.G.A footprint.

The device features byte and page write facility, 10,000 Write Erase cycle capability and data retention time of 10 years.

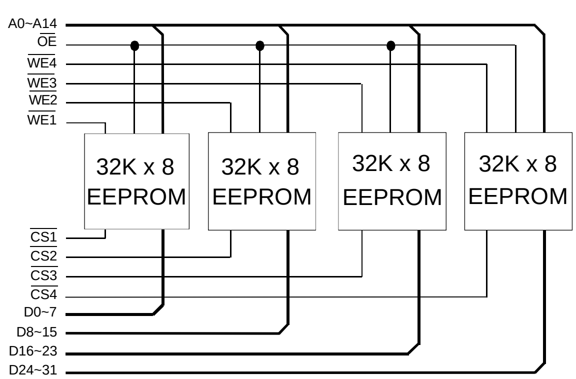
The device may be screened in accordance with MIL-STD-883

1,048,576 bit CMOS High Speed EEPROM

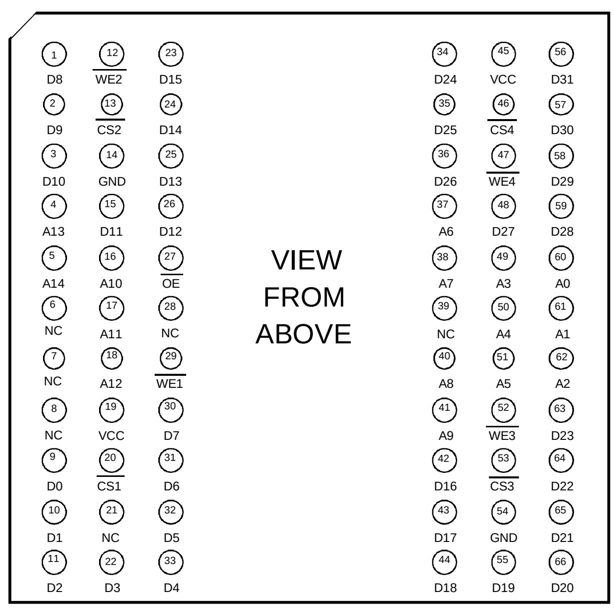
Features

Very Fast access times of 70/90/120 ns.
User Configurable as 8 / 16 / 32 bit wide.
Upgradeable footprint.
Operating Power 1760 mW (max).
Standby Power 1320 mW (max).
Package Suitable for Thermal Ladder Applications.
Single byte and Page Write operation.
DATA Polling and Toggle Bit for End of Write Detection.
Hardware and Software Data Protection.
May be screened in accordance with MIL-STD-883.

Block Diagram



Pin Definition



Pin Functions

A0-14	Address Inputs	**D0-31**	Data Inputs/Outputs
CS1-4	Chip Select	**OE**	Output Enable
WE1-4	Write Enable	**NC**	No Connect
V_{CC}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings [(1)]

Temperature Under Bias	T_{BIAS}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
All input voltages (including N.C. pins) with Respect to GND	V_T	-0.6 to +6.25	V
All output voltages with respect to GND	V_{OUT}	-0.6 to V_{CC} +0.6	V
Voltage on $\overline{OE}$ and A9 with Respect to GND	V_{OEA}	-0.6 to +13.5	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated below is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Operating Temp Range	T_A	0	-	70	˚C
	T_{AI}	-40	-	85	˚C (2E1000I)
	T_{AM}	-55	-	125	˚C (2E1000M, MB)

DC Electrical Characteristics (V_{CC}=5.0V±10%, T_A=-55 to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current Address, $\overline{OE}$	I_{LI1}	0V ≤ V_{IN}≤ V_{CC}+1V	-	-	40	µA
$\overline{CS1\sim4}$, $\overline{WE1\sim4}$	I_{LI2}	As above.	-	-	10	µA
Output Leakage Current	I_{LO}	$\overline{CS1\sim4}$=V_{IH}, $V_{I/O}$=GND to VCC	-	-	40	µA
Operating Supply Current	I_{CC32}	f=5MHz, $I_{I/O}$=0mA	-	-	320	mA
Standby Supply Current	I_{SB1}	2.0V≤$\overline{CS1\sim4}$≤V_{CC}+1V	-	-	240	mA
Output Low Voltage	V_{OL}	I_{OL} = 6.0mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

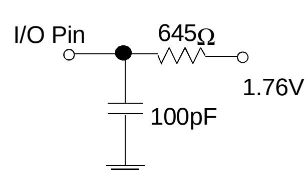
Capacitance (V_{CC}=5V±10%,T_A=25˚C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	26	34	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V, 8 bit mode	42	58	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Test Load



AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	-70 min	-70 max	-90 min	-90 max	-12 min	-12 max	Unit
Read Cycle Time	t_{RC}	-	70	-	90	-	120	ns
Address to Output Delay	t_{ACC}	-	70	-	90	-	120	ns
$\overline{CS1\sim4}$ to Output Delay[1]	t_{CS}	-	70	-	90	-	120	ns
$\overline{OE}$ to Output Delay [2]	t_{OE}	0	40	0	45	0	50	ns
CS1~4 or $\overline{OE}$ to Output Float [3,4]	t_{DF}	0	40	0	45	0	50	ns
Output Hold from $\overline{OE}$, CS1~4 or Address, (whichever occured first)	t_{OH}	0	-	0	-	0	-	ns

Notes: (1) $\overline{CS1\sim4}$ may be delayed up to t_{ACC} - t_{CS} after the address transition without impact on t_{ACC}.
(2) $\overline{OE}$ may be delayed up to t_{CS} - t_{OE} after the falling edge of $\overline{CS1\sim4}$ without impact on t_{CS} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
(3) t_{DF} is specified from $\overline{OE}$ or $\overline{CS1\sim4}$ whichever occurs first (C_L = 5pF).
(4) This parameter is only sampled and is not 100% tested.

Write Cycle

Parameter	Symbol	min	typ	max	Unit
Address, $\overline{OE}$ Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE1\sim4}$ or $\overline{CS1\sim4}$)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, $\overline{OE}$ Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Time to Data Valid	t_{DV}	NR[1]	-	-	ns

Note: (1) NR = No Restriction

Page Mode Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	5	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte/Word Load Cycle Time	t_{BLC}	-	-	150	µs
Write Pulse Width High	t_{WPH}	50	-	-	ns

See notes on page 6, Mode Write Waveform.

$\overline{DATA}$ Polling Characteristics

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	0	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{OE}$ to Output Delay[1]	t_{OE}				ns
Write Recovery Time	t_{WR}	0	-	-	ns

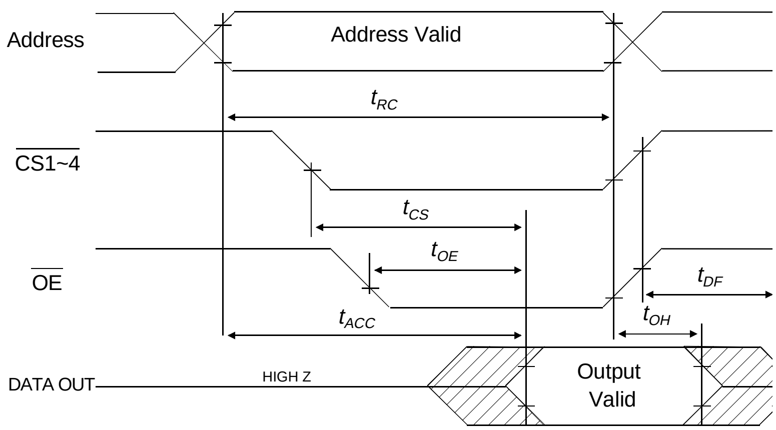
Note : (1) See AC Read Characteristics.

Toggle Bit Characteristics (1,2,3,4)

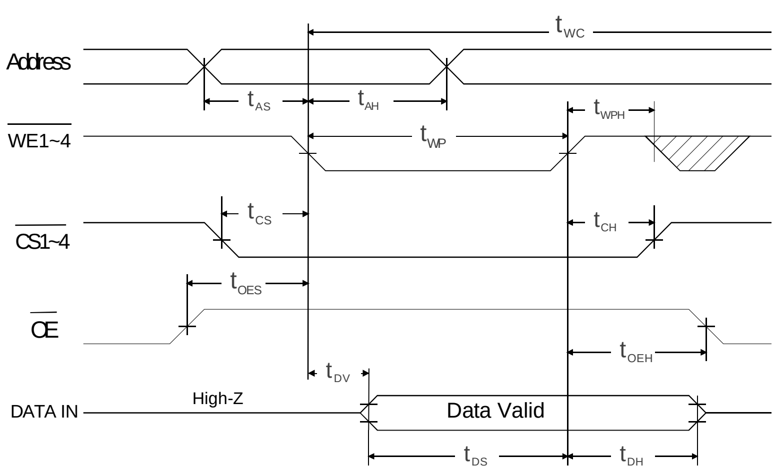
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Data Hold Time	t_{DH}	10	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns
$\overline{OE}$ to Output Delay (1)	t_{OE}				ns
OE High Pulse	t_{OEHP}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) See AC Read Characteristics.
(2) Toggling either $\overline{OE}$ or $\overline{CS1\sim4}$, or both $\overline{OE}$ and $\overline{CS1\sim4}$ will operate toggle bit.
(3) Beginning and ending state of D6 will vary.
(4) Any address location may be used but the address should not vary.

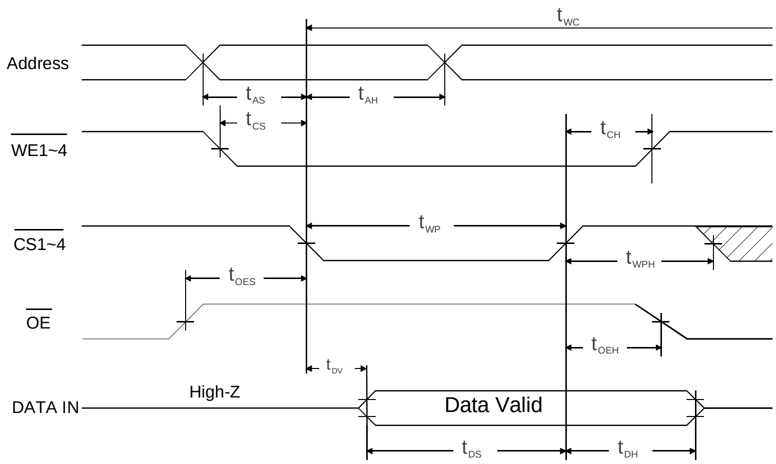
Read Cycle Timing Waveform (1,2,3,4)



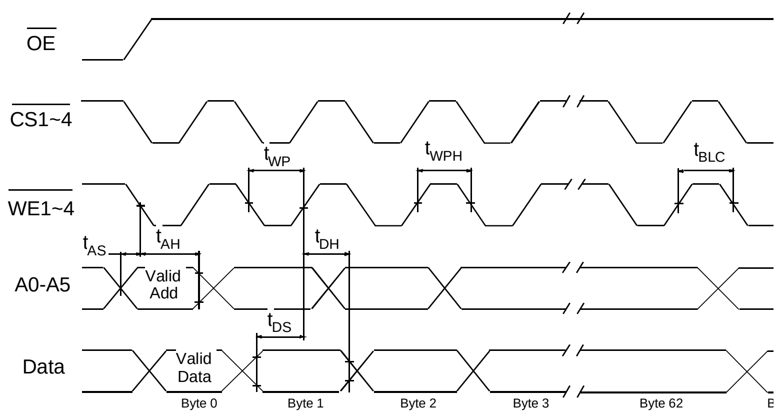
AC Write Waveform - $\overline{WE1\sim4}$ Controlled



AC Write Waveform - $\overline{\text{CS1~4}}$ Controlled

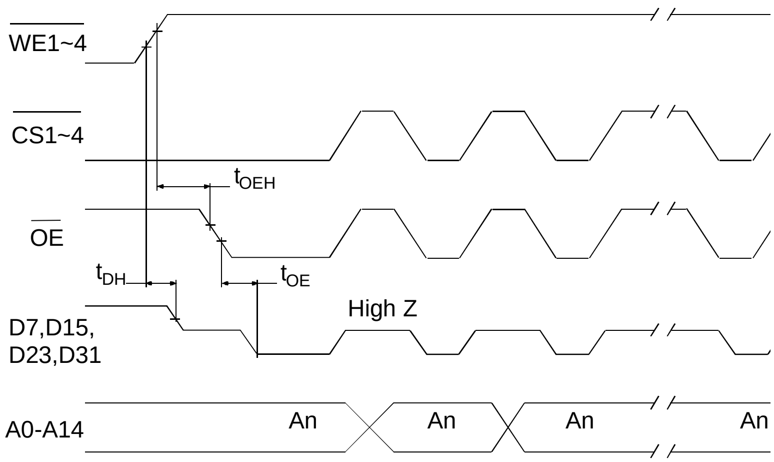


Page Mode Write Waveform [1,2]

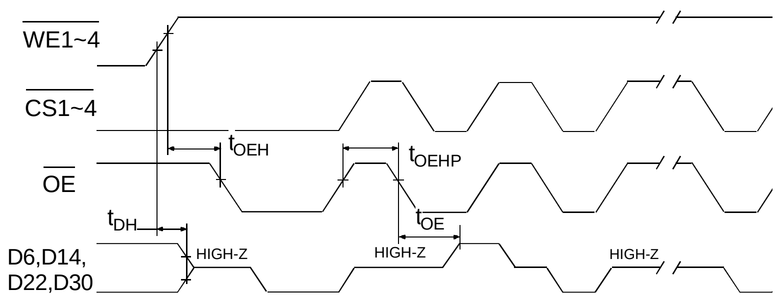


Note: (1) A6 through A14 must specify the page address during each high to low transition of $\overline{\text{WE1~4}}$ (or $\overline{\text{CS1~4}}$).
(2) $\overline{\text{OE}}$ must be high only when $\overline{\text{WE1~4}}$ and $\overline{\text{CS1~4}}$ are both low.

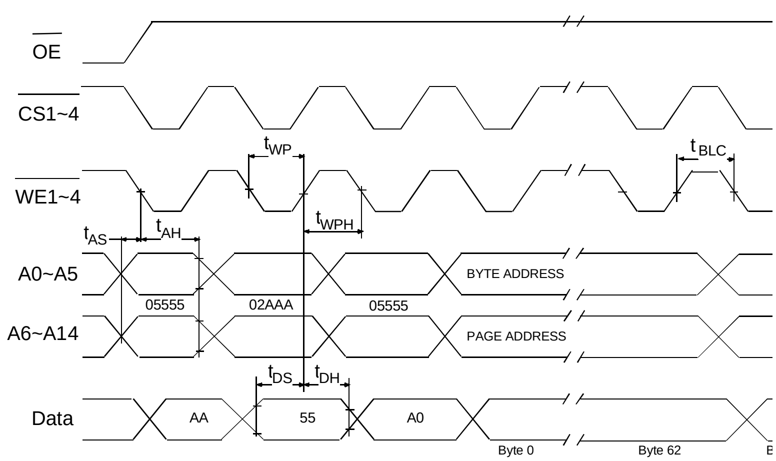
$\overline{\text{DATA}}$ Polling Waveform (1)



Toggle Bit Waveform (1,2,3,4)

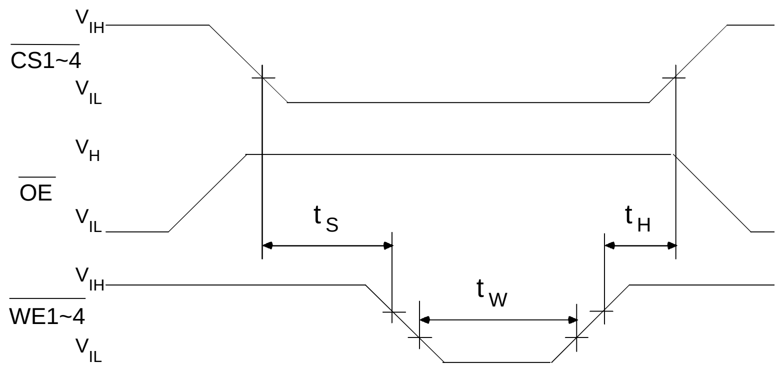


Software Protected Write Waveform (1,2)



Notes: (1) A6 through A14 must specify the page address during each high to low transition of $\overline{\text{WE1\textasciitilde4}}$ (or $\overline{\text{CS1\textasciitilde4}}$).
(2) $\overline{\text{OE}}$ must be high only when $\overline{\text{WE1\textasciitilde4}}$ and $\overline{\text{CS1\textasciitilde4}}$ are both low.

Chip Erase Waveform



$t_S = t_H = 5\mu s$ (min) $t_W = 10$ ms (min) $V_H = 12V \pm 0.5V$

Device Operation

Where references are made to byte/word operations, the user will control the memory configuration of 8, 16, or 32 bits wide using $\overline{CS1\sim4}$.

Read

The PUMA 2E1000 read operations are initiated by both Output Enable and Chip Select(s) LOW, while Write Enable(s) is HIGH. The read operation is terminated by either Chip Select(s) or Output Enable returning HIGH. This dual-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impendence state when either Output Enable or Chip Select is HIGH.

Write

Write operations are initiated when both Chip Select(s) and Write Enable(s) are LOW and Output Enable is HIGH. The PUMA 2E1000 supports both a Chip Select(s) and Write Enable(s) controlled write cycle. That is, the address is latched by the falling edge of either Chip Select(s) or Write Enable(s), whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select(s) or Write Enable(s), whichever occurs first. A byte/word write operation, once initiated, will automatically continue to completion, within 10 ms max.

Page Mode Write

The page write feature of the PUMA 2E1000 allows the entire memory to be written in typically 5.12 seconds. Page Write allows 1 to 64 bytes/words of data to be written into the device during a single programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A6 through A14) for each subsequent valid write cycle to the part, during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte/word write cycle, the host can write up to 63 bytes/words in the same manner as the first byte/word written. Each successive byte/word load cycle, started by the Write Enable(s) HIGH to LOW transition, must begin within 150 µs of the falling edge of the preceding Write Enable(s). If a subsequent Write Enable(s) HIGH to LOW transition is not detected within 150 µs, the internal automatic programming cycle will commence.

The A0 to A5 inputs are used to specify which bytes/words within the page are to be written. The bytes/words may be loaded in any order and altered within the same load period. Only bytes/words which are specified for writing will be written; unnecessary cycling of other bytes/words within the page does not occur.

$\overline{\text{DATA}}$ Polling

The PUMA 2E1000 features $\overline{\text{DATA}}$ Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte/word written will produce the complement of that data on D7. Once the programming is complete, D7 will refect the true data. Note: If the the PUMA 2E1000 is in a protected state and an illegal write operation is attempted $\overline{\text{DATA}}$ Polling will not operate. $\overline{\text{DATA}}$ Polling may begin at any time during the write cycle.

TOGGLE bit

In addition to $\overline{\text{DATA}}$ polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

Hardware Data Protection

The PUMA 2E1000 provides hardware features to protect non-volatile data from inadvertent writes.

- V_{CC} Sense - If V_{CC} is below 3.8V (typical) the write function is inhibited.
- V_{CC} Power-on-Delay - Once V_{CC} has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write.
- Write Inhibit - Holding any one of $\overline{OE}$ Low, $\overline{CS}$ High, $\overline{WE}$ High inhibits write cycles
- Noise Filter - Pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CS}$ inputs will not initiate a write cycle.

Software Data Protection

The PUMA 2E1000 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA 2E1000 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA 2E1000.

MODE	$\overline{CS1\sim4}$	$\overline{OE}$	$\overline{WE1\sim4}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	1	0	Data in
Standby/Write inhibit	1	X	X	High-Z
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	High-Z
Chip Erase (1)	0	1	0	High-Z

0 = V_{IL} : 1 = V_{IH} : X = V_{IH} or V_{IL}

Notes : (1) $\overline{OE}$ must be 12.0V ± 0.5V

Device Indentification

An extra 64 bytes of EEPROM memory are avaliable to the user for device identification, accessed by placing 12V±0.5V on A9 and using locations $7FC0_H$ to $7FFF_H$. These locations can be used during the initial programming of each EEPROM to record data such as issue number and release date, and subsequent reprogramming can change these locations to record the alterations performed.

Chip Erase

All of the memory locations on the PUMA 2E1000 can be erased in 10 ms by placing 12.0V±0.5V onto $\overline{OE}$ and controlling $\overline{WE1\sim4}$ and $\overline{CS1\sim4}$ to follow the Chip Erase timing characteristics. This function will operate even if the module is in Software Data Protection Mode as explained later.

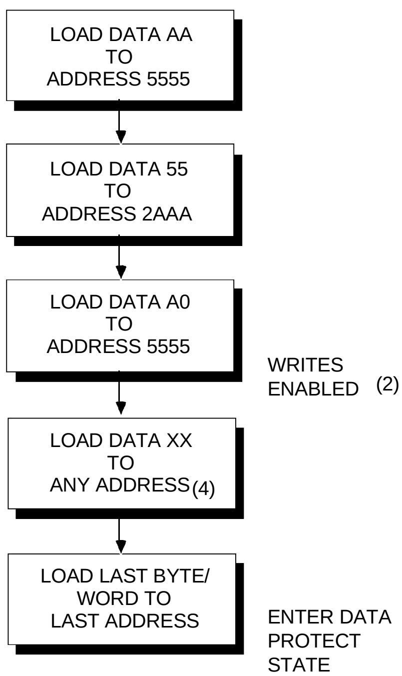
Software Data Protection

Software controlled data protection, once enabled by the user, necessitates the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of 3 Writes to 3 specific addresses must be performed, and must be reused for each subsequent Write cycle. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

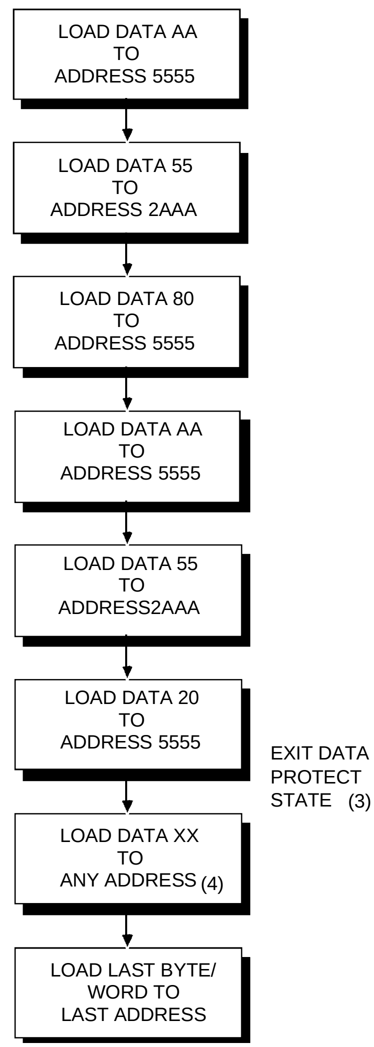
Note that the PUMA 2E1000 is supplied with the Software data Protection feature **disabled**.

The algorithms to enable and disable the protection are shown below:

SDP Enable



SDP Disable



Once initiated, the enable sequence of write operations should not be interrupted

Notes :
(1) Data D7 - D0 (hex); Address A14 - A0 (hex).
(2) Write Protect Mode will be activated at end of Write even if no other data is loaded.
(3) Write protect state will be disabled at end of write period even if no other data is loaded.
(4) 1 to 64 bytes/words of data can be loaded.

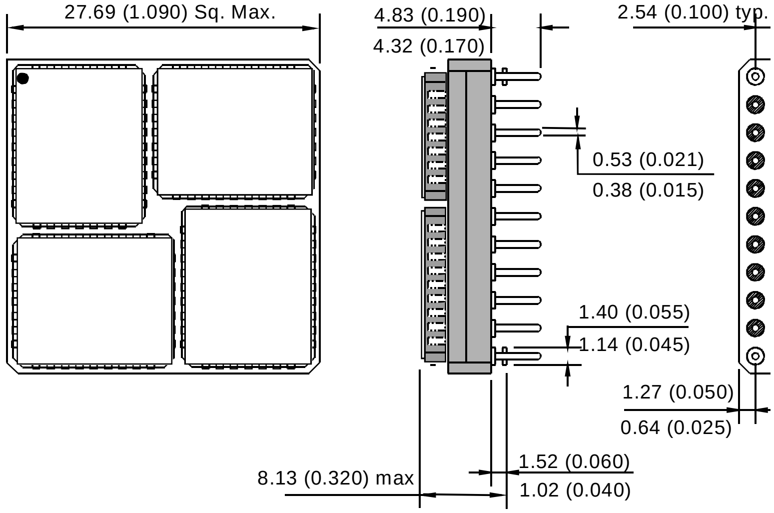
Note: Load Data above represents 8 bit mode. For 16 or 32 bit mode, place the load data in the 2 bytes or all 4 bytes on the data lines, respectively. Eg/ 8 bit load data = 55_{HEX}, 16 bit load data = 5555_{HEX}.

All software write commands must obey the Page Write timing specifications.

The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes/words must be loaded to specific locations in the EEPROM as shown.

Note here the use of the word 'load' to describe enabling and disabling the protection modes in preference to 'write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes/ words at those addresses will be overwritten with AA,55,A0, this is not the case.

Package Details Dimensions in mm (inches).



Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883 method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65˚C to +150˚C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25˚C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125˚C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25˚C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2E1000MB-70

Speed	70	=	70 ns
	90	=	90 ns
	12	=	120 ns
Temp. range/screening	Blank	=	Commercial Temp.
	I	=	Industrial Temp.
	M	=	Military Temp.
	MB	=	Screened in accordance with MIL-STD-883
Memory Type	E1000	=	EEPROM (Configurable as 32Kx32, 64Kx16 or 128Kx8)

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed at any time without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.