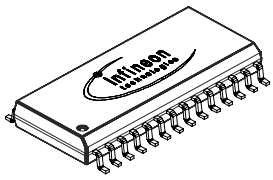
Fault Tolerant CAN - LDO TLE 6262 G

Final Data Sheet

1 Overview



P-DSO-28-6
Enhanced Power

1.1 Features

- Standard fault tolerant differential CAN-transceiver (TLE6254 LS CAN cell)
- Bus failure management
- Low power mode management
- CAN data transmission rate up to 125 kBaud
- Low-dropout voltage regulator 5V ± 2%
- Two Low Side Switches
- Three High Side Switches
- Power on and under-voltage reset generator
- Vcc supervisor
- Window watchdog
- Programable time base
- Integrated fail-safe mechanism
- Standard 16 bit SPI-Interface
- Wide input voltage and temperature range
- Enhanced power P-DSO-Package

Type	Ordering Code	Package
TLE 6262 G	on request	P-DSO-28-6

Description

The TLE 6262 G is a monolithic integrated circuit in a P-DSO-28-6 package, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a 16 bit SPI interface to control and monitor the IC. Further there are integrated three high side switches, two low side switches, a window watchdog circuit and a reset circuit. Both, the window watchdog and reset function are referring to a time base that is programmable via an external resistor.

The IC is designed to withstand the severe conditions of automotive applications.

1.2 Pin Configuration

(top view)

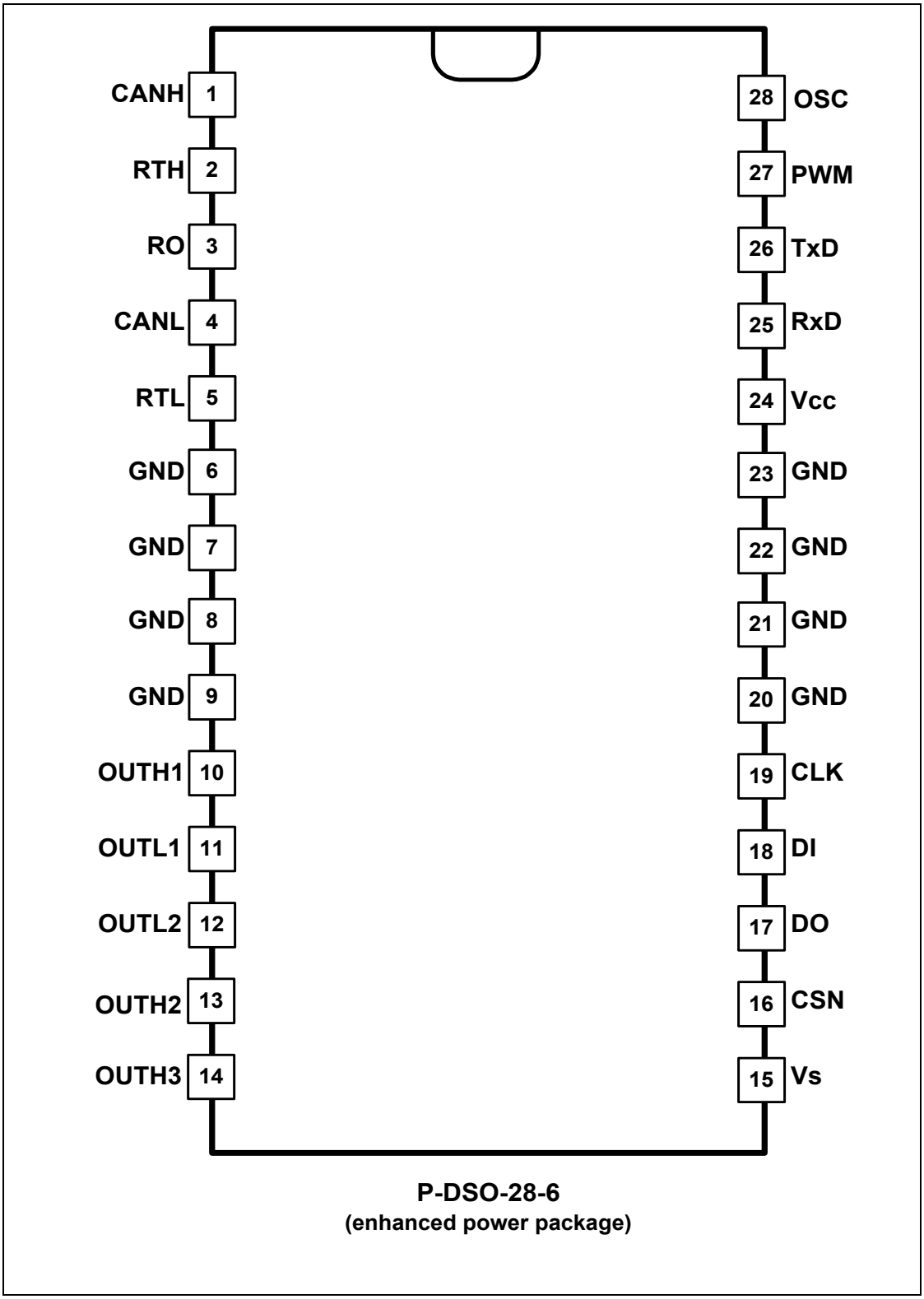


Figure 1

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	CANH	**CAN-H bus line**; HIGH in dominant state
2	RTH	**Termination input** for CANH
3	RO	**Reset output**; open drain output; integrated pull up; active low
4	CANL	**CAN-L bus line**; LOW in dominant state
5	RTL	**Termination input** for CANL
6, 7, 8, 9, 20, 21, 22, 23	GND	**Ground**; to reduce thermal resistance place cooling areas on PCB close to this pins.
10	OUTH1	**High side output 1**; controlled via PWM input and/or SPI input, short circuit protected
11	OUTL1	**Low side output 1**; SPI controlled, with active zener
12	OUTL2	**Low side output 2**; SPI controlled, with active zener
13	OUTH2	**High side output 2**; SPI controlled
14	OUTH3	**High side output 3**; SPI controlled, in low power mode controlled by internal autotiming function if selected
15	V_S	**Power supply**; block to GND directly at the IC with ceramic capacitor
16	CSN	**SPI interface chip select not**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs
17	DO	**SPI interface data out**; this tristate output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see **table 3** for diagnosis protocol
18	DI	**SPI interface data in**; receives serial data from the control device; serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) being transferred first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **table 2** for input data protocol
19	CLK	**SPI interface clock input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs

1.3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
24	V_{CC}	**Output voltage regulator**; 5V logic supply, block to GND with an 100nF external ceramic capacitor directly at the IC + external capacitor $C_Q \geq 22$ µF
25	RxD	**CAN Receive data output;**
26	TxD	**CAN Transmit data input;** integrated pull up
27	PWM	**Pulse width control**; for high side switch 1
28	OSC	**Oscillator input**; time base for power on reset, watchdog window and stand by timer for HS3, to program connect external resistor to GND

1.4 Functional Block Diagram

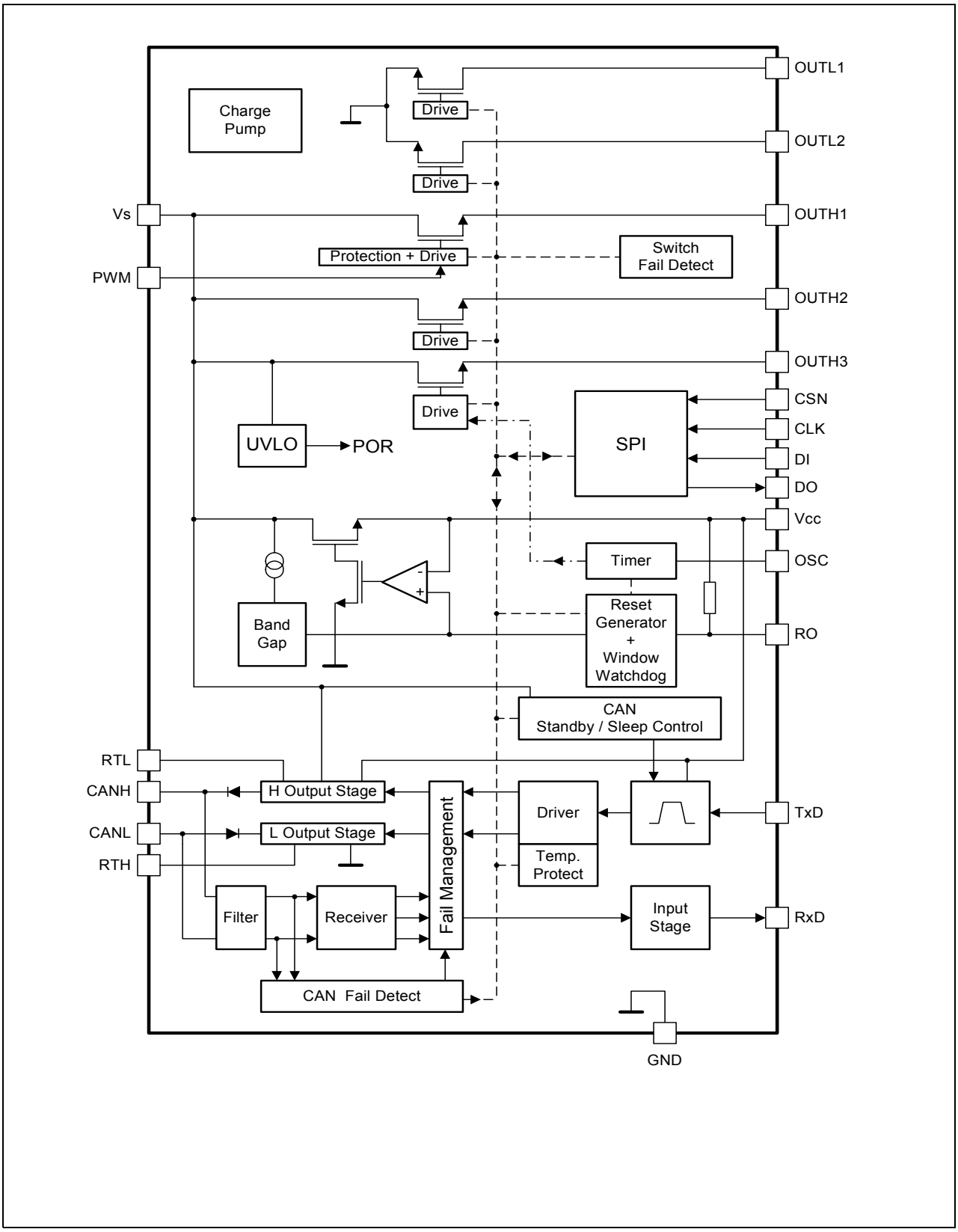


Figure 2

1.5 Circuit Description

The TLE 6262 G is a monolithic IC, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a SPI interface to control and monitor the IC. Further there are integrated three high side switches, two low side switches, a window watchdog circuit and a reset circuit. Both, the window watchdog and reset function are referring to a time base that is programmable via an external resistor.

Figure 2 shows a block schematic diagram of the **TLE 6262 G**

Table 1: mode truth table

Feature	normal mode	Receive-only mode	V_{BAT} stand-by mode
V_{CC}	ON	ON	ON
Reset	ON	ON	ON
Watchdog	ON[1)]	ON[1)]	ON[1)]
SPI	ON	ON	ON
CAN transmit	ON	OFF	OFF
CAN receive	ON	ON	OFF[2)]
OUTHS 1[3) 4) 5)]	ON	ON	ON
OUTHS 2[3) 5)]	ON	ON	ON
OUTHS 3[3) 5)]	ON	ON	ON
OUTHS3-auto timing[3) 5)]	OFF	ON	ON
OUTLS 1[3) 6)]	ON	ON	ON
OUTLS 2[3) 6)]	ON	ON	ON

[1)] at low V_{CC} output current only active when watchdog undercurrent function is not activated

[2)] a bus wake-up is monitored by setting the RxD output low

[3)] only active when selected via SPI

[4)] also active when driven via the PWM input

[5)] automatically disabled when a reset occurs

[6)] automatically disabled when a reset or watchdog reset respectively, occurs or the watchdog is disabled by the undercurrent function

CAN Transceiver

The TLE 6262 is optimized for low speed data transmission up to 125 kbaud in automotive applications. Normally a differential signal is transmitted or received respectively. When a bus wiring failure (see **table 4**) is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Therefore it is equipped with one differential receiver and four single ended comparators (two for each bus line). To avoid false triggering by external RF influences the single wire modes are activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay. The bus failures are monitored via the diagnosis protocol of the SPI. Therefore it is possible to distinguish 6 CAN bus failures or failure groups on the bits 8 to 13 (see **table 3**).

To reduce EMC caused by the transceiver the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (bus-failure) the EMC performance of the system is degraded from the differential mode.

The differential receiver threshold is set to typ. -2.8 V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2, 3a and 4 with a noise margin as high as possible. When one of the bus failures 3, 5, 6, 6a, and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and output stage.

The CAN-transceiver offers three different operation modes that are controlled via the SPI: the normal operation mode, Receive-only mode and V_{bat} stand-by mode. Please see the state diagram (**figure 3**). In the V_{bat} stand-by mode the RTL output voltage is switched to V_S.

In case of a wake-up via the bus lines or one of the bus lines respectively, the TLE 6262 automatically sets the RxD output LOW. To send respectively receive messages the CAN-transceiver can now be set in normal operation mode or receive-only mode by the microcontroller.

When a reset occurs the transceiver circuit is automatically switched to V_{bat}-stand-by mode because the SPI input bits are automatically set LOW for this event.

A thermal shutdown of the CAN-transceiver circuit is monitored via the SPI diagnosis bit 15.

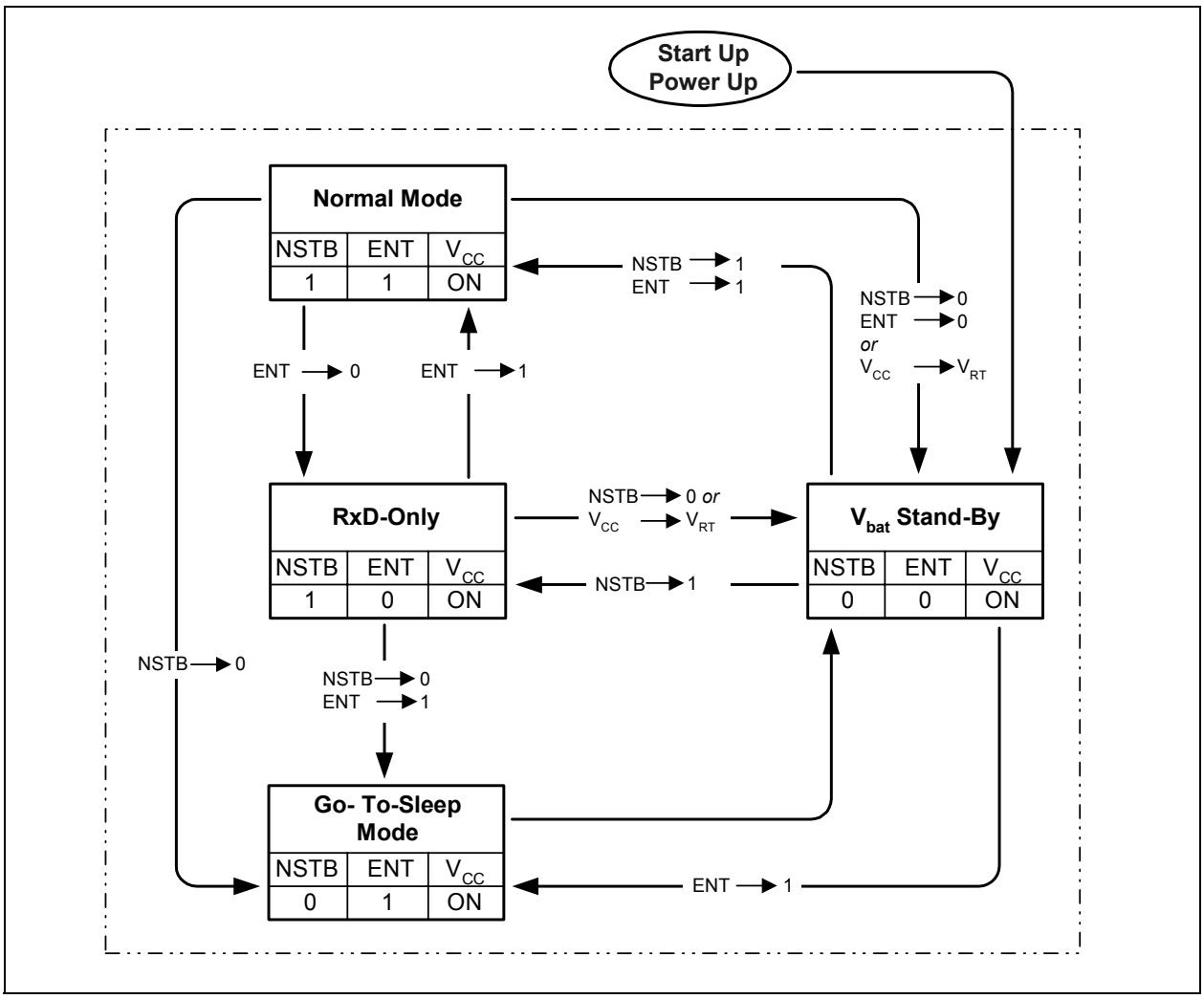


Figure 3: State Diagram

Low Dropout Voltage Regulator

The TLE 6262 is able to drive external 5V loads up to 45 mA. Its output voltage tolerance is less than ± 2%. In addition the regulator circuit drives the internal loads like the CAN-transceiver circuit.

An external reverse current protection is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_{VCC} \geq 100$ nF. Nevertheless a lot of applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or negative transients. Furthermore the due function of e.g. the reset and 3V-supervisor circuit are supported by a larger output capacitance because of their reaction times. Therefore a output capacitance $C_{VCC} \geq 10$ µF is recommended.

SPI (serial peripheral interface)

The 16-bit wide programming word or input word (see table 1) is read in via the data input DI, and this is synchronized with the clock input CLK supplied by the µC. The diagnosis word appears synchronously at the data output DO (see **table 3**).

The transmission cycle begins when the chip is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point.

For details of the SPI timing please refer to **figure 3 to 7**.

Oscillator

All internal delay times are referring to the internal oscillator frequency, which is set by an external resistor from pin OSC to GND. The oscillator frequency and the resulting internal cycling time can be calculated by the equations:

$$f_{OSC} = \frac{28,45 \times 10^{9}\,[\mathrm{Hz}\Omega]}{R_{OSC}}$$

$$t_{CYL} = \frac{32}{f_{OSC}}$$

Window Watchdog, Reset and 3V-Supervisor

When the output voltage V_{CC} exceeds the reset threshold voltage V_{RT} the reset output RO is switched HIGH after a delay time of 16 cycles. This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an under-voltage condition of the output voltage ($V_{CC} < V_{RT}$) appears, the reset output RO is switched LOW again. The LOW signal is guaranteed down to an output voltage $V_{CC} \geq 1V$. Please refer to **fig.11**, reset timing diagram.

Should the output voltage fall short of the 3V-supervisor threshold V_{ST} an internal flip-flop is set LOW. The SPI diagnosis bit 7 monitors this. In normal operation this flip-flop has to be activated via the SPI input bit 7. This feature is useful e.g. to monitor that the RAM data of the microcontroller might be damaged or the application is connected to V_S the first time.

After the above described delayed reset (LOW to HIGH transition of RO) the window watchdog circuit is started by opening a long open window of 32 cycles. Now the microcontroller has to service a watchdog trigger signal via the SPI interface (input bit 0). A watchdog trigger is detected as a falling edge by sampling for 2 cycles a HIGH followed by 2 cycles LOW of the SPI input bit 0. The long open window ensures a simple and fast

synchronization of the TLE 6262 watchdog timing to the watchdog services of the microcontroller.

After the first trigger the watchdog has to be serviced by meeting an open window of 20 cycles that follows a closed window of 12 cycles. A correct watchdog service immediately results in starting the next closed window. Please refer to **fig. 10**, watchdog timing diagram.

If the trigger signal does not meet the open window (trigger to early or to late) the reset output RO is set LOW for a period of 4 cycles. Afterwards a long open window is started again. In addition, the SPI diagnosis bit 2 is set HIGH to monitor a watchdog reset.

Both, the undervoltage reset and the watchdog reset are setting all SPI input bits LOW.

To avoid a cyclic wake-up of the microcontroller in low power mode (sleep mode) the watchdog circuit can be automatically disabled at low output currents ($I_{CC} < I_{CCWD}$). To activate this feature the SPI input bit 8 has to be set HIGH. In this under-current mode the low side switches are switched off automatically by the TLE 6262 to guarantee fail-save operation of the application. When the microcontroller returns back to normal mode ($I_{CC} > I_{CCWD}$) the first closed window is transformed to an open window so that the total open window time is 32 cycles. This ensures a more simple and fast synchronization of the TLE 6262 watchdog timing to the watchdog services of the microcontroller.

Flash program mode

To disable the watchdog feature a flash program mode is available. This mode is selected by applying a voltage of $6.8V < V_{PWM} < 7.2V$ at pin PWM. This is useful e.g. if the flash-memory of the micro has to be programmed and therefore a regular watchdog triggering is not possible. If the SPI is required in the flash program mode to change e.g. the mode of the TLE6262 the first input telegram has to be “00000000”.

High Side Switch 1

The high side output OUTH1 is able to switch loads up to 250 mA. Its on-resistance is 1.0 Ω typ. @ 25°C. This switch can be controlled either via the PWM input or the SPI input bit 1. When the input PWM is used it has to be enabled by setting the SPI input bit 11 HIGH. In case of both control inputs being active the PWM signal is masked by the SPI signal (see **fig. 8**, High Side Switch 1 Timing Diagram).

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 0 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6262 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. Further OUTH1 is protected against short circuit and overload. The SPI diagnosis bit 1 indicates an overload of OUTH1. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit.

This is flagged by the SPI diagnosis bit 3. Moreover the switches are disabled when a reset occurs.

High Side Switch 2

The high side output OUTH2 is able to switch loads up to 250 mA. Its on-resistance is 1.0 Ω typ. @ 25°C. This switch is controlled via the SPI input bit 2.

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 0 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6262 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI diagnosis bit 3. Moreover the switches are disabled when a reset occurs.

High Side Switch 3

The high side output OUTH3 is able to switch loads up to 150 mA. Its on-resistance is 1.5 Ω typ. @ 25°C. This switch is controlled via the SPI input bits 3 and 4. To supply external wake-up circuits in low power mode (sleep mode or Vbat-stand-by mode), the output OUTH3 can be periodically activated by the internal oscillator circuit. For activating this feature the SPI input bits 3 and 4 have to be set HIGH. The autotiming period is 128 internal cycle times; the on-time is 2 cycles. In case of a watchdog reset the autotiming period may be shorter.

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 0 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6262 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI diagnosis bit 3. Moreover the switches are disabled when a reset occurs.

Low Side Switches 1/2

The two low side outputs OUTL1 and OUTL2 are able to switch loads up to 100 mA. Their on-resistance is 1.5 Ω (typ.) @ 25°C. This switches are controlled via the SPI input bits 5 and 6. In case of high inrush currents a built in zener circuit (typ. 37 V) activates the switches to protect them.

The SPI diagnosis bit 14 monitors a thermal shutdown of the switches, whereas bit 0 flags a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6262 by switching off functions of minor priority before the temperature threshold of the thermal shutdown is reached. The SPI diagnosis bits 5/6

are giving a feedback about current status of OUTL1/OUTL2. As soon as the under-voltage condition of the supply voltage is met (V_S < V_{UVOFF}), the switches are automatically disabled by the under-voltage lockout circuit. This is flagged by the SPI diagnosis bit 3. In addition the outputs OUTL1 and OUTL2 are also disabled when the watchdog is switched off in undercurrent state or when a reset occurs.

Table 2

Input Data Protocol

BIT	
15	not used
14	not used
13	not used
12	not used
11	PWM Enable
10	CAN Enable Transmit
9	CAN Not Stand-By
8	Watchdog Control
7	Supervisor Enable
6	LS-Switch 2
5	LS-Switch 1
4	HS3 Auto Timing
3	HS-Switch 3
2	HS-Switch 2
1	HS-Switch 1
0	Watchdog Trigger

H = ON
L = OFF

Table 3

Diagnosis Data Protocol

BIT	
15	Thermal Shutdown Transceiver
14	Thermal Shutdown Switches
13	CAN Failure 2 and 4
12	CAN Failure 1 and 3a
11	CAN Failure 6
10	CAN Failure 6a
9	CAN Failure 6a, 5 and 7
8	CAN Failure 3
7	Vcc < 3V
6	Status LS2
5	Status LS1
4	not used
3	Vs Undervoltage Lockout
2	Window Watchdog Reset
1	Overload HS1
0	Temperature Prewarning

H = ON
L = OFF

Table 4

CAN bus line failure cases (according to ISO 11519-2)

failure #	**failure description**
1	CANL line interrupted
2	CANH line interrupted
3	CANL shorted to Vbat, CANL > 7.2 V
3a (no ISO failure)	CANL shorted to Vcc; 3.2 V < CANL < 7.2 V
4	CANH shorted to GND
5	CANL shorted to GND
6	CANH shorted to Vbat; CANH > 7.2 V
6a (no ISO failure)	CANH shorted to Vcc; 1.8 V < CANH < 7.2 V
7	CANL shorted to CANH

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	-0.3	28	V	–
Supply voltage	V_S	-0.3	40	V	t_p< 0.5s; t_p/T < 0.1
Regulator output voltage	V_{CC}	-0.3	5.5	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-10	28	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	-40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Logic input voltages (DI, CLK, CSN, OSC, PWM, TxD)	V_I	-0.3	V_{CC} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Logic output voltage (DO, RO, RxD)	$V_{DO/RO/RD}$	-0.3	V_{CC} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Termination input voltage (RTH, RTL)	$V_{TL/TH}$	-0.3	V_S +0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Electrostatic discharge voltage at pin CANH, CANL	V_{ESD}	-4000	4000	V	human body model; C = 100pF, R = 1.5kΩ
Electrostatic discharge voltage	V_{ESD}	-2000	2000	V	human body model; C = 100pF, R = 1.5kΩ
Currents					
Output current; Vcc	I_{CC}	–	–	A	internally limited
Output current; OUTH1	I_{OUTH1}	*)	0.3	A	*) internally limited
Output current; OUTH2	I_{OUTH2}	-0.7	0.3	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTH3	I_{OUTH3}	-0.5	0.2	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTL1	I_{OUTL1}	-0.2	0.4	A	t_p< 0.5s; t_p/T < 0.1
Output current; OUTL2	I_{OUTL2}	-0.2	0.4	A	t_p< 0.5s; t_p/T < 0.1

2.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	27	V	After V_S rising above $V_{UV\ ON}$
Supply voltage slew rate	dV_S/dt	-0.5	5	V/µs	–
Supply voltage increasing	V_S	-0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	-0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (DI, CLK, CSN, PWM, TxD)	V_I	-0.3	V_{CC}	V	–
Output current	I_{CC}		35	mA	
Output current	I_{CC}		45	mA	T < 0.1s
Output capacitor	C_{CC}	22		µF	
SPI clock frequency	f_{CLK}	–	1	MHz	–
OSC-Adjust Resistor	R_{OSC}	51	680	kΩ	Ta=-40°C; f = 10kHz
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances					
Junction pin	$R_{thj\text{-}pin}$	–	25	K/W	measured to pin 7
Junction ambient	$R_{thj\text{-}a}$	–	65	K/W	–
Thermal Prewarning and Shutdown (junction temperatures)					
Thermal prewarning ON temperature	T_{jPW}	120	170	°C	bit 0 of SPI diagnosis word; hysteresis 30°K (typ.)
Thermal shutdown temp.	T_{jSD}	150	200	°C	hysteresis 30°K (typ.)
Ratio of SD to PW temp.	T_{jSD} / T_{jPW}	1.05	–	–	–
Thermal shutdown temp. CAN	T_{jSD}	135	160	°C	hysteresis 10°K (typ.)

2.3 Electrical Characteristics

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current Pin V_S						
Current consumption	I_S	–	5	10	mA	
Quiescent current $I_{SSB1} = I_S - I_{CC}$	I_{SSB1}	–	180	280	µA	low power mode; V_S=12V; T_j=25°C
Voltage Regulator; Pin V_{CC}						
Output voltage	V_{CC}	4.9	5.0	5.2	V	0.1mA < I_{CC}< 30mA
Output voltage	V_{CC}	4.8	5.0	5.5	V	0A < I_{CC} < 100µA
Line regulation	ΔV_{CC}	-20		20	mV	9 V < V_S < 15 V; I_{CC} = 10mA
Load regulation	ΔV_{CC}	-25		25	mV	0.1mA < I_{CC}< 30mA; V_S = 9V
Power supply ripple rejection	$PSRR$		40		dB	V_S < 1 Vss; $C_Q \geq$ 22µF; 100Hz< f <100kHz
Output current limit	I_{CCmax}	45	60		mA	1)
Drop voltage $V_{DR} = V_S - V_{CC}$	V_{DR}		0.15	0.45	V	I_{CC} = 30 mA; see note 1)
Oscillator; Pin OSC						
Oscillating frequency	f_{OSC}		62.8		kHz	R_{OSC} = 453kΩ
Internal cycling time $(1/32 * f_{OSC})^{-1}$	t_{CYL}	383	509	637	µs	R_{OSC} = 453kΩ

1) measured when the output voltage V_{CC} has dropped 100 mV from the nominal value obtained at 13.5 V input voltage V_S

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset Generator; Pin RO						
Reset threshold voltage	V_{RT}	4.0	4.3	4.65	V	
Reset low output voltage	V_{RO}		0.2	0.4	V	I_{RO} = 1mA ($V_{CC} \geq V_{RT}$) or $V_{CC} \geq$ 1V (I_{RO} = 200 µA)
Reset high output voltage	V_{RO}	4.0		V_{CC}+ 0.1	V	
Reset pull up current	I_{RO}	20	150	500	µA	V_{RO} = 0V
Reset reaction time	t_{RR}	1	3	10	µs	$V_{CC} < V_{RT}$ to RO = L
Reset delay time (16 cyl.)	t_{RD}	6.1	8.1	10.2	ms	R_{OSC} = 453kΩ
3 V Supervisor; (bit 7 of SPI diagnosis word)						
Supervisor threshold voltage	V_{ST}	2.3	2.7	3.1	V	
Supervisor reaction time	t_{SR}	2	8	20	µs	$V_{CC} < V_{ST}$ to diagnosis bit 7 = L
Watchdog Generator						
Watchdog trigger time	t_{WD}	7.6	10	12.3	ms	R_{OSC} = 453kΩ
Closed window time (12 cyl.)	t_{CW}	4.6	6.1	7.6	ms	R_{OSC} = 453kΩ
Open window time (20 cyl.)	t_{OW}	7.7	10.2	12.7	ms	R_{OSC} = 453kΩ
Watchdog reset-puls time (4 cyl.)	t_{WDR}	1.5	2.0	2.6	ms	R_{OSC} = 453kΩ
Watchdog activating current	I_{CCWD}	2	4	12	mA	T_j < 85 °C; Watchdog OFF when $I_{CC} < I_{CCWD}$ and SPI-input bit 8 = H
Watchdog activating current hysteresis	$I_{CCWDhys}$		0.5		mA	

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Long open window (32 cyl.)	$I_{CCWDhys}$	12.2	16.2	20.4	ms	R_{OSC} = 453kΩ sleep mode (WD OFF) to normal mode
Switches						
Under-Voltage Lockout (bit 3 of SPI diagnosis word)						
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.35	6.00	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.50	4.85	5.20	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
High Side Output OUTH1; (controlled by PWM or bit 1 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTH1} = -0.25 A	$R_{DSON\ H1}$	–	1.0	2.0	Ω	
			1.5	4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH1}	-5.0	-3.0	-0.5	V	I_{OUTH1} = – 0.25 A
Clamp diode forward voltage	V_{OUTH1}		0.8	1	V	I_{OUTH1} = 0.25 A
Leakage current	I_{OLH1}	-100	-5	–	µA	V_{OUTH1} = 0 V
Switch ON delay time	t_{dONH1}		10	100	µs	PWM to OUTH1; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH1}		20	100	µs	PWM to OUTH1; R_L = 100 Ω
Overcurrent shutdown threshold	I_{SDH1}	-1.0	-0.6	-0.3	A	–
Shutdown delay time	t_{dSDH1}	10	25	50	µs	
Current limit	I_{OCLH1}	-2.0	-1.0	-0.5	A	

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PWM Input to control OUTH1; Pin PWM (high active)						
H-input voltage threshold	V_{IH}	–	–	0.7 $\times V_{CC}$	V	–
L-input voltage threshold	V_{IL}	0.2 $\times V_{CC}$	–	–	V	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull down current	I_I	5	25	180	µA	V_I = 0.2 * V_{CC}
Input capacitance	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V
High Side Output OUTH2; (controlled by bit 2 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTH2} = -0.25 A	$R_{DSON\ H2}$	–	1.0	2.0	Ω	
			1.5	4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH2}	-5.0	-3.0	-0.5	V	I_{OUTH2} = – 0.25 A
Clamp diode forward voltage	V_{OUTH2}		0.8	1	V	I_{OUTH2} = 0.25 A
Leakage current	I_{OLH1}	-100	-5	–	µA	V_{OUTH2} = 0 V
Switch ON delay time	t_{dONH1}		10	100	µs	CSN high to OUTH2; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH1}		20	100	µs	CSN high to OUTH2; R_L = 100 Ω
High Side Output OUTH3; (controlled by bit 3 and bit 4 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTH3} = -0.15 A	$R_{DSON\ H3}$	–	1.5	3.0	Ω	
			2.0	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTH3}	-5.0	-3.0	-0.5	V	I_{OUTH3} = – 0.15 A
Clamp diode forward voltage	V_{OUTH3}		0.8	1	V	I_{OUTH3} = 0.15 A
Leakage current	I_{OLH3}	-100	-5	–	µA	V_{OUTH3} = 0 V

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Leakage current	I_{OLH3}	–	5		µA	V_{OUTH3} = 5 V
Switch ON delay time	t_{dONH3}		10	100	µs	CSN high to OUTH3; R_L = 100 Ω
Switch OFF delay time	t_{dOFFH3}		20	100	µs	CSN high to OUTH3; R_L = 100 Ω
Auto time period (128 cyl.)	t_{PH3}	49	65	82	ms	R_{OSC} = 453kΩ; SPI-bit 4 = H, no WD reset
Auto time ON duty cycle (2 cyl.)	D.C.		1/64			referring to t_{PH3}
Low Side Output OUTL1 (bit 5 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTL1} = 0.1 A	$R_{DSON\ L1}$	–	1.5	3.0	Ω	
			2.0	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener clamp voltage	V_{OUTL1}	32	37	42	V	I_{OUTL1} = – 0.1 A
Leakage current	I_{OLL1}			5	µA	V_{OUTL1} =15 V; T_j < 85°C
Switch ON delay time	t_{dONL1}		5	50	µs	CSN high to OUTL1; R_L = 100 Ω
Switch OFF delay time	t_{dOFFL1}		5	50	µs	CSN high to OUTL1; R_L = 100 Ω
Low Side Output OUTL2 (bit 6 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTL2} = 0.1 A	$R_{DSON\ L2}$	–	1.5	3.0	Ω	
			2.0	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener clamp voltage	V_{OUTL2}	32	37	42	V	I_{OUTL2} = – 0.1 A
Leakage current	I_{OLL2}			5	µA	V_{OUTL2} =15 V; T_j < 85°C
Switch ON delay time	t_{dONL2}		5	50	µs	CSN high to OUTL2; R_L = 100 Ω
Switch OFF delay time	t_{dOFFL2}		5	50	µs	CSN high to OUTL2; R_L = 100 Ω

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CAN-Transceiver						
Receiver Output R×D						
HIGH level output voltage	V_{OH}	V_{CC} – 0.9	–	V_{CC}	V	I_0 = – 250µA
LOW level output voltage	V_{OL}	0	–	0.9	V	I_0 = 1.25mA
Transmission Input T×D						
HIGH level input voltage threshold	V_{IH}		0.52× V_{CC}	0.70× V_{CC}	V	
LOW level input voltage threshold	V_{IL}	0.30× V_{CC}	0.48× V_{CC}		V	
HIGH level input current	I_{IH}	-140	-40	-10	µA	V_i = 4 V
LOW level input current	I_{IL}	-600	-200	-40	µA	V_i = 1 V
Bus Lines CANL, CANH						
Differential receiver recessive-to-dominant threshold voltage	$V_{dRxD(rd)}$	-2.8	-2.5	-2.2	V	
Differential receiver dominant-to-recessive threshold voltage	$V_{dRxD(dr)}$	-3.1	-2.9	-2.5	V	
CANH recessive output voltage	V_{CANHr}	0.1	0.2	0.3	V	TxD = V_{CC}; R_{RTH} < 4 kΩ
CANL recessive output voltage	V_{CANLr}	V_{CC} - 0.2	–	–	V	TxD = V_{CC}; R_{RTL} < 4 kΩ
CANH dominant output voltage	V_{CANHd}	V_{CC} -1.4	V_{CC} -1.0	V_{CC}	V	TxD = 0 V; I_{CANH} = – 40 mA

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CANL dominant output voltage	V_{CANLd}	–	1.0	1.4	V	TxD = 0 V; I_{CANL} = 40 mA
CANH output current	I_{CANH}	-110	-80	-50	mA	V_{CANH} = 0 V; TxD = 0 V
		-5	0	5	µA	sleep mode; V_{CANH} = 12 V
CANL output current	I_{CANL}	50	80	110	mA	V_{CANL} = 5 V; TxD = 0 V
		-5	0	5	µA	sleep mode; V_{CANL} = 0 V; V_S = 0 V
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{det(th)}$	6.5	7.3	8.0	V	normal operation mode
CANH wake-up voltage threshold	V_{WAKEH}	1.2	1.9	2.7	V	–
CANL wake-up voltage threshold	V_{WAKEL}	2.2	3.1	3.9	V	–
CANH single-ended receiver threshold	V_{CANH}	1.6	2.1	2.6	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold	V_{CANL}	2.4	3.0	3.4	V	failure case 6 and 6a
CANL leakage current	I_{CANLl}	-5	0	5	µA	V_{CC} = 0 V, V_S = 0 V, V_{CANL} = 13.5 V, T_j < 85 °C
CANH leakage current	I_{CANHl}	-5	0	5	µA	V_{CC} = 0 V; V_S = 0 V; V_{CANH} = 5 V; T_j < 85 °C
Termination Outputs RTL, RTH						
RTL to V_{CC} switch-on resistance	R_{RTL}	–	40	95	Ω	I_o = – 10 mA;
RTL to BAT switch series resistance	R_{oRTL}	5	15	30	kΩ	V_{BAT}-stand-by

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
RTH to ground switch-on resistance	R_{RTH}	–	40	95	Ω	I_o = 10 mA
RTH output voltage	V_{oRTH}	–	0.7	1.0	V	I_o = 1 mA; Vbat-stand-by mode
RTH pull-down current	I_{RTHpd}	40	75	120	µA	failure cases 6 and 6a
RTL pull-up current	I_{RTLpu}	-120	-75	-40	µA	failure cases 3, 3a, 5 and 7

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CAN-Transceiver						
Dynamic Characteristics						
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.2	2.1	µs	10% to 90%; C_1 = 10 nF; C_2 = 0; R_1 = 100 Ω
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.3	0.6	1.3	µs	10% to 90%; C_1 = 1 nF; C_2 = 0; R_1 = 100 Ω
Minimum dominant time for wake-up on CANL or CANH	$t_{wu(min)}$	12	20	38	µs	stand-by mode; V_S = 13.5 V
Failure cases 3 and 6 detection time	t_{fail}	30	45	80	µs	
Failure case 6a detection time		2.0	4.8	8.0	ms	
Failure cases 5, 6, 6a and 7 recovery time		30	45	80	µs	
Failure cases 3 recovery time		250	500	750	µs	
Failure cases 5 and 7 detection time		1.0	2.0	4.0	ms	
Failure cases 5 detection time	t_{fail}	0.4	1.0	2.4	ms	stand-by modes; V_S = 13.5 V
Failure cases 6, 6a and 7 detection time		0.8	4.0	8.0	ms	stand-by modes; V_S = 13.5 V
Failure cases 5, 6, 6a and 7 recovery time		0.4	1.0	2.4	µs	stand-by modes; V_S = 13.5 V

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	1.5	2.1	µs	C_1 = 100 pF; C_2 = 0; R_1 = 100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	1.7	2.4	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.8	2.5	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	2.0	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 =100 Ω; bus failure cases 3, 5, 6, 6a and 7
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{PD(H)}$	–	1.5	2.0	µs	C_1 = 100 pF; C_2 = 0; R_1 =100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.5	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.0	2.1	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.5	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection	n_e	–	4	–	–	
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
TxD permanent dominant disable time	t_{TxD}	1.3	2.0	3.5	ms	

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SPI-Interface						
Logic Inputs DI, CLK and CSN						
H-input voltage threshold	V_{IH}	–	–	0.7 * V_{CC}	V	–
L-input voltage threshold	V_{IL}	0.3 * V_{CC}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull up current at pin CSN	I_{ICSN}	-100	-25	-5	µA	V_{CSN} = 0.7 × V_{CC}
Pull down current at pin DI and CLK	$I_{ICLK/DI}$	5	25	100	µA	V_{DI} = 0.2 × V_{CC}
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	-10	–	10	µA	V_{CSN} = V_{CC} 0 V < V_{DO} < V_{CC}
Tri-state input capacitance	C_{DO}	–	10	15	pF	V_{CSN} = V_{CC} 0 V < V_{CC} < 5.25 V
Data Input Timing						
Clock period	t_{pCLK}	1000	–	–	ns	–
Clock high time	t_{CLKH}	500	–	–	ns	–
Clock low time	t_{CLKL}	500	–	–	ns	–
Clock low before CSN low	t_{bef}	500	–	–	ns	–

2.3 Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = -100 µA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; CAN-transceiver circuitry: – 40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CSN setup time	t_{lead}	500	–	–	ns	–
CLK setup time	t_{lag}	500	–	–	ns	–
Clock low after CSN high	t_{beh}	500	–	–	ns	–
DI setup time	t_{DISU}	250	–	–	ns	–
DI hold time	t_{DIHO}	250	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	–
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	–
Data Output Timing						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.2 V_{CC}; V_{DO} > 0.7V_{CC}; C_L = 100 pF

3 Timing Diagrams

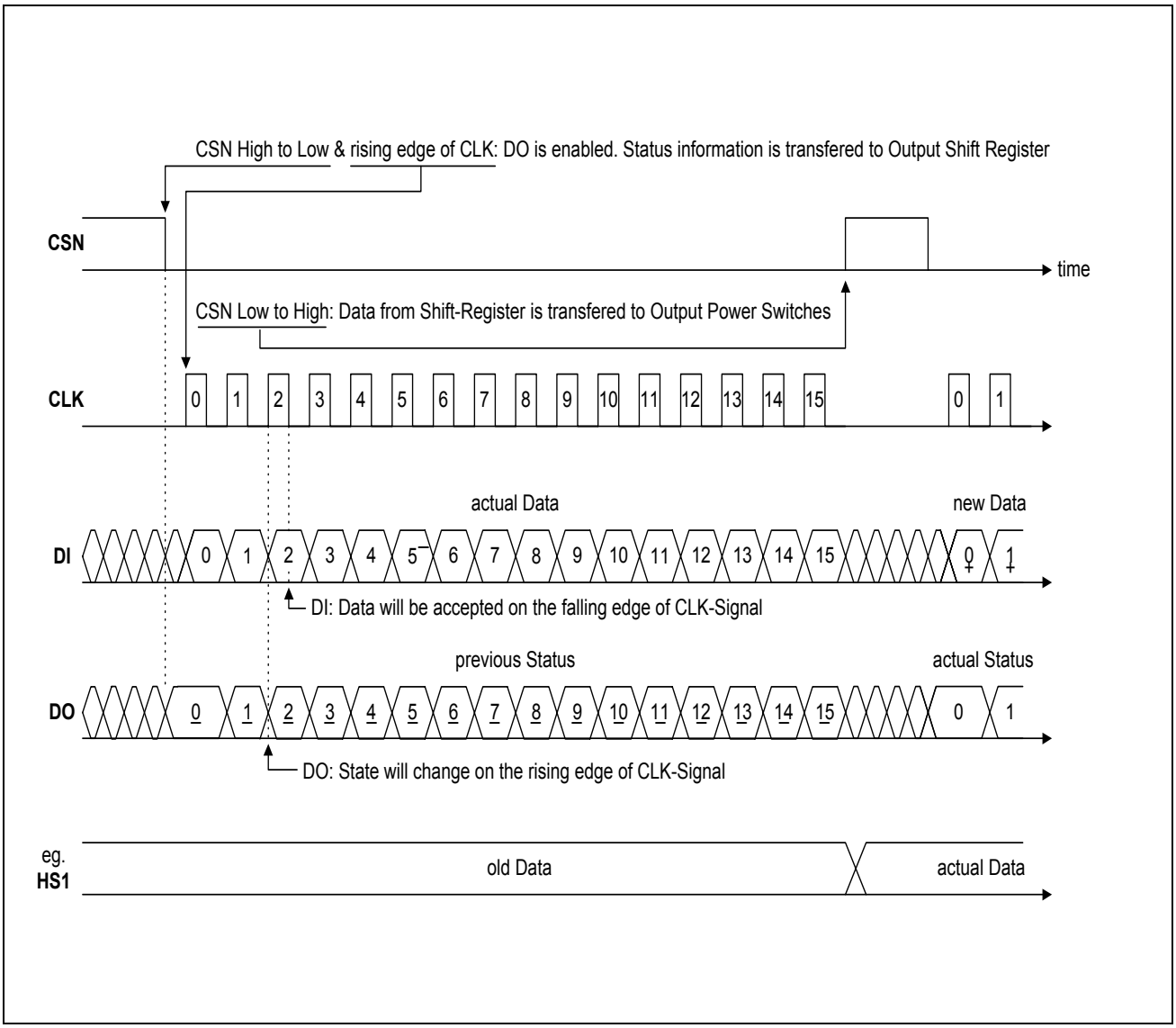


Figure 4
Data Transfer Timing

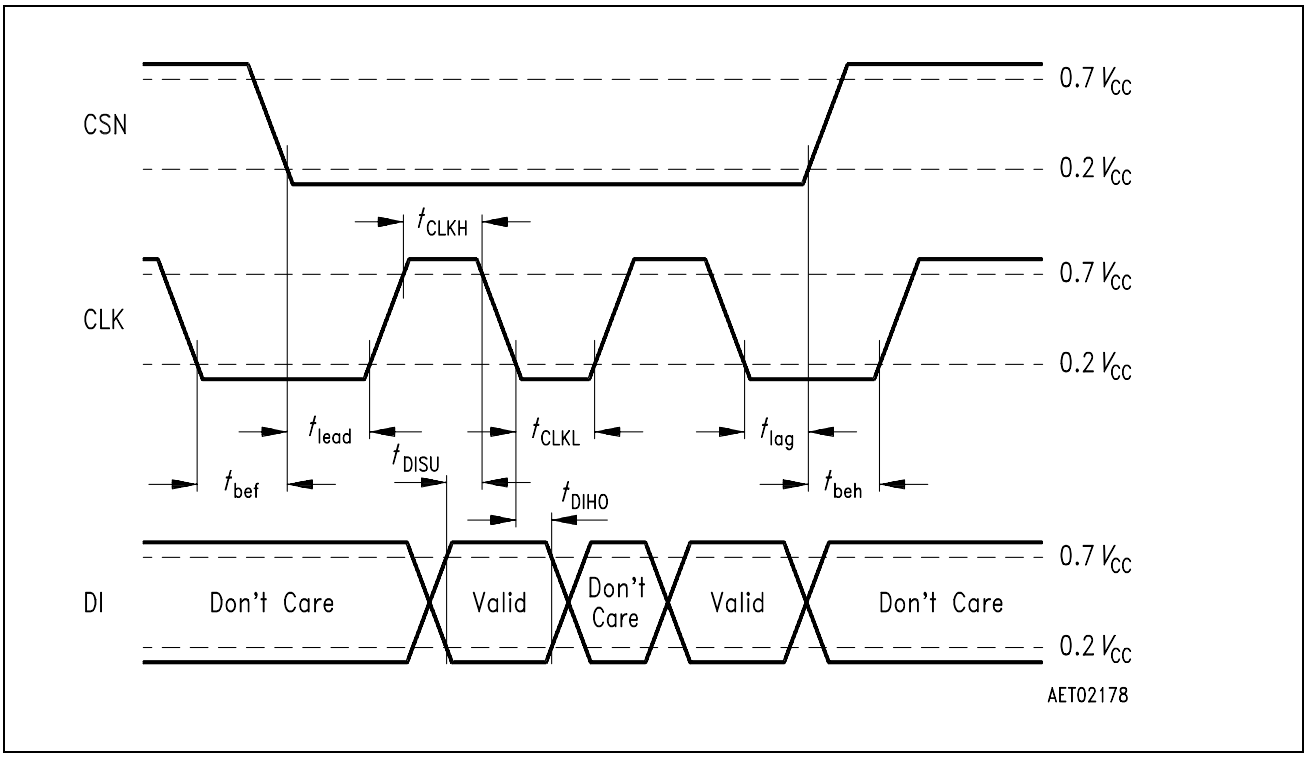


Figure 5
SPI-Input Timing

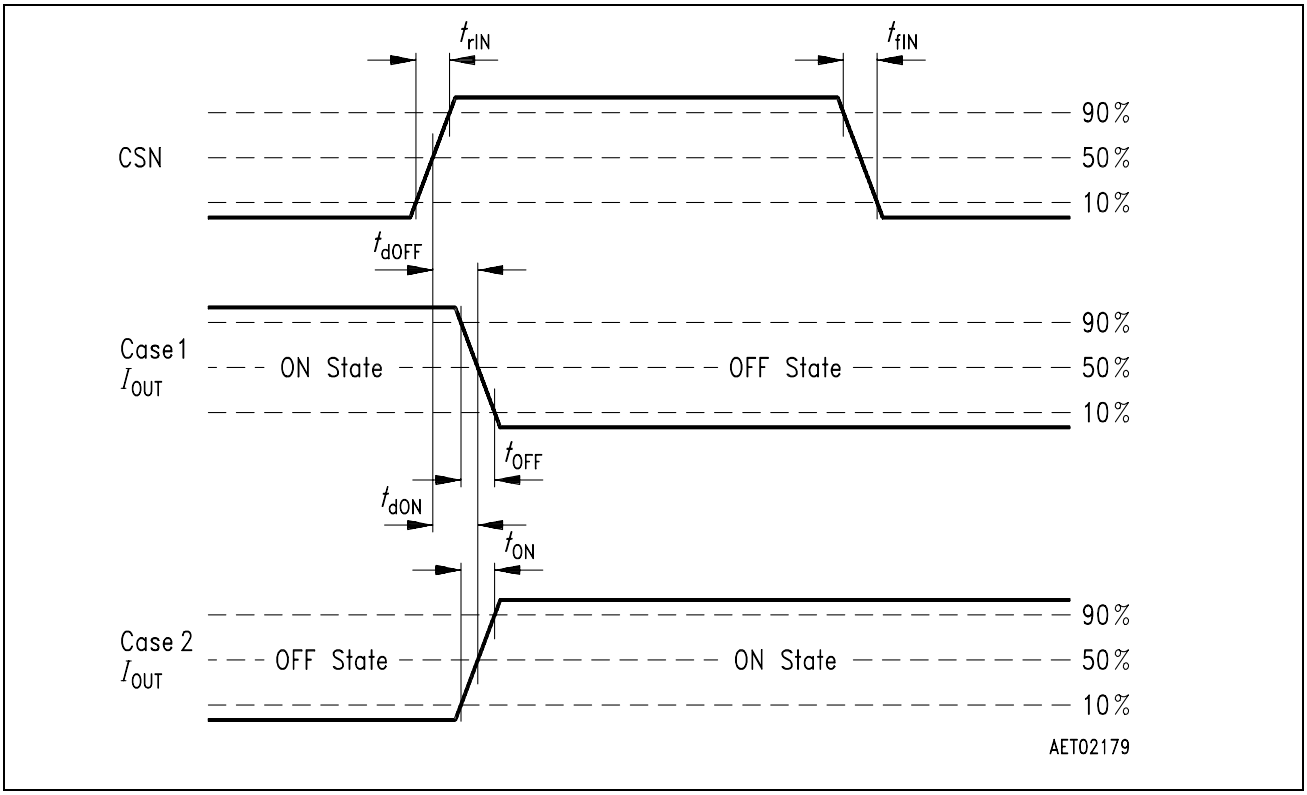


Figure 6
Turn OFF/ON Time

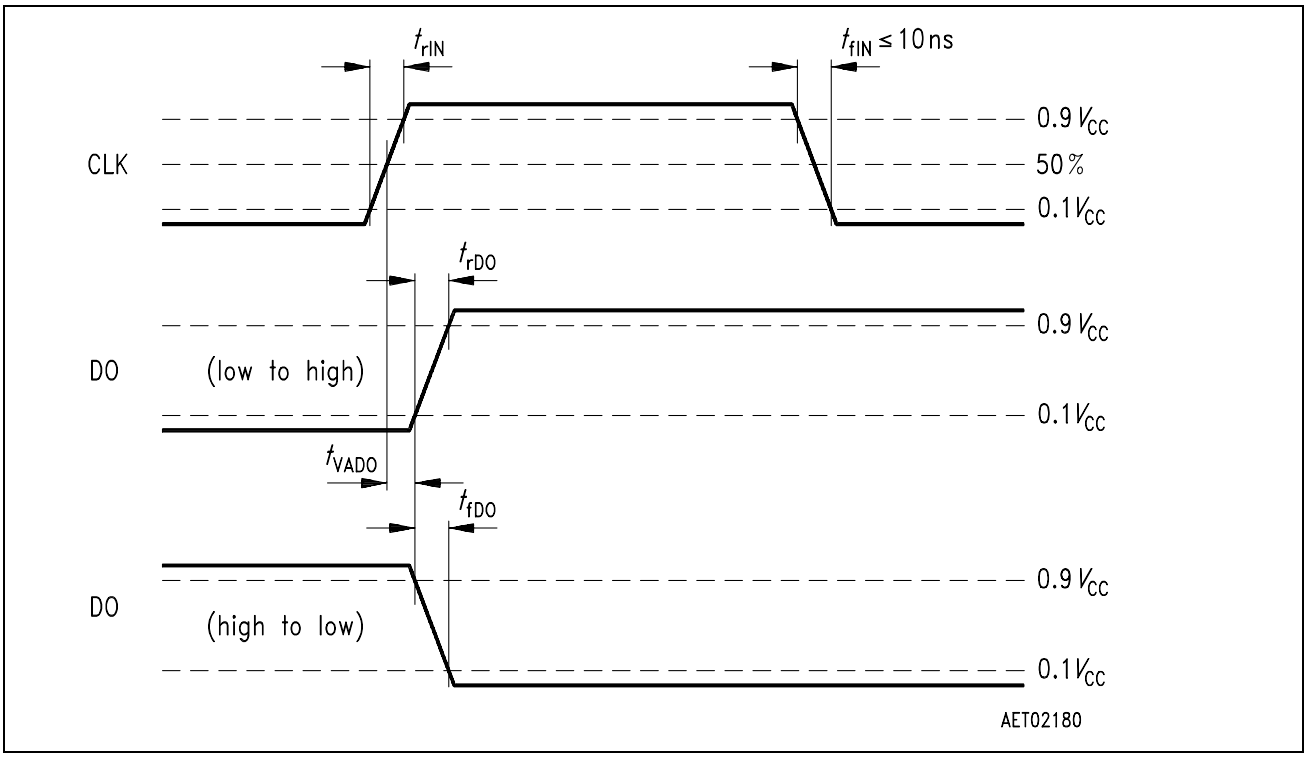


Figure 7
DO Valid Data Delay Time and Valid Time

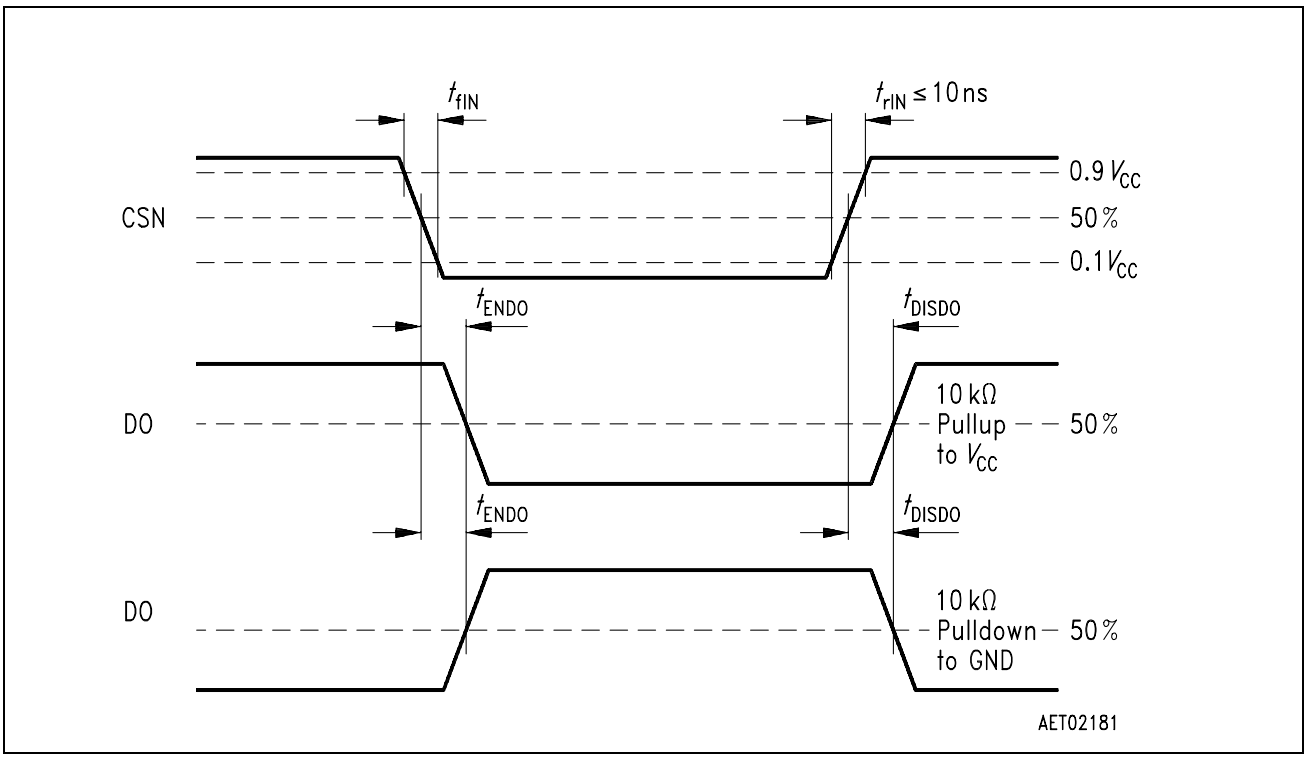


Figure 8
DO Enable and Disable Time

Figure 9: High Side Switch1 Timing Diagram

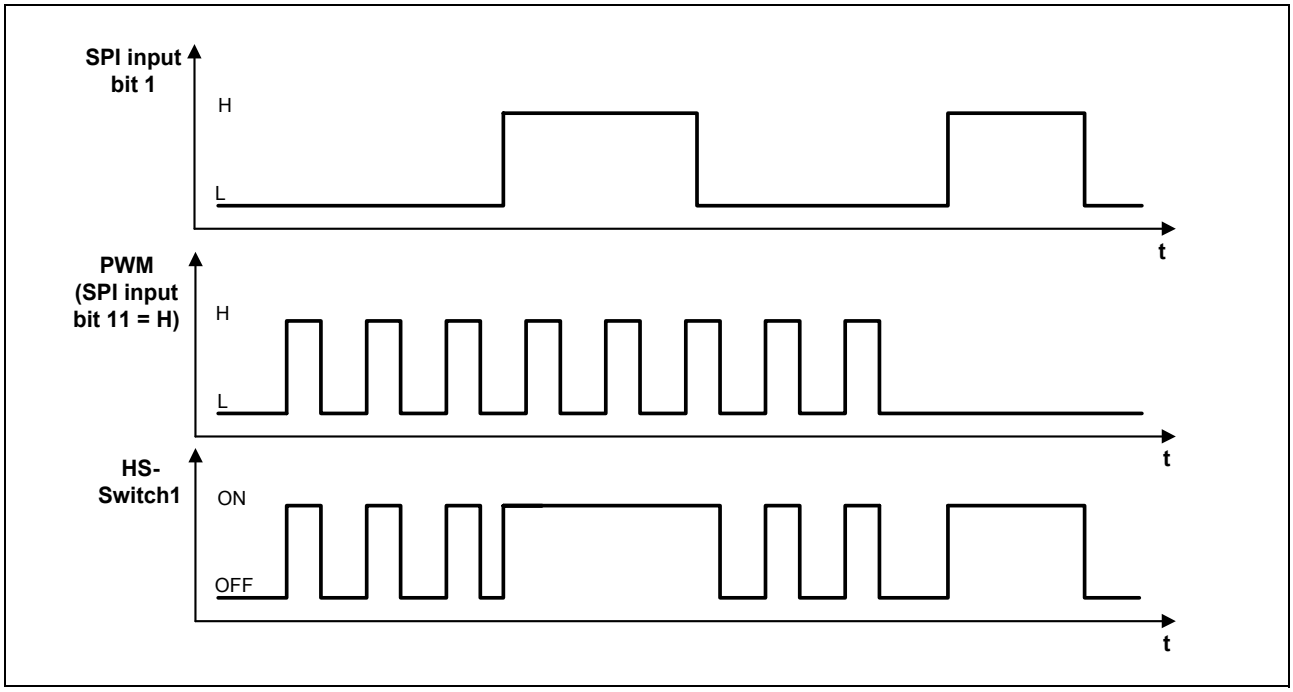


Figure 10: Watchdog Time-out Definitions

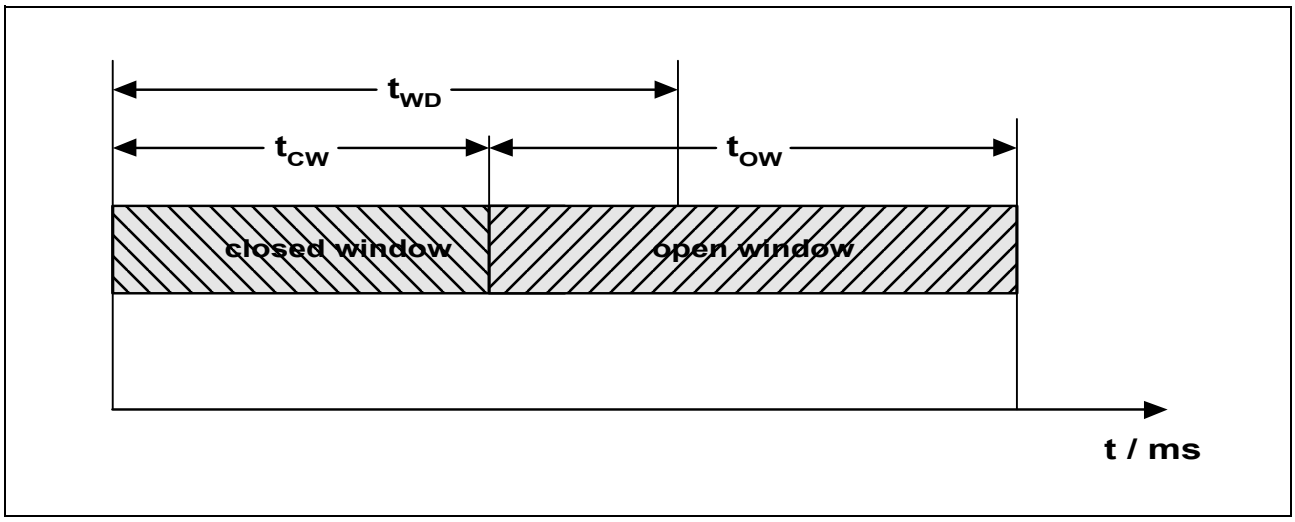


Figure 11: Watchdog Timing Diagram

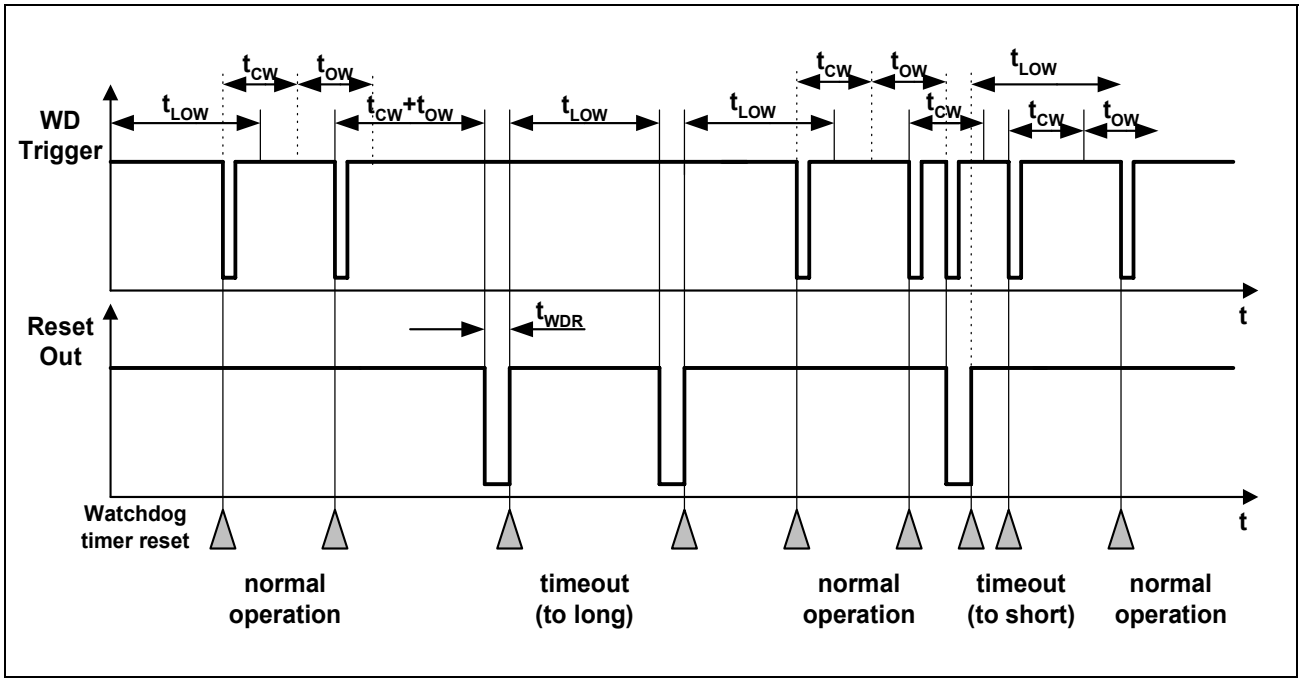
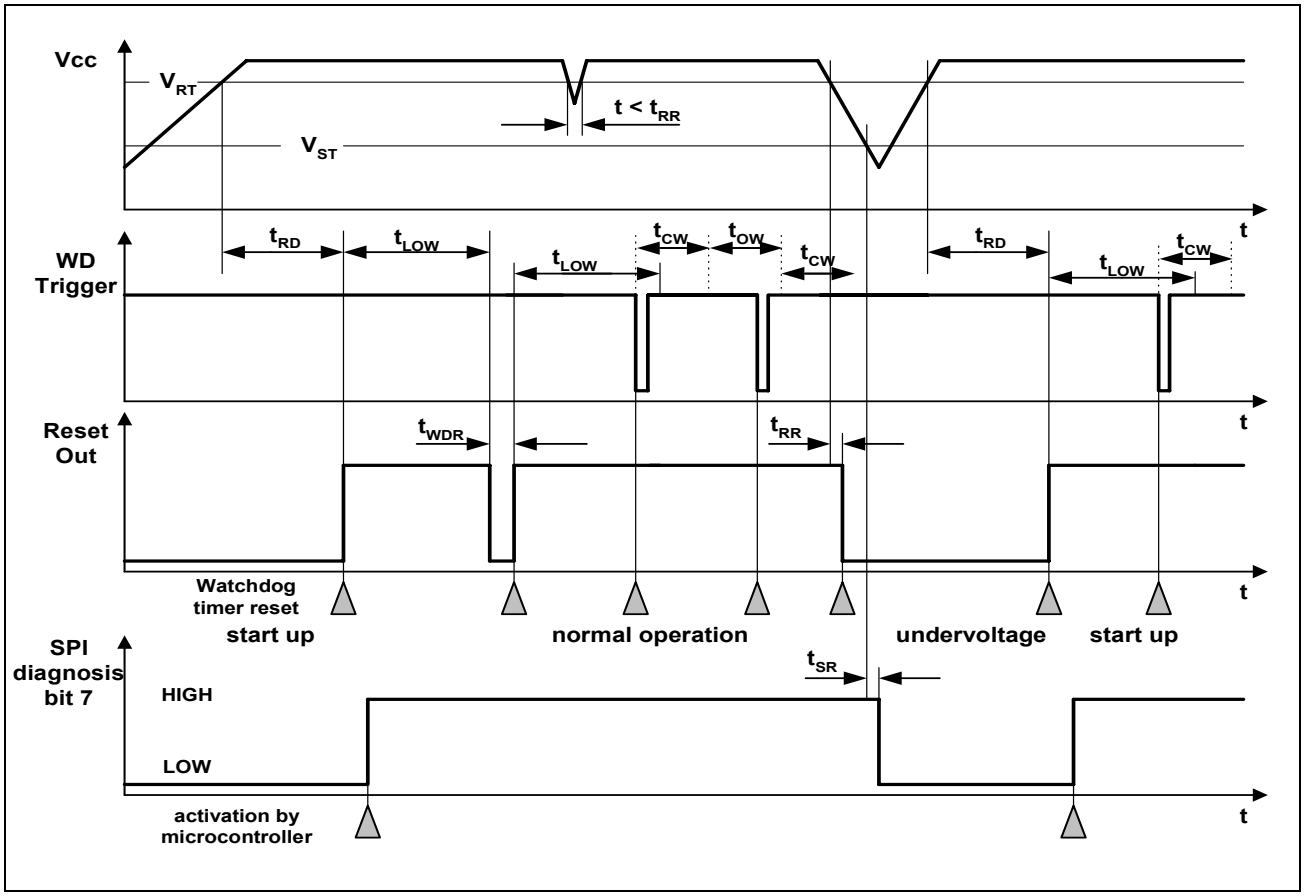


Figure 12: Reset Timing Diagram



4 Application

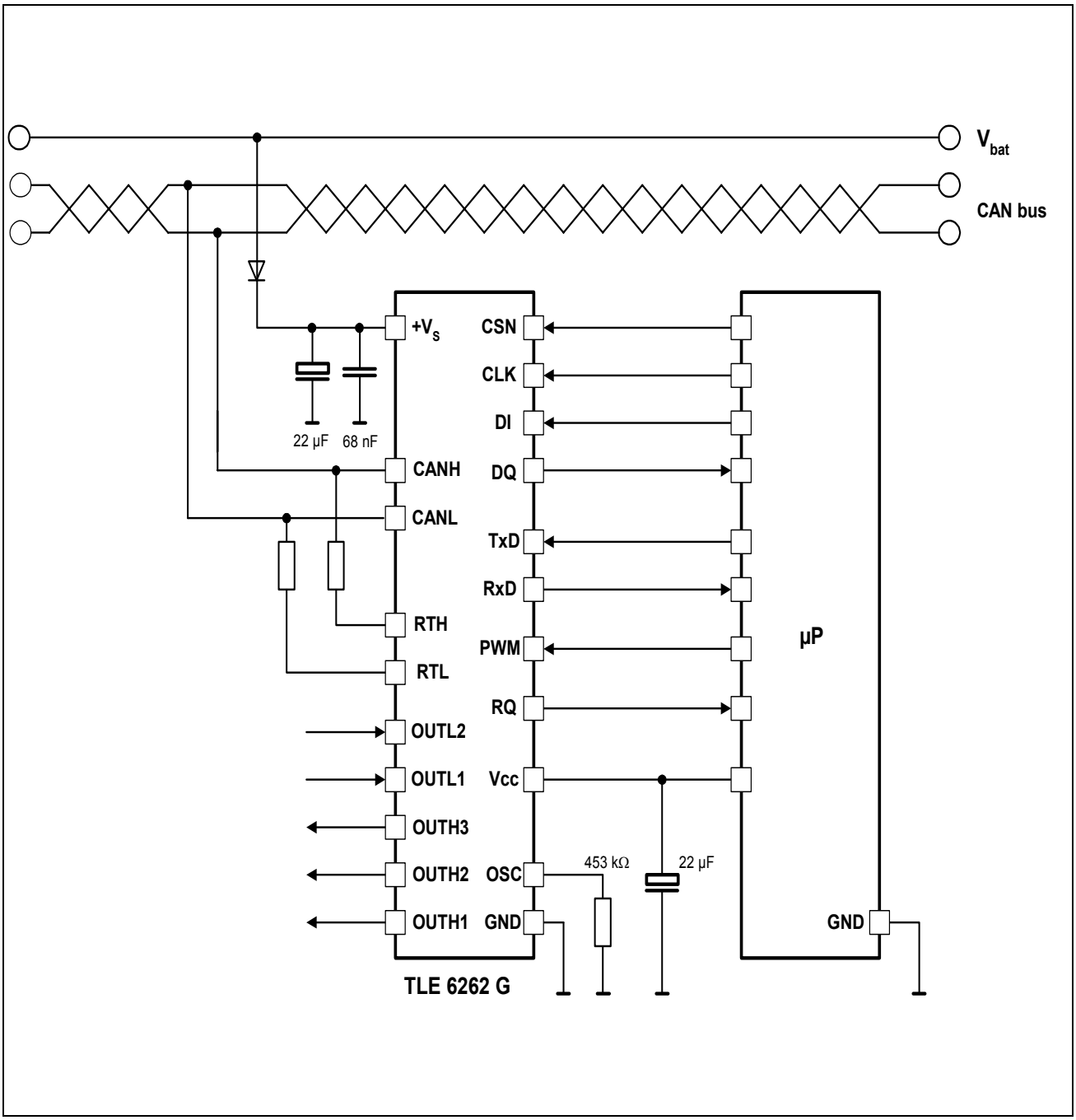
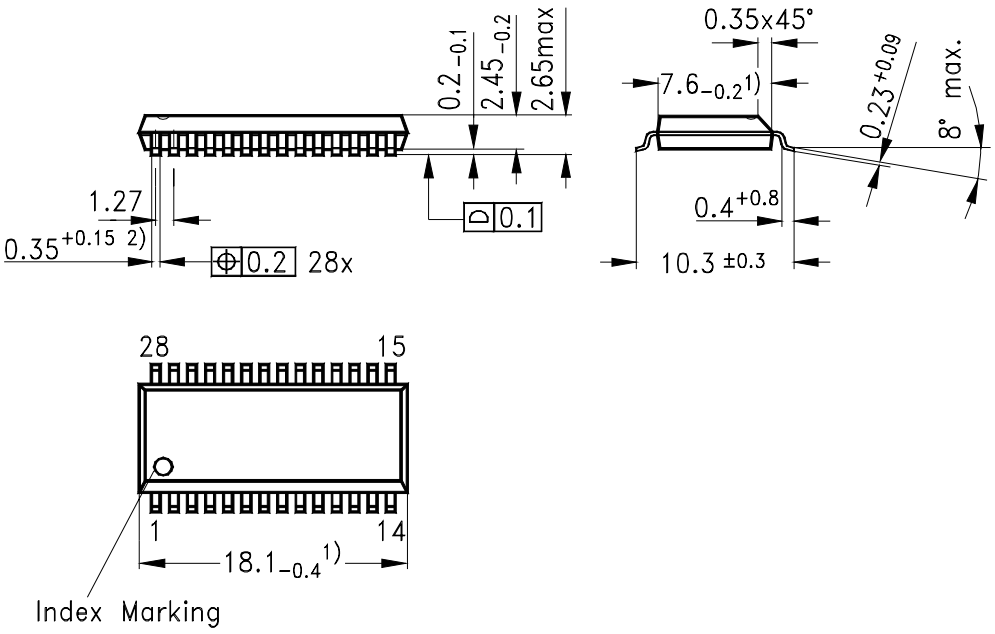


Figure 13
Application Circuit

5 Package Outlines

P-DSO-28-6
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

Edition 1999-10-12

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