## Class-D Audio Power Amplifier with USB / I<sup>2</sup>S Interface

### **Features**

FSM

- Compliant with USB Specification v1.1, and USB 2.0 full speed
- Embedded high efficiency, high performance class D stereo amplifier
- Support I<sup>2</sup>S input and I<sup>2</sup>S output interface of master mode
  - Sampling frequencies(Fs) : 48kHz
- +6dB enhancement(Theater function)
- Support both bus-powered and self-powered operation
- Supports Win Me//2000/XP and MacOS
- True plug-and-play application, no driver is required for basic USB speaker application
- Support volume/mute control with external button
- Built-in 5V to 3.3V regulator for internal device operation
- Total efficiency 80% for 8Ω load @ -1dB 1kHz sine wave input
- Loudspeaker PSNR & DR (A-weighting) 80dB (PSNR), 78dB (DR) with Bead filter

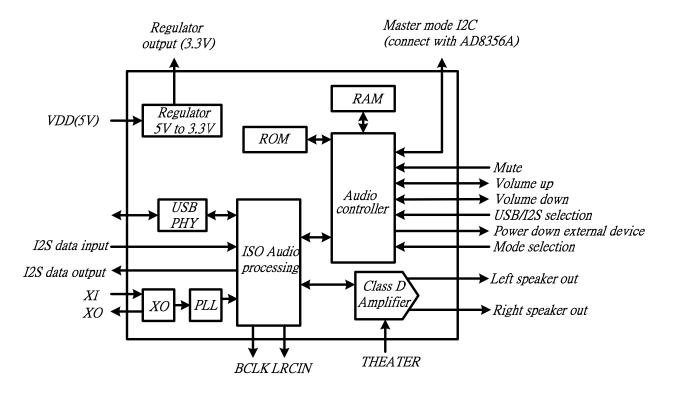
## Functional Block Diagram

82dB (PSNR), 78dB (DR) with Chock filter

- Anti-pop design
- Over-temperature protection
- Under-voltage shutdown
- Short-circuit detection
- 12 MHz Crystal Input
- 32-pin LQFP(Pb free)

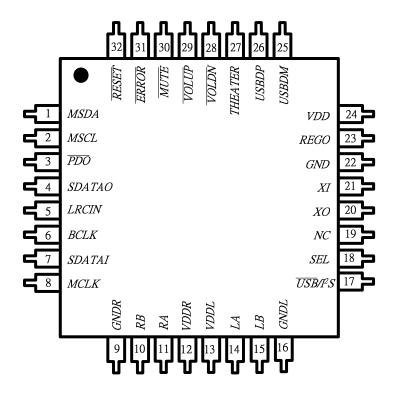
### **Description**

AD62550A is a single chip of Class-D audio amplifier with USB/I<sup>2</sup>S interface. When using the power supplied from the USB port, AD62550A can drive a pair of up to 1W speakers due to the built-in, high efficiency and high performance class D amplifiers. The device also has an I<sup>2</sup>S input port and I<sup>2</sup>S output port. The I<sup>2</sup>S input port allows other external audio sources to use the class D amplifier to share the speakers. The I<sup>2</sup>S output port allows other high performance audio device (i.e. AD8356A/AD8256A) to be controlled by AD62550A.



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### Pin Assignment



### **Pin Description**

| Pin | Name   | Туре | Description                           | Characteristics                  |
|-----|--------|------|---------------------------------------|----------------------------------|
| 1   | MSDA   | I/O  | I <sup>2</sup> C's SDA of Master mode | Schmitt trigger TTL input buffer |
| 2   | MSCL   | 0    | I <sup>2</sup> C's SCL of master mode |                                  |
| 3   | PDO    | 0    | Power-down output (Note1)             |                                  |
| 4   | SDATAO | 0    | Serial audio output (Note1)           |                                  |
| 5   | LRCIN  | 0    | L/R clock output(Fs) (Note1)          |                                  |
| 6   | BCLK   | 0    | BCLK output(64xFs) (Note1)            |                                  |
| 7   | SDATAI | I    | Serial audio data input               | Schmitt trigger TTL input buffer |
| 8   | MCLK   | 0    | Master clock(256xFs)                  |                                  |
| 9   | GNDR   | Р    | Ground for right channel              |                                  |
| 10  | RB     | 0    | Right channel output-                 |                                  |
| 11  | RA     | 0    | Right channel output+                 |                                  |
| 12  | VDDR   | Р    | Supply for right channel              |                                  |
| 13  | VDDL   | Р    | Supply for left channel               |                                  |
| 14  | LA     | 0    | Left channel output+                  |                                  |
| 15  | LB     | 0    | Left channel output-                  |                                  |
| 16  | GNDL   | Р    | Ground for left channel               |                                  |

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| 17 | $\overline{\text{USB}}/\text{I}^2\text{S}$ | 1   | Low is USB mode, high is I <sup>2</sup> S mode | Schmitt trigger TTL input buffer |  |
|----|--|-----|--|----------------------------------|--|
|    |  | - 1 | -  |                                  |  |
| 18 | SEL  |     | Mode selection bit                             | Schmitt trigger TTL input buffer |  |
| 19 | NC   | NC  | No connection                                  |                                  |  |
| 20 | ХО   | 0   | Crystal output                                 |                                  |  |
| 21 | XI   | Ι   | Crystal input                                  |                                  |  |
| 22 | GND  | Р   | Ground   |                                  |  |
| 23 | REGO                                       | 0   | 3.3V regulator output                          |                                  |  |
| 24 | VDD  | Р   | 5V supply voltage                              |                                  |  |
| 25 | USBDM                                      | I/O | USB data D-                                    |                                  |  |
| 26 | USBDP                                      | I/O | USB data D+                                    |                                  |  |
| 27 | THEATER                                    | I   | Theater mode, high active                      | Schmitt trigger TTL input buffer |  |
| 28 | VOLDN                                      | I   | Volume down, low active                        | With internal pull-up resistor   |  |
| 29 | VOLUP                                      | Ι   | Volume up, low active                          | With internal pull-up resistor   |  |
| 30 | MUTE                                       | I   | Power-down and mute of Class D                 | Schmitt trigger TTL input buffer |  |
| 31 | ERROR                                      | 0   | Error output                                   | Open-Drain output                |  |
| 32 | RESET                                      | Ι   | Reset signal                                   | Schmitt trigger TTL input buffer |  |

Note1: Must be strapped resistor 1MΩ to 3.3V(REGO) or GND. BCLK, LRCIN and PDO must be strapped to GND. SDATAO is strapped to GND by 1MΩ when AD62550A's volume/mute is controlled by external button, otherwise strapped to 3.3V when AD62550A is I<sup>2</sup>C slave mode for SEL1 is logic LOW.

### Absolute Maximum Ratings

| Symbol           | Parameter  | Min  | Max | Units |
|------------------|--|------|-----|-------|
| VDD              | Supply for regulator input                                       | 0    | 5.5 | V     |
| VDDL(R)          | Supply for Left (Right) Channel                                  | 0    | 5.5 | V     |
| Vi               | Input Voltage  | -0.3 | 3.6 | V     |
| T <sub>stg</sub> | Storage Temperature  | -65  | 150 | °C    |
| Ta               | Ambient Operating Temperature                                    | 0    | 70  | °C    |
|                  | Voltage Difference between $V_{\text{DDL}}$ and $V_{\text{DDR}}$ | -1   | 1   | V     |
|                  | Voltage Difference between $V_{DDL}(V_{DDR})$ and DVDD/AVDD      | -3   | 3   | V     |
|                  | V <sub>DDL</sub> (V <sub>DDR</sub> ) Power-on Voltage Ramp       |      | 0.2 | V/μs  |

#### **Recommended Operating Conditions**

| Symbol  | Parameter                     | Тур     | Units |  |
|---------|-------------------------------|---------|-------|--|
| VDD     | Supply for regulator input    | 4.5~5.5 | V     |  |
| VDDL(R) | Supply for Driver Stage       | 3.0~5.0 | V     |  |
| Ta      | Ambient Operating Temperature | 0~70    | °C    |  |