图形点阵液晶显示模块使用手册

YB12864AO1

LCD MODULE USER MANUAL

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1. FUNCTIONS & FEATURES

Features

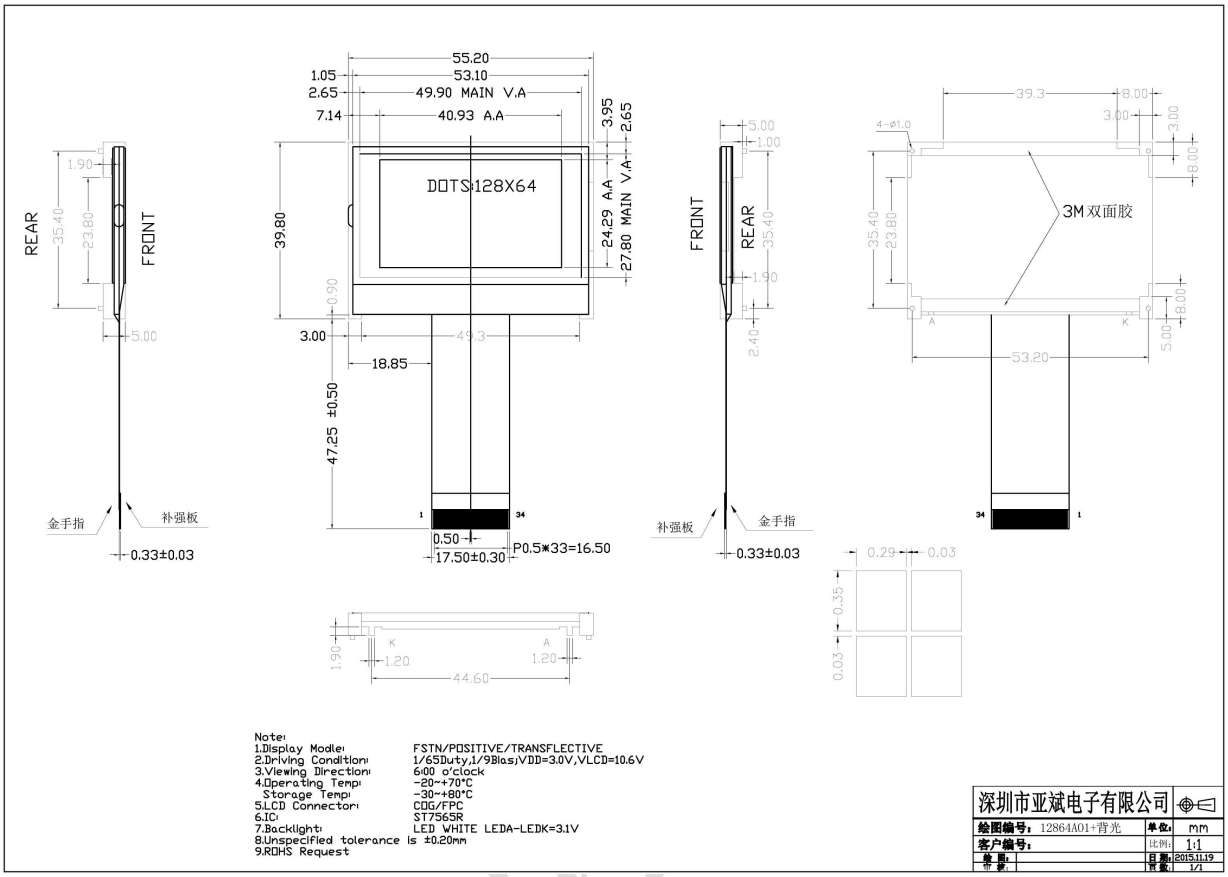
- Dot Matrix: 128×64 Dots
- LCD Mode: FSTN/POSITIVE/TRANSMISSIVE
- Controller IC:ST7565R
- Driving Method: 1/65 Duty; 1/9 Bias
- Viewing Angie: 6 O'clock direction
- 8080 MCU Interface OR 6800 MCU Interface OR 4-SPI
- Operating voltage: 3.3V
- Operating Temperature Range: -20 to +70℃
- Storage Temperature Range : -30 to +80℃

2. MECHANICAL SPECIFICATIONS

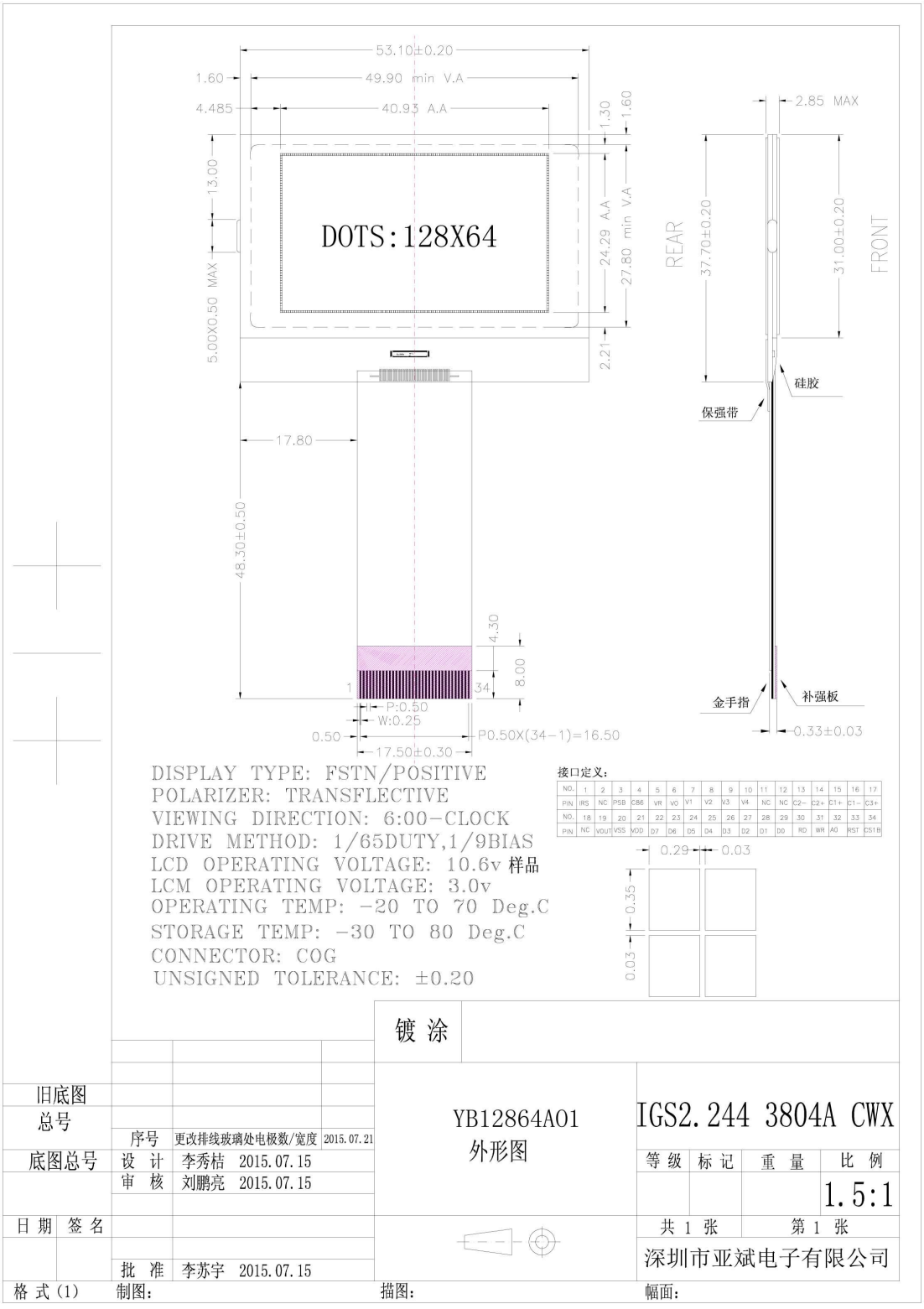
ITEM	SPECIFICATIONS	UNIT
Module Size(L×W×H)	55.2L×39. 8W×5.5（max）H	mm
View Area(W×H)	49.9×24.29	mm
Effective v/area	40.93×24.29	mm
Effective Area	128×64	dot
Dot Pitch(W×H)	0.29×0.35	mm
Dot Size(W×H)	0.32×0.38	mm

3. EXTERNAL DIMENSIONS

LCD+BLK:



LCD:


53.10±0.20
1.60
49.90 min V.A
4.485
40.93 A.A
1.30
1.60
13.00
DOTS:128X64
5.00X0.50 MAX
24.29 A.A
27.80 min V.A
2.21
2.85 MAX
REAR
37.70±0.20
31.00±0.20
FRONT
硅胶
保强带
17.80
48.30±0.50
4.30
8.00
1
34
P:0.50
W:0.25
0.50
P0.50X(34-1)=16.50
17.50±0.30
金手指
补强板
0.33±0.03
DISPLAY TYPE: FSTN/POSITIVE
POLARIZER: TRANSFLECTIVE
VIEWING DIRECTION: 6:00-CLOCK
DRIVE METHOD: 1/65DUTY,1/9BIAS
LCD OPERATING VOLTAGE: 10.6v 样品
LCM OPERATING VOLTAGE: 3.0v
OPERATING TEMP: -20 TO 70 Deg.C
STORAGE TEMP: -30 TO 80 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20
接口定义:
0.29
0.03
0.35
0.03
镀 涂
旧底图总号
总号
序号 更改排线玻璃处电极数/宽度 2015.07.21
底图总号
设 计 李秀桔 2015.07.15
审 核 刘鹏亮 2015.07.15
日 期 签 名
批 准 李苏宇 2015.07.15
YB12864A01
外形图
IGS2.244 3804A CWX
等 级 标 记 重 量 比 例
1.5:1
共 1 张 第 1 张
深圳市亚斌电子有限公司
格 式 (1) 制图: 描图: 幅面:

4. PIN DESCRIPTION

ITEM	SYMBOL	LEVEL	FUNCTION
1	IRS	H/L	This terminal selects the resistors for the V_0 voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V_0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal
2	NC	-	No connection
3	PSB	H/L	This pin configures the interface to be parallel mode or serial mode. P/S = "H": Parallel data input/output. P/S = "L": Serial data input.
4	C86	H/L	This is the MPU interface selection pin. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.
5	VR	-	Output voltage regulator terminal. Provides the voltage between VSS and V_0 through a resistive voltage divider. IRS = "L" : the V_0 voltage regulator internal resistors are not used. IRS = "H" : the V_0 voltage regulator internal resistors are used.
6	V0	-	This is a multi-level power supply for the liquid crystal drive. $V_0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq Vss$
7	V1		
8	V2		
9	V3		
10	V4		
11~12	NC	-	No connection
13	C2-	-	DC/DC voltage converter.
14	C2+		
15	C1+		
16	C1-		
17	C3+		
18	NC	-	No connection
19	VOUT	-	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.
20	VSS	0V	Power Ground
21	VDD	+3.3V	Power Supply For Logic
22~29	D7~D0	H/L	8-Bit data BUS
30	RD/E	H/L	6800:Read/Write control input pin.

			8080:Read enable input pin.
31	RW	H/L	6800: Read/Write control input pin.(R/W="H": read.R/W="L": write.) 8080: Write enable input pin.
32	A0	H/L	It determines whether the access is related to data or command. A0="H" : Indicates that signals on D[7:0] are display data. A0="L" : Indicates that signals on D[7:0] are command.
33	RST	H/L	Hardware reset input pin. When RSTB is "L", internal initialization is executed and the internal registers will be initialized.
34	CS1B	L	Chip select input pin. Interface access is enabled when CSB is "L". When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.

5. MAXIMUM ABSOLUTE LIMIT (T=25°C)

Items	Symbol	Min	Max	Unit	Condition
Supply Voltage	Vdd	2.5	3.3	V	Vss=0V
Input Voltage	Vin	0	Vdd	V	Vss=0V
Operating Temperature	Top	-20	+70	℃	No Condensation
Storage Temperature	Tst	-40	+80	℃	No Condensation

Note: Voltage greater than above may damage the module
All voltages are specified relative to Vss=0V

6. ELECTRICAL CHARACTERISTICS

6.1 DC Characteristics (VSS=0V, Ta=-20~+70° C)

Items	Symbol	Min	Max	Unit	Condition
Supply Voltage	Vdd	2.4	3.3	V	Vss=0V
Input Voltage	Vin	0	Vdd	V	Vss=0V
Operating Temperature	Top	-20	+70	℃	No Condensation
Storage Temperature	Tst	-40	+80	℃	No Condensation

Note: Voltage greater than above may damage the module
All voltages are specified relative to Vss=0V

7. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

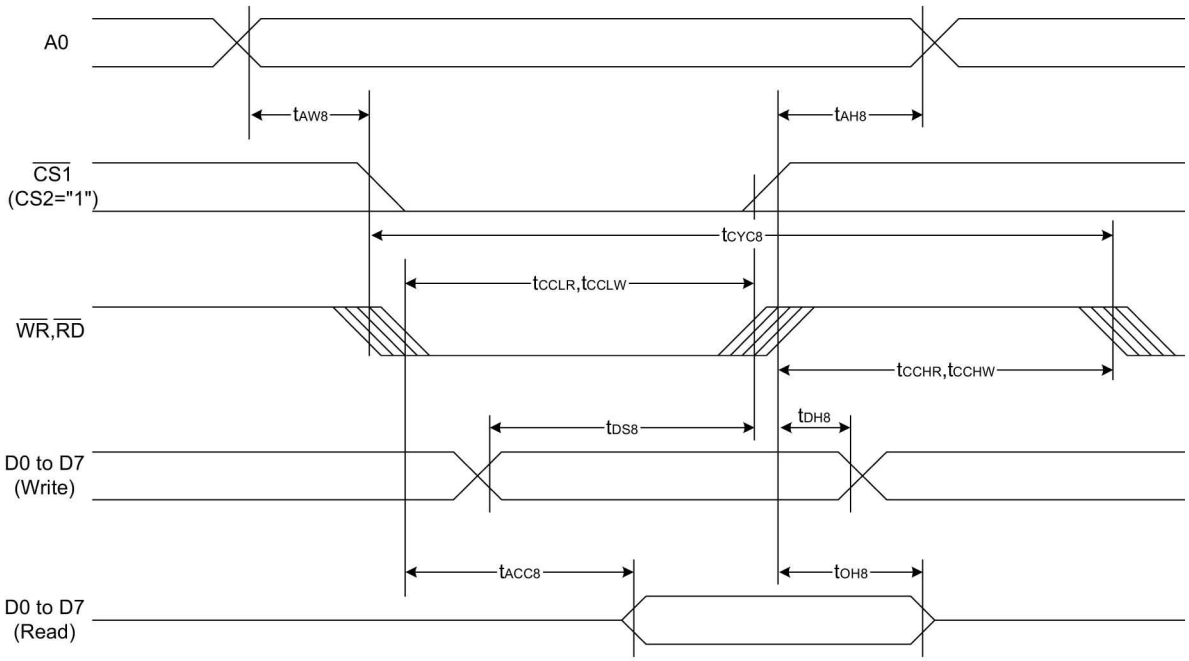


Figure 37

Table 24

(VDD = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

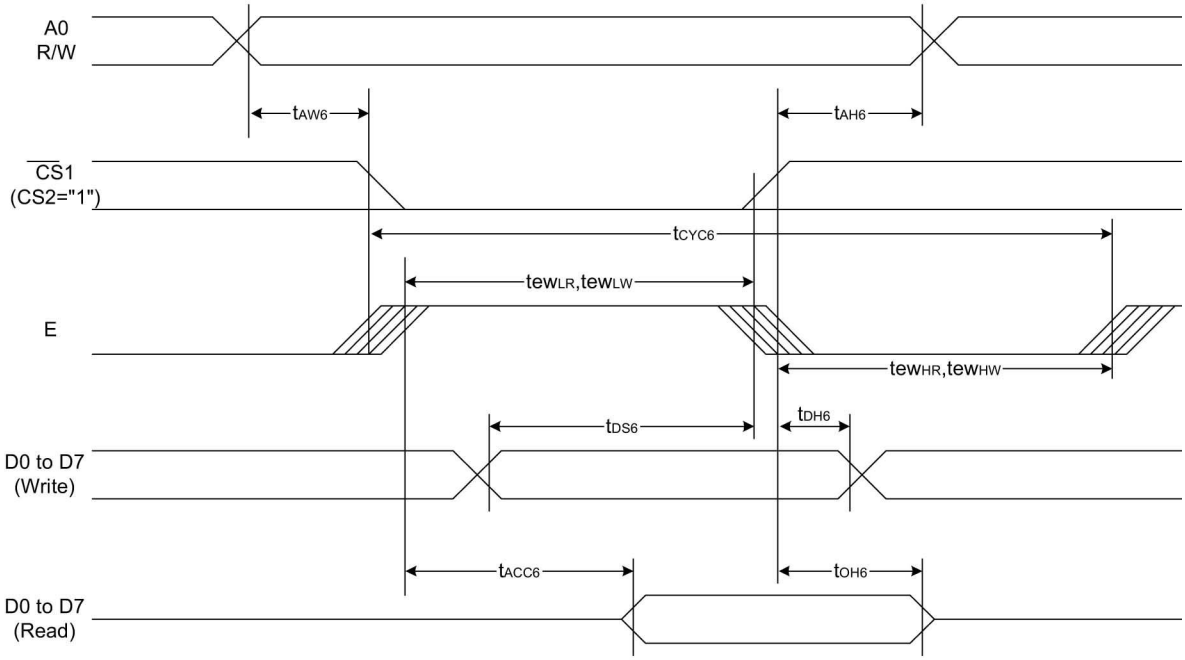


Figure 38

Table 26

(VDD = 3.3V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

The 4-line SPI Interface

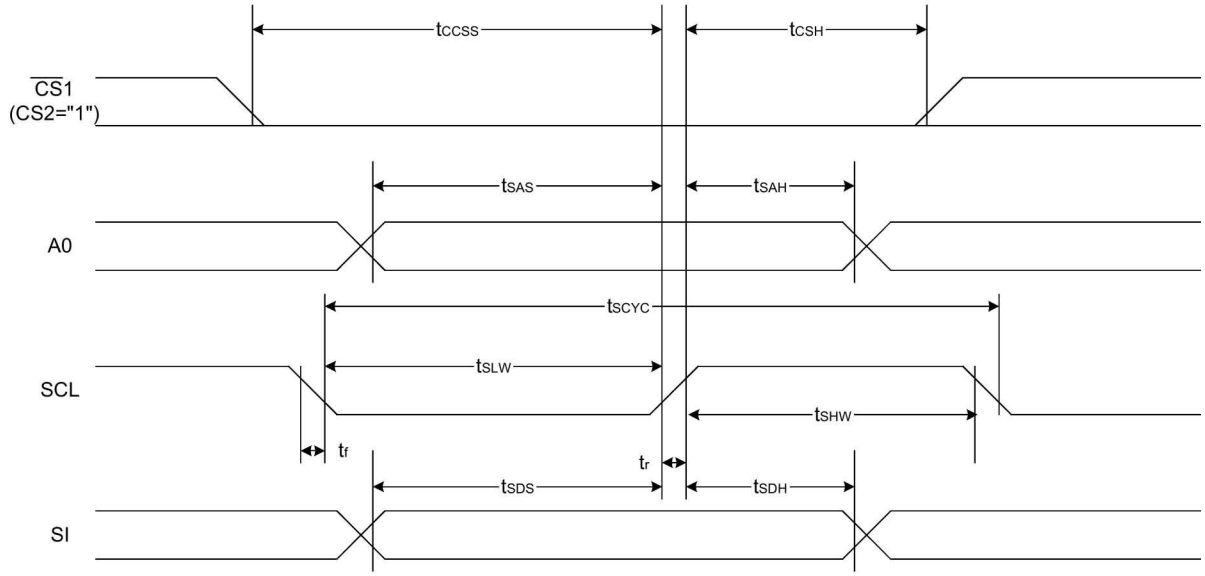


Figure 39

Table 28

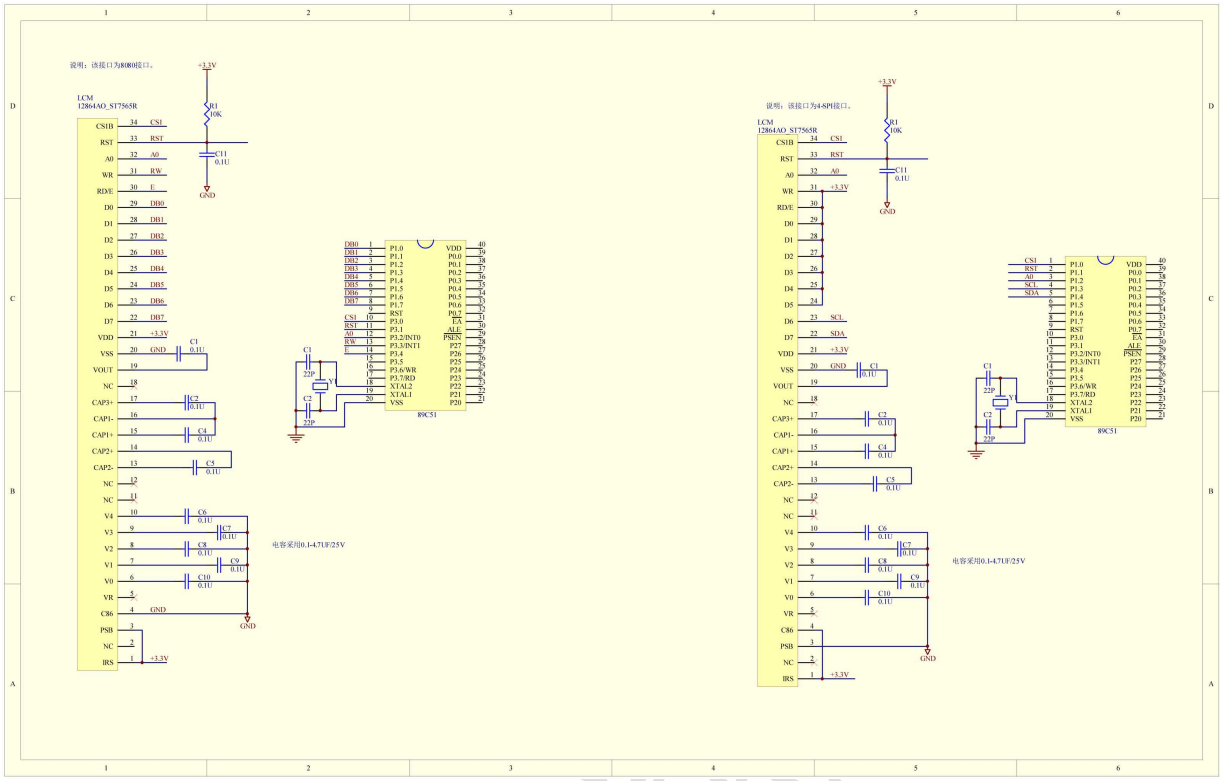
(VDD = 3.3V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		50	—	ns
SCL “H” pulse width		Tshw		25	—	
SCL “L” pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

Table 29

(VDD = 2.7V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		100	—	ns
SCL “H” pulse width		TSHW		50	—	
SCL “L” pulse width		TSLW		50	—	
Address setup time	A0	TSAS		30	—	
Address hold time		TSAH		20	—	
Data setup time	SI	TSDS		30	—	
Data hold time		TSDH		20	—	
CS-SCL time	CS	TCSS		30	—	
CS-SCL time		TCSH		60	—	



8. Hardware Reset Timing

Reset Timing

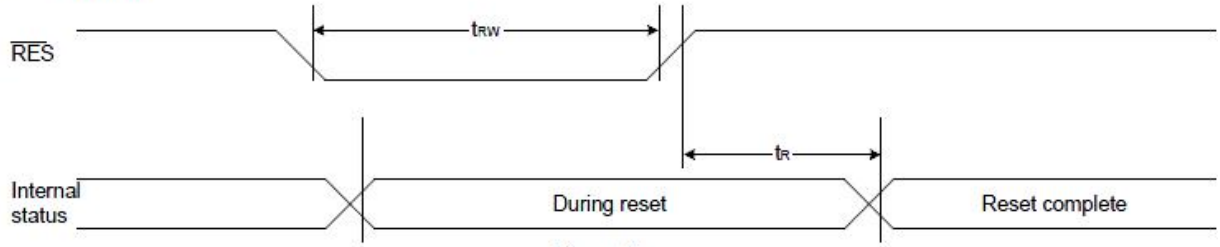


Figure 41

Table 30

(V_{DD} = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.0	us
Reset "L" pulse width	/RES	t_{RW}		1.0	—	—	us

Table 31

(V_{DD} = 2.7V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	2.0	us
Reset "L" pulse width	/RES	t_{RW}		2.0	—	—	us

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

9. INSTRUCTION TABLE

Table 16: Table of ST7565R Commands (Note) *: ignored data

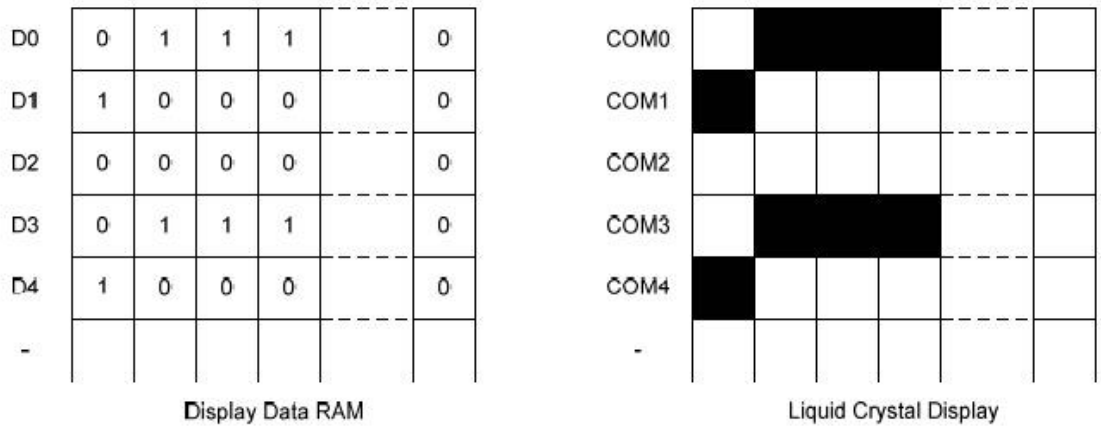
Command	Command Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0	0	0 Electronic volume value	0	0	1	Set the V_0 output voltage electronic volume register
(19) Sleep mode set	0	1	0	1 *	0 *	1 *	0 *	1 *	1 *	0 0	0 1 0	0: Sleep mode, 1: Normal mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

NOTE:

- Do not use any other commands not listed, or the system malfunction may result.
- For the details of rte display commands, please refer to ST7565R datasheet.

10. Display Data RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 192-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages (Page 0~Page 7) of 8lines and the 9th page (Page 8) with a single line (D0 only). Data is written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The LCD controller and MPU interface operate independently, data can be written into RAM at the same time when data is being displayed without flicker on
LCD.



Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page Address” instruction. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons and display data D0 is only valid.

Column Address Circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). The DDRAM column address is specified by the “Set Column Address” command. The specified column address is incremented (+1) with each display data read/write access. This allows the MPU display data to be accessed continuously. Control flag MY can invert the output order of the COM pads. And the MX flag makes it possible to invert the relationship between the Column Address and the SEG outputs. It is necessary to rewrite the display data into DDRAM after changing MX flag setting.

Please refer to ST7565R datasheet.

11. Application Circuits

12 .DESIGN AND HANDING PRECAUTION

12.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module.Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

12.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

12.3 Never attempt to disassemble or rework the LCD module.
12.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
12.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
12.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
12.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
12.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
12.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
12.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12.11 Take care and prevent get hurt by the LCD panel edge.
12.12 Never operate the LCD module exceed the absolute maximum ratings.
12.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
12.14 Never apply signal to the LCD module without power supply.
12.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
12.16 LCD module reliability may be reduced by temperature shock.
12.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module