

## –36V, –200mA, 超低噪音, 负电源线性稳压器

### 特性

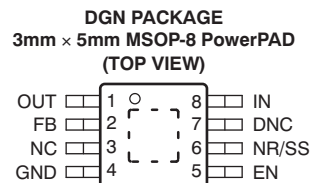
- 输入电压范围: **–3 V 至 –36 V**
- 噪音:
  - **14 $\mu$ V<sub>RMS</sub> (20Hz 至 20kHz)**
  - **15.1 $\mu$ V<sub>RMS</sub> (10Hz 至 100kHz)**
- 电源纹波抑制:
  - **72dB (120Hz)**
  - **≥ 55dB (10Hz 至 700kHz)**
- 可调输出电压: **–1.18V to –35V**
- 最大输出电流: **200mA**
- 压差: **216 mV** (在 **100 mA** 电流下)
- 采用 **≥ 2.2  $\mu$ F** 陶瓷电容器时可保持稳定
- **CMOS** 逻辑电平兼容型使能引脚
- 内置、固定、电流限制及热关断保护功能
- 采用具有高散热性能的 **MSOP-8 PowerPAD™** 封装

### 应用范围

- 用于运算放大器、**DAC**、**ADC** 和其它高精度模拟电路的供电轨
- 音频
- 后置 **DC/DC** 转换器稳压及纹波滤除
- 测试和测量
- **RX, TX, 和 PA** 电路
- 工业仪器仪表
- 基站和电信基础设施
- **–12V 和 –24V** 工业总线

### 支持国防、航天和医疗应用

- 受控基线
- 一个组装/测试场所
- 一个制造场所
- 在军用温度范围内 (**–55°C/125°C**)工作
- 产品生命周期有所延长
- 拓展的产品变更通知
- 产品可追溯性



### 说明

TPS7A3001 是一款负高电压 (–36 V)、超低噪声(15.1 $\mu$ V<sub>RMS</sub>, 72dB PSRR) 线性稳压器, 此稳压器能提供 200 mA 的最大负载电流。

这些线性稳压器包括 **CMOS** 逻辑电平兼容使能引脚和可编程电容器软启动功能, 此功能可实现定制的电源管理方案。其它特点包括内置的限流及热关断保护功能, 此功能用于在故障情况下对器件及系统的保护。

TPS7A3001 采用双极型技术设计而成, 并且非常适合于高准确度、高精度的仪器仪表应用。在此类应用中, 规整的电源电压对于系统性能的最大化至关重要)。这种设计使其成为功率运算放大器、模数转换器 (**ADC**)、数模转换器 (**DAC**) 及其它高性能模拟电路的最佳选择。

此外, TPS7A3001 线性稳压器也适合于后置 **DC/DC** 转换器的稳压操作。通过滤除 **DC/DC** 开关转换所固有的输出电压纹波, 可在灵敏仪器仪表、测试和测量、音频和射频的应用中将系统性能最大化。

对于需要正向和负向高性能轨的应用, 请考虑TI的正向高电压、超低噪音线性稳压器 **TPS7A49xx** 系列产品。



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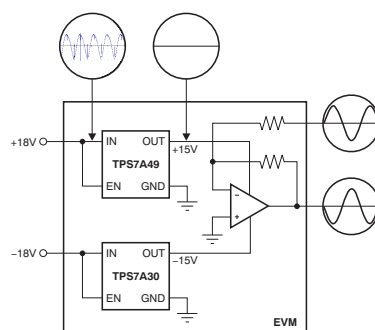
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English Data Sheet: **SBVS174**

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图 1. 典型应用

用于高性能模拟电路的后置 **DC/DC** 转换器调节



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>J</sub>	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	DGN	TPS7A3001MDGNTEP	PXCM	V62/11619-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN pin to GND pin	–36	+0.3	V
	OUT pin to GND pin	–33	+0.3	V
	OUT pin to IN pin	–0.3	+36	V
	FB pin to GND pin	–2	+0.3	V
	FB pin to IN pin	–0.3	+36	V
	EN pin to IN pin	–0.3	+36	V
	EN pin to GND pin	–36	+36	V
	NR/SS pin to IN pin	–0.3	+36	V
	NR/SS pin to GND pin	–2	+0.3	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T <sub>J</sub>	–55	+135	°C
	Storage, T <sub>stg</sub>	–65	+150	°C
Electrostatic discharge rating	Human body model (HBM)		1500	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS7A3001	UNITS
		DGN	
		8 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	69.3	°C/W
θ <sub>JC(top)</sub>	Junction-to-case(top) thermal resistance	40.3	
θ <sub>JB</sub>	Junction-to-board thermal resistance	39.0	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.4	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	38.7	
θ <sub>JC(bottom)</sub>	Junction-to-case(bottom) thermal resistance	17.8	

(1) 有关传统和新的热度的更多信息，请参阅 IC 封装热量 应用报告 [SPRA953](http://www.ti.com/lit/zip/spra953)。

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range		-36.0		-3.0	V
$V_{REF}$	Internal reference	$V_{NR/SS} = V_{REF}$	-1.22	-1.184	-1.142	V
$V_{OUT}$	Output voltage range <sup>(2)</sup>	$ V_{IN}  \geq  V_{OUT(NOM)}  + 1.0\text{V}$	-35.0		$V_{REF}$	V
	Nominal accuracy	$T_J = +25^\circ\text{C}$ , $ V_{IN}  =  V_{OUT(NOM)}  + 0.5\text{V}$	-1.5		+1.5	% $V_{OUT}$
	Overall accuracy	$ V_{OUT(NOM)}  + 1.0\text{V} \leq  V_{IN}  \leq 35\text{V}$ $1\text{mA} \leq I_{OUT} \leq 200\text{mA}$	-2.85		+2.85	% $V_{OUT}$
$\left  \frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}} \right $	Line regulation	$T_J = +25^\circ\text{C}$ , $ V_{OUT(NOM)}  + 1.0\text{V} \leq  V_{IN}  \leq 35\text{V}$		0.14		% $V_{OUT}$
$\left  \frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}} \right $	Load regulation	$T_J = +25^\circ\text{C}$ , $1\text{mA} \leq I_{OUT} \leq 200\text{mA}$		0.04		% $V_{OUT}$
$ V_{DO} $	Dropout voltage	$V_{IN} = 95\% V_{OUT(NOM)}$ , $I_{OUT} = 100\text{mA}$		216		mV
		$V_{IN} = 95\% V_{OUT(NOM)}$ , $I_{OUT} = 200\text{mA}$		325	600	mV
$I_{LIM}$	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$	220	330	500	mA
$I_{GND}$	Ground current	$I_{OUT} = 0\text{mA}$		55	100	$\mu\text{A}$
		$I_{OUT} = 100\text{mA}$		950		$\mu\text{A}$
$ I_{SHDN} $	Shutdown supply current	$V_{EN} = +0.4\text{V}$		1.0	3.0	$\mu\text{A}$
		$V_{EN} = -0.4\text{V}$		1.0	3.0	$\mu\text{A}$
$I_{FB}$	Feedback current <sup>(3)</sup>			14	100	nA
$ I_{EN} $	Enable current	$V_{EN} =  V_{IN}  =  V_{OUT(NOM)}  + 1.0\text{V}$		0.48	1.0	$\mu\text{A}$
		$V_{IN} = V_{EN} = -35\text{V}$		0.51	1.0	$\mu\text{A}$
		$V_{IN} = -35\text{V}$ , $V_{EN} = +15\text{V}$		0.50	1.2	$\mu\text{A}$
$V_{+EN\_HI}$	Positive enable high-level voltage	$T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$	+2.0		+15	V
$V_{+EN\_LO}$	Positive enable low-level voltage		0		+0.4	V
$V_{-EN\_HI}$	Negative enable high-level voltage		$V_{IN}$		-2.0	V
$V_{-EN\_LO}$	Negative enable low-level voltage		-0.4		0	V
$V_{NOISE}$	Output noise voltage	$V_{IN} = -3\text{V}$ , $V_{OUT(NOM)} = V_{REF}$ , $C_{OUT} = 10\mu\text{F}$ , $C_{NR/SS} = 10\text{nF}$ , BW = 10Hz to 100kHz		15.1		$\mu\text{V}_{RMS}$
		$V_{IN} = -6.2\text{V}$ , $V_{OUT(NOM)} = -5\text{V}$ , $C_{OUT} = 10\mu\text{F}$ , $C_{NR/SS} = C_{BYP}^{(4)} = 10\text{nF}$ , BW = 10Hz to 100kHz		17.5		$\mu\text{V}_{RMS}$
PSRR	Power-supply rejection ratio	$V_{IN} = -6.2\text{V}$ , $V_{OUT(NOM)} = -5\text{V}$ , $C_{OUT} = 10\mu\text{F}$ , $C_{NR/SS} = C_{BYP}^{(4)} = 10\text{nF}$ , $f = 120\text{Hz}$		72		dB
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		+170		$^\circ\text{C}$
		Reset, temperature decreasing		+150		$^\circ\text{C}$
$T_J$	Operating junction temperature range		-55		+125	$^\circ\text{C}$

(1) At operating conditions,  $V_{IN} \leq 0\text{V}$ ,  $V_{OUT(NOM)} \leq V_{REF} \leq 0\text{V}$ . At regulation,  $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$ .  $I_{OUT} > 0$  flows from OUT to IN.

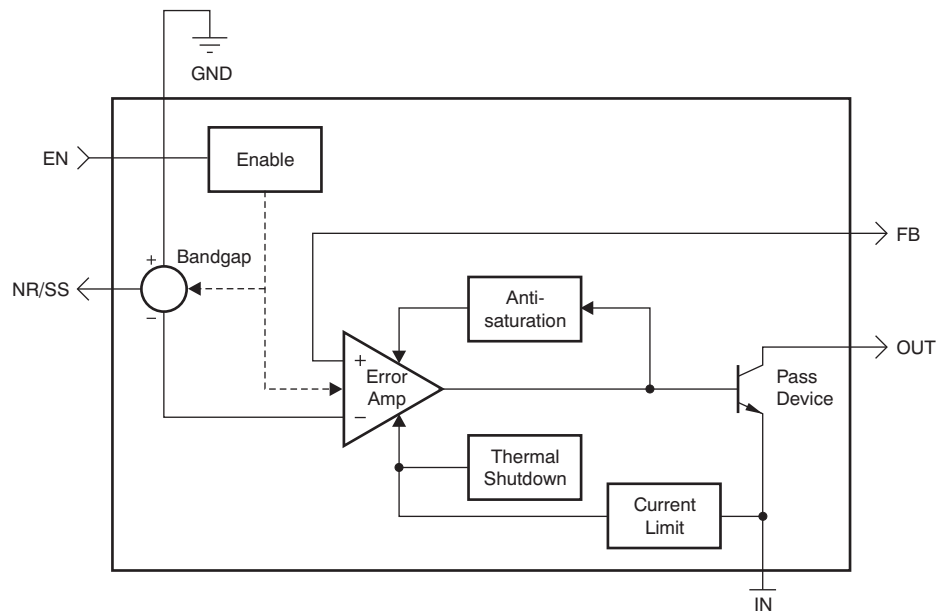
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than  $5\mu\text{A}$  is required.

(3)  $I_{FB} > 0$  flows into the device.

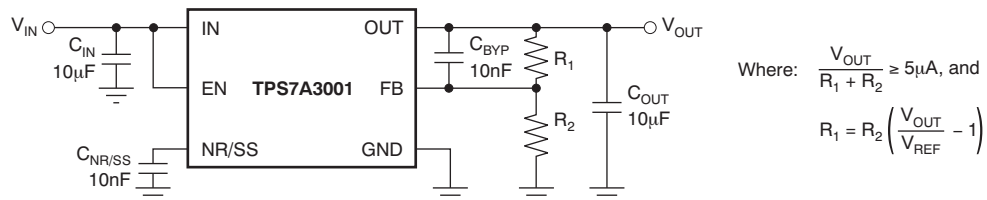
(4)  $C_{BYP}$  refers to a bypass capacitor connected to the FB and OUT pins.

## DEVICE INFORMATION

### FUNCTIONAL BLOCK DIAGRAM



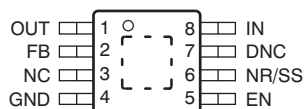
### TYPICAL APPLICATION CIRCUIT



**Maximize PSRR Performance and Minimize RMS Noise**

## PIN CONFIGURATION

### DGN PACKAGE MSOP-8 (TOP VIEW)



## PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
OUT	1	Regulator output. A capacitor $\geq 2.2\mu\text{F}$ must be tied from this pin to ground to assure stability.
FB	2	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	Not internally connected. This pin must either be left open or tied to GND.
GND	4	Ground
EN	5	This pin turns the regulator on or off. If $V_{\text{EN}} \geq V_{+\text{EN\_HI}}$ or $V_{\text{EN}} \leq V_{-\text{EN\_HI}}$ , the regulator is enabled. If $V_{+\text{EN\_LO}} \geq V_{\text{EN}} \geq V_{-\text{EN\_LO}}$ , the regulator is disabled. The EN pin can be connected to IN, if not used. $ V_{\text{EN}}  \leq  V_{\text{IN}} $ .
NR/SS	6	Noise reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
DNC	7	<b>DO NOT CONNECT.</b> Do not route this pin to any electrical net, not even GND or IN.
IN	8	Input supply
PowerPAD		Must either be left open or tied to GND. Solder to printed circuit board (PCB) plane to enhance thermal performance.

## TYPICAL CHARACTERISTICS

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

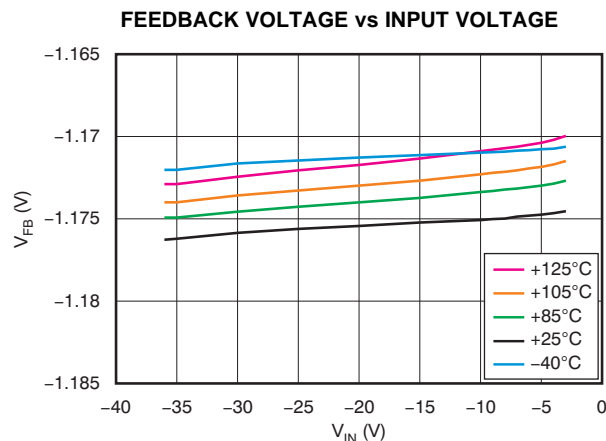


Figure 2.

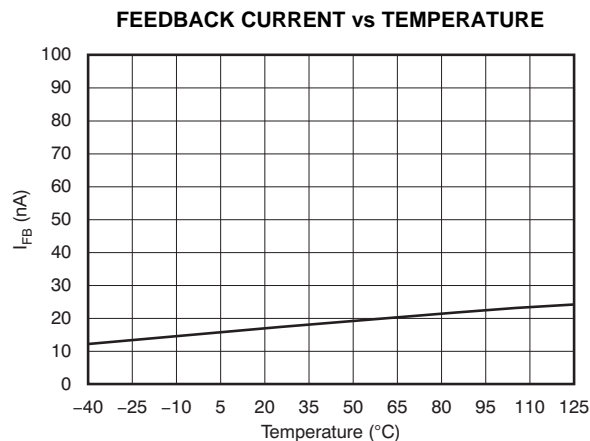


Figure 3.

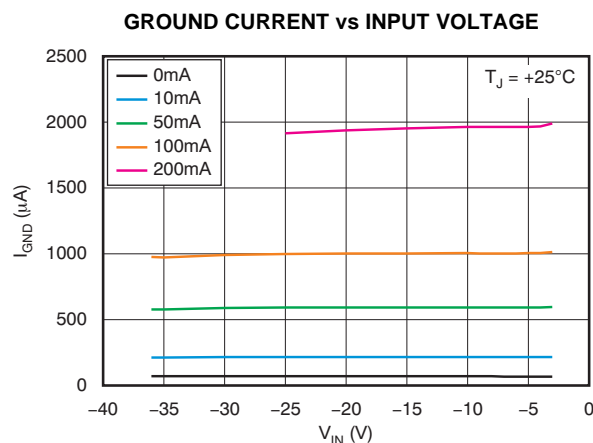


Figure 4.

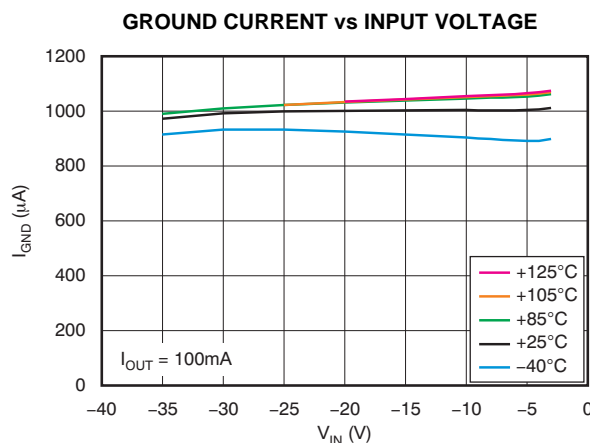


Figure 5.

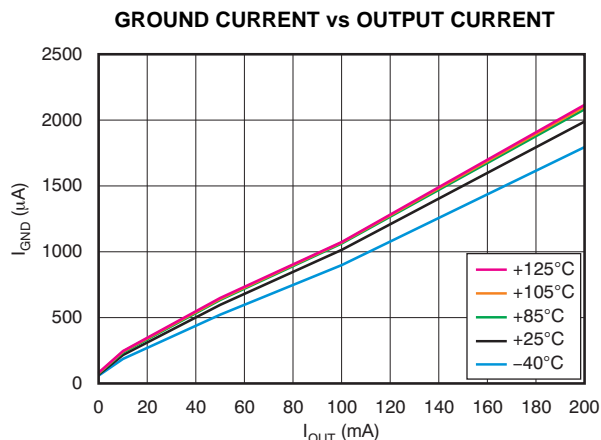


Figure 6.

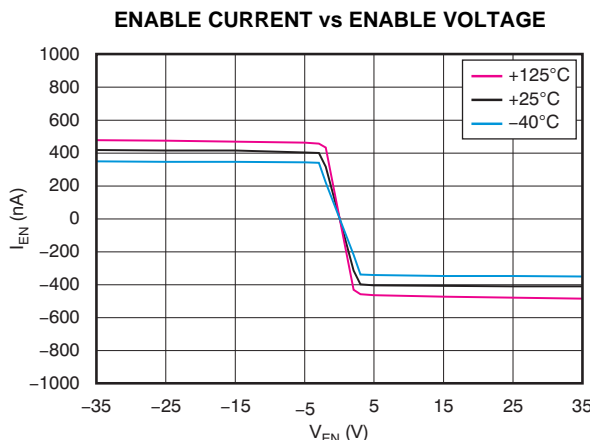


Figure 7.

### TYPICAL CHARACTERISTICS (continued)

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

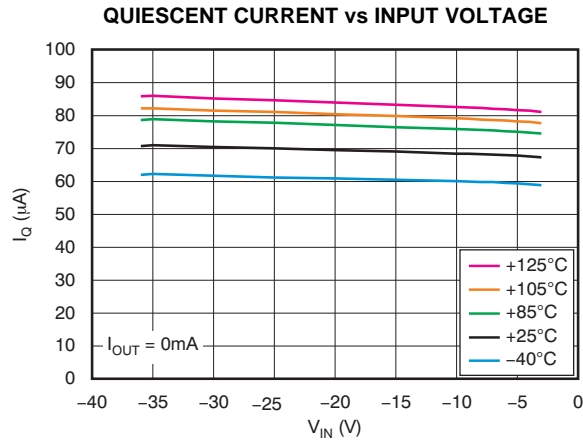


Figure 8.

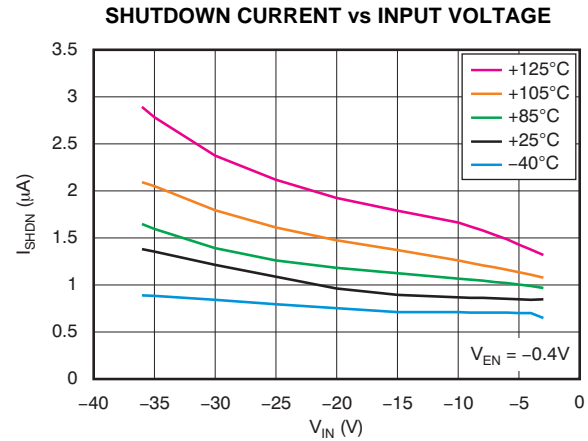


Figure 9.

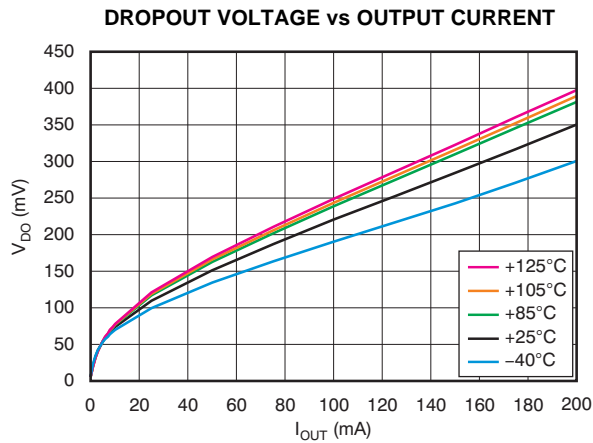


Figure 10.

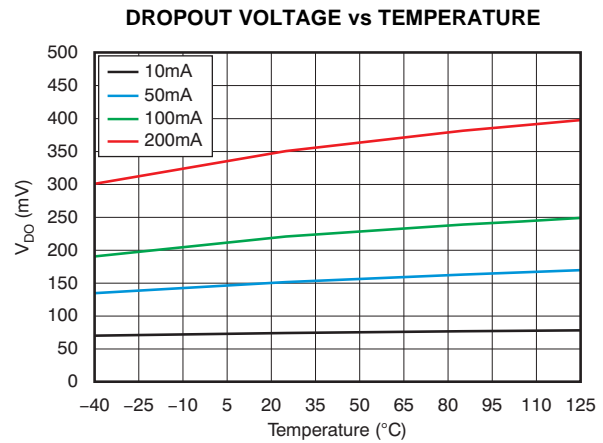


Figure 11.

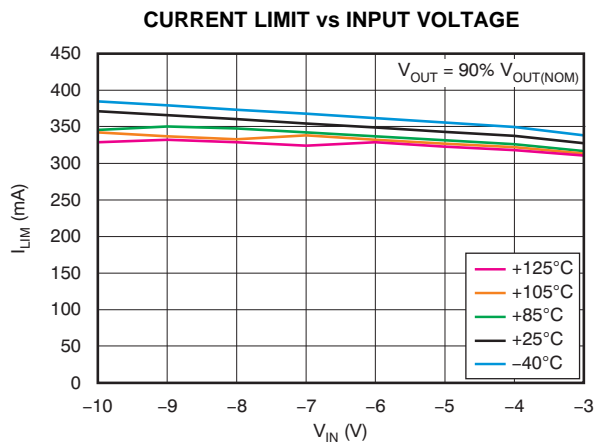


Figure 12.

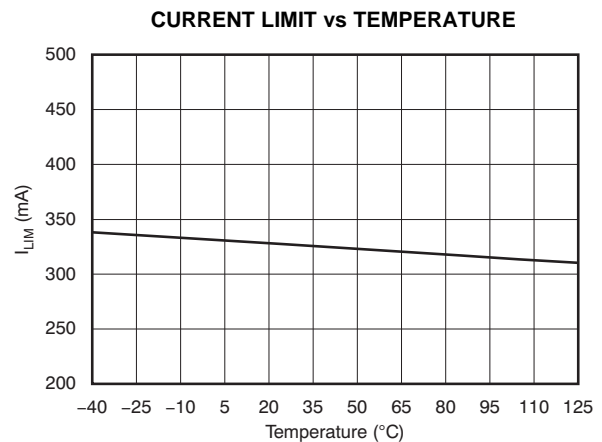


Figure 13.



## TYPICAL CHARACTERISTICS (continued)

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

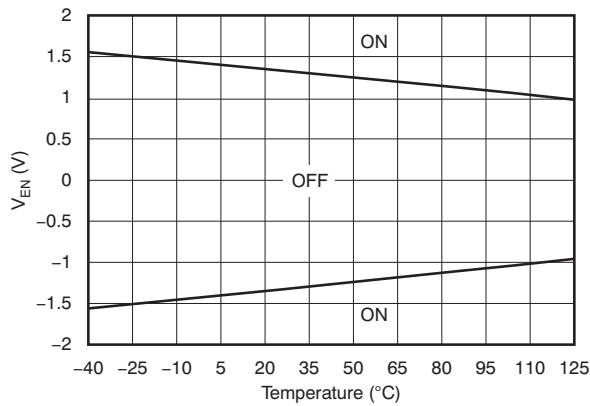


Figure 14.

POWER-SUPPLY REJECTION RATIO vs  $C_{OUT}$

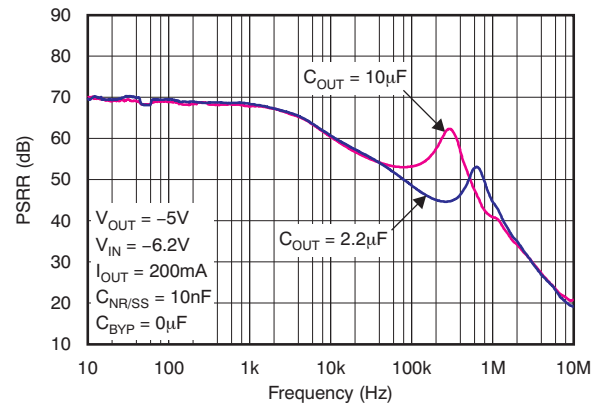


Figure 15.

LINE REGULATION

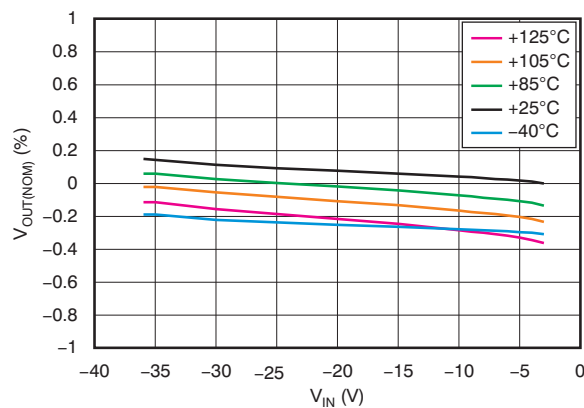


Figure 16.

POWER-SUPPLY REJECTION RATIO vs  $C_{NR/SS}$

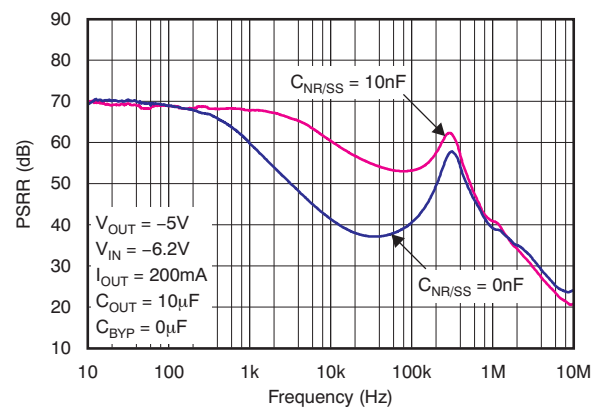


Figure 17.

LOAD REGULATION

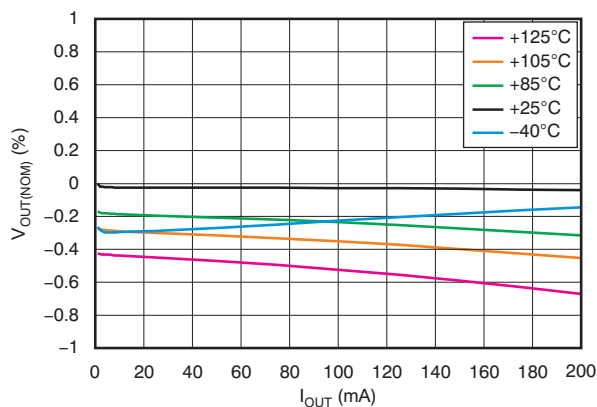


Figure 18.

POWER-SUPPLY REJECTION RATIO vs  $C_{BYP}$

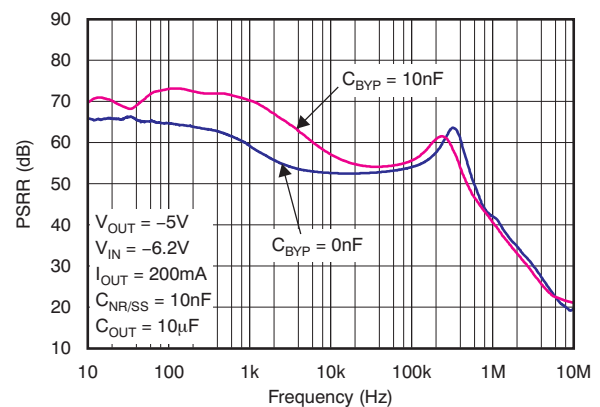
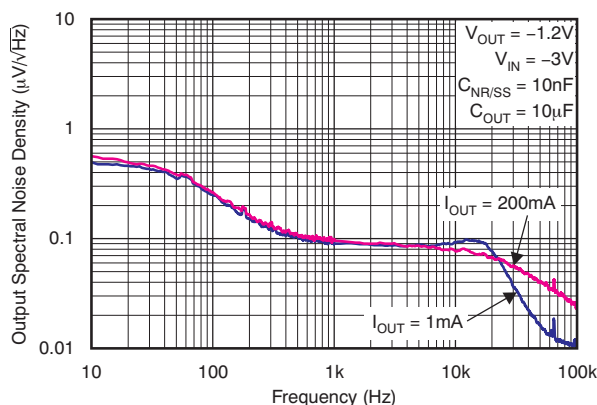


Figure 19.

### TYPICAL CHARACTERISTICS (continued)

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

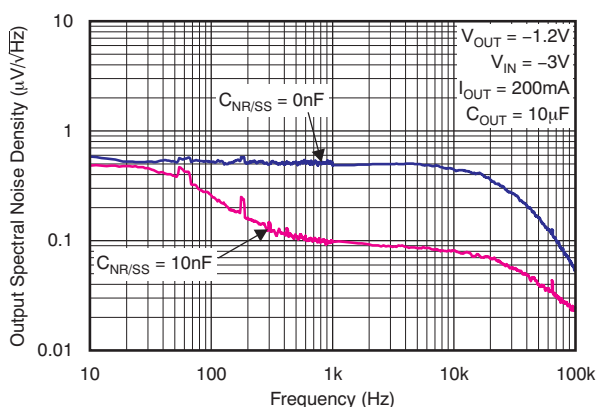
#### OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT



$I_{OUT}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.13	14.73
200mA	17.13	16.71

Figure 20.

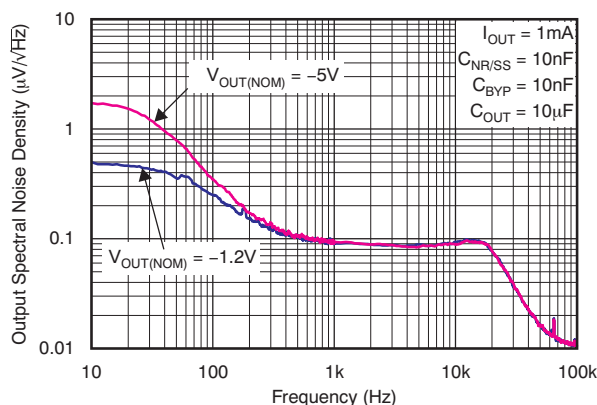
#### OUTPUT SPECTRAL NOISE DENSITY vs $C_{NR/SS}$



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	80.00	79.83
10nF	17.29	16.81

Figure 21.

#### OUTPUT SPECTRAL NOISE DENSITY vs $V_{OUT(NOM)}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
-5V	17.50	15.04
-1.2V	15.13	14.73

Figure 22.

## TYPICAL CHARACTERISTICS (continued)

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.

### CAPACITOR-PROGRAMMABLE SOFT START

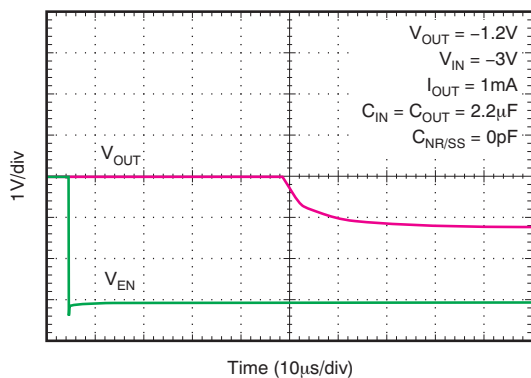


Figure 23.

### CAPACITOR-PROGRAMMABLE SOFT START

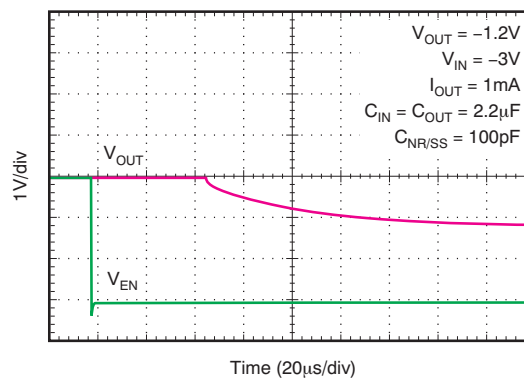


Figure 24.

### CAPACITOR-PROGRAMMABLE SOFT START

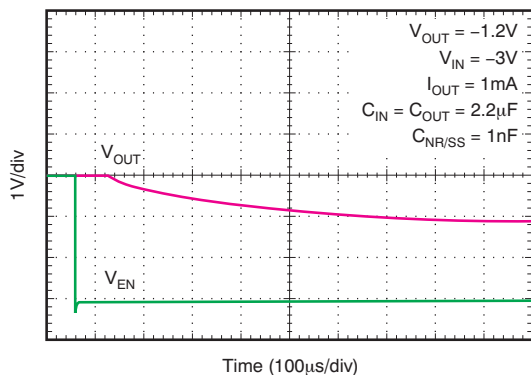


Figure 25.

### CAPACITOR-PROGRAMMABLE SOFT START

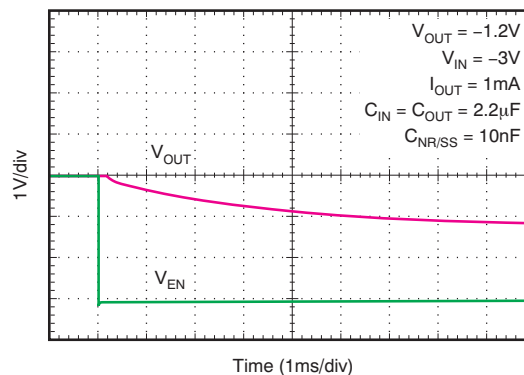


Figure 26.

### LINE TRANSIENT RESPONSE

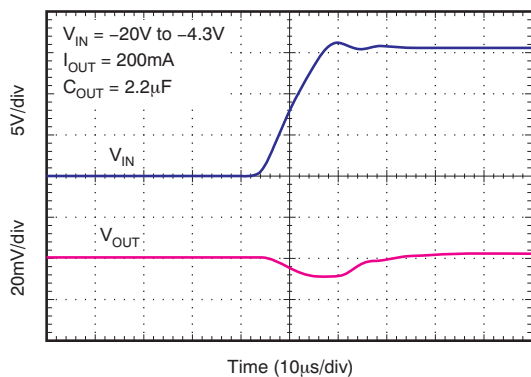


Figure 27.

### LINE TRANSIENT RESPONSE

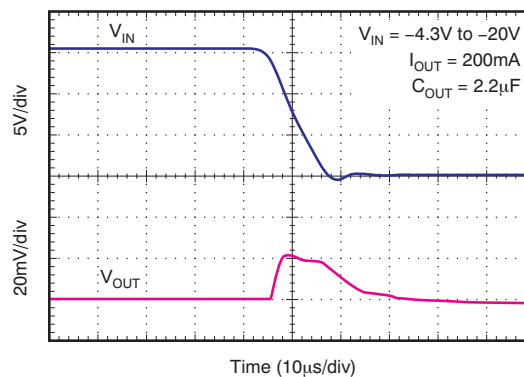
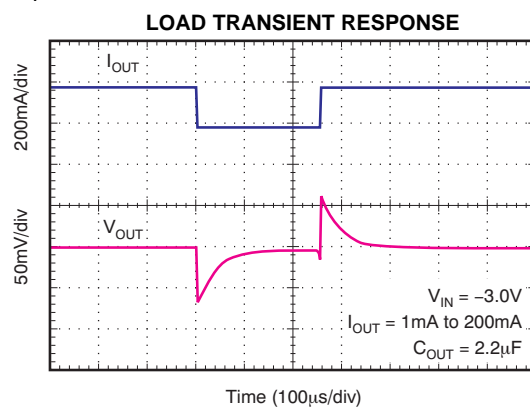


Figure 28.

### TYPICAL CHARACTERISTICS (continued)

At  $T_J = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$  or  $|V_{IN}| = 3.0\text{V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 2.2\mu\text{F}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR/SS} = 0\text{nF}$ , and the FB pin tied to OUT, unless otherwise noted.



**Figure 29.**

## THEORY OF OPERATION

### GENERAL DESCRIPTION

The TPS7A3001 belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal performance MSOP-8 with PowerPAD package make this device ideal for high-performance analog applications.

### ADJUSTABLE OPERATION

The TPS7A3001 has an output voltage range of  $-1.174$  to  $-35$ V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 30.

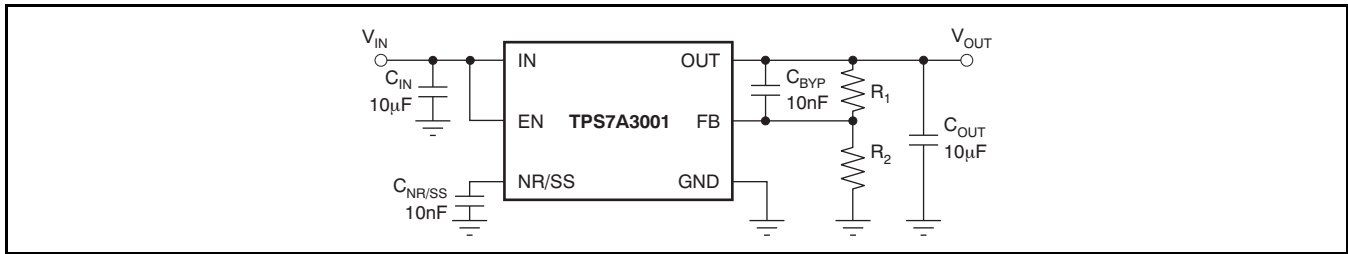


Figure 30. Adjustable Operation for Maximum AC Performance

$R_1$  and  $R_2$  can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than  $5\mu\text{A}$ .

$$R_1 = R_2 \left( \frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right), \text{ where } \frac{V_{\text{OUT}}}{R_1 + R_2} \geq 5\mu\text{A} \quad (1)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

### ENABLE PIN OPERATION

The TPS7A3001 provides a dual polarity enable pin (EN) that turns on the regulator when  $|V_{\text{EN}}| > 2.0\text{V}$ , whether the voltage is positive or negative, as shown in Figure 31.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as  $V_{\text{IN}}$ , or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

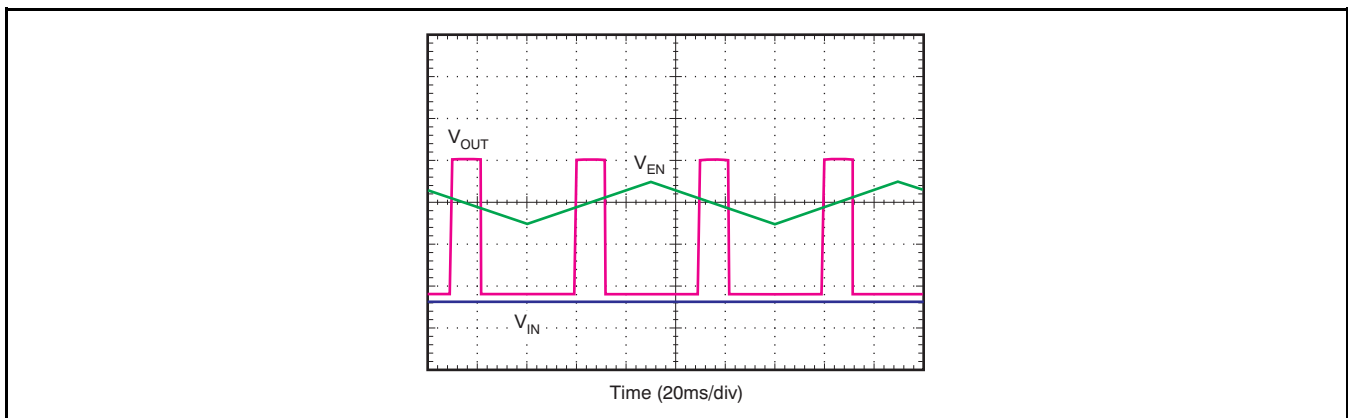


Figure 31. Enable Pin Positive/Negative Threshold

## CAPACITOR RECOMMENDATIONS

Low ESR capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

## INPUT AND OUTPUT CAPACITOR REQUIREMENTS

This negative, high-voltage linear regulator achieves stability with a minimum input and output capacitance of 2.2 $\mu$ F; however, it is highly recommended to use a 10 $\mu$ F capacitor to maximize ac performance.

## NOISE REDUCTION AND BYPASS CAPACITOR REQUIREMENTS

Although noise reduction and bypass capacitors ( $C_{NR/SS}$  and  $C_{BYP}$ , respectively) are not needed to achieve stability, it is highly recommended to use 0.01 $\mu$ F capacitors to minimize noise and maximize ac performance.

## MAXIMUM AC PERFORMANCE

In order to maximize noise and PSRR performance, it is recommended to include 10 $\mu$ F or higher input and output capacitors, and 0.01 $\mu$ F noise reduction and bypass capacitors, as shown in [Figure 30](#). The solution shown delivers minimum noise levels of 15.1 $\mu$ V<sub>RMS</sub> and power-supply rejection levels above 55dB from 10Hz to 700kHz; see [Figure 19](#) and [Figure 20](#).

## OUTPUT NOISE

The TPS7A3001 provides low output noise when a noise reduction capacitor ( $C_{NR/SS}$ ) is used.

The noise reduction capacitor serves as a filter for the internal reference. By using a 0.01 $\mu$ F noise reduction capacitor, the output noise is reduced by almost 80% (from 80 $\mu$ V<sub>RMS</sub> to 17 $\mu$ V<sub>RMS</sub>); see [Figure 21](#).

TPS7A3001 low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

## POWER-SUPPLY REJECTION

The 0.01 $\mu$ F noise reduction capacitor greatly improves TPS7A3001 power-supply rejection, achieving up to 20dB of additional power-supply rejection for frequencies between 110Hz and 400kHz.

Additionally, ac performance can be maximized by adding a 0.01 $\mu$ F bypass capacitor ( $C_{BYP}$ ) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10Hz to 200kHz; see [Figure 19](#).

The very high power-supply rejection of the TPS7A3001 makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

## TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

## APPLICATION INFORMATION

### POWER FOR PRECISION ANALOG

One of the primary TPS7A3001 applications is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

In conjunction with its positive counterpart, the [TPS7A49xx](#) family of positive high-voltage linear regulators, this negative high voltage linear regulator provides ultralow noise positive and negative voltage rails to high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

### POST DC/DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC/DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A3001 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post dc/dc converter filtering, as shown in [Figure 32](#). It is highly recommended to use the maximum performance schematic shown in [Figure 30](#). Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in [Figure 19](#).

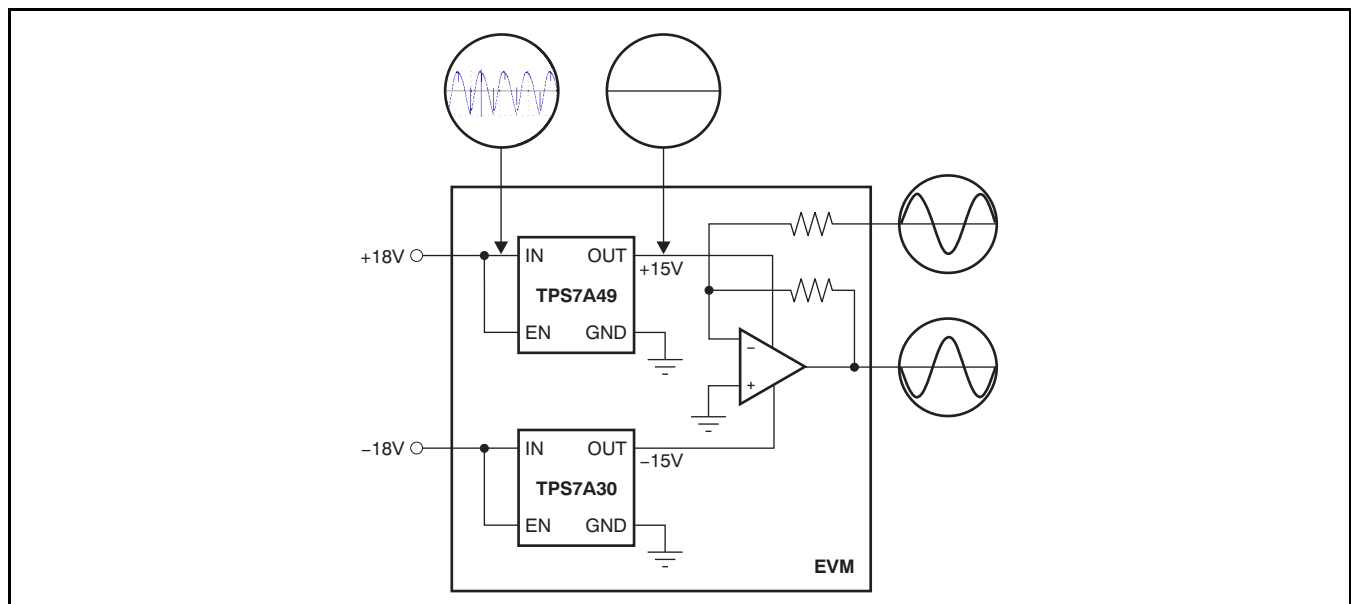


Figure 32. Post DC/DC Converter Regulation to High-Performance Analog Circuitry

### AUDIO APPLICATIONS

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20Hz to 20kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio ( $> 55\text{dB}$ ) and low noise at the audio band of the TPS7A3001 maximize performance for audio applications; see [Figure 19](#).

## LAYOUT

### PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A3001 are available at the end of this product datasheet and at [www.ti.com](http://www.ti.com).

### BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor ( $C_{IN}$ ,  $C_{OUT}$ ,  $C_{NR/SS}$ ,  $C_{BYP}$ ) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product datasheet, use the same layout pattern used for TPS7A30 evaluation board, available at [www.ti.com](http://www.ti.com).

### THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A3001 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A3001 into thermal shutdown degrades device reliability.

### POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

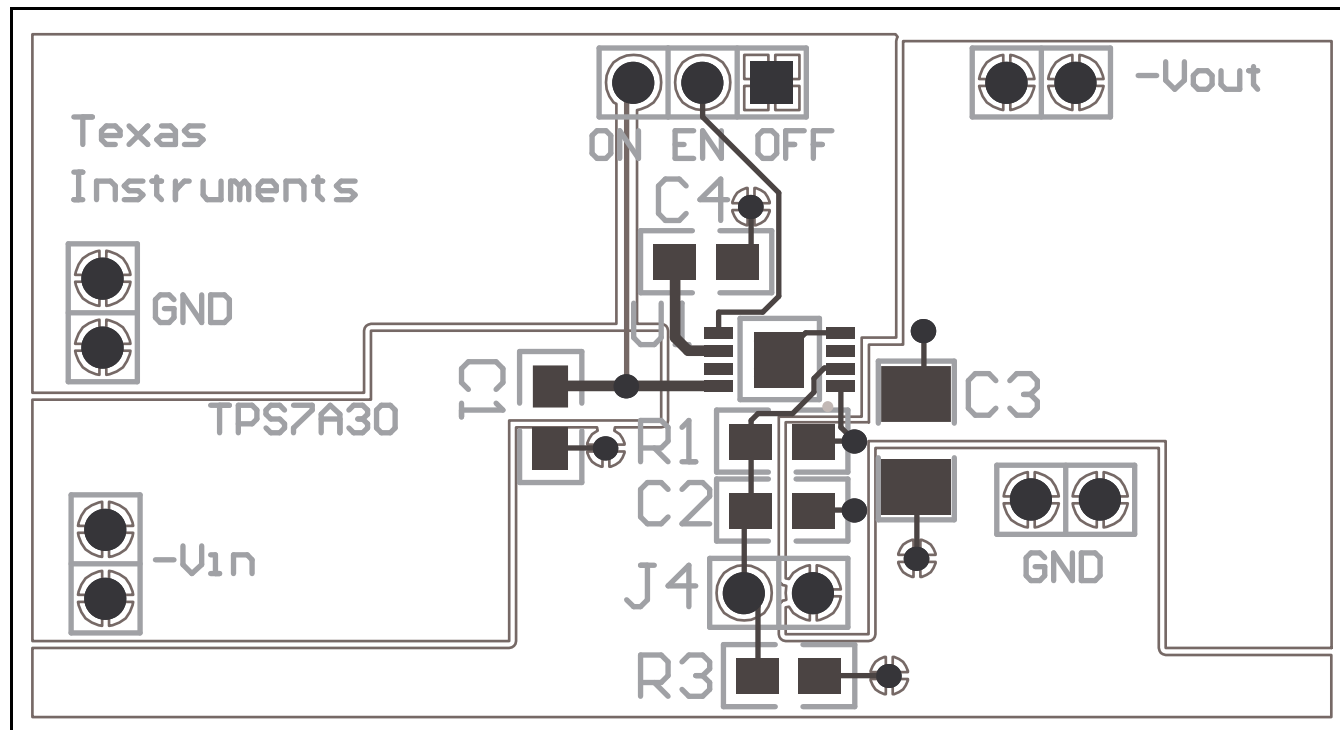
### SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

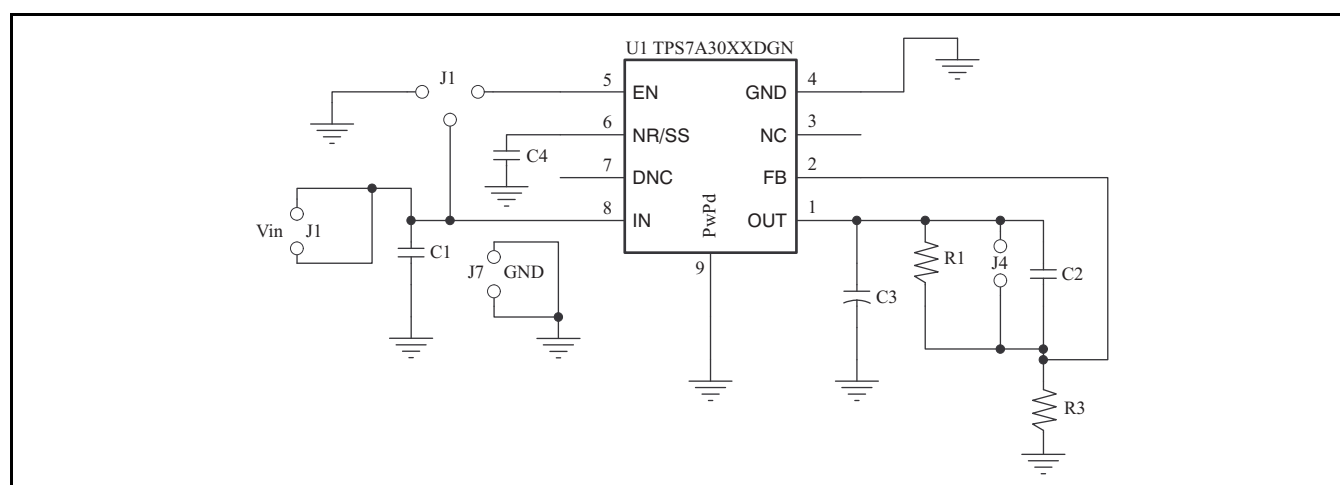


The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

It may be possible to obtain acceptable performance with alternate PCB layouts; however, the layout shown in Figure 33 and the schematic shown in Figure 34 have been shown to produce good results and are meant as a guideline.



**Figure 33. PCB Layout Example**



**Figure 34. Schematic for PCB Layout Example**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS7A3001MDGNTEP	ACTIVE	MSOP- PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
V62/11619-01XE	ACTIVE	MSOP- PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TPS7A3001-EP :**

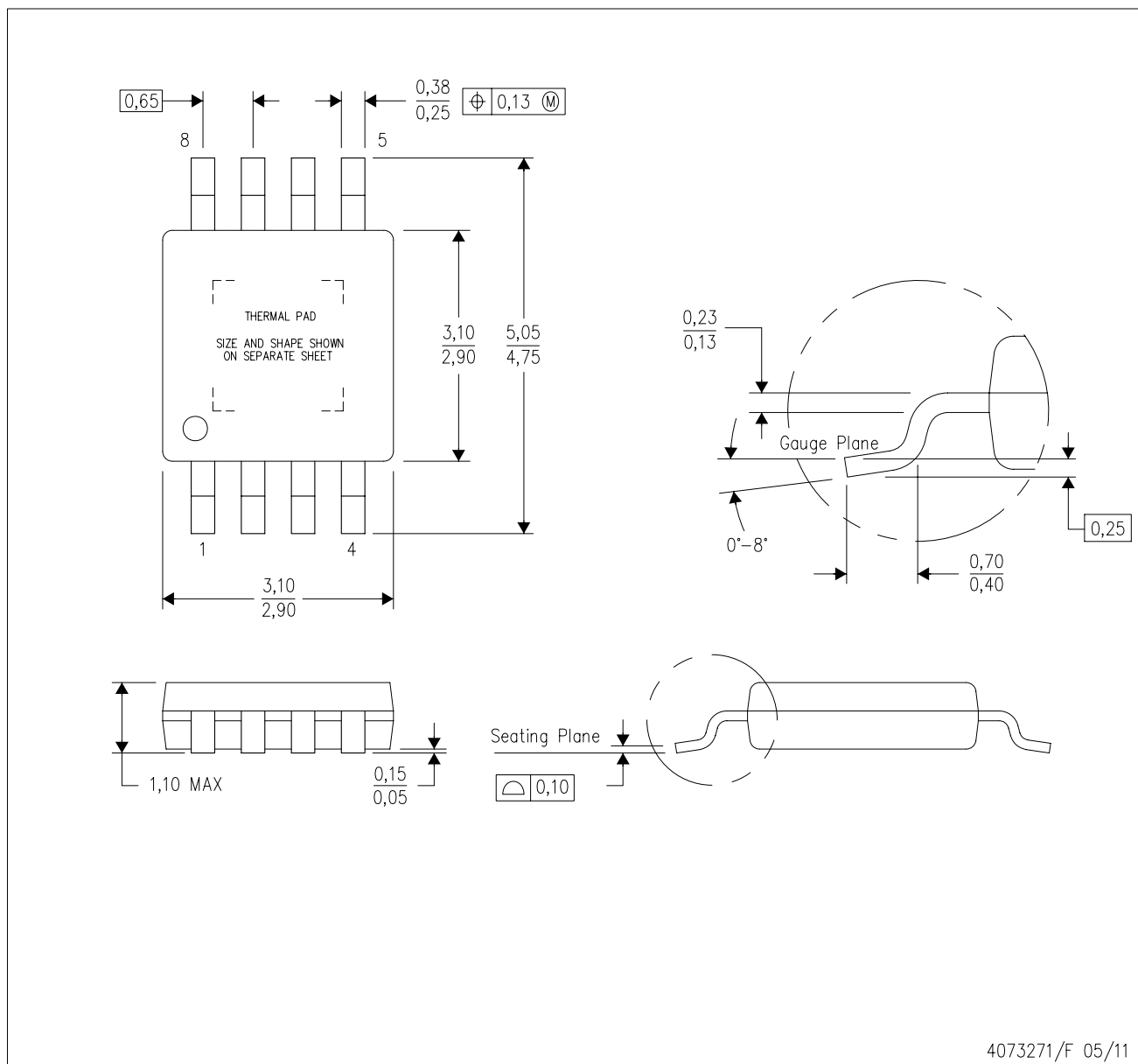
- Catalog: [TPS7A3001](#)

NOTE: Qualified Version Definitions:

- 
- Catalog - TI's standard catalog product

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



4073271/F 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

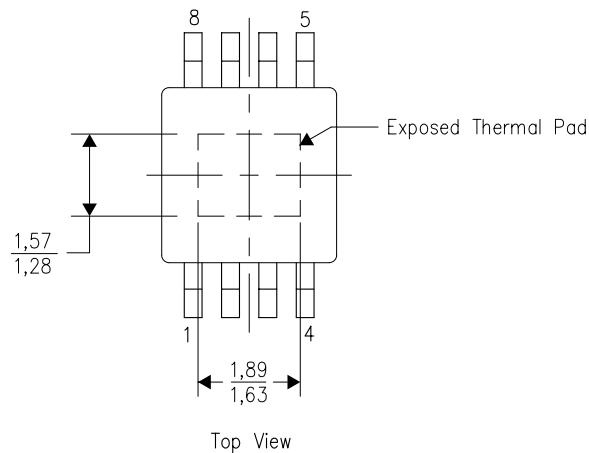
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

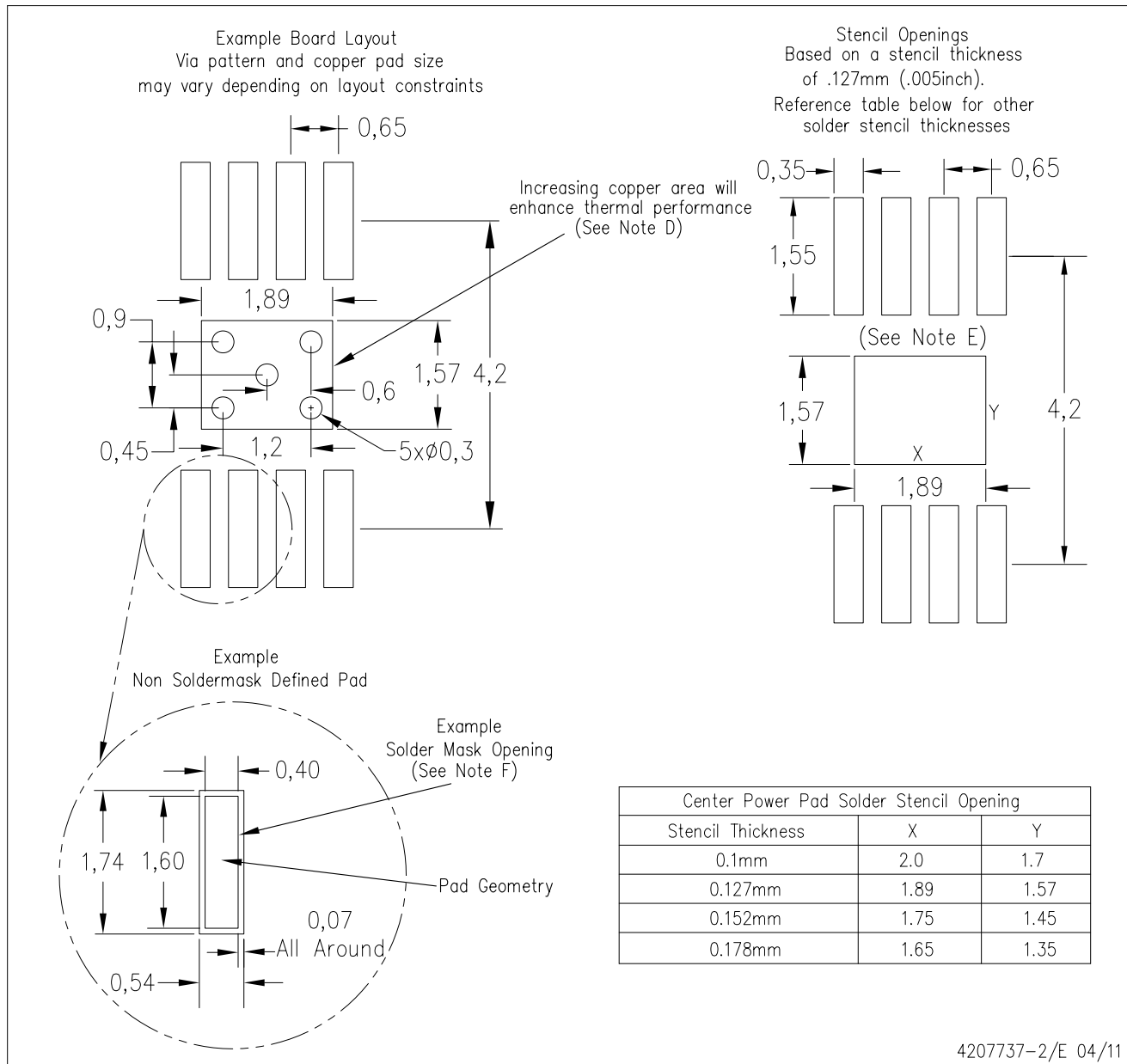
4206323-2/H 05/11

NOTE: All linear dimensions are in millimeters

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DGN (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">http://www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">http://www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">http://www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">http://www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">http://www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">http://www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
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