

1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the JK Electronics technical support website (<http://cafe.naver.com/avrstudio>).

These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers is the number one influence. If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at <mailto:master@deviceshop.net>.

1.3. Limited Warranty

JK Electronics warrants this product to be free of defects in material and workmanship for a period of six month from date of buy. During this warranty period JK Electronics will repair or replace the defective unit in accordance with the following process:

This limited warranty does not cover damages resulting from lightning or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit .In no event shall JK Electronics be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this products.

Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact JK Electronics to arrange for any repair service and to obtain repair charge information.

4. License of this manual

이 매뉴얼의 JK전자에 의해서 번역, 수정, 작성 되었고 소유권 또한 JK전자의 것입니다.
소유권자의 허가를 받지 않고 무단으로 수정, 삭제하거나 배포 할 수 없습니다.

2010 Copyright by JK Electronics.

1. 6410 Development Board Overview	4
1.1 The 6410 development board as a whole description.....	4
1.2 6410 development board optional hardware components	5
1.3 E6CORE core board Function	5
1.4 Pin definition of the core board and package description	7
1.4.1 The definition of the core panel pin	7
1.4.2 Core Board Package Description.....	7
2. 6410 development board hardware, instructions	8
2.1 The need to be clearly points.....	8
2.2 The development board interface definition and use	9
2.2.1 Debug serial port pin definition and the use	9
2.2.2 USB-to-serial cable connected with the development board.....	9
2.2.3 RJ45 interface definition and access	10
2.2.4 Definition analog video interface pins were used by.....	11
2.2.5 USB interface definition	13
2.2.6 LCD Interface Definition.....	15
2.2.7 Camera Interface Definition	15
2.2.8 The definition of external expansion interface pins.....	16
2.2.9 SD Card interface definitions and connection.....	16
2.2.10 Audio Interface Overview and Definitions.....	17
2.3 BOOT switch startup configuration instructions.....	18
2.3.1 Hardware connection diagram	18
2.3.2 WinCE Boot startup configuration	19
2.3.3 Linux boot startup configuration	20
2.3.4 Android boot startup configuration	20
2.4 Definition and pin-board push buttons connected	21
2.5 LED lights connected	22
2.6 RESET Reset	22
2.7 System memory allocation map	23
2.8 WIFI module interface definition	23
2.9 GPRS / GSM Module Interface Definition	27
2.10 GPS Module interface definitions.....	29
2.11 Development Board Serial distribution of	30
3. Hardware Design and Analysis.....	31
3.1 S3C6410 processor performance.....	31

3.2 CPU does not use pin approach.....	32
3.3 CPU power supply pin's supply area.....	33
3.4 Design and Analysis of Memory.....	33
3.5 NAND FLASH and NOR FLASH difference between	37
3.6 NAND FLASH MLC and SLC the difference between	40
3.7 NAND FLASH Circuit Design and Analysis of.....	42
3.8 Realization of the power management unit.....	45
3.9 6410 clock signal generation	47
3.10 Design and Analysis of network chips DM9000.....	48
3.11 Audio Design and Analysis.....	50
3.12 WIFI Circuit Design	54
3.13 GPS module circuit design	55
3.14 GPRS / GSM hardware design and analysis	55
3.15 Camera Circuit Design.....	59
3.16 Analog camera interface	61
3.17 RS485 Interface	62
3.18 CAN bus interface	63
4. Analysis of the core board PCB.....	64
4.1 Core PCB board width line of conventional distance	64
4.2 Blind-hole size and pore distribution of buried	66
4.3 DDR cabling requirements and specifications	66
4.4 USB differential alignment rules	67
4.5 Structure of the core plate laminate.....	68
4.6 core plate impedance control	69
5. Tool software and driver installation instructions	77
5.1 DNW0.6C instructions for use	77
5.2 USB Driver Installation	80
5.3 DNW0.6C in the use of USB download	84

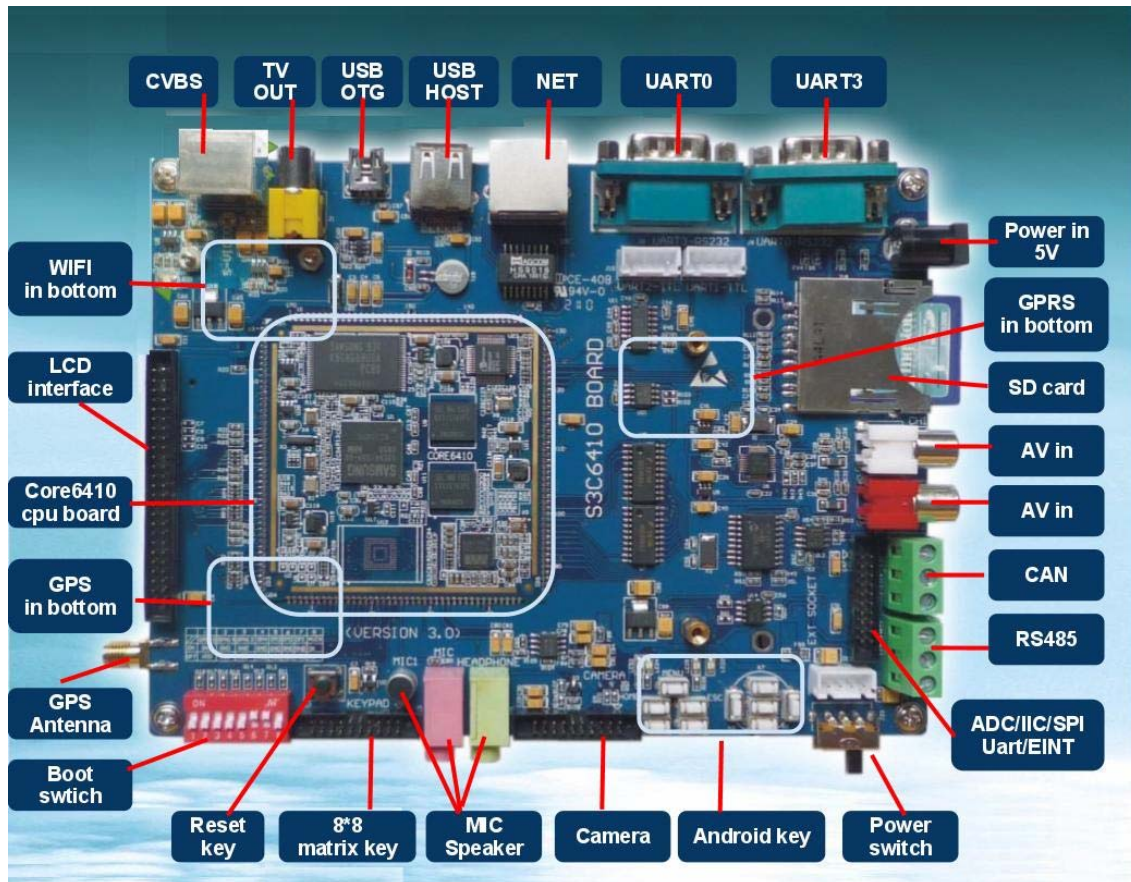
1. 6410 Development Board Overview

1.1 The 6410 development board as a whole description

Real6410 from the floor and the core panel of two parts. The core board named E6Core, E6Core is a mature core of plates used in the actual product.

6410 development board has the following characteristics :

- (1) 24-bit RGB interface and the interface leads to IIC, SPI, TOUCH bus.
- (2) CVBS, TV out interface (amplified by the amplification unit output)
- (3) USB Host 1.1 Interface
- (4) USB OTG 2.0 interface
- (5) RJ45 100M network interfaces, external 1:1.414 transformer
- (6) RS232 interface * 2Port
- (7) External expansion SPI, IIC, ADC (four), external interrupt (3 Road), two-way TTL Uart interface, the above things except ADC can be used as an IO port.
- (8) SD card interface
- (9) 10 Rd phone keypad design
- (10) Two-way LED instructions
- (11) Reset button
- (12) 1.5 W speaker interface
- (13) MIC input circuit
- (14) Headphone jacks (PJ-327)
- (15) Boot preparation switch
- (16) Onboard the GPRS SIM300 module
- (17) Onboard GPS module, antenna interface
- (18) SDIO WIFI interface (using the miniPCI Interface Block)
- (19) 6410 Development Board Images shown in Figure 2



[Figure 2]

1.2 6410 development board optional hardware components

6410 optional external hardware module includes the following

- (1) 4.3 "LCD (with Touch)
- (2) 5.0 "LCD (with Touch)
- (3) 7.0 "LCD (with Touch)
- (4) OV9650 1.3M pixels camera
- (5) OV3640 with a digital camera with zoom

1.3 E6CORE core board Function

E6CORE core board has in the 6cm * 6 cm area on the integrated Samsang's S3C6410 chip, two 16-bit 128M Byte mobile DDR, 1G Byte of the MLC-based NandFlash K9G8G08, power management unit, 100M to state the DAVICOM company's network chip DM9000AEP , with dual input and output of Wolfson's WM9713, SandDisk the iNand Flash, core board 170-pin 2.0mm hole leads to a stamp.



Core board kind shown in Figure 4, the following functions:

- (1) 667 MHz S3C6410X
- (2) 256 Mbyte mobile DDR
- (3) 1G Byte NandFlash
- (4) A separate power input management unit
- (5) Support the Phone connection mode audio input and output management unit
- (6) iNAND Flash support
- (7) 170 Pin-hole leads Stamps

Special statement :

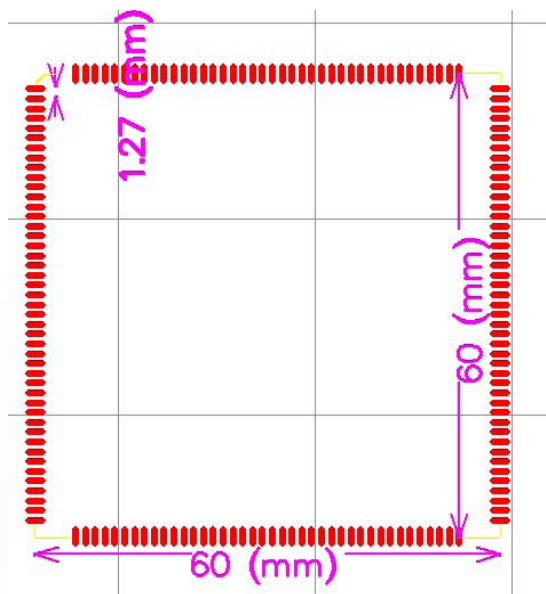
- (1) iNAND in E6CORE the development of the core board is not welding, welding on their own if necessary, the driver temporarily without debugging, Should the use of support, depending on method of Samsung's moviNAND self-debugging.
- (2) In the case without notice to customers, mobile DDR can be changed according to the actual conditions of modern semiconductor-compatible models. Nominal 256M Byte does not change, speed and temperature range does not change.

1.4 Pin definition of the core board and package description

1.4.1 The definition of the core panel pin

Would you reference schematic please.

1.4.2 Core Board Package Description



Thickness : 2.85mm

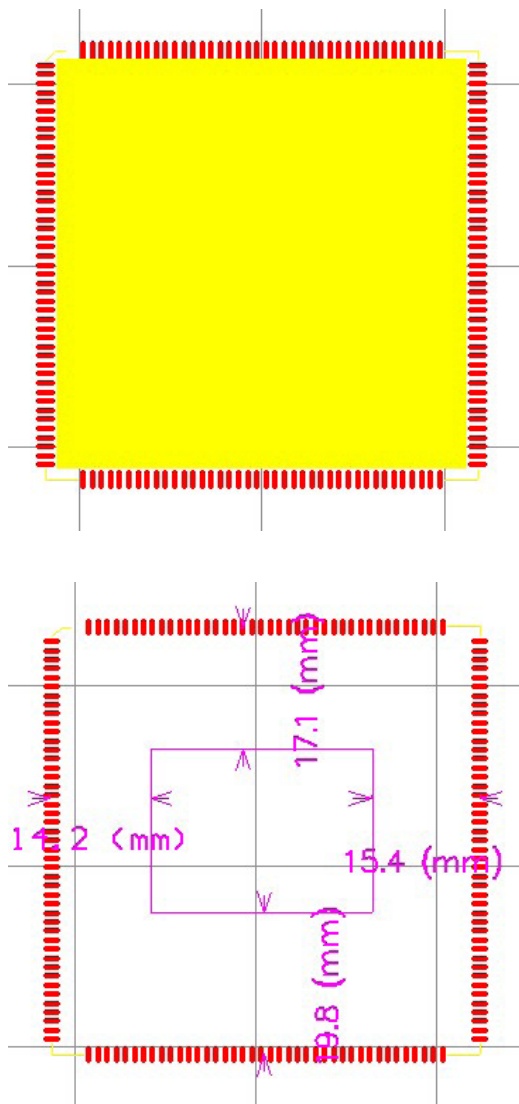
Length : 60mm

Width : 60mm

PIN pitch : 1.27mm

Recommended packages are as follows

- (1) Require an additional floor in the core after the screen printing plate in order to prevent short-circuit the core board and the through-hole as shown in Figure 6
- (2) required as shown in Figure 7, in the bottom layer of open-frame mechanical



Electronics

2. 6410 development board hardware, instructions

2.1 The need to be clearly points

- (1) Real6410 development board used is a 5V/2A power supply, power supply after the confirmation box or a 3A power supply 5V/2A
- (2) Real6410 development board which leads to the serial port and PC serial port pin definition of the same machine, it provides cross-wire serial line, if you use USB-serial cable, please use our cross-wire connection provided by the development board, and then with the USB transfer serial cable connected to the last access to a computer.
- (3) provided by the cable can be directly connected to HUB or PC, development board adaptive
- (4) Check whether the module carried by complete.

2.2 The development board interface definition and use

2.2.1 Debug serial port pin definition and the use

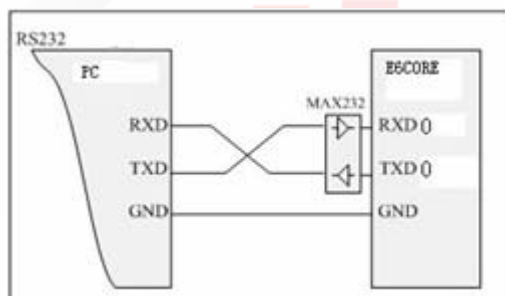
Core TXD0 and RXD0 then CPU-TXD0 and RXD0, that the use of the 6410's Uart0 after the PC connected via RS232, development board the use of public-seat DB9 interface, serial port pin definitions shown in Figure 8



[Figure 8]

1:GND , 2:RXD, 3:TXD, 4:NC, 5:NC, 6:NC, 7:NC, 8:NC, 9:NC

Connected with the PC as shown in Figure 9



[Figure 9]

2.2.2 USB-to-serial cable connected with the development board

General notebook no longer have serial ports, then need to use the USB-serial port to communicate with development board connected to the market mostly moved out of USB-serial port is a standard RS232 DB9 interface on the PC, as shown in Figure 9, the interface is still time need to use to provide cross-line and the development board is connected, and then connected to the serial port on the roll-out.

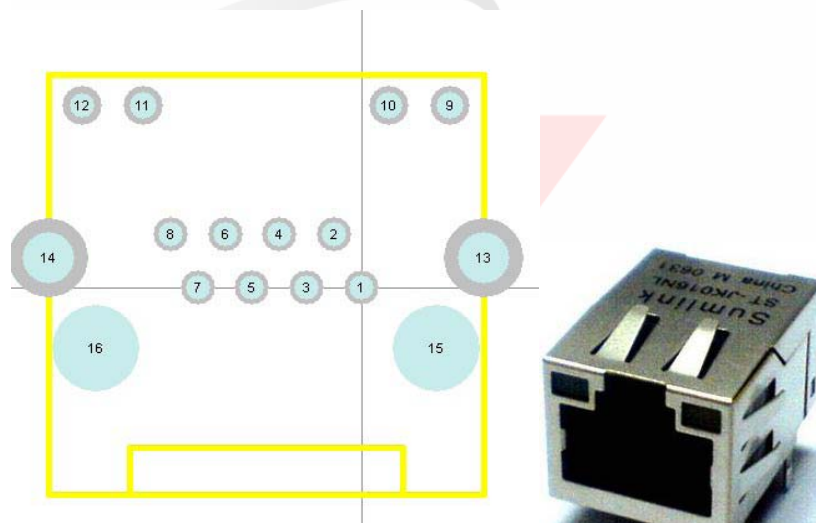


Is equivalent to a standard PC, serial port, still need to cross-wire connection development board

2.2.3 RJ45 interface definition and access

Development board using a standard RJ45 interface, as shown in Figure 11

The pins are defined as follows



Pin	Name	Description
1	TX+	Tranceive Data+
2	TX-	Tranceive Data-
3	RX+	Receive Data+
4	n/c	Not connected
5	n/c	Not connected
6	RX-	Receive Data-
7	n/c	Not connected
8	n/c	Not connected

Extended definition

- (9) LED connection indicator
- (10) LED power indicator Power Connection
- (11) LED speed indicator
- (12) LED speed indicator Power Supply
- (13) GND
- (14) GND

As the development board used in transformers for the HS9016, HS9016 has the auto rotate feature, which can automatically identify and automatically send and receive signals to adapt, which allows us to use the crossover cable or straight-through cable connection routing, HUB or PC.

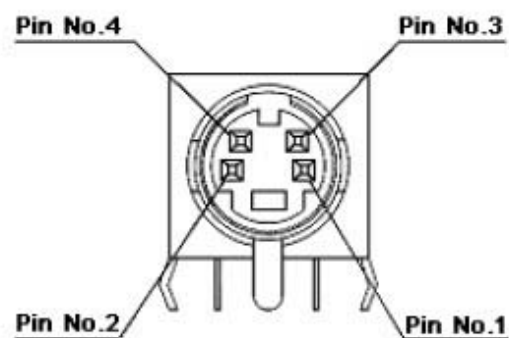
Changliang green, yellow light flashing as normal communication state.

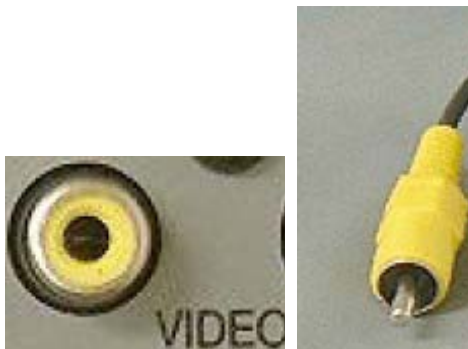
2.2.4 Definition analog video interface pins were used by

Development board provides two analog video output interfaces, that is, RCA interface, and S-Video interfaces, icons are as follows



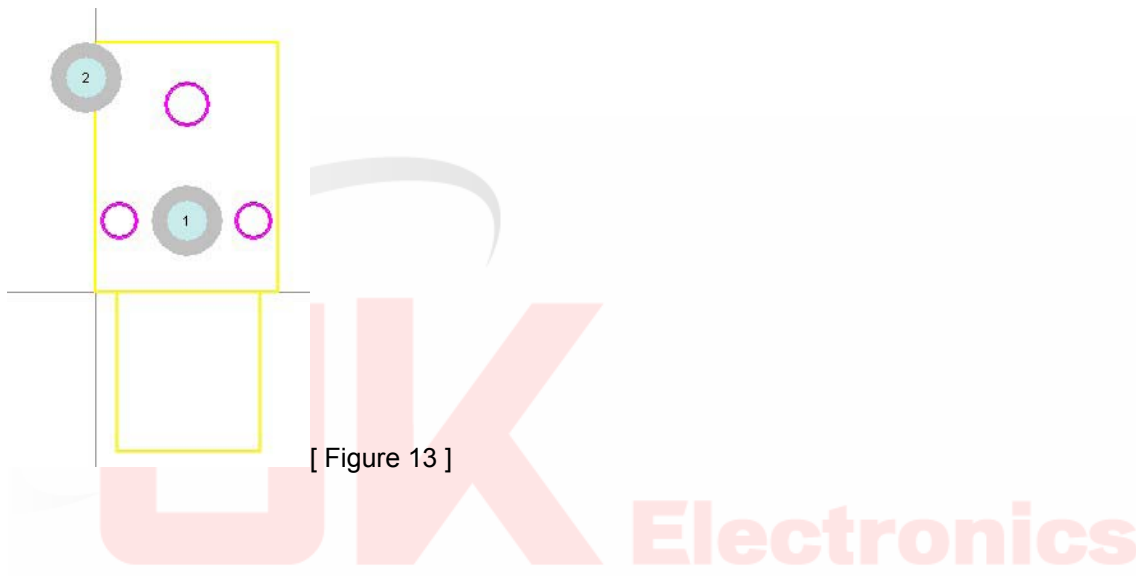
[S-Video interface]





RCA interface

RCA interface, that is, CVBS interface, the transmission of composite video signal, usually the color is yellow, can be directly connected to the TV's yellow RCA port. The package as shown in Figure 13



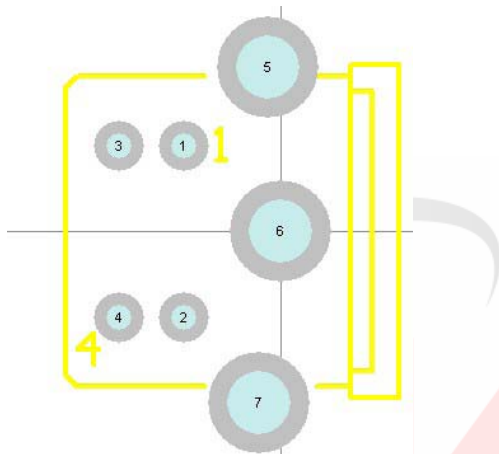
[Figure 13]



RCA Pin Definition

- (1) The video signal
- (2) GND

As CVBS interface transmission, the video signal luminance and chrominance signals of the tone set with the way law spectrum combined together, will lead to bright, color crosstalk, thus affecting the clarity of the image, while the S-Video Isolation and luminance signal Y and color degree of signal C, the two separate transmission makes the luminance signal from the interference of color signals, so S-Video output, more crisp clear images



CVBS Pin definition

- (1) CGND chroma signal GND
- (2) YGND luminance signal GND
- (3) Y luminance signal
- (4) C chroma signal
- (5) NC mounting hole
- (6) NC mounting hole
- (7) NC mounting hole

2.2.5 USB interface definition

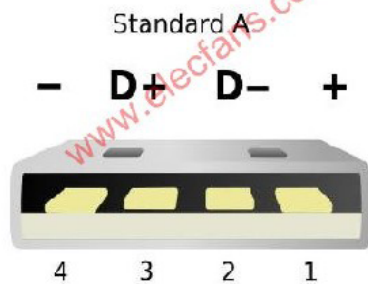
Development board provides two USB interfaces, OTG and USB HOST interface



USB OTG and Pin map

Pin	Name	Color	Description
1	VCC	Red	+5 V
2	D-	White	Data -
3	D+	Green	Data +
4	ID	none	permits distinction of Micro-A- and Micro-B-Plug Type A: connected to Ground Type B: not connected
5	GND	Black	Signal Grou

USB

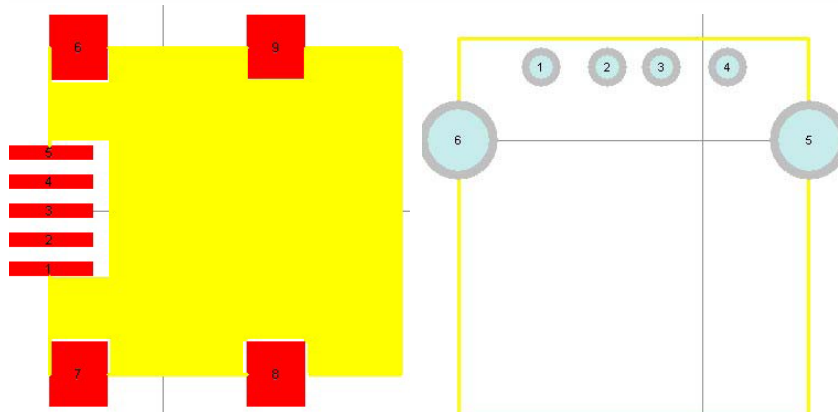


USB HOST device and Pin map

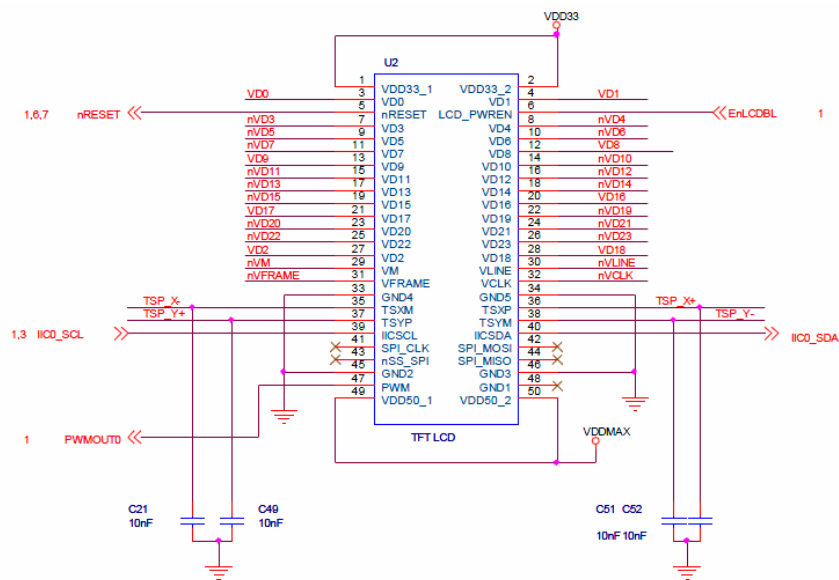
USB PIN Definition

Pin	Name	Cable color	Description
1	VCC	Red	+5V
2	D-	White	Data
3	D+	Green	Data +
4	GND	Black	Ground

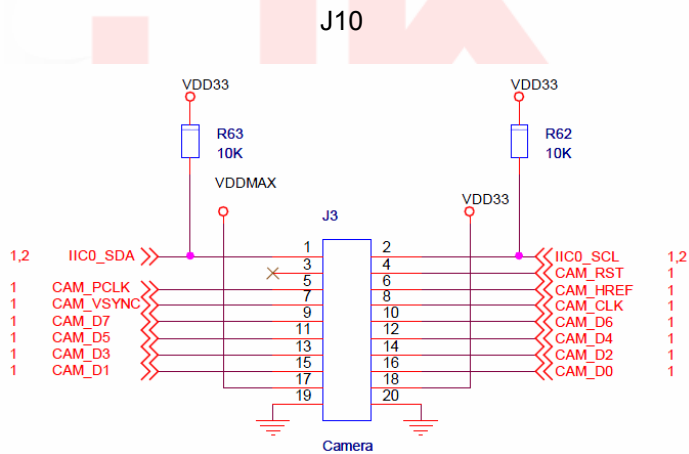
OTG package are as follows



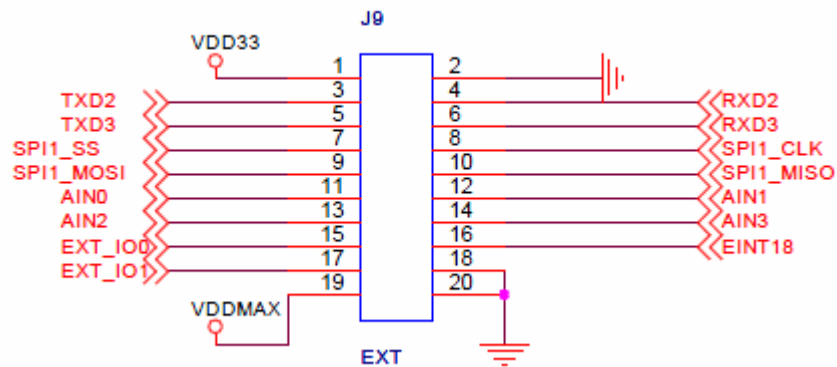
2.2.6 LCD Interface Definition



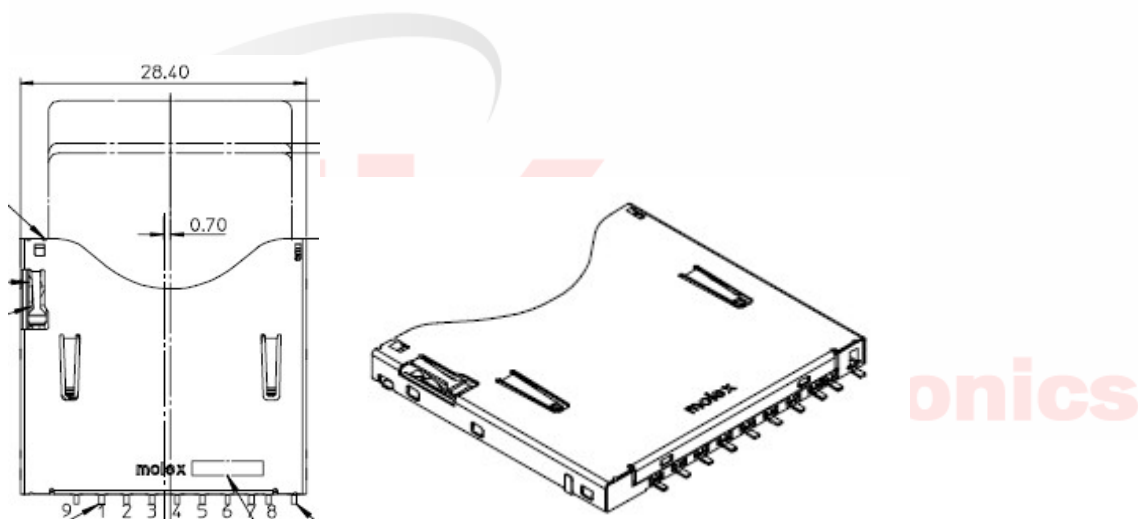
2.2.7 Camera Interface Definition

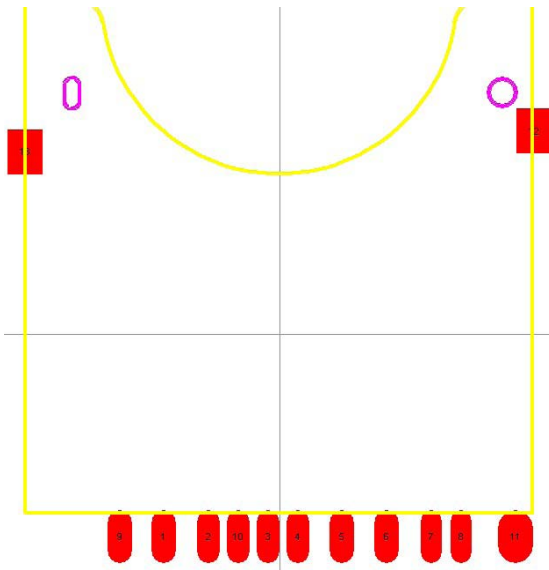


2.2.8 The definition of external expansion interface pins



2.2.9 SD Card interface definitions and connection





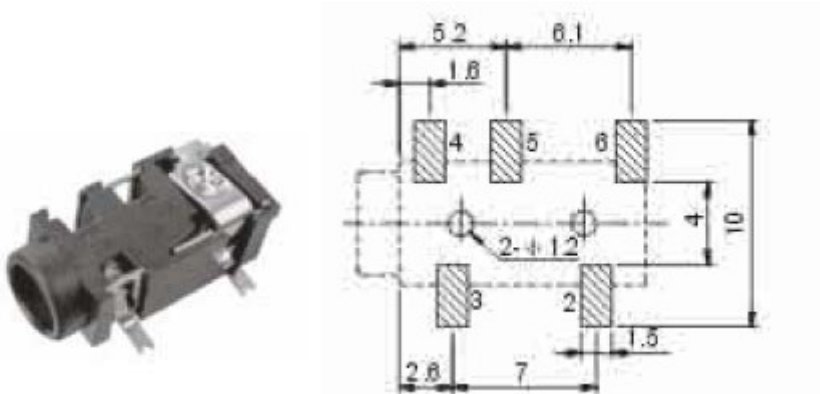
SD Socket Pin Definition

- (1) the data line 3
- (2) CMD signal
- (3) GND
- (4) 3.3 V Power Input
- (5) the clock signal
- (6) GND
- (7) the data line 0
- (8) the data line 1
- (9) the data line 2
- (10) insert the probe pin, low-effective
- (11) protection pin WP, low effective
- (12) GND
- (13) GND

2.2.10 Audio Interface Overview and Definitions

Development board provides three kinds of audio interface : 1.5W audio output, headphone output, electret MIC.

- (1) 1.5 W audio output can directly access speaker, using his legs led to a row of needles
- (2) headphone outputs with PJ327A interface can be accessed by a high degree of 2.5mm headphones, the package is defined as shown in Figure 22
- (3) MIC using electret MIC, see on-board



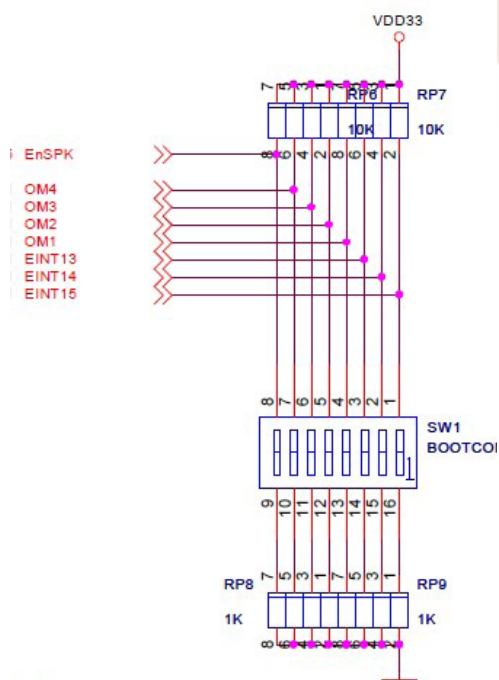
[Figure 22]

* Pin Definition :

- (2) Left channel output
- (3) GND
- (4) Insert the probe
- (5) Right channel output
- (6) NC

2.3 BOOT switch startup configuration instructions

2.3.1 Hardware connection diagram



EINT13, EINT14, EINT15 correspond GPN13, GPN14, GPN15 pin

- Board physical map :



No	J1	J 2	J 3	J 4	J 5	J 6	J 7	J 8
Name	EINT15	EINT14	EINT13	OM1	OM2	OM3	OM4	
On	GND	GND	GND	GND	GND	GND	GND	GND
Off	High	High	High	High	High	High	High	High

2.3.2 WinCE Boot startup configuration

XSELNAN D	OM[4:0]	GPN[15:13]	Boot Device	Function	Clock Source
1	0000X	XXX	RESERVED	RESERVED	XXTlpll if OM[0] is 0. XEXTCLK if OM[0] is 1.
1	0001X			RESERVED	
1	0010X			RESERVED	
1	0011X			RESERVED	
X	0100X		SROM(8bit)	-	
X	0101X		SROM(16bit)	-	
0	0110X		OneNAND ¹⁾	Don't use NAND Device	
X	0111X		MODEM	Don't use Xm0CSn2 for SROMC	
X	1111X	000	IROM ²⁾	SD/MMC(CH0)	
0		001		OneNAND	
1		010		NAND(512Byte, 3-Cycle)	
1		011		NAND(512Byte, 4-Cycle)	
1		100		NAND(2048Byte, 4-Cycle)	
1		101		NAND(2048Byte, 5-Cycle)	
1		110		NAND(4096Byte, 5-Cycle)	
X		111		SD/MMC(CH1)	

Because WinCE using internal IROM way to start using 1GB of NAND, SD card connected to the SD cartoon one, so start the configuration as follows

No	J1	J 2	J 3	J 4	J 5	J 6	J 7	J 8
SD Boot	OFF	OFF	OFF	OFF	OFF	OFF	OFF	NC
NAND Boot	OFF	ON	OFF	OFF	OFF	OFF	OFF	

2.3.3 Linux boot startup configuration

Linux non-IRAM way to start using 1GB of NAND, SD card connected to the channel 1, the Samsung 6410 manual did not disclose the way to start the definition of non-IRAM, and upon inspection that Figure 26 of the 6400 manual RESERVED defined as follows :

EINT13, EINT14, EINT15 correspond GPN13, GPN14, GPN15 pin

XSELNAN D	OM[4:0]	GPN[15:13]	Boot Device	Function	Clock Source
1	0000X		NAND FLASH	512页大小, 3时钟周期	XXTlpl if OM[0] is 0. XEXTCLK if OM[0] is 1.
1	0001X			512页大小, 4时钟周期	
1	0010X			2048页大小, 4时钟周期	
1	0011X			2048页大小, 5时钟周期	
X	0100X	XXX	SROM(8bit)	-	
X	0101X		SROM(16bit)	-	
0	0110X		OneNAND ¹⁾	Don't use NAND Device	
X	0111X		MODEM	Don't use Xm0CSn2 for SROMC	
X	1111X	000	IROM ²⁾	SD/MMC(CH0)	
0		001		OneNAND	
1		010		NAND(512Byte, 3-Cycle)	
1		011		NAND(512Byte, 4-Cycle)	
1		100		NAND(2048Byte, 4-Cycle)	
1		101		NAND(2048Byte, 5-Cycle)	
1		110		NAND(4096Byte, 5-Cycle)	
X		111		SD/MMC(CH1)	

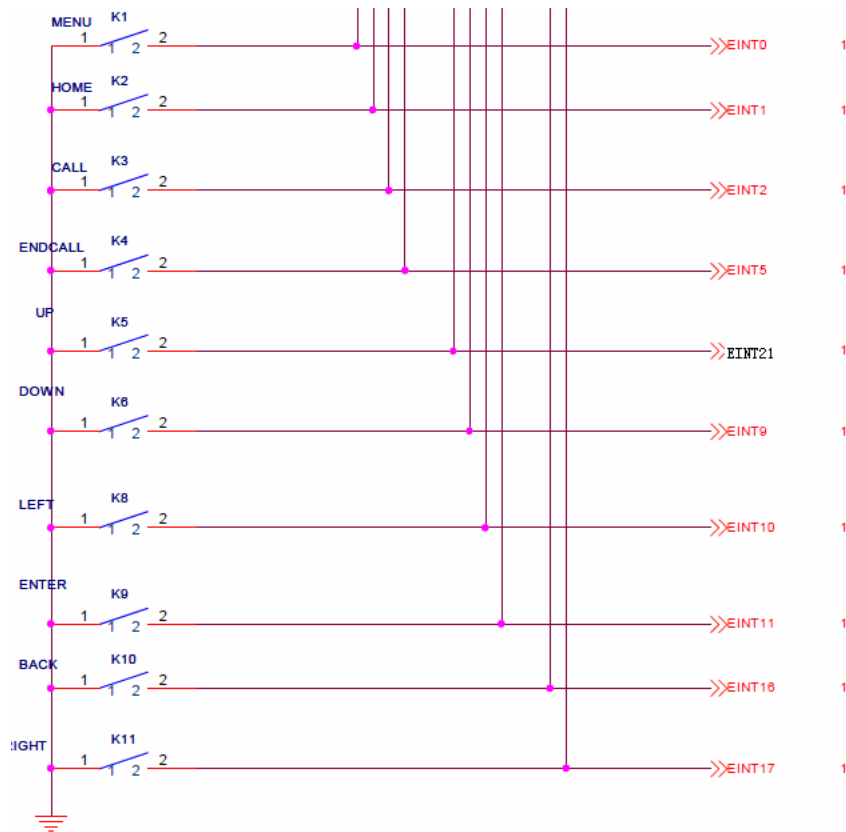
Start configuration options are as follows

No	J1	J 2	J 3	J 4	J 5	J 6	J 7	J 8
SD Boot	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
NAND Boot	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF

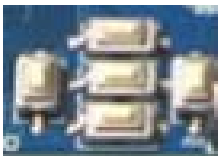
2.3.4 Android boot startup configuration

Reference 2.2.3 Linux boot configuration

2.4 Definition and pin-board push buttons connected



Definitions and connect the arrow keys as shown below

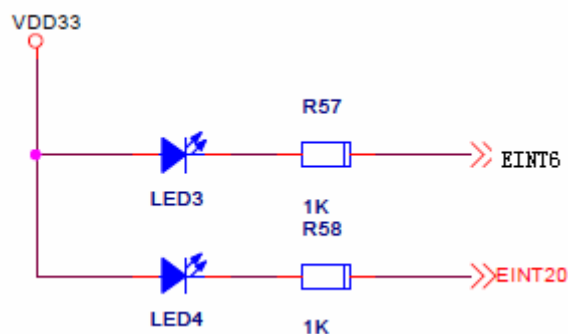


Key Name	K5	K6	K8	K11	K9
Description	Top	Bottom	Left	Right	Center
Interrupt	EINT21	EINT9	EINT10	EINT17	EINT11



Name	K1	K2	K10	K3	K4
Description	MENU	HOME	ESC	CALL	END CALL
Interrupt	EINT0	EINT1	EINT16	EINT2	EINT5

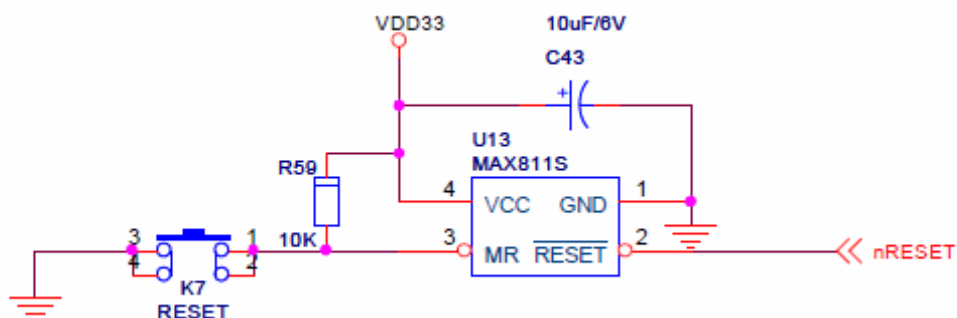
2.5 LED lights connected



LED Name	LED3	LED4
IO Pin	GPL13	GPN6
Interrupt	EINT21	EINT6

When the control pin low when the LED lights, LED light, when you eliminate high

2.6 RESET Reset





When the red mark button (K7) by pressing the system reset (active low reset)

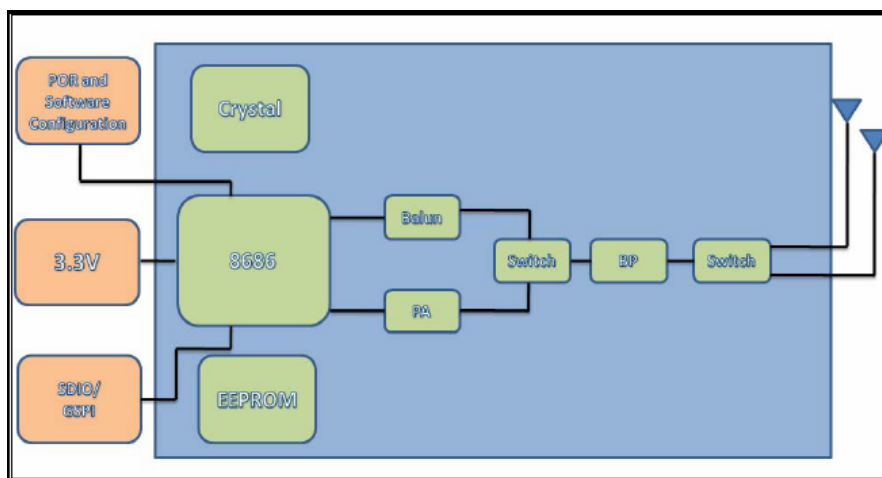
2.7 System memory allocation map

Address		Size (MB)	Description
0x0000_0000	0x07FF_FFFF	128	Booting device region
0x0800_0000	0x0BFF_FFFF	64	Internal ROM
0x0C00_0000	0x0FFF_FFFF	64	Stepping Stone(8KB)
0x1000_0000	0x17FF_FFFF	128	
0x1800_0000	0x1FFF_FFFF	128	DM9000AEP
0x2000_0000	0x27F_FFFF	128	1GBYTE NAND FLASH
0x2800_0000	0x2FFF_FFFF	128	
0x3000_0000	0x37FF_FFFF	128	
0x3800_0000	0x3FFF_FFFF	128	
0x4000_0000	0x47FF_FFFF	128	
0x4800_0000	0x4FFF_FFFF	128	
0x5000_0000	0x5FFF_FFFF	256	256M BYTE Mobile DDR
0x6000_0000	0x6FFF_FFFF	256	

2.8 WIFI module interface definition



WIFI modules GM320 module, which uses SDIO interface and CPU connections. Its internal functions as follows.



Pins are defined as follows :

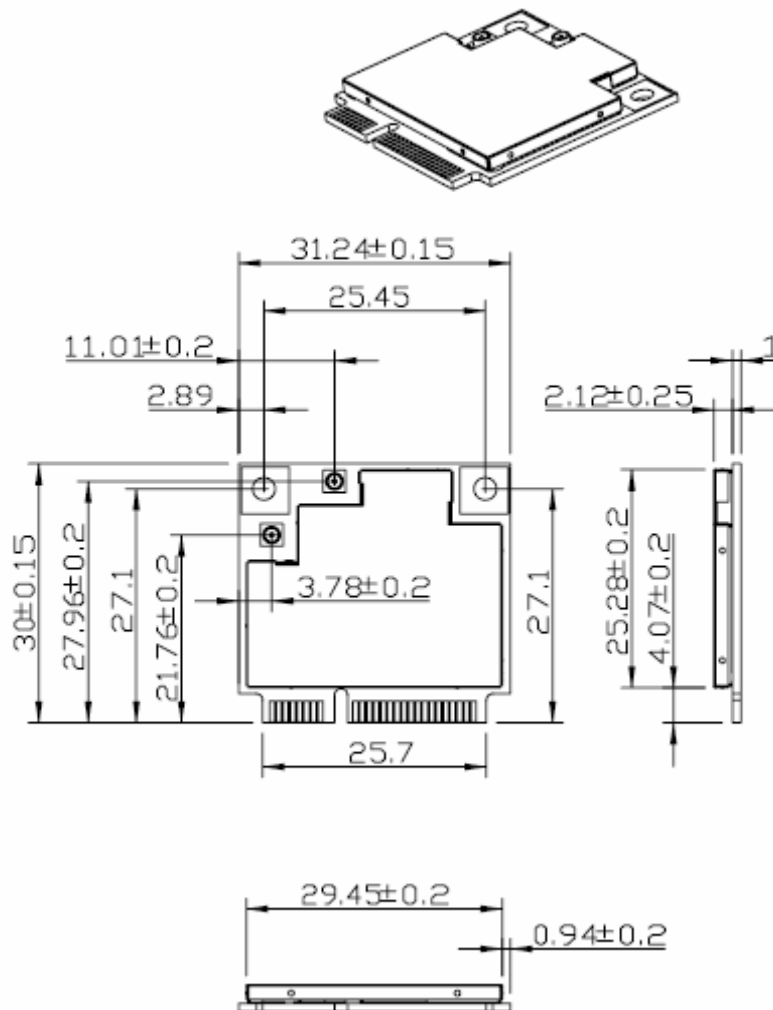
Pin No	Definition	Basic Description	Type	
1	SD_CLK/ SPI_CLK	SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input G-SPI Mode: G-SPI Clock Input	I/O	
2	3.3V	3.3V Power supply	I	
3	SD_CMD/ SPI_SDI	SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input G-SPI Mode: G-SPI Data Input	I/O	
4	GND			
5	SD_DAT[0]/ SPI_SCSn	SDIO 4-bit Mode: Data line bit[0] SDIO 1-bit Mode: Data line SDIO SPI Mode: Data output G-SPI Mode: G-SPI Chip Select Input(active low)	I	
6	RESETn	RESETn: Internal pull-up Reset(active low at least 10ns) (1)When the customer uses the RESETn mode, the SDIO/SPI interface must reboot.	I	
7	SD_DAT[1]/ SPI_SDOn	SDIO 4-bit Mode: Data line bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved G-SPI Mode: G-SPI Data Output(active low)	I/O	
8	SLEEP_CLK	Clock input for external sleep clock Note: SLEEP_CLK is used by the WLAN MAC. The input clock frequency is typically 32kHz/32.768kHz/3.2kHz. The Bluetooth radio chip supply is 3.2kHz. The WLAN requires 32kHz.	I	
9	SD_DAT[2]/ SPI_SINTn	SDIO 4-bit Mode: Data line bit[2](or Read Wait(optional)) SDIO 1-bit Mode: Read Wait(optional) SDIO SPI Mode: Reserved G-SPI Mode: Active G-SPI Interrupt Output(active low)	I/O	
10	PDn	PDn: Internal pull-up Full Power Down(active low as long as system need) 0=full power down mode 1=normal mode Connect to power down pin of host	I	
11	SDIO Card Detect	Tie to ground.		
12	WIFI Wake Up Host	Host Wake up WIFI, reserved for future use, left test point or NC.	I/O	
13	SD_DAT[3]	SDIO 4-bit Mode: Data line bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select(active low)	I/O	
14	3.3V	3.3V Power supply	I	
15	LED	Transmit power or receive ready LED.		
16	3.3V	3.3V Power supply	I	
17	GND			
18	GND			
19	Host Wake UP WIFI	WLAN MAC wake-up in /Interrupt in Software uses this pin or through SDIO as a method of getting the device out of deep sleep, note (1)	I/O	
20	NC			

CS

Pin No	Definition	Basic Description	Type	
21	Host interface select(1)	Host Interface select: SDIO: floating (default in pad) SPI: Tie 100k to ground	O	
22	NC			
23	GND			
24	NC			
25	NC			
26	NC			
27	NC			
28	NC			
29	GND			
30	3.3V	3.3V Power supply	I	
31~33	NC			
34	GND			
35	ECSN	SDIO: Tie to GND GSP: Floating	O	
36~39	NC			
40	GND			
41	NC			
42	Host interface select(2)	Host Interface select: SDIO: floating (default in pad) SPI: Tie 100k to ground	O	
43~47	NC			
48,50,52	Test pins	Please left test points	I/O	
49,51	NC			

 CJIK Electronics

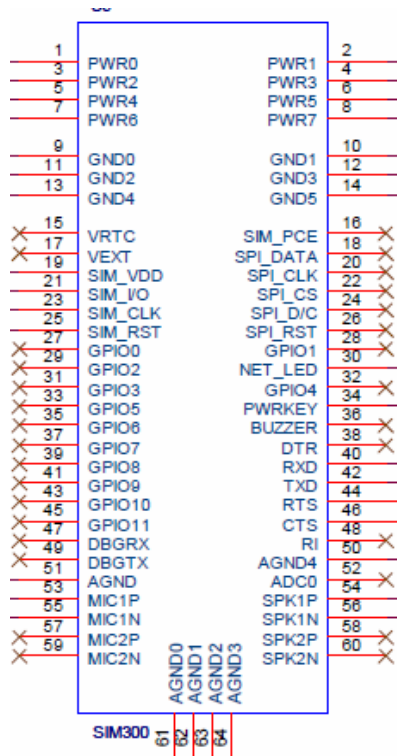
Module dimensions are as follows :



tronics

2.9 GPRS / GSM Module Interface Definition

GSM pin definitions shown in the figure, more description to refer to the SIM300 Hardware Guide.



Power Supply			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
VBAT		Eight BAT pins of the board-to-board connector are dedicated to connect the supply voltage. The power supply of SIM300 has to be a single voltage source of VBAT= 3.4V...4.5V. It must be able to provide sufficient current in a transmit burst which typically rises to 2A, mostly, these 8 pins are voltage input	Vmax= 4.5V Vmin=3.4V Vnorm=4.0V
VRTC	I/O	Current input for RTC when the battery is not supplied for the system. Current output for backup battery when the main battery is present and the backup battery in low voltage state.	Vmax=2.0V Vmin=1.2V Vnorm=1.8V Inorm= 20uA
VDD_EXT	O	Supply 3.0V voltage for external circuit. By measure this pin, user can judge the system is on or off. When the voltage is low, the system is off. Otherwise, the system is on.	Vmax=3.15V Vmin=2.85V Vnorm=3.0V Imax=60mA
GND		Digital ground	

Power on or power off			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
PWRKEY	I	Voltage input for power on key. PWRKEY get a low level Voltage for user to power on or power off the system. The user should keep pressing the key for a moment when power on or power off the system. Because the system need margin time assert the software.	VILmax=0.3*VBAT VIHmin=0.7*VBAT VImax=VBAT
Audio interfaces			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
MIC1P MIC1N	I	Positive and negative voice-band input	Audio DC Characteristics refer to chapter 3.9.4
MIC2P MIC2N	I	Auxiliary positive and negative voice-band input	
SPK1P SPK1N	O	Positive and negative voice-band output	
SPK2P SPK2N	O	Auxiliary positive and negative voice-band output	
Buzzer	O	Buzzer Output	
AGND		Analog ground	
GERNERAL PURPOSE input/output			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
KBC0-KBC4	O	The GPO can be configured by AT command for outputting high or low level voltage. All of the GPOs are initial low without any setting from AT command.	VILmin=0V
KBR0-KBR4	I		VILmax=0.3 *VDD_EXT
SPI_DATA	I/O		VIHmin=0.7*VDD_EXT
SPI_CLK	O		VIHmax= VDD_EXT+0.3
SPI_CS	O		VOLmin=GND
SPI_D/C	O		VOLmax=0.2V
SPI_RST	O	Normal Input/Output Port	VOHmin= VDD_EXT-0.2
Network LED	O		VOHmax= VDD_EXT
GPIO8	I/O	Normal Input/Output Port	
Serial l interface			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
DTR	I	Data Terminal Ready	VILmin=0V
RXD	I	Receive Data	VILmax=0.3*VDD_EXT
TXD	O	Transmit Data	VIHmin=0.7*VDD_EXT
RTS	I	Request to Send	VIHmax= VDD_EXT+0.3
CTS	O	Clear to Send	VOLmin=GND

RI	O	Ring Indicator	VOLmax=0.2V
DCD	O	Data Carrier detection	VOHmin= VDD_EXT-0.2
Serial 2 interface			VOHmax= VDD_EXT
DBGTX	O	Serial interface for debugging and communication	
DBGRX	I		
SIM interface			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
SIM_VDD	O	Voltage Supply for SIM card	The voltage can be select by software either 1.8v or 2.8V
SIM_I/O	I/O	SIM Data Output	VILmin=0V
SIM_CLK	O	SIM Clock	VILmax=0.3*SIM_VDD
SIM_PRESENCE	I	SIM Card Detection	VIHmin=0.7*SIM_VDD
SIM_RST	O	SIM Reset	VIHmax= SIM_VDD+0.3
			VOLmin=GND
			VOLmax=0.2V
			VOHmin= SIM_VDD-0.2
			VOHmax= SIM_VDD
AUXADC			
PIN NAME	I/O	DESCRIPTION	DC CHARACTERISTICS
ADC0	I	General purpose analog to digital converter.	Input voltage value scope 0V to 2.4V

2.10 GPS Module interface definitions

Note: GPS module is compatible with the possibility of using models, but the pin and the definition and performance parameters are consistent with

RXB	P1	P20	GND
TXB	P2	P19	RF_IN
PPS	P3	P18	GND
TXA	P4	P17	VCC_RF
RXA	P5	P16	BOOT_SET
GND	P21	P22	GND
NC	P6	P15	GPIO15
GPIO0	P7	P14	GPIO14
GPIO1	P8	P13	GPIO13
RF_PWR	P9	P12	VCC
ON_OFF	P10	P11	V_RTC



EB818 Pin assignment description		
Pin 1	RXB	Serial Data input port B for user's application (not currently used).
2	TXB	Serial Data output port B for user's application (not currently used).
3	PPS	1PPS Time mark output
4	TXA	Serial Data output port A
5	RXA	Serial Data input port A
6	NC	
7	GPIO0	General purpose I/O
8	GPIO1	General purpose I/O
9	RF_PWR	RF_PWR ON/OFF
10	ON_OFF	Edge triggered soft on/off request. Should only be used to wake up chip.(must be Low)
11	V_RTC	Battery backup input. 2.8V to 3.3V ,10uA typical.
12	VCC	3V +/- 0.15V power input (System Power)
13	GPIO13	General purpose I/O
14	GPIO14	General purpose I/O
15	GPIO15	LED indicate for GPS status
Tracking Mode :  Fixed Mode : Hi 		
16	BOOT_SET	Reserved for re-programming flash(pull high)
17	VCC_RF	RF POWER 2.85V
18	GND	Power GND
19	RF_IN	Antenna input
20	GND	Power GND
21	GND	Power GND
22	GND	Power GND

2.11 Development Board Serial distribution of

UART No	UART0	UART1	UART2	UART3
Use	DB9 Standard	GPRS(SIM3000)	GPS	External Expand
Level	RS232	TTL	TTL	TTL
External Expand	NC	NC	Expand	Expand

3. Hardware Design and Analysis

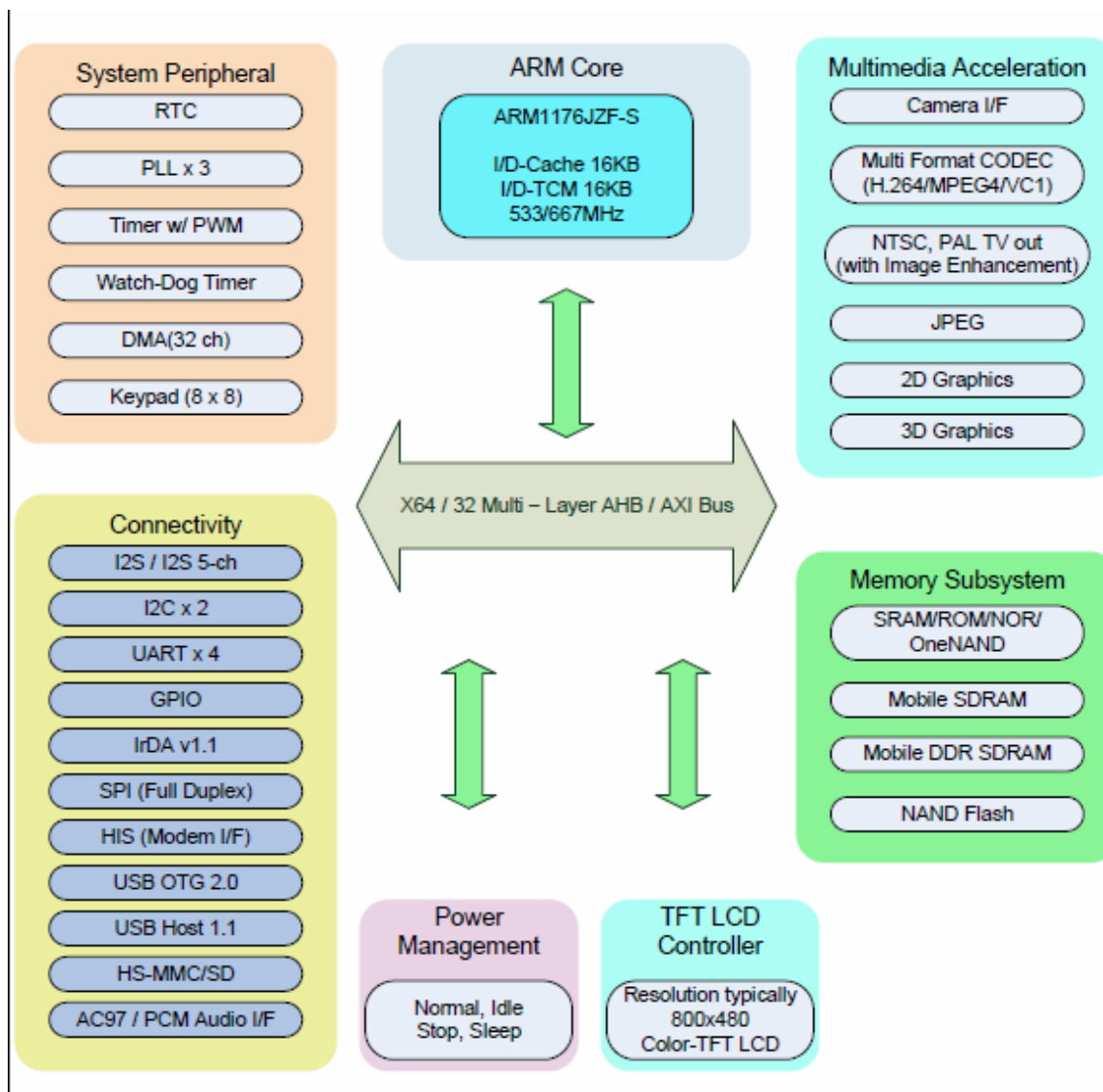
3.1 S3C6410 processor performance

SAMSUNG's S3C6410 is a 16/32-bit based ARM1176 high-performance low-power general-purpose microprocessors RSIC for handheld, mobile and other devices.

S3C6410 is a low-power, cost-effective, high-performance for mobile phones and general-purpose processing RSIC processor. For 2.5G and 3G communication services to provide an optimized hardware performance, using 64/32bit internal bus architecture, combines the AXI, AHB, APB bus. There are a lot of powerful hardware accelerators, including sports video processing, audio processing, 2D acceleration, display processing and scaling. An integrated MFC (Multi-Format video Codec) support MPEG4/H.263/H.264 and VC1 decoding codec, the hardware codec support for real-time video conferencing, as well as NTSC and PAL formats for TV output. In addition, built-in one the most advanced technologies, 3D accelerator support OpenGL ES1.1 / 2.0 and D3DM API to achieve 4M triangles / s for 3D acceleration.

S3C6410 includes optimized external memory interface, which can meet the high-end data communications services in bandwidth requirements. Interface is divided into two-way, DRAM and Flash/ROM/DRAM port. DRAM port can be configured to support Mobile DDR, DDR, Mobile SDRAM, SDRAM. Flash/ROM/DRAM port to support NOR-Flash, NAND-Flash, OneNAND, CF, ROM and other types of external memory and arbitrary Mobile DDR, DDR, Mobile SDRAM, SDRAM memory.

In order to reduce the overall system cost and improve the overall functionality, S3C6410 includes many hardware peripherals features: Camera interface, TFT 24bit true color LCD controller, system management unit (power clocks, etc.), 4-channel UART, 32-channel DMA, 4 channel timer, general-purpose I / O port, I2S bus, I2C bus, USB Host, High-Speed USB OTG, SD Host and high-speed MMC card interface and the internal PLL clock generator. Of its internal functional block diagram is as follows.



3.2 CPU does not use pin approach

Would you reference schematic please.

3.3 CPU power supply pin's supply area

VDDRTC	1.8V~3.0V	XrtcXTI, XrtcXTO
VDDMEM0	1.8V~3.3V	Xm0ADDR[19:0], Xm0DATA[15:0], Xm0CSn[5:0], Xm0OEn, Xm0VEn, Xm0ADV, Xm0SMCLK, Xm0VWAITn, Xm0RDY0/ALE, Xm0RDY1/CLE, Xm0INTsm0/FWEn, Xm0INTsm1/FREn, Xm0RPN/RnB, Xm0INTATA, Xm0Cdata, Xm0BEn[1:0], GPQ[6:2]
VDDSS	1.8V~3.3V	Xm0INTata, Xm0RESETata, Xm0INPACKata, Xm0REGata, Xm0VEata, Xm0OEata, Xm0CData
VDDMEM1	1.8V~2.5V	Xm1ADDR[15:0], Xm1DATA[31:0], Xm1CSn[1:0], Xm1CKE[1:0], Xm1SCLK, Xm1SCLKn, Xm1RASn, Xm1CASn, Xm1WEn, Xm1DQM[3:0], Xm1DQS[3:0]
VDDEXT	1.8V~3.3V	XuRXD[3:0], XuTXD[3:0], XuCTS[1:0], XuRTSn[1:0], XirSDBW, Xi2cSCL, Xi2cSDA, XspiMISO[0], XspiCLK[0], XspiMOSI[0], XspiCS[0], SciCLK, XciHREF, XciPCLK, XciRSn, XciVSYNC, XciDATA[7:0], XpwmECLK, XpwmTOUT[1:0]
VDDMMC	1.8V~3.3V	XspiMISO[1], XspiCLK[1], XspiMOSI[1], XspiCS[1], XmmcCLK[1:0], XmmcCMD[1:0], XmmcDATA0[3:0], XmmcCDN0, XmmcDATA1[7:0]
VDDPCM	1.8V~3.3V	XpcmDCLK[1:0], XpcmEXTCLK[1:0], XpcmFSYNC[1:0], XpcmSIN[1:0], XpcmSOUT[1:0]
VDD_LCD	1.8V~3.3V	XvVD[23:0], XvHSYNC, XcVSYNC, XvVDEN, XvVCLK
VDDHI	1.8V~3.3V	XhiDATA[17:0], XhiADDR[12:0], XhiCSn, XhiCSn_main, XhiCSn_sub, XhiWEn, XhiOEn, XhiRQn
VDDSYS	1.8V~3.3V	XEINT[15:0], XnRESET, WR_TEST, XsRSTOUTn, XjTRSTn, XjTMS, XjTCK, XjRTCK, XjTDI, XjTDO, XjDBGSEL, XOM[4:0], XSELNAND, XPVRRGTON, XnBATF, X27mXTI, X27mXTO, XXTI, XXTO, XEXTCLK
VDDADC	3.3V	Xadc_AIN[7:0]
VDDDAC	3.3V	XdacOUT_0, XdacOUT_1, XdacIREF, XdacVREF, XdacCOMP
VDDUH	3.3V	XuhDN, XuhDP
VDDOTG	3.3V	XusbDP, XusbDM, XusbXTI, XusbXTO, XusbREXT, XusbVBUS, XusbID, XusbDRVVBUS

3.4 Design and Analysis of Memory

Development board with 256M Byte mobile DDR, by two 16-bit mobile DDR composed of 32-bit-wide 256M Byte.

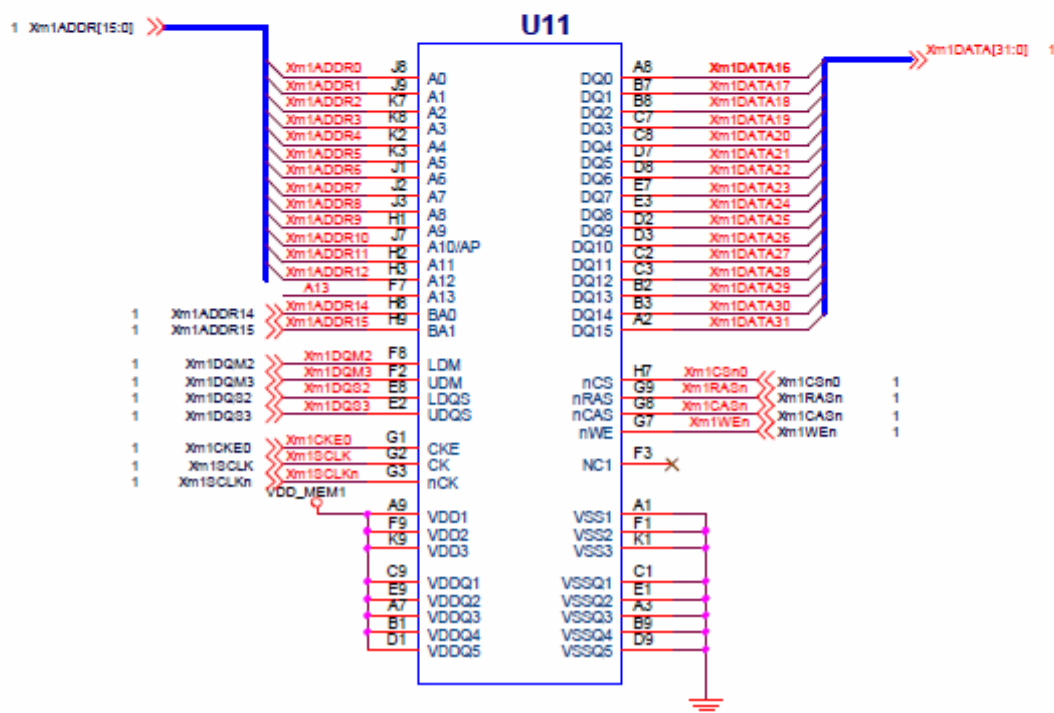
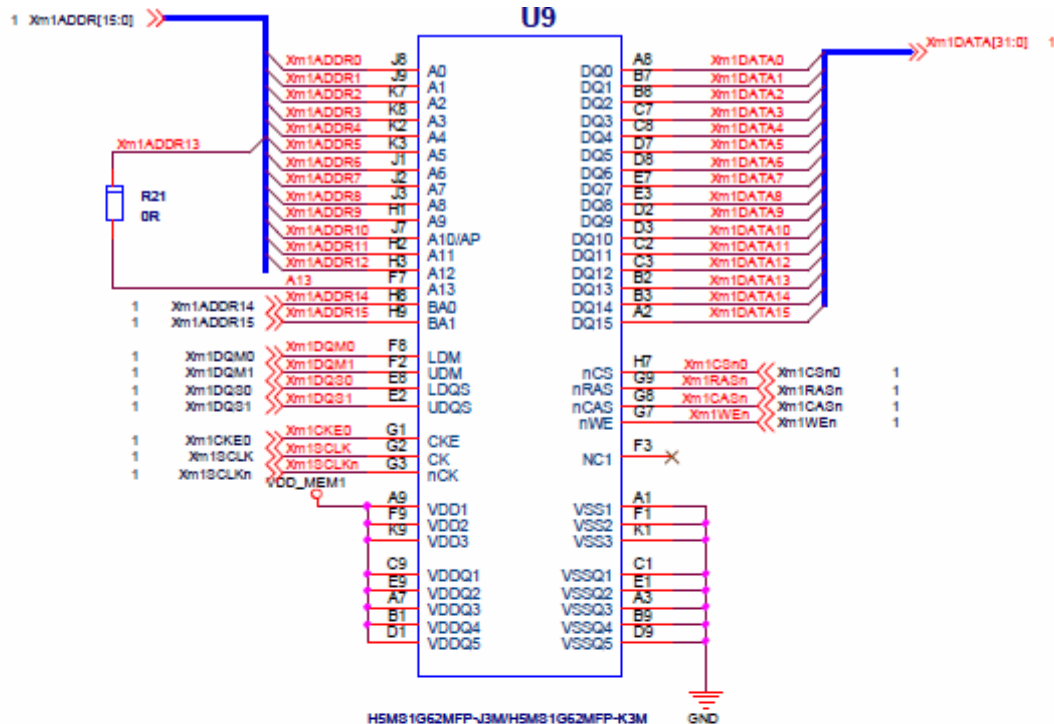
6410 to support Mobile DDR, SDRAM, DDRI. Taking into account the speed and power consumption, because of Mobile DDR (mDDR) has the following characteristics, so use them for future development board design.

- (1) Low power consumption, the generation of conventional DDRI.
- (2) low-voltage, 1.8V.
- (3) Support SLEEP Function.

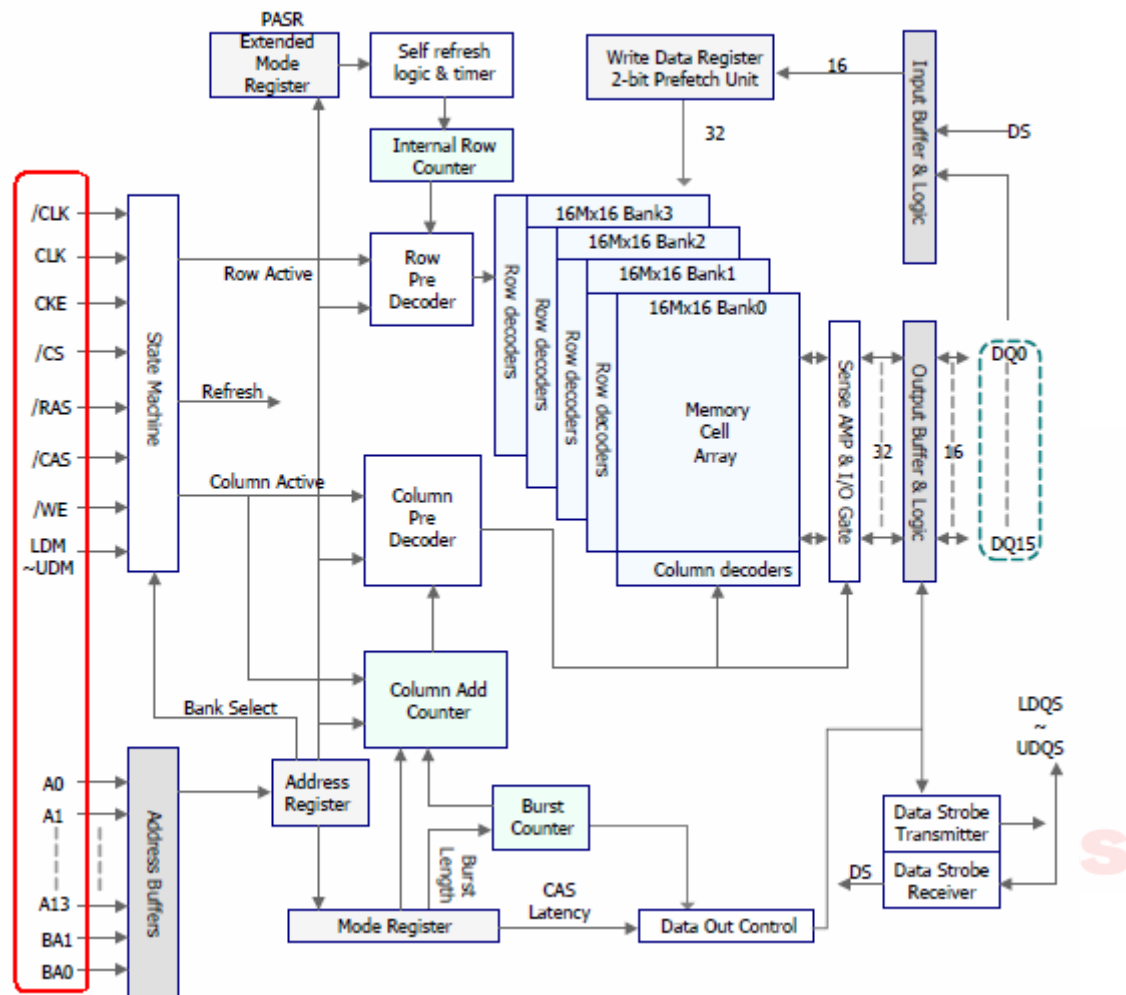
(4) BGA package, effectively reduce PCB area.

(5) Generally do not need to string-side resistor and pull-up resistor designed to Facilitate.

Schematic diagram is as follows:



16Mbit x 4banks x 16 I/O Mobile DDR SDRAM



As red box shows the required pin, while the 6410 offers a pin to meet the above requirements,

Table 5-1. Memory Port 1 Pin Description

Signal	Type	Description
Xm1SCLK	Output	Memory clock
Xm1SCLKn	Output	Memory clock (negative)
Xm1CKE[1:0]	Output	Clock enable per chip
Xm1CSN[1:0]	Output	Chip select per chip (active low)
Xm1RAS	Output	Row address strobe (active low)
Xm1CAS	Output	Column address strobe (active low)
Xm1WEN	Output	Write enable (active low)
Xm1ADDR[13:0]	Output	Address bus
Xm1ADDR[15:14]	Output	Bank select
Xm1DATA[31:0]	Inout	Data bus
Xm1DQM[3:0]	Output	Data bus mask bits
Xm1DQS[3:0]	Inout	Data strobe inout, DDR and mDDR only

S3C6410 has two bus interfaces, which Xm1 interface support mDDR, which Xm1SCLK and Xm1SCLKn composition of differential clock signals, to connect the memory clock terminal CLK and /CLK terminal. Note that when the CLK signal wiring is very susceptible to interference, and must go into a differential pair, and asked not to GND and power through a different plane. 6410's Xm1 interface provides two-way chip-select signal for connecting the memory, in the design, although we use the two pieces of memory, but due to the low 16-bit data lines connected to the U9, while a high 16 connected to the U11, so that one word (4 bytes) of storage means there is a lower 16-bit on the U9, U11 on the existence of a high 16. Obviously, the two memory chip select should be the same, then the Xm1CS0, the corresponding clock enable signal Xm1CLKE0. In the 6410 architecture Xm1CS0 physical address 0x50000000.

Table 2-2. Device Specific Address Space

Address		Size(MB)	Description	Note
0x0000_0000	0x07FF_FFFF	128MB	Bootling Device Region by XOM Setting	Mirrored Region
0x0800_0000	0x0BFF_FFFF	64MB	Internal ROM	
0x0C00_0000	0x0FFF_FFFF	64MB	Stepping Stone (Boot Loader)	
0x1000_0000	0x17FF_FFFF	128MB	SR0MC Bank0	
0x1800_0000	0x1FFF_FFFF	128MB	SR0MC Bank 1	
0x2000_0000	0x27FF_FFFF	128MB	SR0MC Bank 2	
0x2800_0000	0x2FFF_FFFF	128MB	SR0MC Bank 3	
0x3000_0000	0x37FF_FFFF	128MB	SR0MC Bank 4	
0x3800_0000	0x3FFF_FFFF	128MB	SR0MC Bank 5	
0x4000_0000	0x47FF_FFFF	128MB	Reserved	
0x4800_0000	0x4FFF_FFFF	128MB		
0x5000_0000	0x5FFF_FFFF	256MB	DRAM Controller of the Memory Pprt1	
0x6000_0000	0x6FFF_FFFF	256MB		

Xm1CAS and Xm1RAS respectively mDDR column selection signals and row address selection signals, for the conduct of the memory row and column address of choice. Xm1WE for the memory write signal.

Xm1DQM and Xm1DQS, screening and selection of bytes, respectively, to meet in accordance with byte or half-word read.

3.5 NAND FLASH and NOR FLASH difference between

NOR and NAND is now on the market two main types of non-volatile flash memory technology. Intel in 1988, developed the first NOR flash technology, completely changed the original EPROM and EEPROM by dominating the world situation. Then, in 1989, Toshiba issued a NAND flash architecture that emphasized reducing the cost per bit, higher performance, and the same as the disk can easily upgrade through the interface. However, after more than a decade later, there are a considerable number of hardware engineers distinguish between NOR and NAND flash memory. Phase "flash memory" often with similar "NOR memory," used interchangeably. Many in the industry have also not sure NAND flash memory technology in relation to the strength of the NOR technology, because in most cases a small amount of flash memory is only used to store the code, when a number of NOR flash memory is more suitable. The NAND is ideal for high-density data storage solution. NOR is characterized by the implementation of chip (XIP, eXecute In Place), so the application can be run directly from within the flash memory without having to read the code then the system RAM. NOR's transmission efficiency high, 1 ~ 4MB of small volume carries a high cost-effectiveness, but low write and

erase speeds significantly affect its performance. NAND structure can provide a very high cell density, can achieve high storage density, and the write and erase speed quickly. Application of NAND difficulties lie in the management and the need to flash a special system interface.

Performance Comparison :

Flash memory is nonvolatile memory, can be called the block of memory cell block erase and re-programming. Any flash device write operation can only be empty or have been erased within the unit, so in most cases, following the implementation of a write operation must be erased before. NAND device implementation of the erase operation is very simple, while the NOR requires that before carrying out the target block erase all of the bits are written to 0. Because when you erase the NOR device is 6 ~ 128KB of the block, and the implementation of a write/erase operation time for 5s, contrast, erase the NAND device is 8 ~ 32KB of the block, and perform the same the operation of a maximum of only 4ms.

The implementation of the different erase block size of the NOR and the further widening the performance gap between the NADN, statistics show that for a given set of write operations (in particular, is to update the small files more erase operations must be based on the NOR The unit carried out. Thus, when selecting a storage solution, the designer must weigh the following factors.

- NOR read speeds slightly faster than NAND.
- NAND write speeds much faster than NOR.
- NAND erase the speed of 4ms the 5s faster than NOR.
- Most write operations need to be erasure.
- NAND erase unit smaller, the corresponding erase circuit less.

Interface differences :

NOR flash with SRAM interface, there is enough address pins to addressing, you can easily access each of its internal byte. NAND devices use complex I/O port to the serial access to data, each product or vendor of the methods may vary. 8-pin is used to send control, address and data information. NAND read and write operations using 512-byte blocks, which is a bit like a hard disk management of such operations, and quite naturally, based on NAND memory can replace the hard disk or other block device.

Capacity and cost :

NAND flash cell size is almost half the NOR device, due to the production process more simple, NAND structure can be in a given die size to provide a higher capacity, thus a corresponding reduction in the price. NOR flash accounted for 1 ~ 16MB flash memory capacity of most of the market, while NAND flash is used in the 8 ~ 128MB's products, which also shows the main application of NOR for code storage medium, NAND for data storage, NAND in the CompactFlash, Secure Digital, PC Cards and MMC memory card market, the largest share.

Reliability and durability :

Flash medium with a need to focus on issues considered is reliability. For the MTBF of the systems that need to be extended, Flash is a very appropriate storage solutions. From life (durability), digital switching and bad block processing to compare the three aspects of the reliability of NOR and NAND.

Life (durability) :

In the NAND flash memory erase each block the maximum number of times one million times, while the NOR's endurance is the hundreds of thousands of times. NAND Memory In addition to 10 to 1 advantage of the block erase cycles, a typical NAND block size 8 times smaller than the NOR device, each block of NAND memory in a given time, the deletion of fewer number of times. All flash devices are plagued by the phenomenon of digital switching. In some cases (rare, NAND occur more often than NOR), a bit reversal will occur or be reversed in the report. A change may not be obvious, but when it occurs in a critical document, this small failure can cause system downtime. If only the report there is a problem to read a few possible resolved. Of course, if this place really has changed, you must use the error detection / error correction (EDC / ECC) algorithm. Bit reversal more problems found in NAND flash memory, NAND vendors recommend the use of NAND flash memory, when, while using the EDC / ECC algorithms. This question is used inverted NAND storage media information is not fatal. Of course, if a local storage device to store the operating system, configuration files or other sensitive information, you must use the EDC / ECC system to ensure reliability.

Bad block handling :

NAND devices bad blocks are randomly distributed. Some time ago that there have been efforts to eliminate bad blocks, but found the finished product rate is too low, the price is too high, simply uneconomical. NAND devices are needed to initialize media scan to detect bad blocks and bad blocks marked as unavailable. In the ready-made devices, the adoption of reliable methods do not carry out this deal will lead to high failure rates.

Easy to use :

Can be very direct NOR-based flash memory can be as connected as any other memory and can be run directly in the above code. Due to the need I / O interface, NAND is much more complicated. NAND devices to access a variety of methods vary due to manufacturer. The use of NAND devices, you must first write the driver can continue to perform other operations. Write information to the NAND device requires considerable skill, because designers can not write to the bad blocks, which means that throughout the NAND device must be a virtual map.

Software Support :

When discussing software support, it should distinguish the basic read / write / erase operations and high levels for disk emulation and flash management algorithm of the software, including performance optimization. In the NOR device to run the code does not require any software support, in the NAND device on the same operation, usually the driver, that is, memory technology driver (MTD), NAND and NOR devices during write and erase operations need to MTD.

NOR devices are required when using the MTD is relatively less, many manufacturers offer NOR devices for more advanced software, including the M-System's TrueFFS driver, the driver was Wind River System, Microsoft, QNX Software System, Symbian and used by Intel and other vendors. Driver is also used on the DiskOnChip product simulation and NAND flash memory management, including error correction, bad block handling and loss of balance.

3.6 NAND FLASH MLC and SLC the difference between

Flash products can be divided into three major structures, namely the single-layer storage (Single Level Cell; SLC), including Samsung Electronics, Hynix, Micron (Micron) and Toshiba are the users of this technology, the second is a multi-storey Storage (Multi Level Cell; MLC), there are Toshiba, Renesas use, the last is the Infineon (Infineon) and Saifun Semiconductors joint use of NROM technology co-developed a number of storage (Multi Bit Cell; MBC) SLC technology and EEPROM the same, but in the floating gate and the source of the oxide film being thinner, the data write is through to the floating gate voltage of the electric He Jia, and then can source can be stored charge eliminated, through this way, can store a message unit, in a SLC read and write in only two states 0 or 1, this technology provides fast programming and read, but this was somewhat limited in silicon efficiency must be reinforced by a more advanced process technologies in order to move upward SLC process technologies. MLC is the Intel (Intel) in September 1997 the first successfully developed, and its role is two units of information

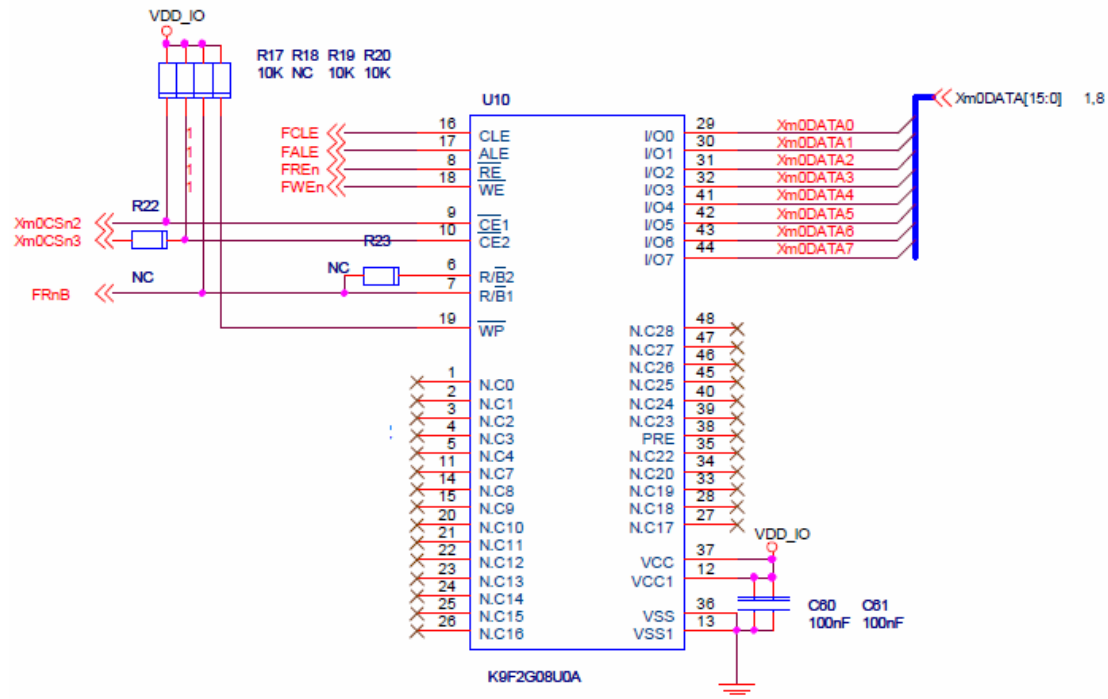
into a storage unit, and then the use of different potentials of charge, through the memory storage of accurate voltage control to read and write to make Flash the capacity to increase substantially in the MLC in a reading and writing are 00,01,10 or 11 four states, it means that MLC memory when more precise control of the charging voltage of each memory cell, when it is read and write require a longer charging time to ensure the reliability of data. [attach] 145 [/attach] MLC architecture can have better storage density, can be used together with older manufacturing processes to improve the product prepared by the capacity, without additional investment in production equipment, cost of ownership and yield advantages. However, with MLC architecture is difficult to tolerate the shortcomings of users, first and foremost a short life, MLC architectures can tolerate only about 1 million access, well below the SLC structure of 10 million. Secondly, access speed, SLC architecture than the MLC architecture to more than three times faster, plus MLC architecture for more power consumption.

SLC and MLC performance comparison of the project.

	SLC	MLC
Voltage	3.3/1.8V	3.3V
Technology	0.12μm	0.16μm
Page/Block	2KB/128KB	512B/32KB or 2KB/256KB
Seek Time	25μs	70μs
Page programming time	250μs	1.2ms
Regional programming	Support	Not Support
Writing rate	Greater than 8MB/S	1.5MB/S
Can be endurance	100,000 times	1 million times

3.7 NAND FLASH Circuit Design and Analysis of

S3C6410 supports MLC and SLC-type NAND FLASH, connect the circuit as shown below



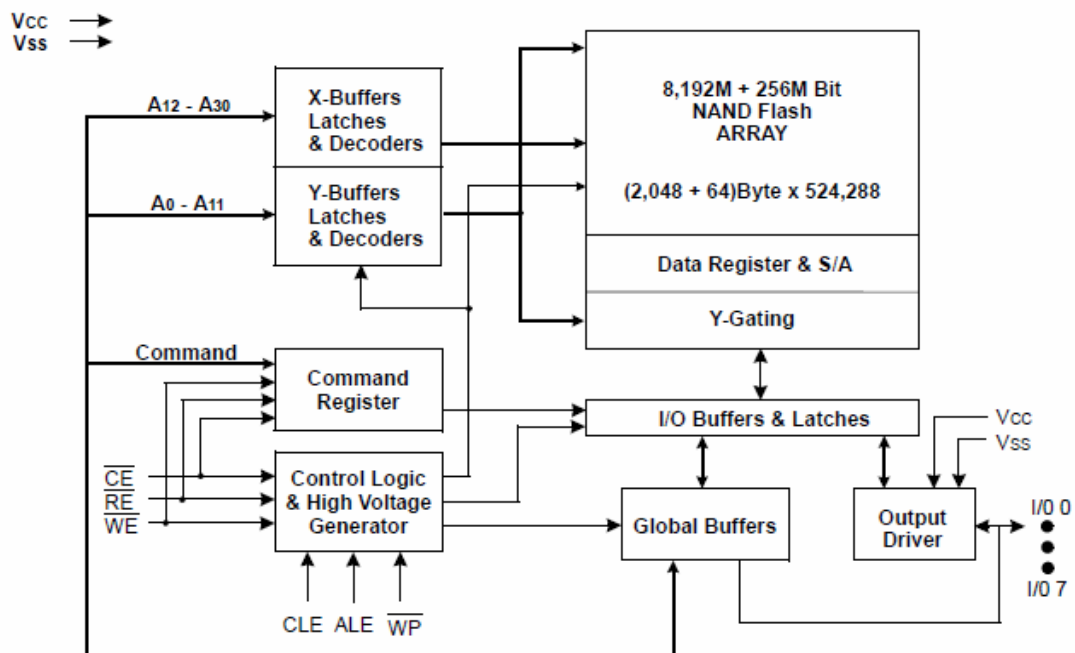
Is compatible with more than schematic design, supports both MLC, also supported the SLC, using SLC, for example, K9F1G08, K9F2G08, at this time, R22 R29 and R18 do not welded. MLC when using MLC FLASH pin according to the definition of reasonable welding, development board comes standard with the use of 1G Byte of the MLC-based NAND FLASH, this time can all be resistance welded. NAND FLASH connected to the 6410's Xm0 bus, the data line 8, use Xm0DATA0-Xm0DATA7, as NAND are non-linear addressing, so no need to connect address line. MLC-based FLASH uses a 3.3V power supply, received VDDIO. FALE the address for the NAND FLASH enabled client, when this signal is high, that sent the address, this time to send NAND FLASH site by N times, where N times for NAND FLASH size of the total number of bytes of space / Each 1Byte. FCLE that sent a command, such as Erase command. FREn and FWEn access NAND read and write signals. FRnB is a NAND FLASH busy judge.

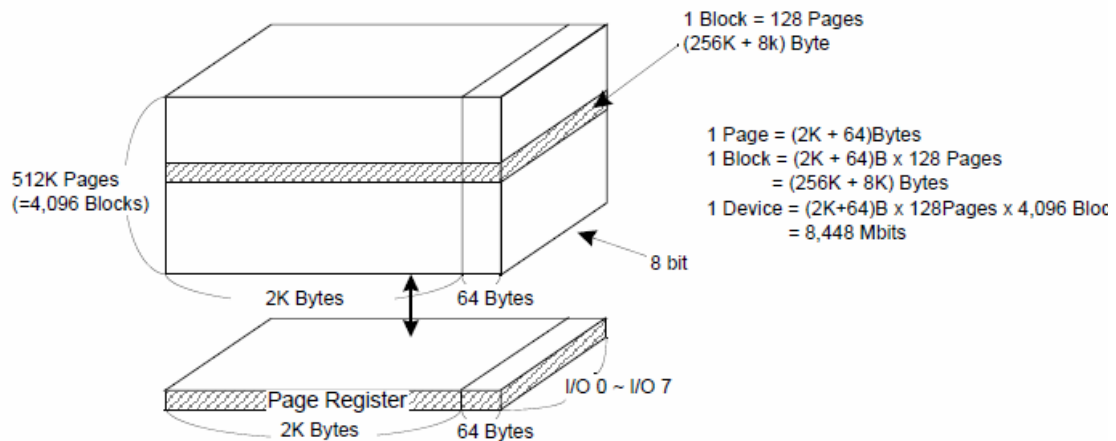
As shown below, we know that the physical NAND starting address 0x20000000

Table 2-2. Device Specific Address Space

Address		Size(MB)	Description	Note
0x0000_0000	0x07FF_FFFF	128MB	Bootling Device Region by XOM Setting	Mirrored Region
0x0800_0000	0x0BFF_FFFF	64MB	Internal ROM	
0x0C00_0000	0x0FFF_FFFF	64MB	Stepping Stone (Boot Loader)	
0x1000_0000	0x17FF_FFFF	128MB	SROMC Bank0	
0x1800_0000	0x1FFF_FFFF	128MB	SROMC Bank 1	
0x2000_0000	0x27FF_FFFF	128MB	SROMC Bank 2	
0x2800_0000	0x2FFF_FFFF	128MB	SROMC Bank 3	
0x3000_0000	0x37FF_FFFF	128MB	SROMC Bank 4	
0x3800_0000	0x3FFF_FFFF	128MB	SROMC Bank 5	
0x4000_0000	0x47FF_FFFF	128MB	Reserved	
0x4800_0000	0x4FFF_FFFF	128MB		
0x5000_0000	0x5FFF_FFFF	256MB		
0x6000_0000	0x6FFF_FFFF	256MB	DRAM Controller of the Memory Pprt1	

Development board using MLC for K9G8G08, its structure shown below:





	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	Row Address
5th Cycle	A28	A29	A30	*L	*L	*L	*L	*L	Row Address

K9G8G08 can be seen from the table, each the size of 2K, we do not calculate C, 64 bytes, each BLOCK 128 pages, a total of $128 * 2K = 256K$, the entire FLASH contains 4096 BLOCK A total of 1G byte. Address is divided into five sub-transmission, which issued the first two pages address the next three-byte address within the page, CPU to pages way to access FLASH. NAND FLASH command control word in the following table.

Table 1. Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Two-Plane Page Program ⁽²⁾	80h----11h	81h----10h	
Block Erase	60h	D0h	
Two-Plane Block Erase	60h----60h	D0h	
Random Data Input ⁽¹⁾	85h	-	
Random Data Output ⁽¹⁾	05h	E0h	
Read Status	70h		O

3.8 Realization of the power management unit

According to section 3.3 the voltage requirements, and we merge.

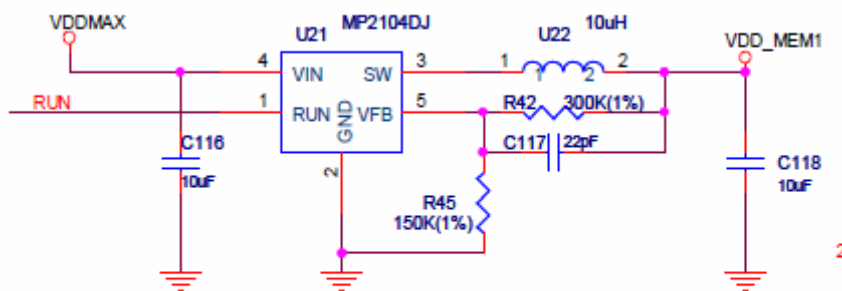
Which need to generate the following voltages.

- (1) VDDIO 3.3V is not controlled
- (2) VDDARM 1.2V controlled
- (3) VDDINT 1.2V controlled
- (4) VDDPLL 1.2V controlled
- (5) VDDMEM1 1.8V is not controlled
- (6) VDDALIVE 1.2V is not controlled
- (7) VDDOTG 3.3V controlled
- (8) VDDOTI 1.2V controlled
- (9) VDDADC 3.3V is not controlled

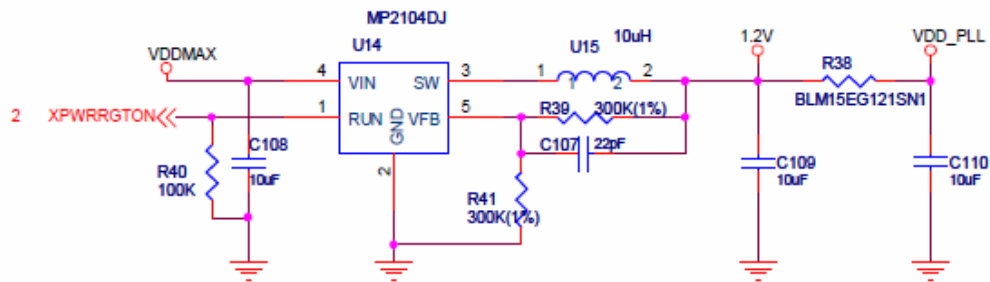
We will be one of 2348 they merged into the way power supply, you can SLEEP, turn off the power in this way to reduce the current. The VDDIO, VDDALIVE, VDDALIVE not be closed, other power supply can shut down the corresponding registers inside the CPU to achieve closure.

In order to improve power conversion performance, we use DCDC to provide high current power supply. The LDO uses a small current to convert.

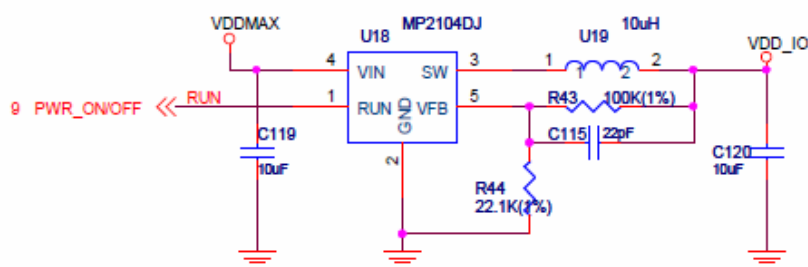
Circuit diagram is as follows:



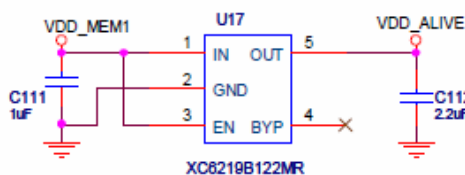
1.8V for mobile DDR



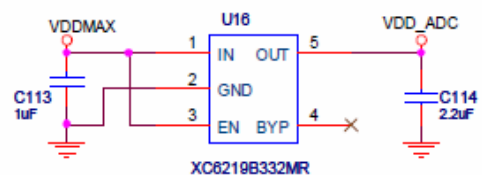
1.2V for PLL INT ARM and OTGI



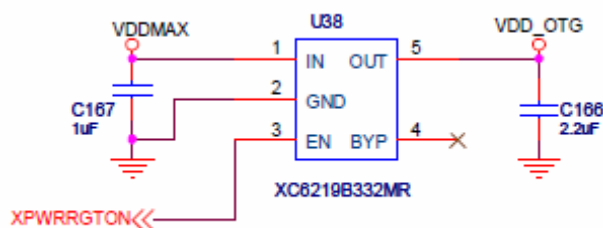
3.3V FOR SYSTEM



1.2V for ALIVE



3.3V FOR ADC or DAC



DCDC converter IC using **MPS** MPS to mention the company's MP2104DJ, it is a buck of the DCDC, the IC has the following characteristics

(1) The conversion efficiency of up to 95%

- (2) 1.7 MHz switching frequency
- (3) 600 mA of current output
- (4) wide voltage 2.5V-6V
- (5) the output voltage can be adjusted to as low as 0.6V
- (6) thermal protection
- (7) short-circuit protection
- (8) <0.1uA shutdown current
- (9) a small SOT23-5 package, effectively saving PCB area

To sum up, it is very suitable for handheld device applications.

LDO uses the company's XC6219 is a **TOREX** toirex products, this series product has the following characteristics :

XC6219 series is highly precise, low noise, using CMOS manufacturing process LDO voltage regulator chip. With low output noise, high ripple rejection, low input-output differential and very fast turn-on time. XC6219 series chip includes a reference voltage source, an error op amp, driver transistor, current limiter and a phase compensation circuit. XC6219 series of voltage limiter foldback circuit for the current limiter and the output pin to provide short circuit protection. XC6219 series, the output voltage can be set by laser trimming the output voltage range is from 0.9V to 5.0V, interval 50mV. XC6219 series can be used with low ESR ceramic capacitors, in order to reduce program costs and can improve the stability of the output, and has excellent transient response and wide frequency high ripple rejection, even if the load changes can ensure that the circuit stability. XC6219 series with CE, allowing chips to stop working in order to reduce power consumption.

3.9 6410 clock signal generation

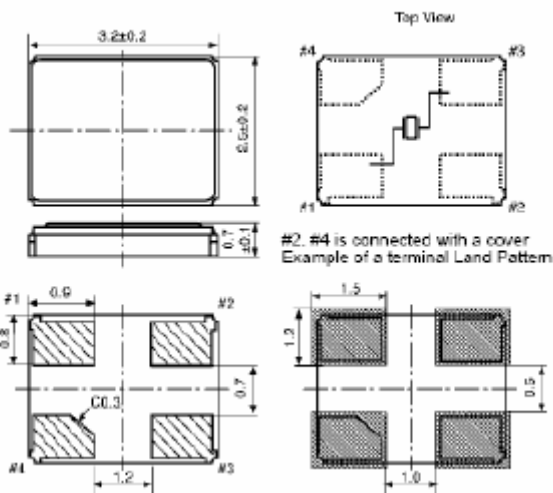
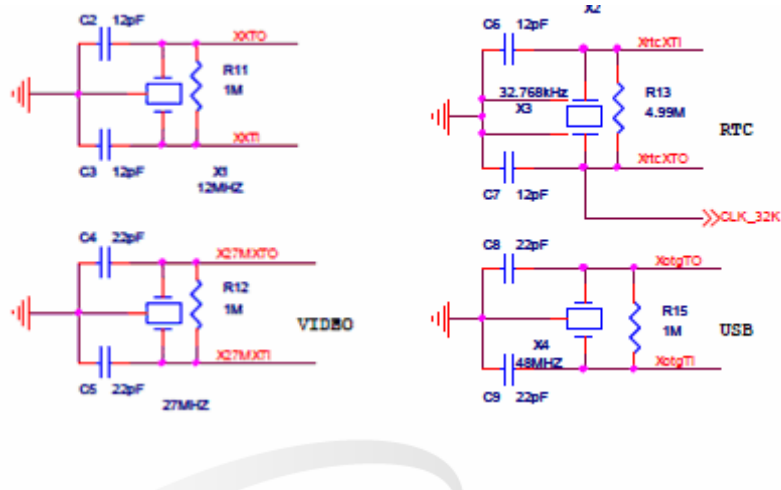
6410 needs four clock signals, are as follows.

- (1) master clock, 12MHZ.
- (2) Video clock signal 27HZ, for the display module, such as the MFC LCD TV module provides the clock signal.
- (3) USB clocks, 48MHZ, for the USB SD Card SDIO clock signal provided.
- (4) RTC clock, 32.768KHZ, for real-time clock module provides the clock signal.

It is the 123 you can choose to use active or passive crystal oscillator, in addition to the master clock, the 2 and 3, the need for a CPU register configuration to generate a corresponding clock,

choose the passive or active. The master clock is used for active or passive, by OM0 pins to configure, when the OM0 pulled, the use of passive crystal, when the home is low, the use of active crystal, when the use of passive crystal When, XEXTCLK pin need pulled.

Integrated on the requirements, design as shown below, due to cost considerations, passive crystal.



Electronics

3.10 Design and Analysis of network chips DM9000

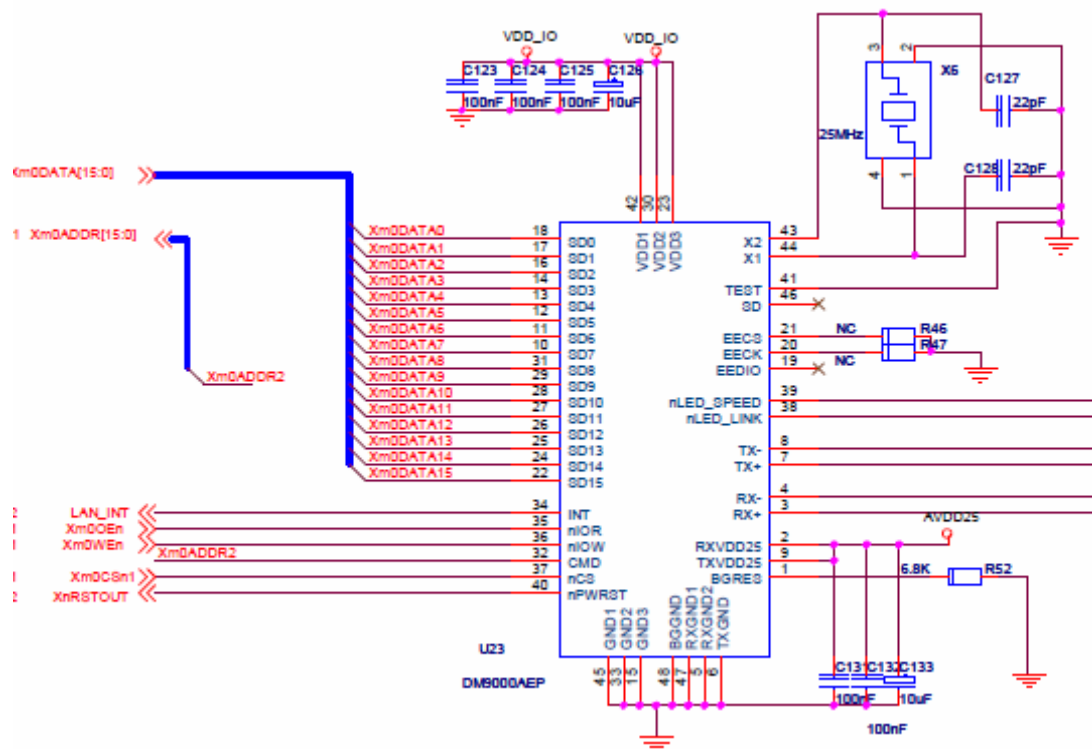
Small embedded devices to achieve Internet access, TCP / IP is the first to address the underlying hardware issues, namely, the physical layer protocol. Ethernet has a mature technology, low-cost networking products, a wealth of development tools and technical support, when the obstacles encountered in the development of fieldbus, the Ethernet control network technology for its obvious advantages of rapid development, and gradually formed a Fieldbus new standard - Ethernet. Taking into account most of the domestic LAN Ethernet, with the

switched networks, broadband networks, the development of Ethernet-based embedded devices with Internet access applications practical significance.

The existing embedded systems, most of the choices are the 10Mb / s Ethernet cards, its transmission rate slow, now people can no longer meet the requirements. While the other 10/100Mb/s card chip or a process complicated or costly is not suitable for industrial manufacturing. The DM9000 is a fully integrated low cost single-chip Fast Ethernet controller with a generic processor interface. It is designed for low power consumption, high processing performance, and its design is very simple, so it can be easy to complete the different systems of software driver development.

DM9000 - DAVICOM company's 10/100Mb/s adaptive Ethernet chips. Its characteristics are: Support 8-bit, 16-bit, 32-bit data bus width; register operation is simple and effective, there are mature Linux driver support; 3.3V interface level; the cost is very low; can also use the MII interface and the PHY chip connection.

- Connect the hardware as a whole
- 6410 logic diagram to connect with the DM9000



DM9000 is a 16-bit bus, and then in the 6410's Xm0 the bus.

DM9000 Default I/O base address is 300H. CMD pin used to set the COMMAND mode, CMD is high, select the data port. CMD is low, the selected address port. Data ports and address of the

port address code decided by the following formula:

DM9000 address port = high chip select address +300H+0H

DM9000 data port = high chip select address +300H+4H

Among them, high chip select address provided by the S3C6410's Bank1, namely: 0x18000000

DM9000 CMD pin connected to the 6410's Xm0 address lines ADDR2, it can be used to select to send the address or data.

DM9000 The IOR and IOW bus connected to the 6410 reading and writing pins of Xm0

DM9000 reset pin connected to the reset output of 6410 to ensure the CPU is running and then reset the chip.

Fat break.

DM9000 interrupt pin connected to the CPU-EINT7 pin, high level trigger interrupt

DM9000's EECS and EECK pins can select 8-bit or 16-bit bus and high-low touch

Table 2-2. Device Specific Address Space

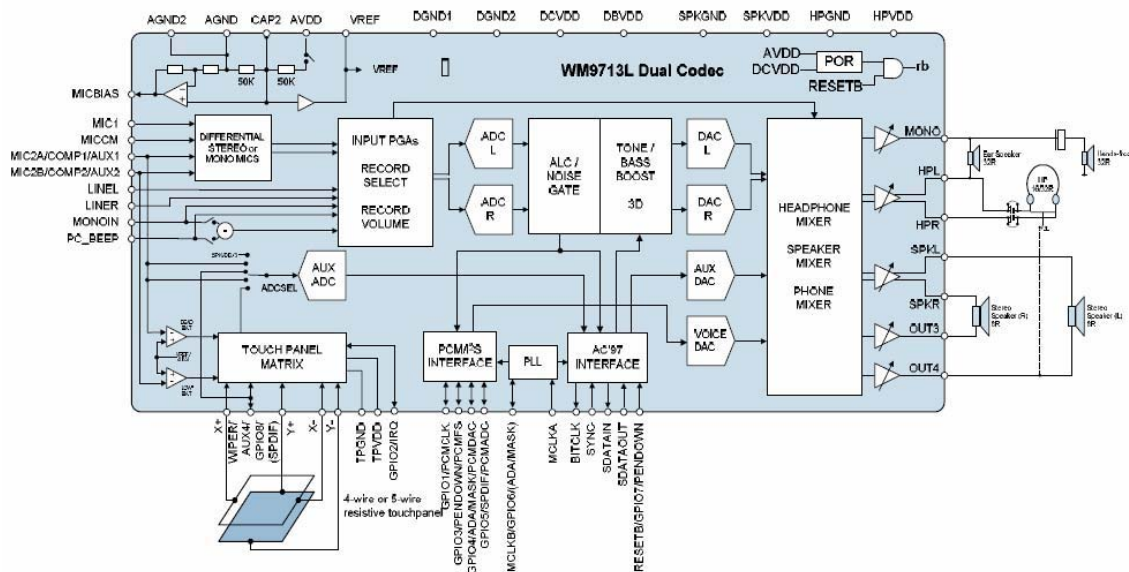
Address		Size(MB)	Description	Note
0x0000_0000	0x07FF_FFFF	128MB	Booting Device Region by XOM Setting	Mirrored Region
0x0800_0000	0x0BFF_FFFF	64MB	Internal ROM	
0x0C00_0000	0x0FFF_FFFF	64MB	Stepping Stone (Boot Loader)	
0x1000_0000	0x17FF_FFFF	128MB	SROMC Bank0	
0x1800_0000	0x1FFF_FFFF	128MB	SROMC Bank 1	
0x2000_0000	0x27FF_FFFF	128MB	SROMC Bank 2	
0x2800_0000	0x2FFF_FFFF	128MB	SROMC Bank 3	
0x3000_0000	0x37FF_FFFF	128MB	SROMC Bank 4	
0x3800_0000	0x3FFF_FFFF	128MB	SROMC Bank 5	
0x4000_0000	0x47FF_FFFF	128MB	Reserved	
0x4800_0000	0x4FFF_FFFF	128MB		
0x5000_0000	0x5FFF_FFFF	256MB	DRAM Controller of the Memory Pprt1	
0x6000_0000	0x6FFF_FFFF	256MB		

3.11 Audio Design and Analysis

WM9713L is a highly integrated input/output devices, designed for mobile computing and communications and design. The chip uses dual codec architecture to run through the AC link interface supports high-fidelity (Hi-Fi) stereo codec functions, but also through a PCM type Synchronous Serial Port (SSP) additional support for the audio codec functionality . The chip also provides a third-assisted digital-analog converter for use with the master codec different sampling rates, support the generation of control tones (supervisory tones), or ring tones. The device can connect directly to a 4-wire or 5-wire touch-screen, mono or stereo microphones, stereo headphones and stereo speakers, thereby reducing the total number of system

components. With headphones, speakers and receiver without capacitor connections, can save cost and printed circuit board area. In addition, it also provides a number of analog input and output pins, and wireless communication devices to connect seamlessly integrated with simulations. AC-97 through a line with the standard single AC-Link interface, you can connect and control all functions of the chip. Can be directly input 24.576MHz master clock, or by on-board phase-locked loop from a 13MHz (or other frequency) clock from within, the PLL supports a wide range of 2.048Mhz to 78.6Mhz input clock. WM9713L operating supply voltage range of 1.8V-3.6V; any part of the chip can be achieved through software control shutdown to reduce power consumption. The device uses a small 7 × 7mm leadless package, handheld and portable systems applications is the ideal solution for :

- (1) AC'97 Rev 2.2 compatible stereo codec
- (2) DAC SNR 94dB, total harmonic distortion of-85dB
- (3) ADC SNR 87dB, total harmonic distortion of-86dB
- (4) Variable audio speed, supports all WinCE sample rates
- (5) Tone control, bass enhancement and 3D sound to enhance
- (6) On-chip 45mW headphone driver
- (7) On-chip 400mW mono or stereo speaker drivers
- (8) Stereo, mono or differential microphone input
- (9) Automatic level control (ALC)
- (10) Mike and Mike jack key test
- (11) Auxiliary mono DAC (ring tones or DC voltage generated)
- (12) Connect to a wireless chip set, seamless interface
- (13) Resistive Touch Screen Interface
- (14) Support for 4-wire and 5-wire panels
- (15) 12-bit resolution, INL ± 2 LSBs (<0.5 pixels)
- (16) X, Y, and touch-pressure (Z) measurement
- (17) Power stroke in sleep mode, the detection
- (18) Support for additional speech codec interface PCM/I2S
- (19) Audio clock generation PLL
- (20) Support input clock range: 2.048MHz-78.6MHz
- (21) 1.8-3.6V power supply voltage (digital supply voltage as low as 1.62V, speaker up to 4.2V)
- (22) 7x7mm 48-pin QFN package

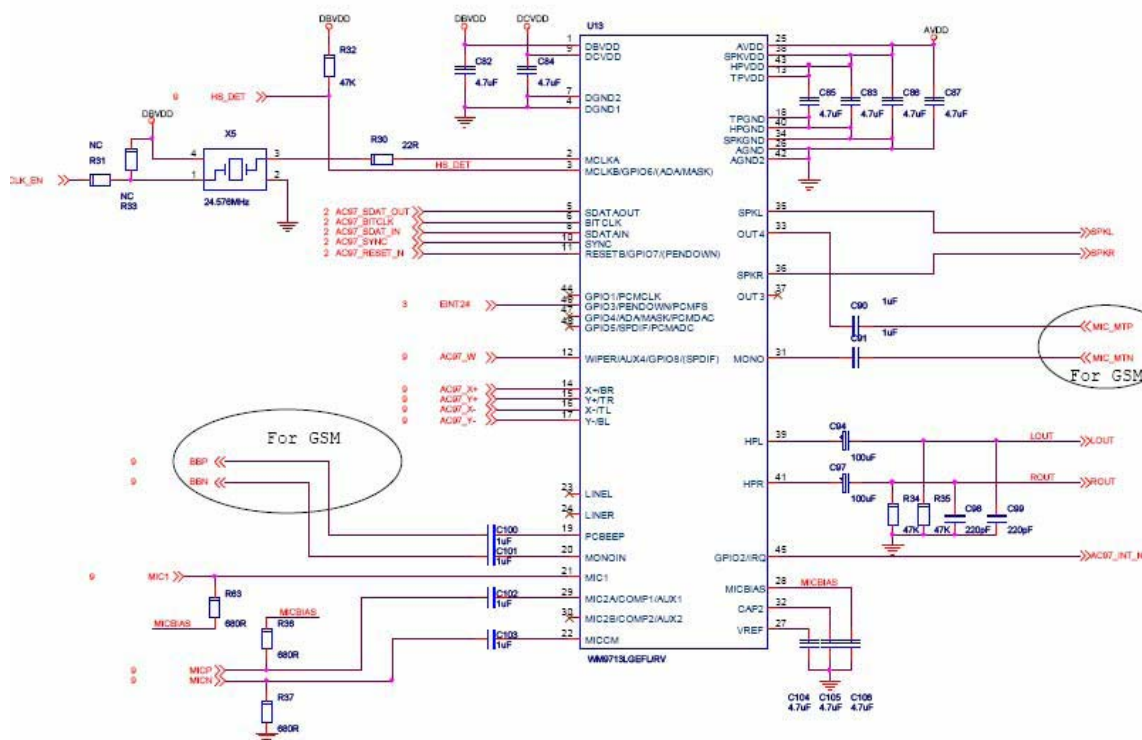


[Functional Block Diagram]

WM9713 using AC97 bus connected with the 6410. We are designed to provide the following features

- (1) LOUT and ROUT integral headphone output.
- (2) SPKL, and the composition SPKR speaker output, but because of the built-in power into a smaller amplification is required an external amplifier.
- (3) MICP, and the composition of Mike MICN differential input, you can directly access MIC.
- (4) MIC1 separate MIC input.
- (5) MIC_MTP and MIC_MTN are WM713 differential output can be directly connected to the GSM audio input.
- (6) BBP and BBN are WM713 differential input can be directly to the GSM audio output
- (7) TOUCH features, core board leads to 5 and 4-wire interface TOUCH.

Its schematic design are as follows

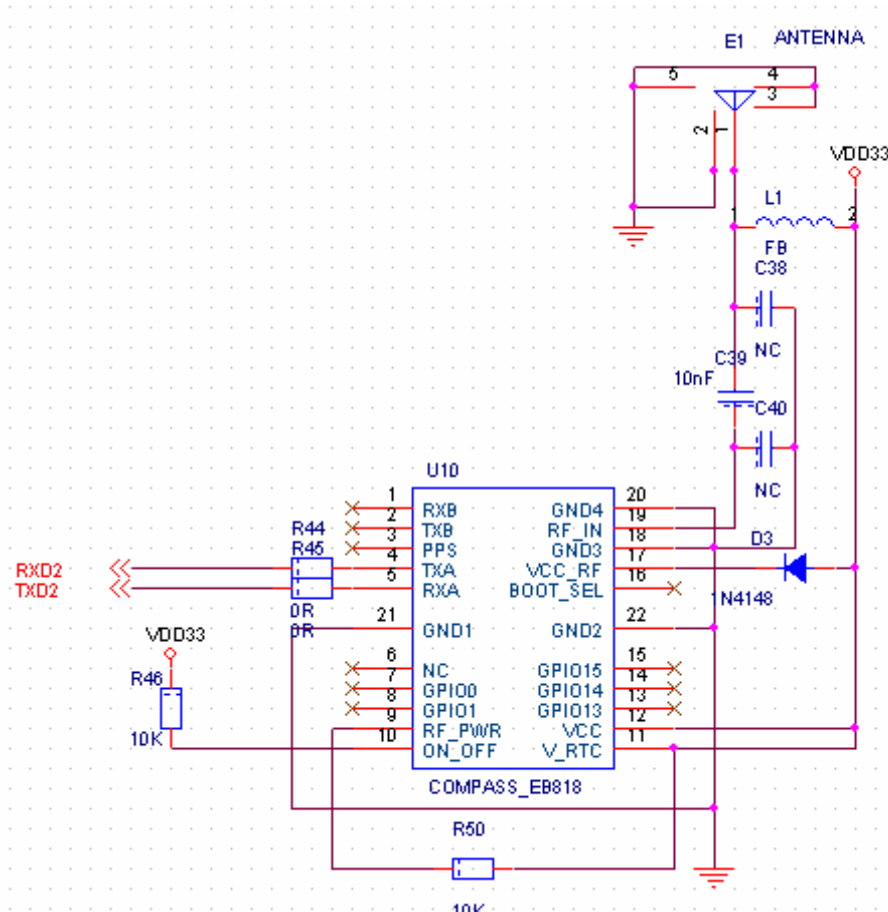


WM9713 using active 24.576MHz as the clock source, the internal PLL circuit and divider circuit can be divided frequency to each module.

WM9713 relatively wide power supply range, 1.8 ~ 3.6V, using the VDDIO power supply can be, its internal modules can not SLEEP in order to achieve energy-saving purposes. We can also go through the AC97 bus, the preparation of the internal registers.

WM9713 has more than one mixer, in order to enable the CPU and the GSM part of the sharing of a MIC and speakers or headphones, we can reasonably with the mixer, so that the path can be carried out as required, reducing the use of external analog switches.

3.13 GPS module circuit design



GPS module connected to the CPU on the UART2 serial port, GPS's ON_OFF pin is the power supply module enable pin, to open high-powered, low contrast. Antenna design part of the module adds a resistors and capacitors, in order to adjust the antenna sensitive.

3.14 GPRS / GSM hardware design and analysis

SIM300 is a small plug-in modules perfect tri-band / quad-band * GSM / GPRS solution uses industry-standard interface, making with GSM / GPRS 900/1800/1900MHz function SIM300C small size and low power voice , SMS, data and fax information, high-speed transmission.

SIM300 excellent performance make it used in many areas, such as WLL, M2M, handheld devices and so on.

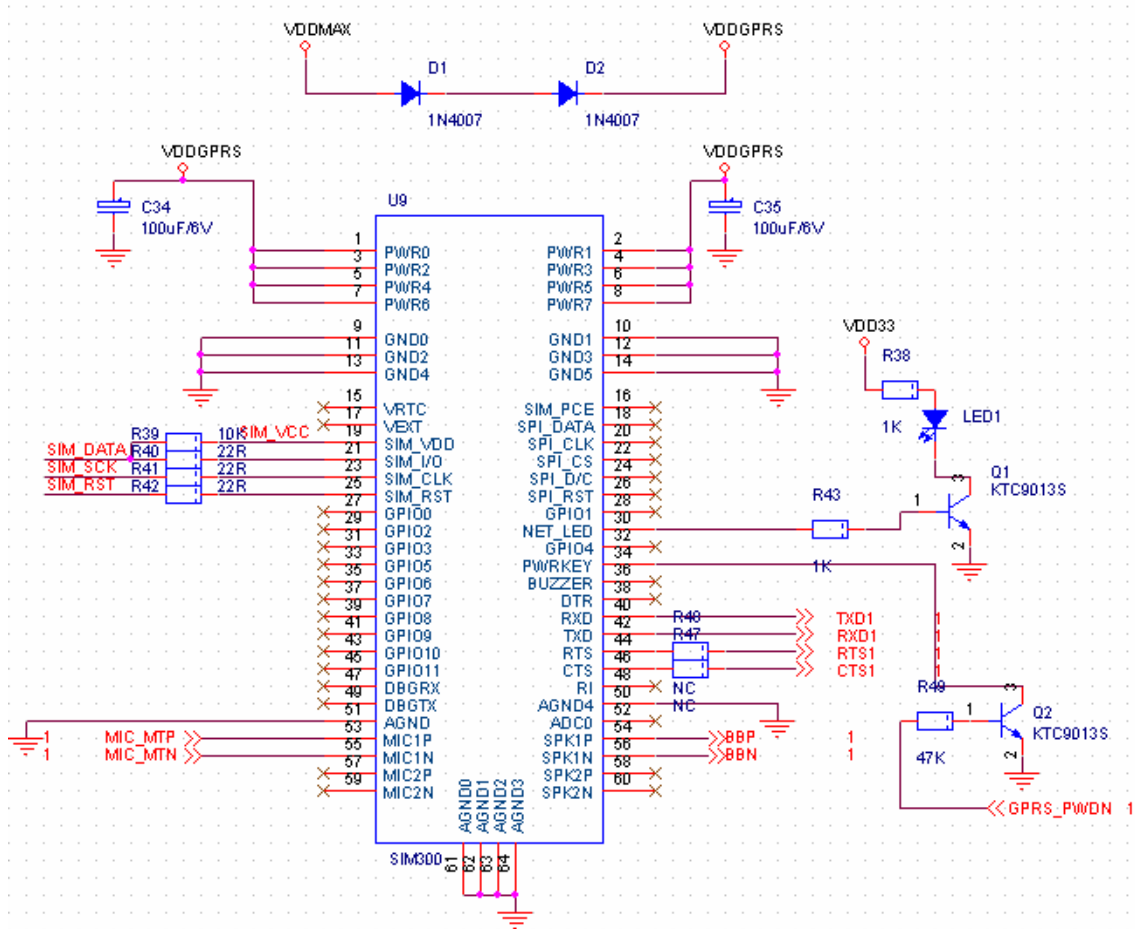
Tri-band / quad-band GSM / GPRS module, Dimensions 40x33x2.85mm support customized MMI and keypad / LCD embedded powerful TCP / IP protocol stack based on mature and reliable technology platform, our wireless communication module will provide you the technical support ranging from product definition to design and manufacture of a full-service

Basic features:

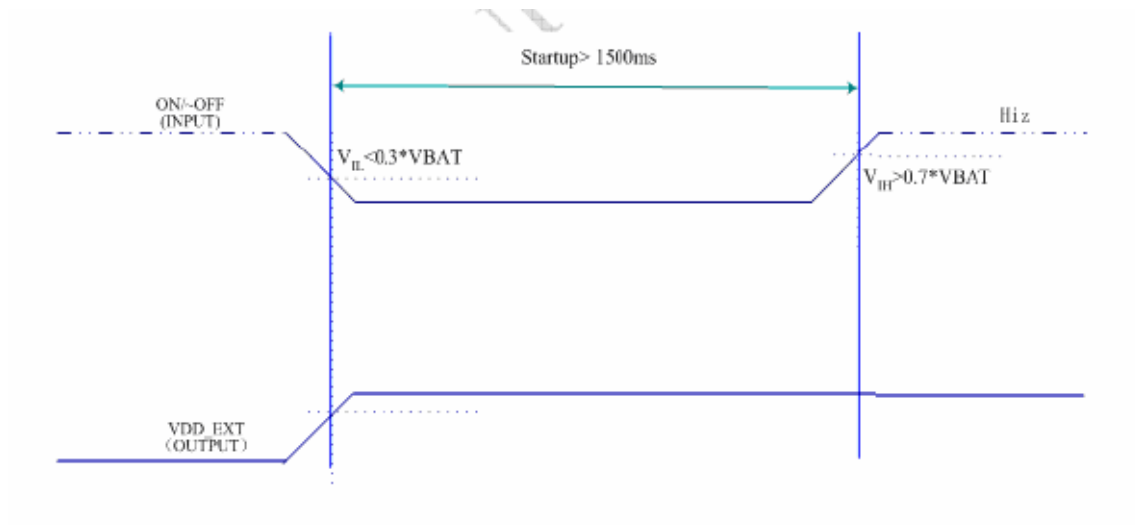
- (1) Tri-band GSM/GPRS900/1800/1900MH or quad-band 850/900/1800/1900MHz
- (2) GPRS (class 10) standard
- (3) GPRS (class B)
- (4) GSM (2/2+) Standard
 - Class 4 (2W @ 850/900MHz)
 - Class 1 (1 W @ 1800/1900MHz)
- (5) Size : 40mm x 33mm x 2.85mm
- (6) Weight : 8g
- (7) Control via AT commands (GSM07.07, 07.05 and enhanced AT commands)
- (8) SIM application toolkit support
- (9) Voltage range of 3.4 .. 4.5 V Low power consumption
- (10) Normal operation temperature : -20°C to +55°C
- (11) Limited operating temperature : -25°C to -20°C and +55°C to +70°C
- (12) Storage temperature : -40°C to +80°C



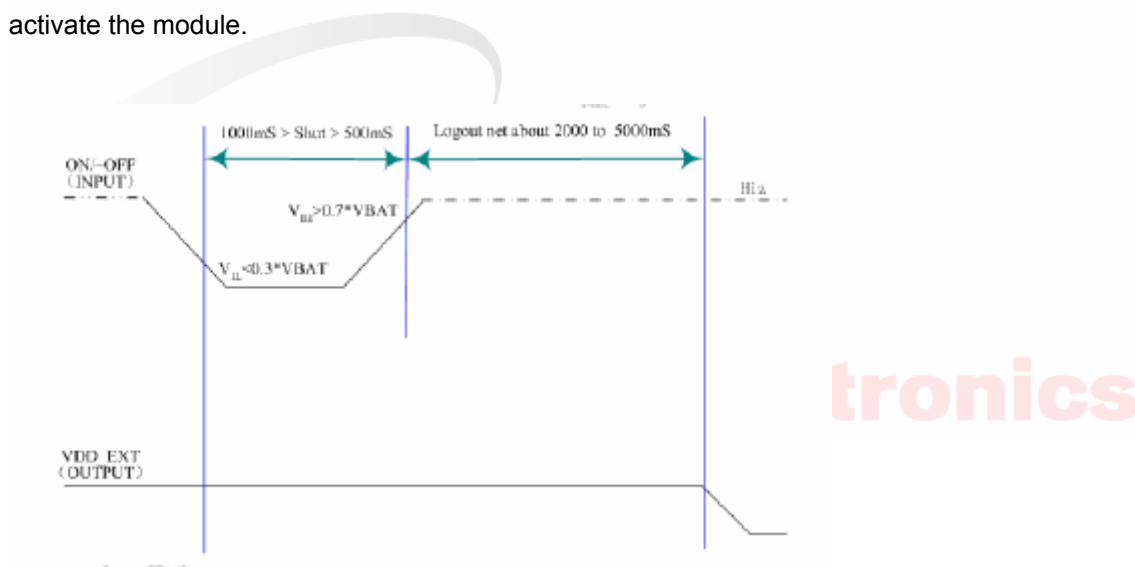
Schematic design of the following



- (1) Power supply design, as GPRS or GSM firing takes a great deal of current, in the design should be able to provide the maximum 1.2A, in the design we use an external 5V input voltage of 2 1N4007 carried out by two step-down, making VDDGPRS In between 3.8-4.5, you can replace a section of diode for low-voltage tubes, such as 1N5820. $5V - 0.7V * 2 = 3.6V$, it is proposed to change one of the 1N4007 for the 1N5280, the $5V - 0.7V - 0.2V = 4.1V$.
- (2) LED instruction: When the GSM module is working properly (not necessarily a connection), then LED lights keep flashing.
- (3) PWRKEY is a module to enable the start-side, SIM300 start requires the following waveform.

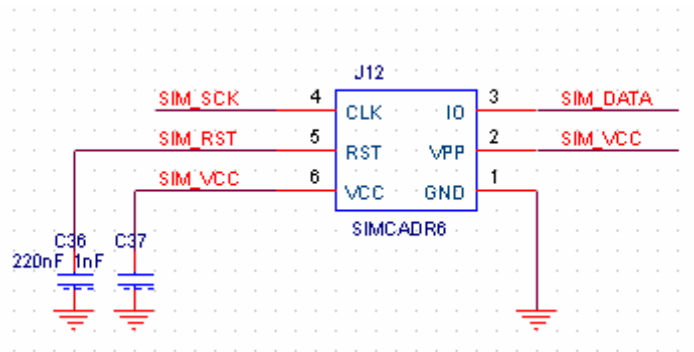


PRKEY pin internal pull-up to the VDDBAT pin, so the design Q2's collector is no longer pulled up to high. Through GPRS_PWDN to control PWRKEY pin to meet the above timing, in order to activate the module.



The above timing module timing is off

(4) SIM connection, as shown below.



(5) TXD1 and RXD1 the serial port to connect to GPRS on, CTS1, and RTS1 can be selected when using the GPRS Internet access, you can not use.

(6) and the CPU in order to use the same MIC and speaker, GSM audio input and output need to receive WM9713 chip, in order to WM9713-chip inter-mixed

(7) AT instruction set, please refer to related documentation.

3.15 Camera Circuit Design

The design of this camera module is compatible with both OV9650 and OV3640 camera module, because both the IO voltage is not the same, so in the design adds a level shifter IC ADG3308, at the same time using tandem exclusion to non-use of ADG3308

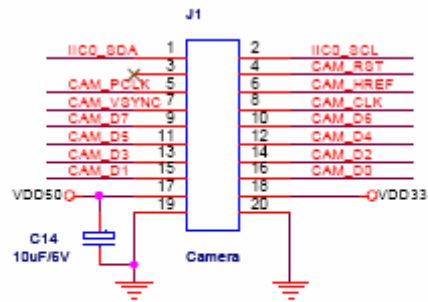
OV's camera module, need to adopt SCCB bus to the configuration, that is, IIC bus, we are in the design of the SCCB bus connected to the CPU of the IIC bus channel 0.

OV series of camera chips need three-way voltage :

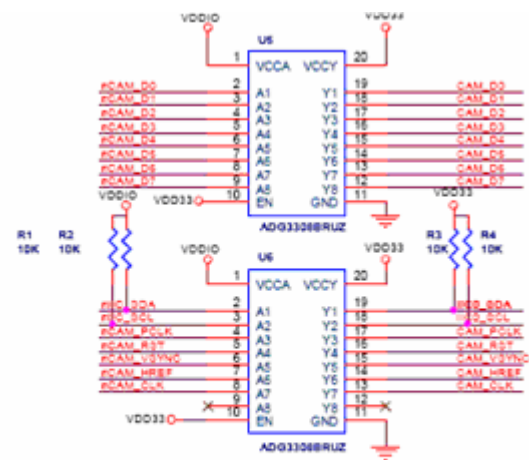
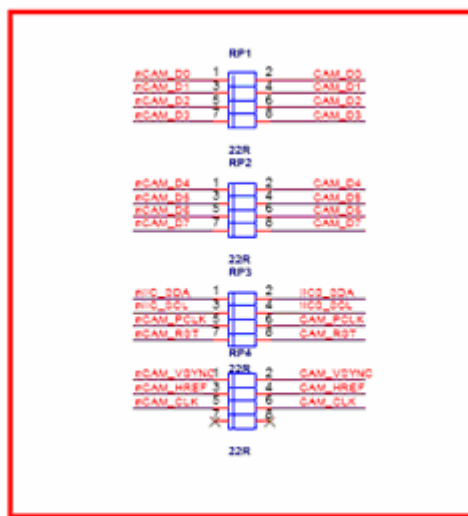
Core voltage, Analog voltage, IO Voltage

We can reference manual, to select the appropriate power LDO to give the module.

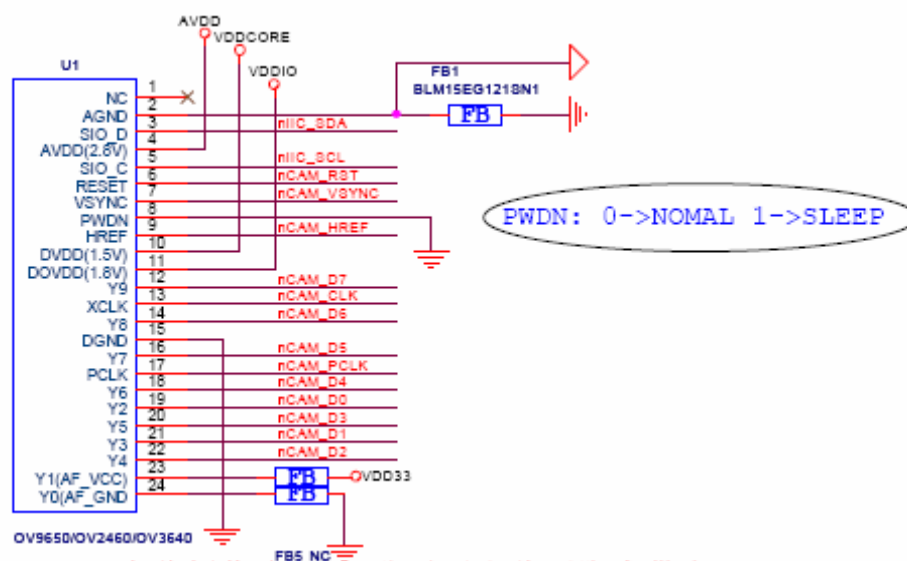
Reference design schematic is as follows.



Extend Camera Socket



Level translators or not switching, according to chip model selection



[Camera module interface (FPC24)]

In need of attention in the design of places :

- (1) the voltage must be specified in the manual range, otherwise it might burn out chips
- (2) the level must be matched, otherwise easy to error, IIC failed to read and write
- (3) PWDN pin is low, so that energy, high power module is turned off
- (4) pay attention to the normal level RESET pin state, otherwise the configuration is unsuccessful IIC
- (5) due to an 8-bit CPU bus, CAMERA, we need to 8-bit bus connected to the OV-chip high-8, the minimum two can connect GND or not received.

3.16 Analog camera interface

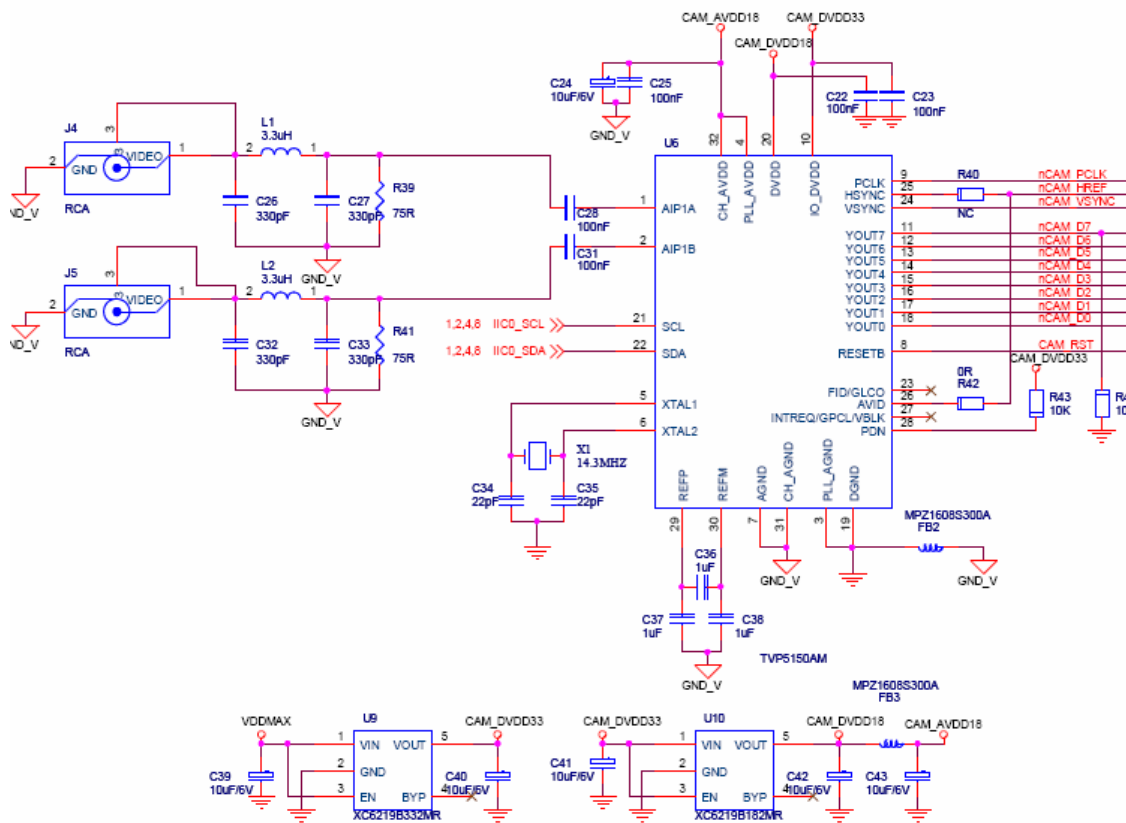
This development board supports analog camera inputs, support PAL and NTSC formats, and this conversion is achieved relying TVP5150, TV5150 convert analog video signals or RGB signals as YCBB signal to pass into the 6410 camera Interface.



Two switch the video signal input, and can only use all the way.

TVP5150 is the ultra-low power consumption, support for NTSC/PAL/SECAM formats, such as high-performance video decoder, in normal working hours, it consumes only 115mW, and has ultra-small package (32-pin TQFP), so it is applicable in portable, high-volume, high-quality and high performance video products. It can receive 2 way composite video signal (CVBS) or 1 Way S-Video signals. MCU I2C bus by setting the internal register, you can output 8-bit ITU-R BT.656 4:2:2 signal (sync signal embedded), and 8-bit 4:2:2 ITU-R BT.601 signal (Synchronous signal separation, single pin output). The development board for compatibility with CMOS camera and TVP5150 input, plus a 74HC245 for signal switching.

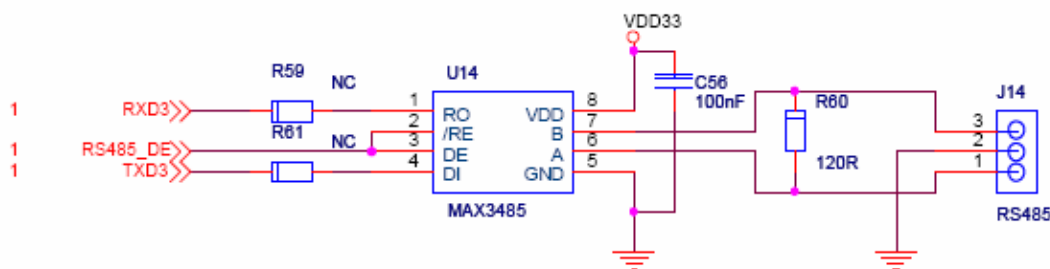
Note : First 8-bit code switch hit the ON state, the TVP5150 signal, OFF state signal for the CMOS camera.



3.17 RS485 Interface

In data communications, computer networks and distributed industrial control systems are often required to use serial communication for data exchange. Currently, RS-232, RS-485, RS-422 interface standard for serial communication of several. RS-232 serial interface standard is the first, a short distance (<15M), low baud rate serial communication which is widely used. Then RS-232 interface standard for the communication distance is short, relatively low baud rate conditions in the RS-232 interface standard based on the proposed the RS-422 interface standard, RS-485 interface standard to overcome these deficiencies. The following detailed RS-232, RS-422, RS-485 interface standard. RS-232 serial interface standard is kind of species in the low-speed serial communications to increase communication distance of the single-ended standards. RS-232 to unbalanced transmission, that is, single-ended communication. The send and receive side data signal is compared to the signal. Therefore, the common-mode rejection ability, coupled with the distributed capacitance twisted pair, the maximum transmission distance is about 15M, the highest rate of 20KBPS, and the only support point to point communication. RS-232 serial interface standard for the limitations, it also raised the RS-422, RS-485 interface standard. RS-485/422 differential receiver with a balanced send and the realization of

communication: the transmitter to the serial port of TTL level signals into differential signals A, B two outputs, after transmission through the cable differential signal at the receiving end will be reduced to TTL level signal. As commonly used twisted pair transmission line, is differential transmission, so the strong anti-interference ability of the common mode, the bus transceiver high sensitivity, can detect voltages as low as 200mV. Therefore, all outside signals can be restored in the 1000 meters. RS-485/422 maximum communication distance of about 1219M, the maximum transfer rate of 10Mb/S, data rate and transmission distance is inversely proportional to the 100Kb/S transfer rate, we can achieve maximum communication distance, even if the required transmission long distances, and needs 485 relay. RS-485 half-duplex mode, supports multi-point data communications. RS-485 bus network topology, matching the general use of the bus terminal structure. That each node using a bus will be connected in series, will not support the ring or star network. If you need to use the joint topology, you must use the 485 or 485 hub repeater can. General maximum support RS-485/422 bus node 32, if you use a special 485 chip can reach 128 or 256 nodes, the largest can support up to 400 nodes.



Users must pay attention to:

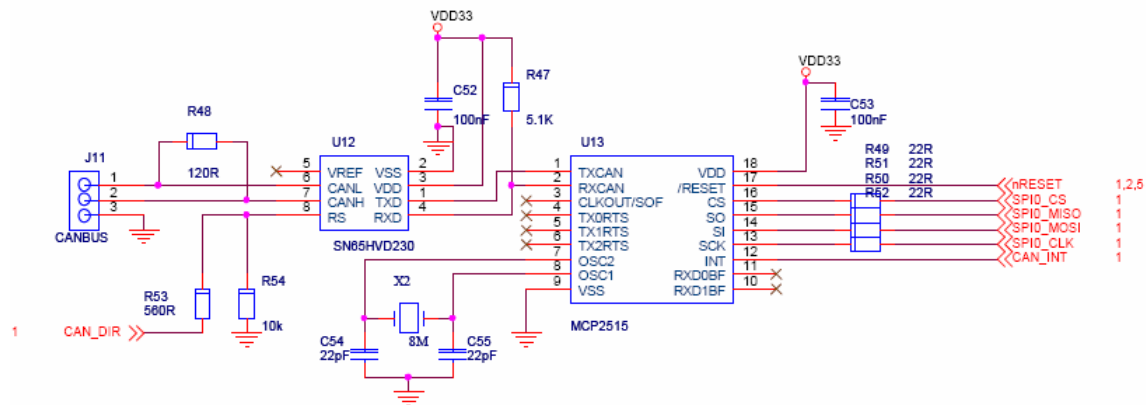
When using the RS485 interface, to be self-R59 and R61 for the 0R welding resistance, or direct short circuit.

The time TXD3 and RXD3 can no longer use for the RS232 interface, that is onboard the J8 I can no longer use TXD3 and RXD3 through MAX3485 converted to RS485 signals, while, after converted to RS232 signal Max3232, then TXD3 and RXD3 as 485 and 232 can not both. Mo into RS232 signal, users must remove their own welding and resistance.

3.18 CAN bus interface

Microchip Introduces MCP2515 is a SPI interface with independent CAN controller. It fully supports the CAN V2.0B technical specifications, communication rates up to 1 Mbps, with 3 to send buffer, 2 reception buffer, 6 29 Acceptance Filter registers and two 29-bit acceptance mask registers [2] ; its SPI interface, the clock frequency of up to 40 MHz, an SPI host interface can be extended to meet the multiple needs of CAN bus interface.

CAN bus communication with its high speed, good resistance to electromagnetic interference, high-reliability serial communication can be realized, so in practical applications has a very high value. However, with the integration of technology continues to evolve, in order to save power and reduce circuit size, some new CAN-bus controller logic using LVTTTL, which requires corresponding bus transceiver. TI SN65HVD230 circuits produced a good solution to this problem.

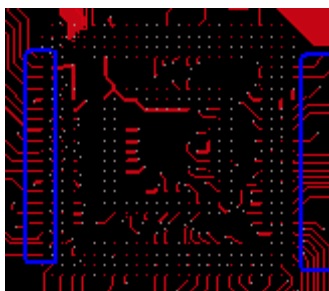


Users should be noted that X2 uses 20MHz crystal, rather than the 8MHz schematic.

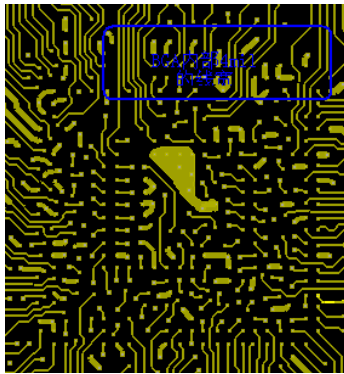
4. Analysis of the core board PCB

4.1 Core PCB board width line of conventional distance

- (1) Conventional signal line line spacing 4mil
- (2) TOP-layer BGA periphery in the first row width 5 mil

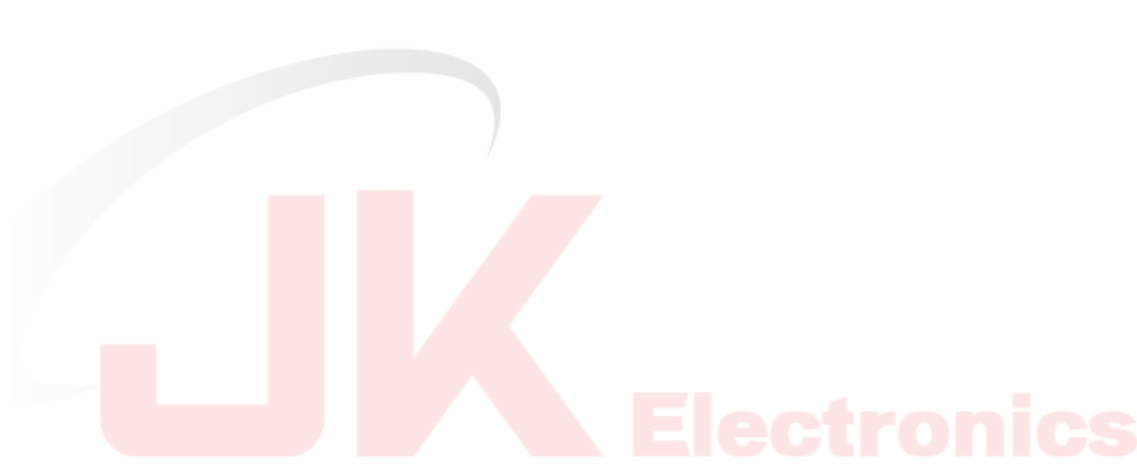


- (3) BGA internal width 4 mil



(4) power supply and GND minimum line width 10mil, the biggest 20mil

Width away from the proposed line is best not to appear 4mil below to facilitate the system board.



4.2 Blind-hole size and pore distribution of buried

The panel board used in the design of blind pass buried hole, there is no hole, in which layer 1-2 blind hole, hole parameters are 10/4

2-7 layer buried hole, hole parameters 16/8, 7-8 layer blind hole, hole parameters are 10/4.

In this plate design, the hole can play as far as possible on the pads hit the pads. Because buried with blind hole design, but a smaller aperture, there is no leakage in the SMD when the phenomenon of tin.

4.3 DDR cabling requirements and specifications

- Power supply and GND alignment rules

- (1) Formation must be close to the signal layer to provide a good return path.

- (2) The phenomenon of formation must be non-fragmented.

- (3) Grounding pin of the processing :

- a) Must be as close to the pin-hole.

- b) The grounding pin bypass capacitor as close to the CPU corresponding grounding pin.

- c) Will be close to the ground pin connected with the alignment.

- (4) power supply pins of the processing :

- a) the power pin bypass capacitors as close to the corresponding CPU power pins.

- b) must be as close to the pin hole.

In the PCB area is allowed under the conditions of bypass capacitors placed as much as possible.

- Data signal alignment rules

Data signals including DQ, DQM, DQS signal is divided into four groups.

The same group of signals must match the length of 1.5mm (about 60mil) or less, and as far as a signal layer alignment, if the same set of signals in different signal layer alignment, the need for impedance matching layer PCB.

Signal Pin	MASK	CLOCK
DQ[7:0]	DQM0	DQS0
DQ[15:8]	DQM1	DQS1
DQ[16:23]	DQM2	DQS2
DQ[24:32]	DQM3	DQS3

- Address control signal alignment rules

Address control signals, including CSn, CKE, ADDR [13:0], BA [1:0], RASn, CASn, WEn, and the AP, the length of matches must be less than 1.5mm.

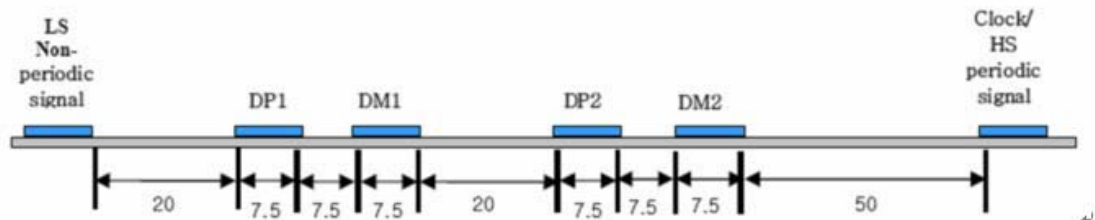
- Clock signal and the SCLK alignment rules SCLKn

SCLKn clock signal SCLK and the alignment must be differential approach than the length of the clock signal data signals and address control signals must be longer. Length of relationship is this :

- (1) Data signal "address control signal" clock signal
- (2) The above three groups of signal difference between the two groups control the length of 10mm (390mil) or less.
- (3) The best part of the impedance for the DDR control within 50-60 ohms.

4.4 USB differential alignment rules

- (1) the clock and differential signal lines should be as short as possible.
- (2) high-speed alignment as far as possible not to have had holes, and use 45 degrees or round the corner.
- (3) do not in crystals, crystal, inductors, magnetic beads, as well as integrated circuits below the alignment.
- (4) the signal line is to ensure that the full power and ground planes.
- (5) the clock signal and the other walking distance between the lines to keep more than 50mil.
- (6) on the signal line width and spacing shown in Figure 1.
- (7) differential signal lines of the length of the difference should be controlled at less than 150mil.



4.5 Structure of the core plate laminate

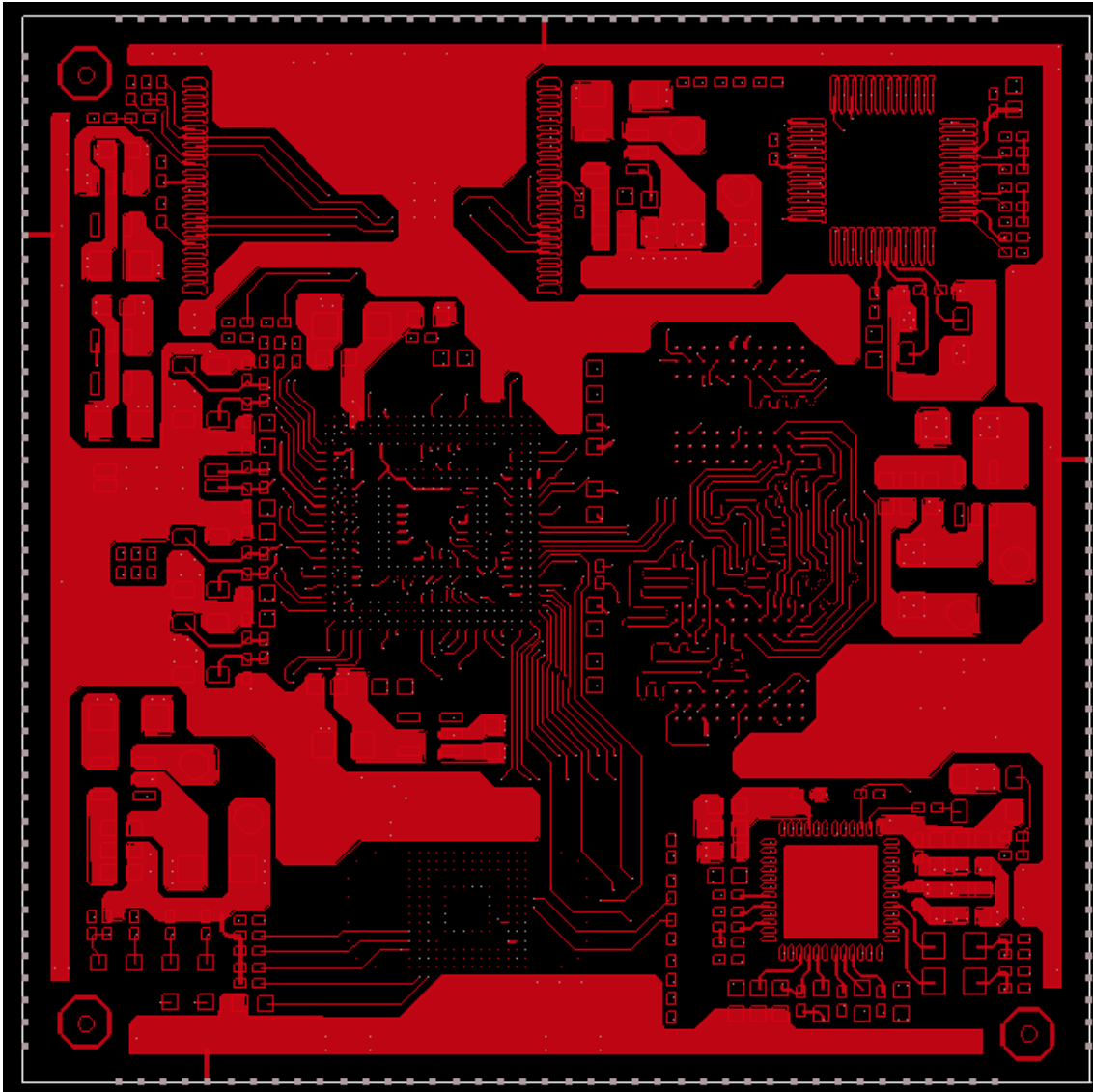
Layer Stackup		Thickness (Mil)	Oz
Silk Top			
Solder Top			
ART01		1.9	0.5
RCC		2.6	
ART02		0.7	0.5
FR4		4.5	
GND03		0.7	0.5
CORE		4	
ART04		0.7	0.5
FR4		9	
ART05		0.7	0.5
CORE		4	
GND06		0.7	0.5
FR4		4.5	
ART07		0.7	0.5
RCC		2.6	
ART08		1.9	0.5
Solder Bot			
Silk Bot			

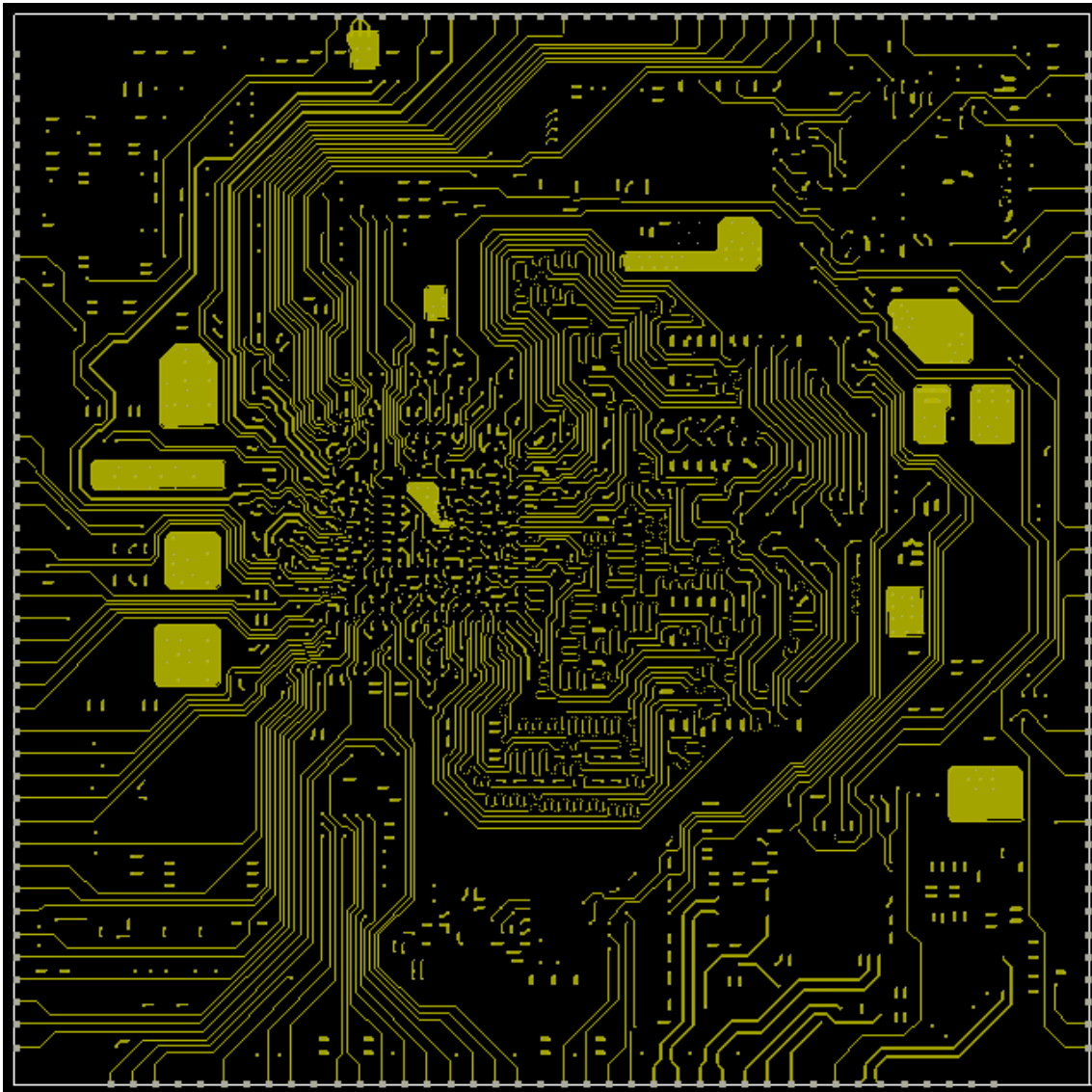
4.6 core plate impedance control

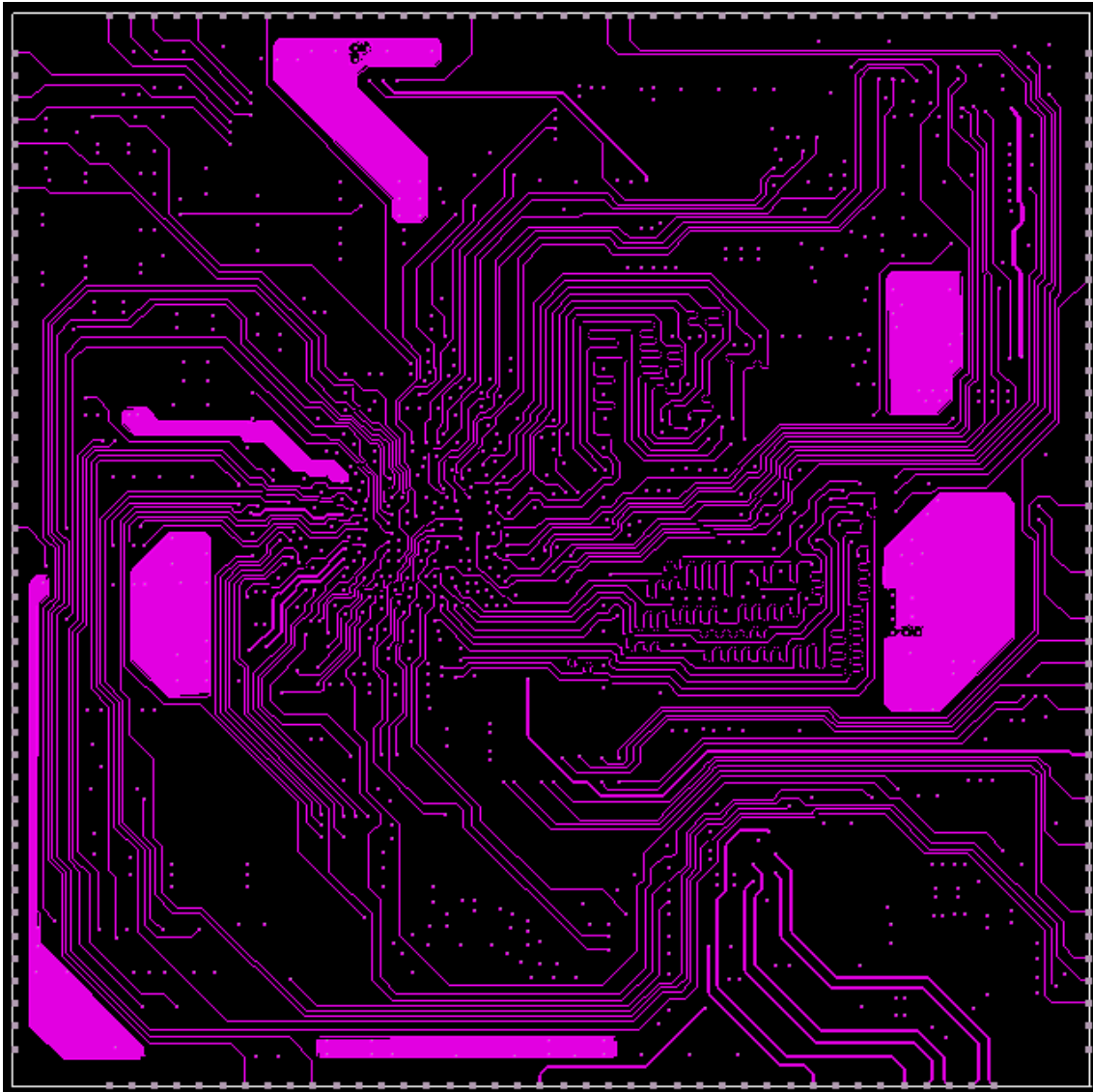
BOARD NAME: CORE6410		LAYERS: 8	BOARD THICKNESS: 1.0mm $\pm$ 10%
UNITS: MILS		OPEN WINDOWS:	SPELL MODE:
SOLDER MASK: IPC SM-840 (COLOR: GREEN)			
SILKSCREEN COLOR: WHITE			
DIELECTRIC MATERIAL: FR-4			
Er@1GHz: 4.2 $\pm$ 0.5			
PLATED TECHNIQS: [4]	1. HASL (Sn/Pb)		
	2. HASL (Pb-Free)		
	3. GOLDEN FINGER, OTHERS SPRAYED WITH TIN SOLDER (Pb-Free)		
	4. ENIG		
	5. OTHERS (ImAg/ImSn/OSP)		
SINGLE IMPEDANCE [Z ₀]	50 $\pm$ 10% Ohm with 5mil trace width for layer 1&8		
	50 $\pm$ 10% Ohm with 4mil trace width for layer 2&4&5		
DIFF. IMPEDANCE [Z _d]	100 $\pm$ 10% Ohm with 5.1/8/5.1 for layer 1		
	100 $\pm$ 10% Ohm with 4.1/8/4.1 for layer 2&5		
SHORT NET NO.	SHORT NET POSITION		
[0]			
DESIGN BY: EDADOC	QA:002	E-MAIL: nida@PCBDOC.COM	Tel: 0755-88852189

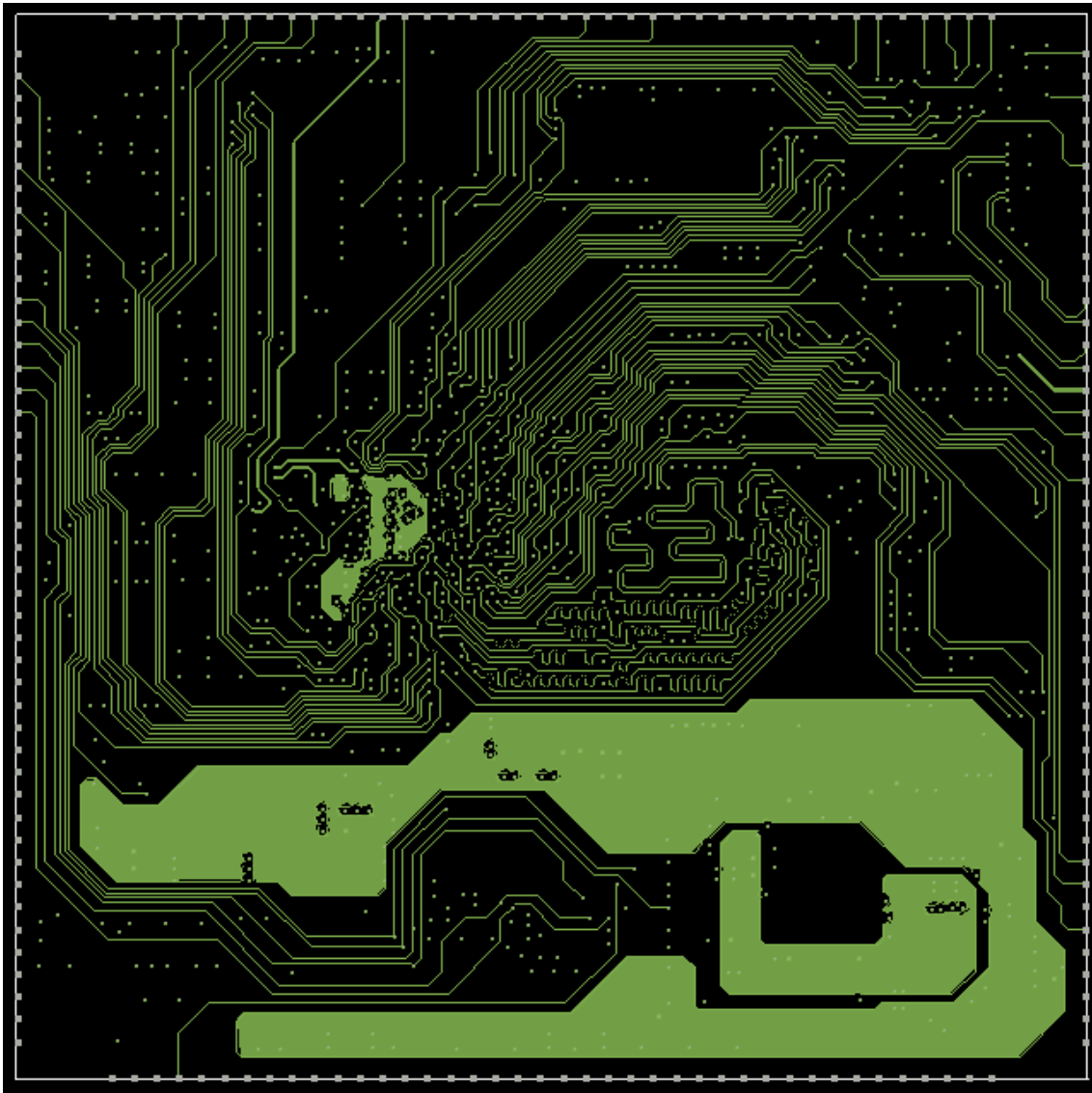


[Figure 4.6] PCB alignment layer to display the

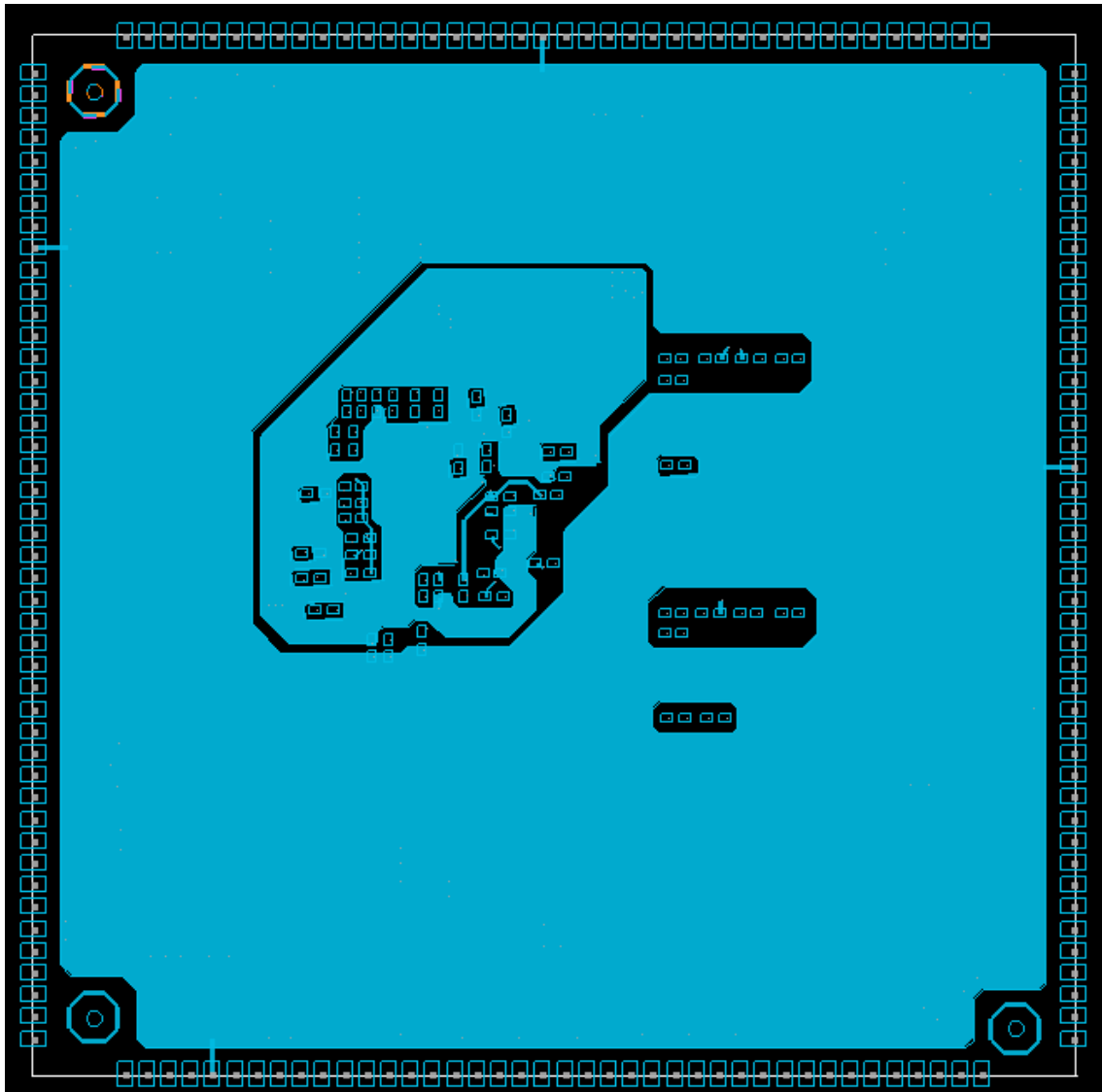




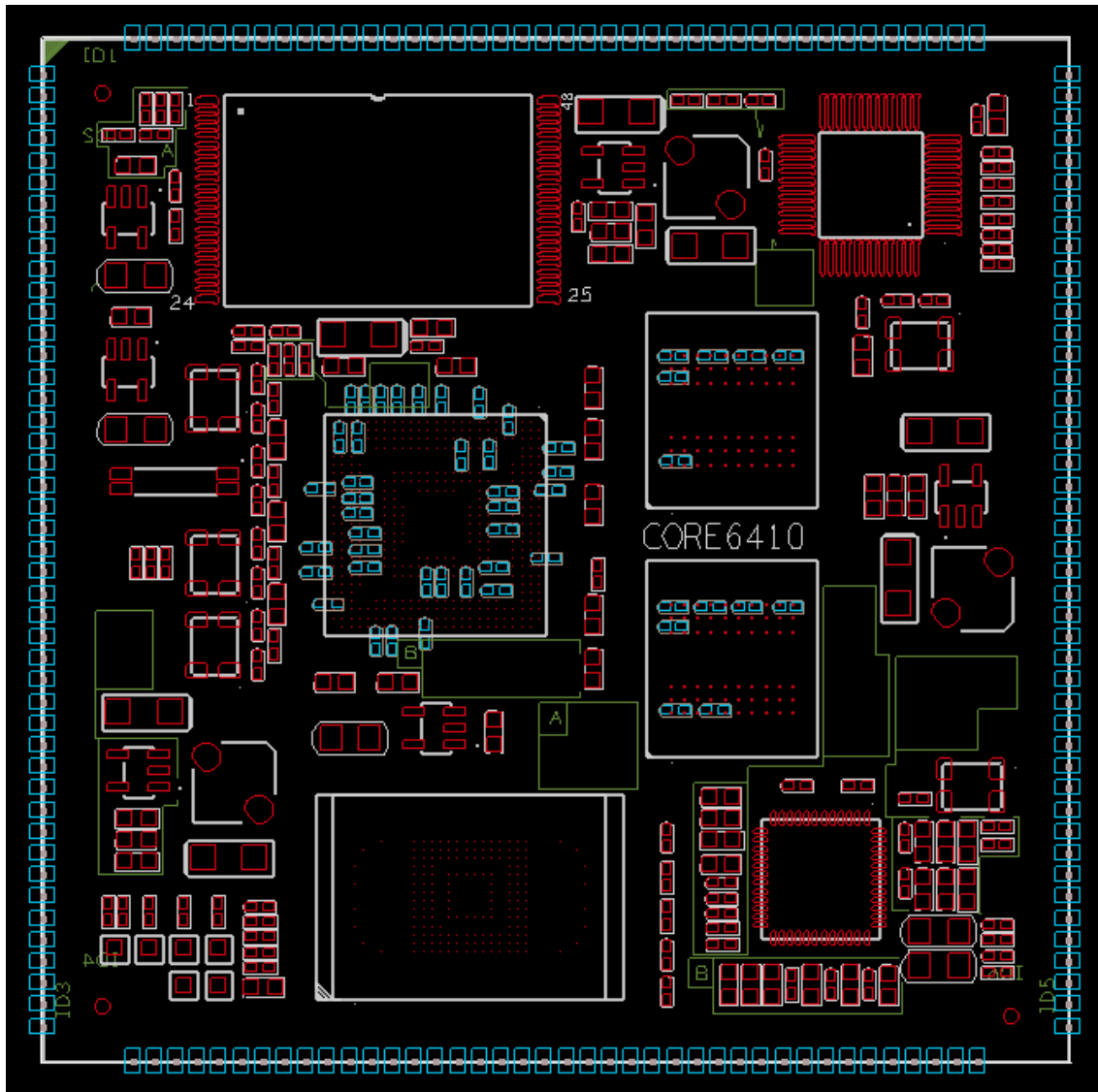








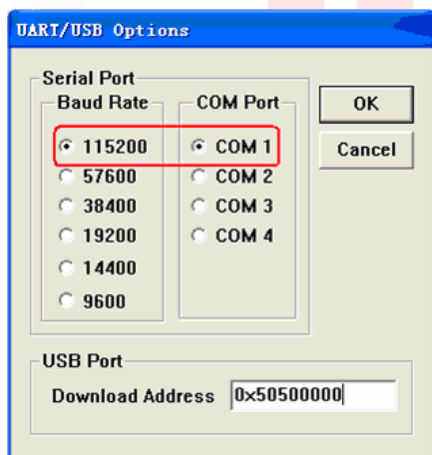
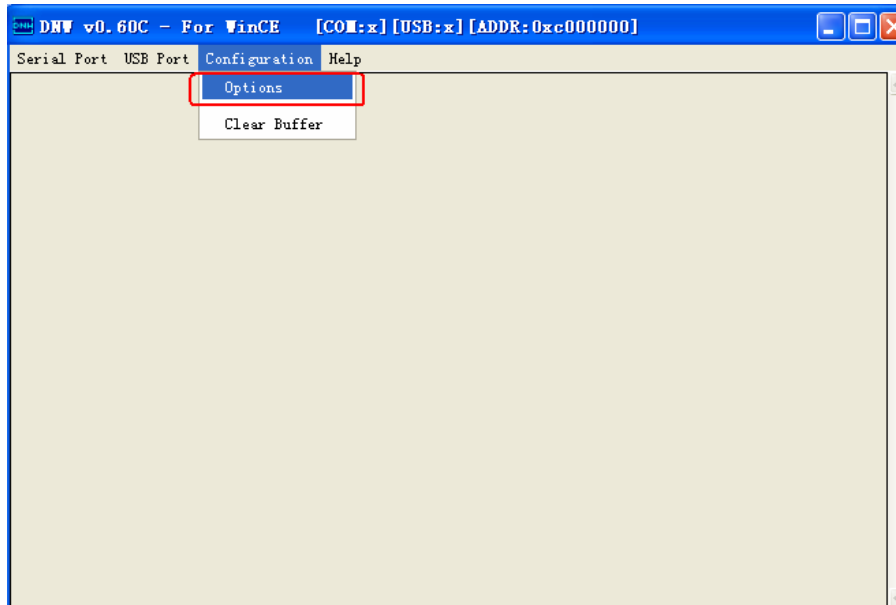
Components Distribution



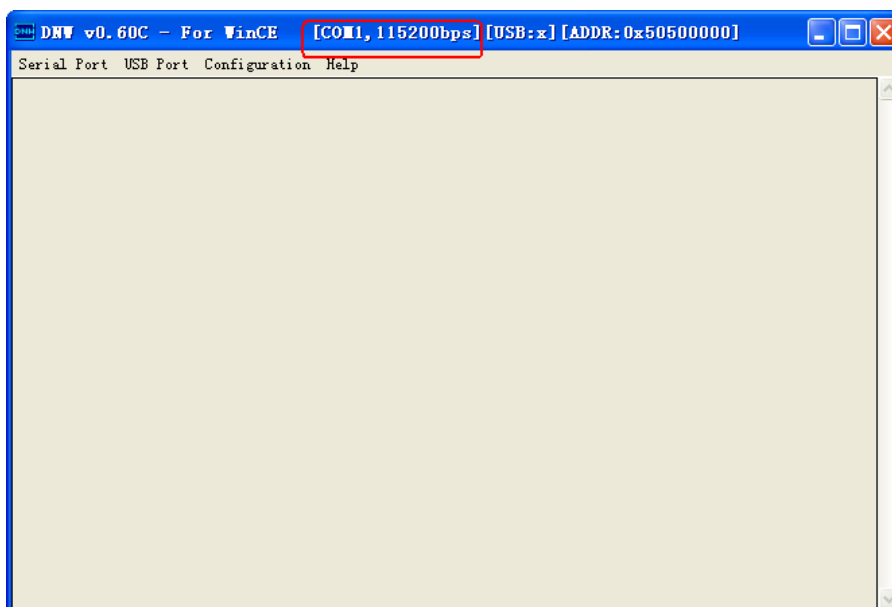
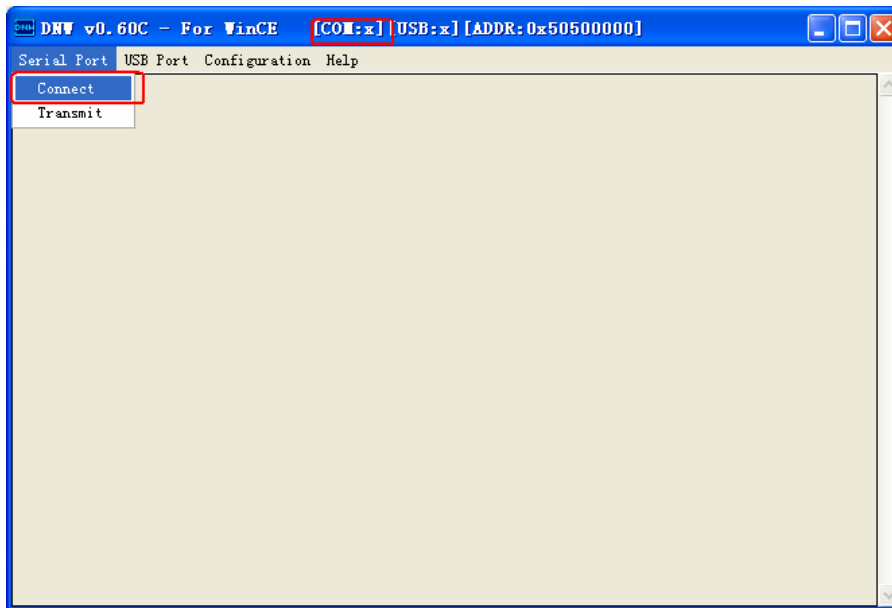
5. Tool software and driver installation instructions

5.1 DNW0.6C instructions for use

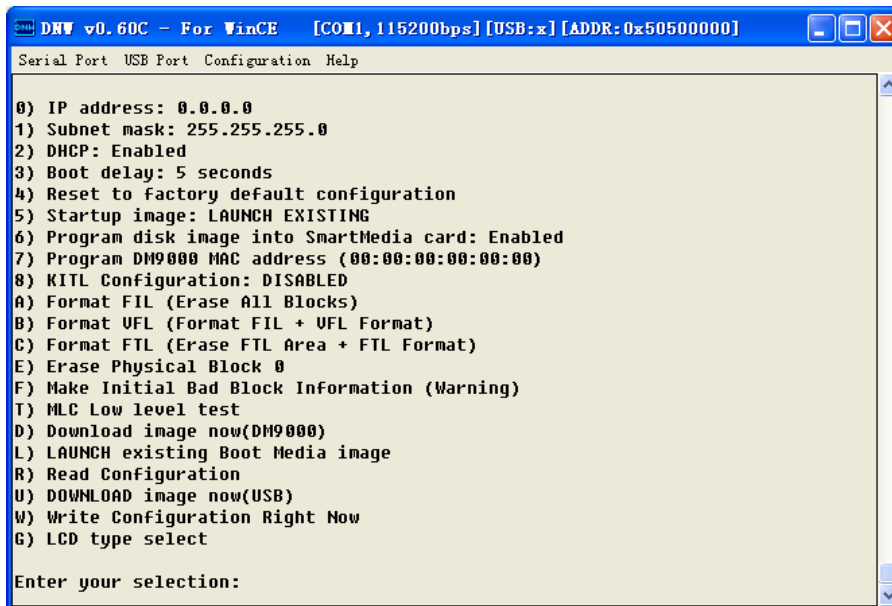
(1) Serial baud rate selection and configuration of



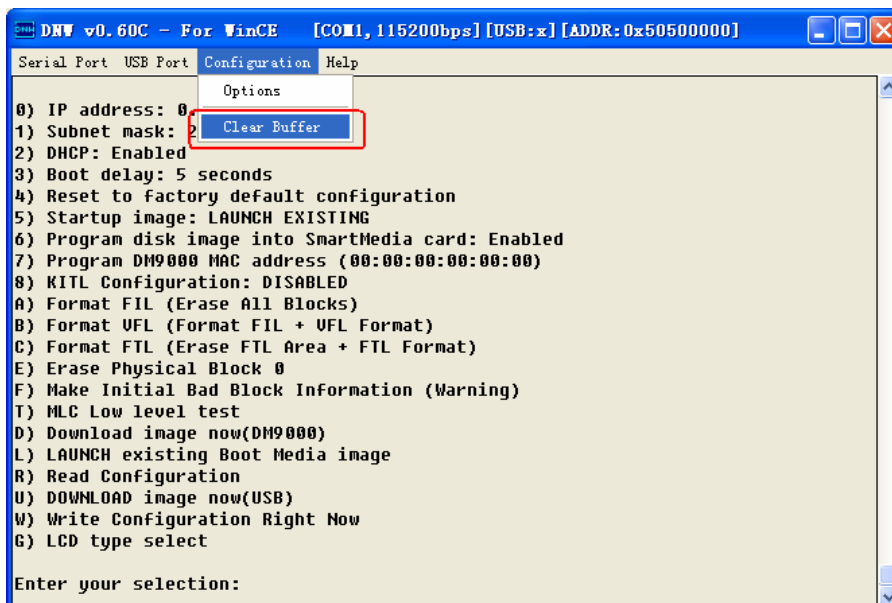
PC에 맞게 통신 속도와 포트 설정



At this point, we can use as a normal serial DNW transfer software to use.

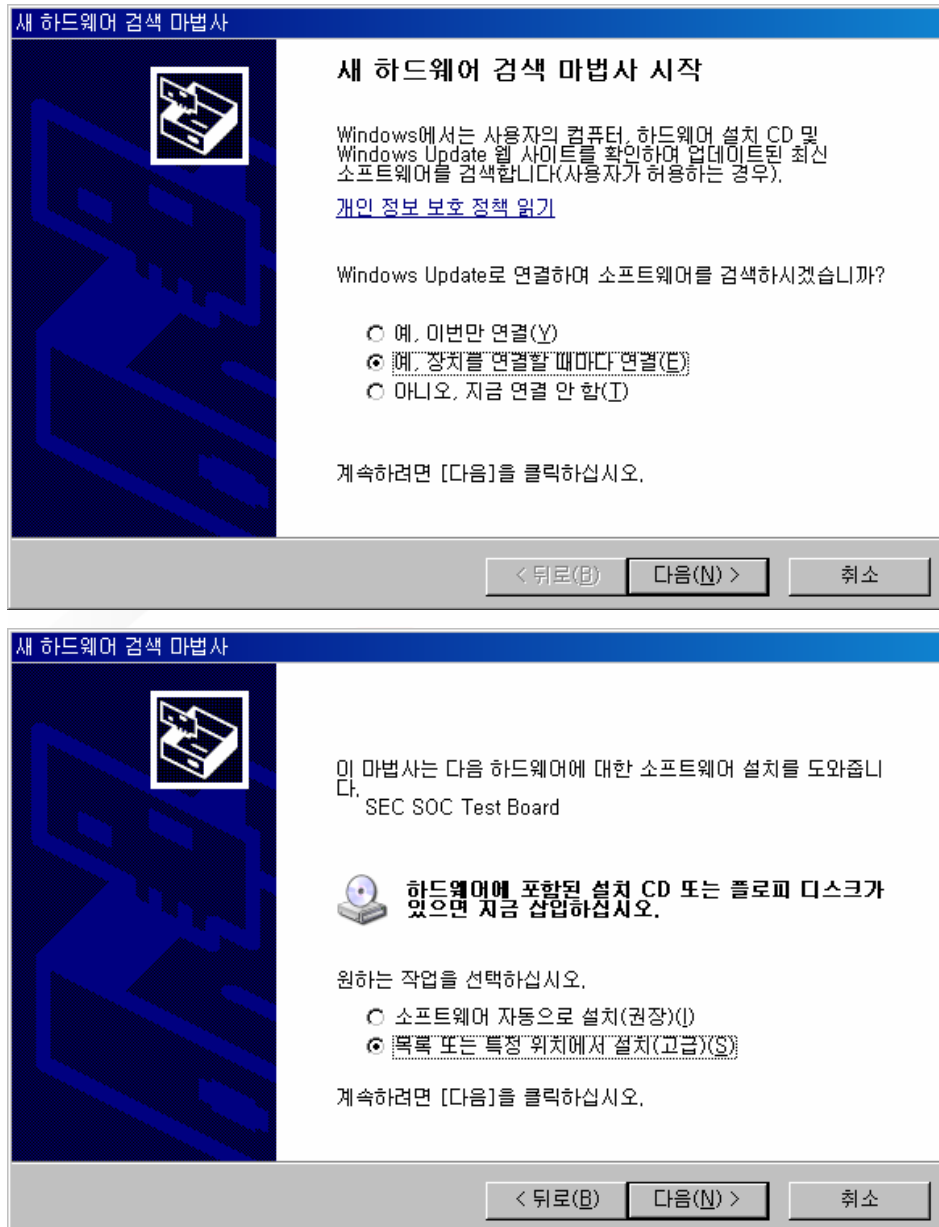


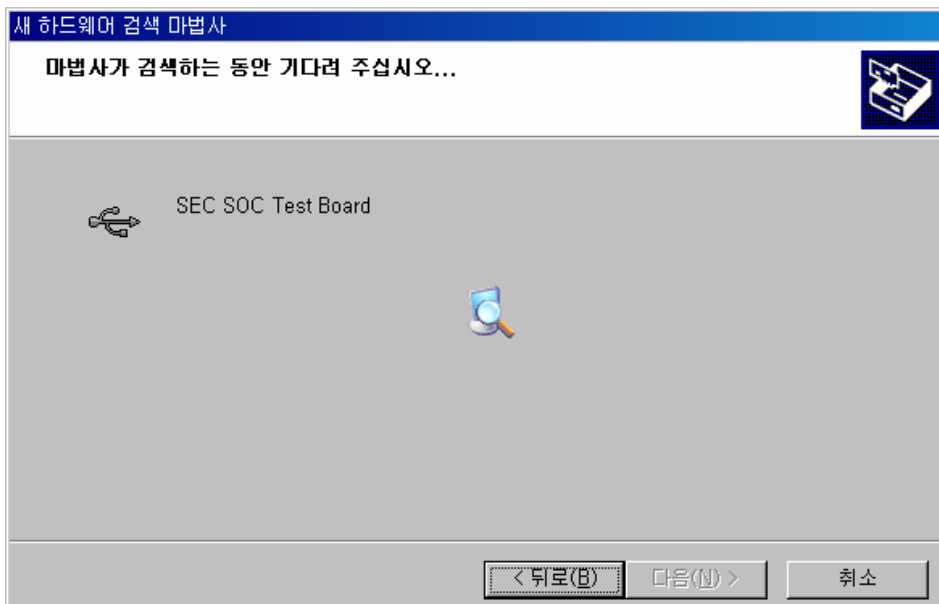
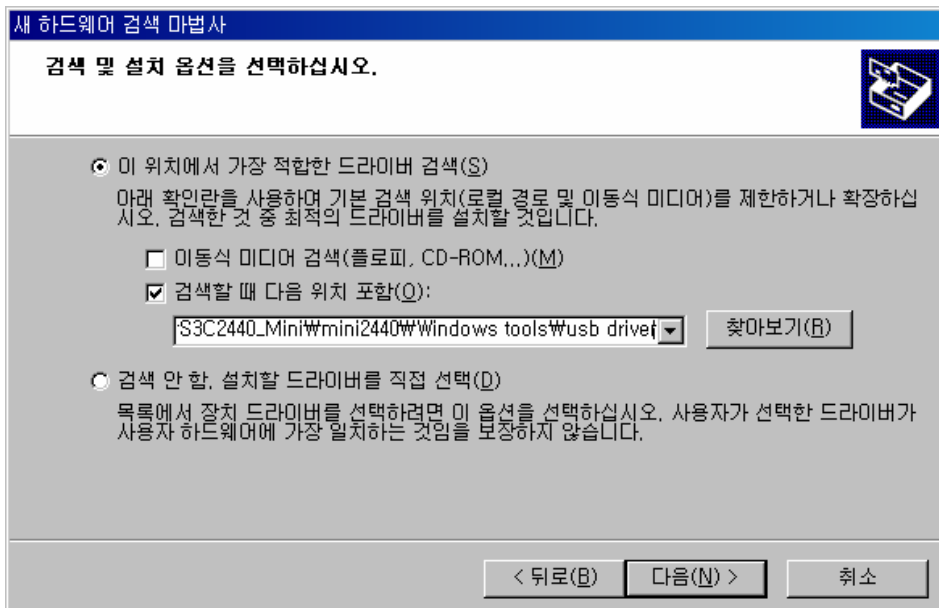
To clear the serial port output

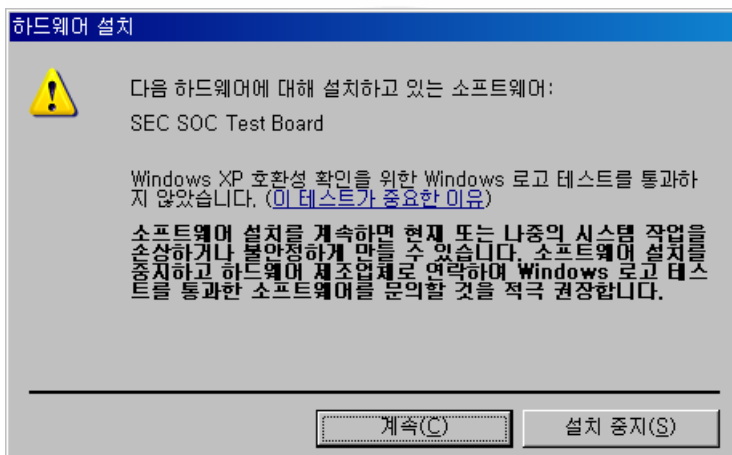
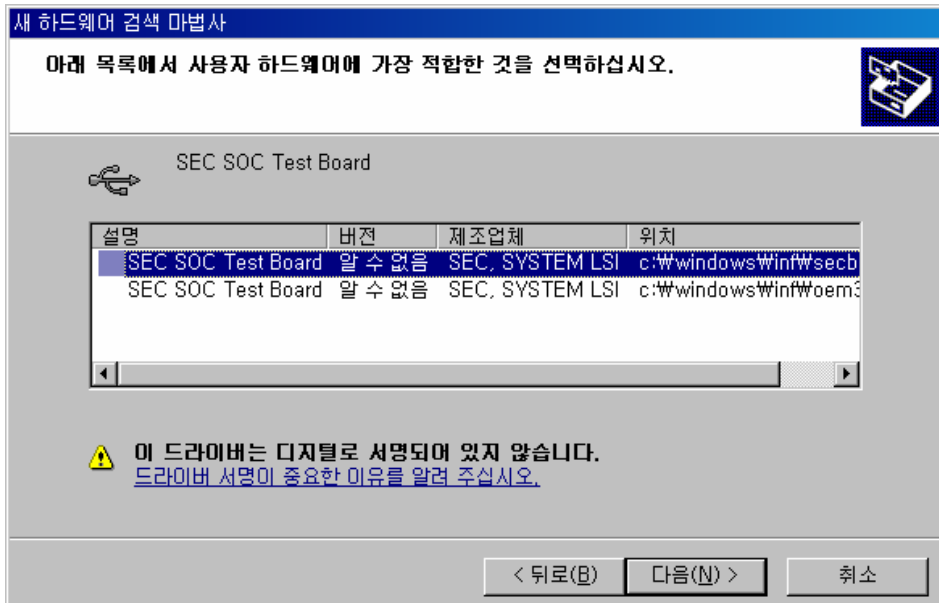


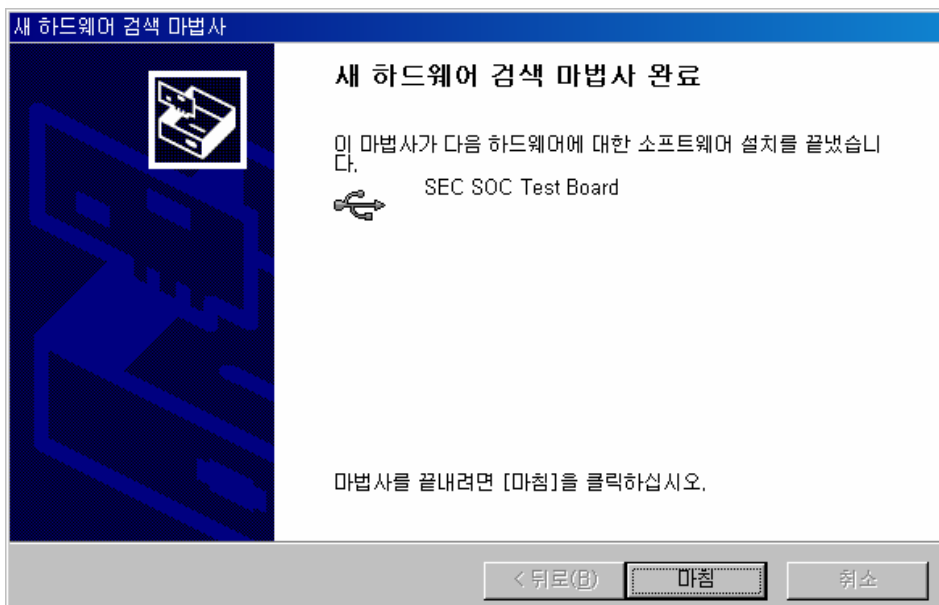
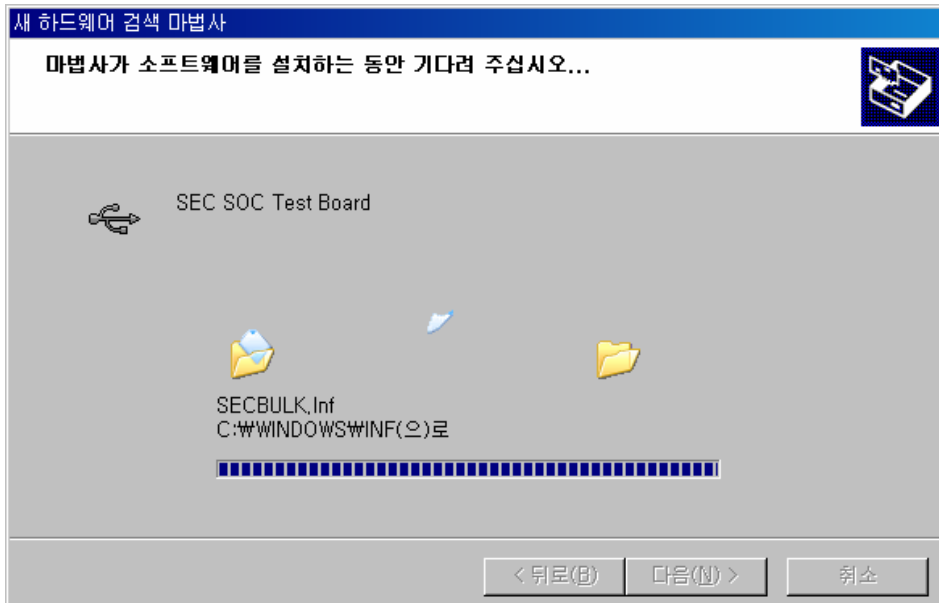
5.2 USB Driver Installation

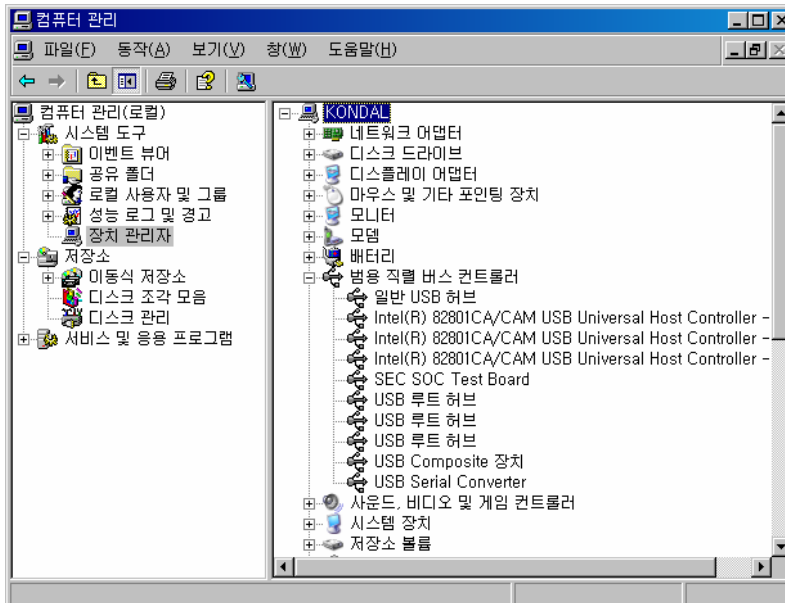
When using the USB download, the first time need to install USB driver.





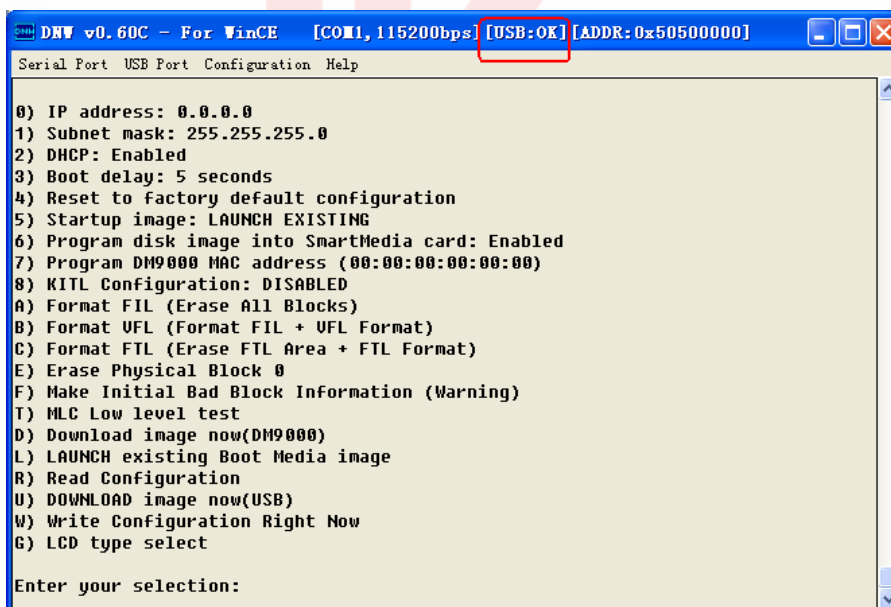


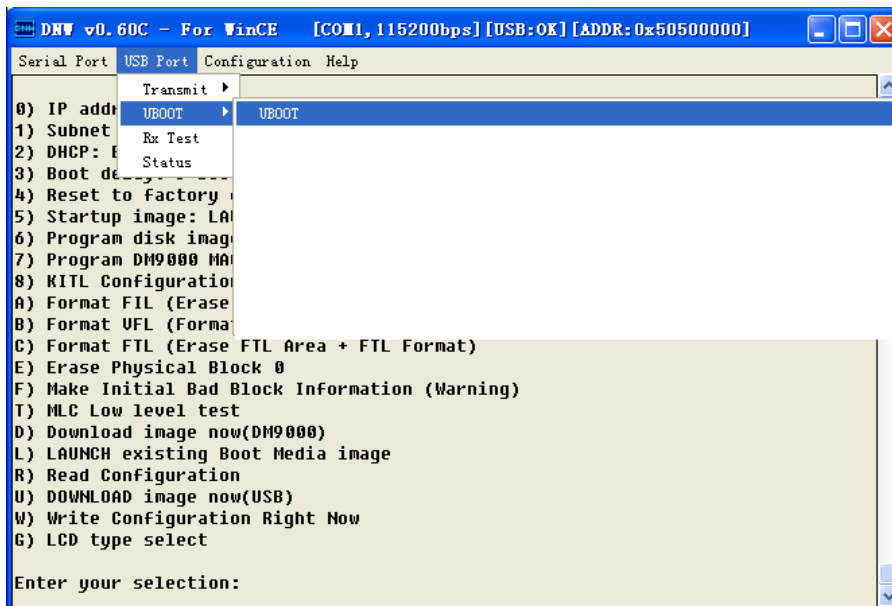




5.3 DNW0.6C in the use of USB download

After the USB driver installation section 5.2, we can find the following characteristics in the DNW.





Download OS image to use "UBOOT" menu.

Detail method to download of OS image, Reference each user guide(Linux, Windows CE, Android)

JK Electronics