N3290x

Data Sheet

ARM926-based Media Processor

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1. GENERAL DESCRIPTION

The N3290xUxDN is built on the ARM926EJ-S CPU core and integrated with JPEG codec, CMOS sensor interface, 32-channel SPU (Sound Processing Unit), ADC, DAC, for meeting various kinds of application needs while saving the BOM cost. The combination of ARM926 @ 200MHz, synchronous DRAM, 2D BitBLT accelerator, CMOS image sensor interface, LCD panel interface, USB 1.1 Host & USB2.0 HS Device makes the N3290xUxDN the best choice for LCD ELA devices.

Maximum resolution for the N3290xUxDN is XVGA (1,024x768) @ TFT LCD panel. The 2D BitBLT accelerator accelerates the graphic compution to make the rendering smooth and off-load CPU to save power consumption.

The N3290xUxDN is well-positioned in terms of cost/performance for the applications which bitmap graphics is extensively used or CMOS Image Sensor (CIS) interface is required.

The N3290xUxDN is for application under Linux OS and leverage the driver availability of emerging functionalities like Wi-Fi, browser, etc. On the other hand, the open source code environment also give the product development more flexible.

To meet the different requirement of the overall system BOM cost, the different size of DRAM is stacked with N3290x main SoC into one package, that is, multi-chip package (MCP). The N32901U1DN is particularly designed with the 128-pin LQFP package and the 1Mbitx16 SDRAM is stacked inside the MCP. The N32903U1DN is particularly designed with the 128-pin LQFP package and the 4Mbitx16 SDRAM is stacked inside the MCP. The 16Mbitx16 SDRAM is stacked inside the N32905UxDN MCP to ensure higher performance and minimize the system design efforts, like EMI & noise coupling. Total BOM cost could be reduced by employing 2-layer PCB along with the elimination of damping resistors, EMI prevention components, etc. Advantages including, but not limited to, less PCB space, shorter lead time, and higher / reliable production yield.

1.1 Applications

- **ELA (Educational Learning Aid)**
- **HMI**
- **Security**
- **Home Appliance**
- **Advertisement**

2. FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 200MHz@1.8V core power operation voltage
  - JTAG interface supported for development and debugging

- **Internal SRAM & ROM**
  - 8KB internal SRAM and 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory card
      - SD card
      - SD-to-NAND flash bridge
    - Raw NAND Flash
    - SPI Flash
    - USB

- **EDMA (Enhanced DMA)**
  - Totally 5 DMA channels supported
    - 4 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - One dedicated channel for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- **Capture (CMOS Sensor I/F)**
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 2M pixel for Still Image Capture, 640x480 (VGA) resolution for MJPEG Video Streaming
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data formats supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
    - Vertical and horizontal scaling-down for preview mode supported
      - The scaling factor is N/M
      - Two pairs of configurable 8-bit N and 8-bit M for vertical and horizontal scaling-down
      - The value of N has to equal to or less than M
    - Frame rate control supported
  - Combines two interlace fields to a single frame supported for data in from TV-decoder

- **JPEG Codec**
  - Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.

- Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
  - Support rotate function in encode mode
- Packet Format
  - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
  - Support decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode

- 2D Accelerator
  - BitBLT operation
    - 2x2 transform matrix with effects:
      - Scale
      - Translate
      - Rotate
      - Shear
    - Alpha blending and color transformation supported
    - Source format for operations: supported color format of source bitmap
  - Fill
    - Rectangle Fill with single color – ARGB8888
    - Fill with blending effect supported
  - Supported color formats
    - Source
      - 16 bits/pixel – RGB565
      - 32 bits/pixel – ARGB8888
      - 1 bit/pixel, 2 bits/pixel, 4 bits/pixel, 8 bits/pixel with RGB color palette
    - Destination
      - 16 bits/pixel – RGB565
      - 32 bits/pixel – ARGB8888

- VPOST

- 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
- Color format supported:
  - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
  - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
- XGA (1024x768), SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
  - The maximum resolution is up to D1 (720X480) for TV output
  - The maximum resolution is up to 1024X768 for TFT LCD panel for still image displaying
  - The maximum resolution is up to 480x272 for TFT LCD panel for MJPEG video displaying up to 25fps.
- Display scaler – to fit different size of LCD panels
  - Horizontal: At most 4.0x scale
  - Vertical: At most 3.0x scale
- For SYNC type LCD:
  - For 8-bit bus
    - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
    - CCIR601 RGB Dummy mode (NTSC/PAL) supported
    - CCIR656 interface supported
    - RGB Through mode supported
  - For 16/18/24-bit bus
    - Parallel pixel data output mode (1-pixel/1-clock)
- NTSC/PAL interlace & non-interlace output supported
- Color format transform supported:
  - Color format transform between YCbCr422 and RGB565
  - Color format transform from YCbCr422 to RGB888
- TV encoder supported
- Dual screen, outputs to TV and LCD simultaneously with same content, supported
  - LCD panel should be 320X240 MPU-type, or 8-bit SYNC-type LCD panel with TV timing
- Notch filter for NTSC supported to remove the rainbow color effect
- Support OSD function to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- Frame Switch Controller
  - Frame relation controlled between VPOST and Capture supported
  - 2 modes supported to switch Frame Buffer Base
    - Frame Ratio Mode (16 selectable ratio)
    - Frame sync mode
  - Double/triple buffers supported

- SPU (Sound Processing Unit)
  - 32 stereo channels supported
  - PCM8/PCM16/4-bit MDPCM/TONE source format supported
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels
  - 10-band equalizer supported
  - Special code supported for loop playing and event detection

- Audio DAC
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- I2S Controller
  - I2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported
- Storage Interface Controller
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC4, ECC8, ECC12 and ECC15 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD

- USB Device Controller
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- USB Host Controller
  - USB1.1 Host one H/W Engine, two pin locations.
  - Fully compliant with USB Revision 1.1 specification
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported

- Timer & Watch-Dog Timer
  - Two 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- PWM
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported

- UART
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 4 signals TX, RX, CTS and RTS supported
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only

- SPI
  - One SPI controller is supported
    - Both master and slave mode are supported in SPI interface
    - Two chip selection signals for two SPI devices

- I2C
  - One I2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported

- Advanced Interrupt Controller
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Daisy-chain priority mechanism supported for interrupts with same priority level
  - Low priority interrupt automatic masking supported for interrupt nesting

- RTC
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported
  - Power-on timeout is supported for low battery protection

- GPIO
  - 80 programmable general purpose I/Os supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- ADC
  - Multi-channel, 10-bit ADC supported
    - 2 channels dedicated for 4-wire resistive touch sensor inputs
    - 2 channels dedicated for Audio ADC with Microphone pre-Amp & AGC
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
    - Input voltage range from 0V ~ 3.3V supported
  - Maximum 25MHz input clock supported
  - Maximum 400K/s conversion rate supported
  - LVR (Low Voltage Reset) supported

- Power Management

- Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
  - Normal Operating Mode
    - Core power is 1.8V and chip is in normal operation
  - CPU Standby Mode
    - Core power is 1.8V and only ARM CPU clock is turned OFF
  - Deep Standby Mode
    - Core power is 1.8V and all IP clocks are turned OFF
  - Power Down Mode
    - Only the RTC power is ON. Other 3.3V and 1.8V power are OFF

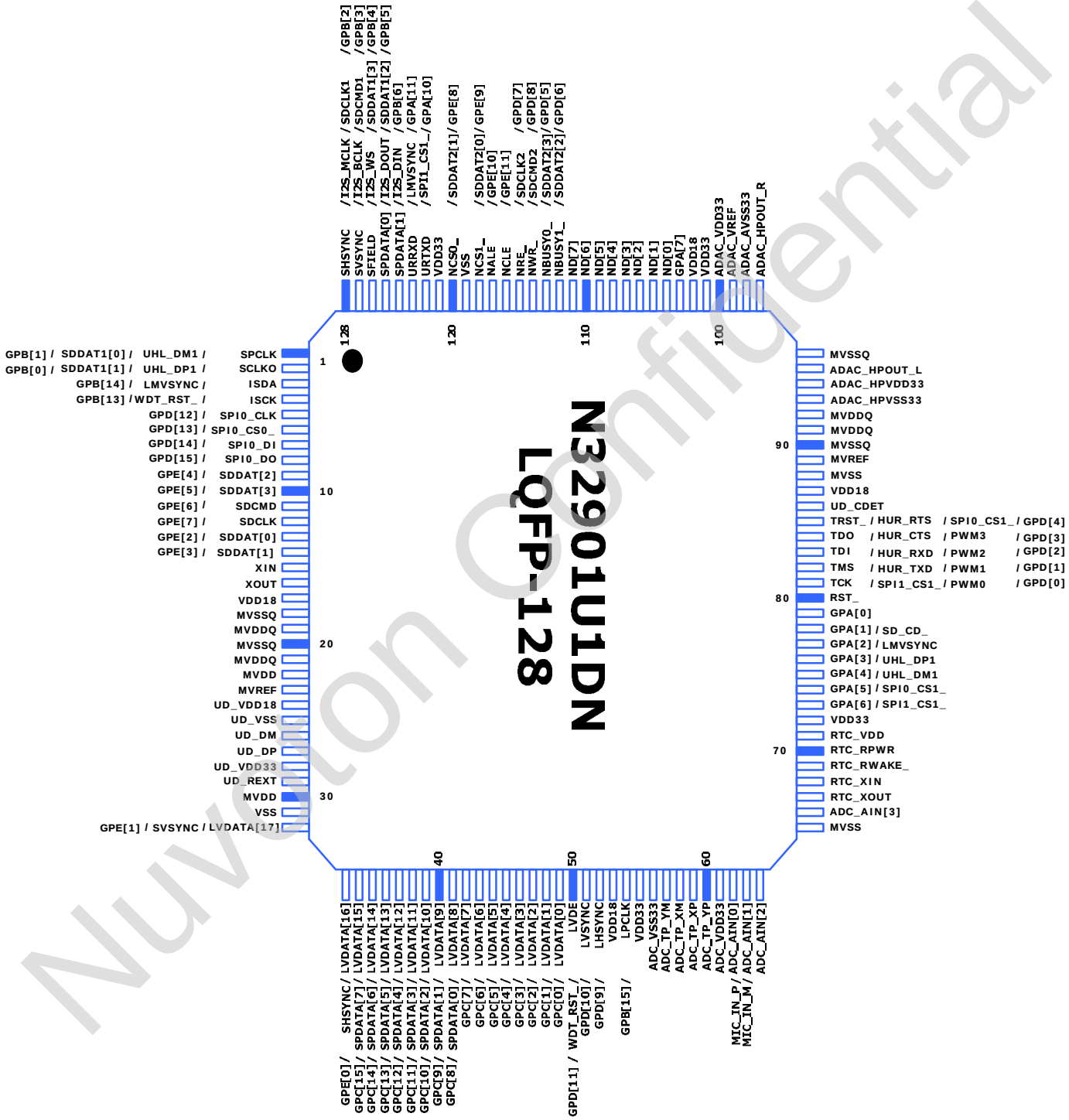
- Software Support
  - Development Tools
    - Bootloader / Diagnostic Program / NAND Writer Program: ADS 1.2 or RVDS 2.x or 3.x
    - Linux Kernel (2.6.17.14) / System Manager: GCC 4.2
    - TurboWriter / Sync Tool: Microsoft VC 6.0
  - NAND Flash File System
    - FAT12, FAT16 and FAT32 with long filename are supported
    - Hidden disk is supported
    - RAM disk is supported
  - S/W audio Library
    - Decoders with ADPCM / MP3 / ACC / OGG / WMA format support
    - 32-polyphony Wavetable MIDI synthesizer
    - Programmable sampling rate and target bit rate
  - USB Driver
    - MS (Mass Storage) Class
    - HID (Human Interface Device) Class

- Operating Voltage
  - I/O: 3.3V
  - Core: 1.8V for 200MHz

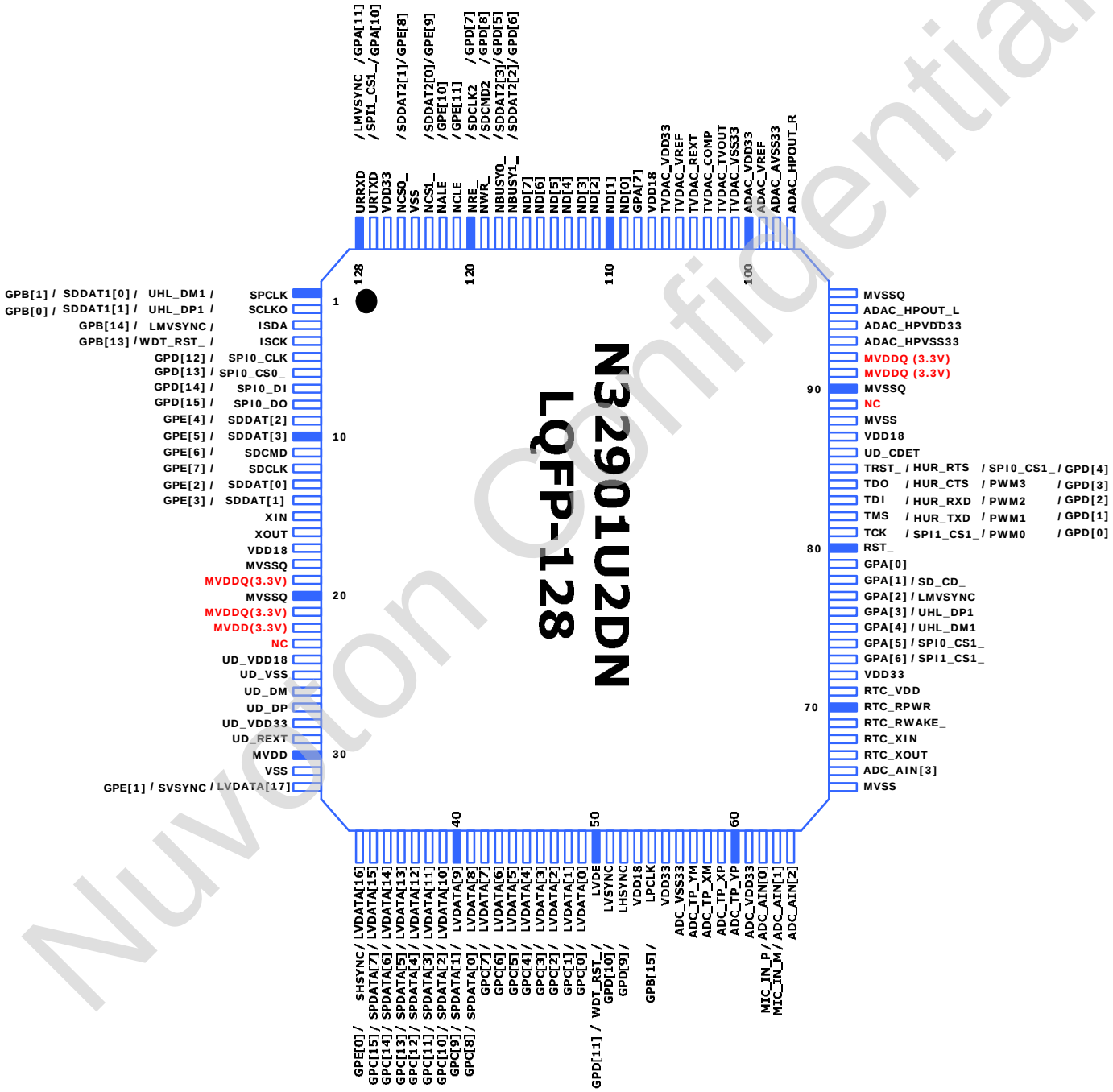
- Package
  - LQFP-128 (MCP, stacked with DDR @ 1.8V and SDR @ 1.8V)

3. PIN DIAGRAM

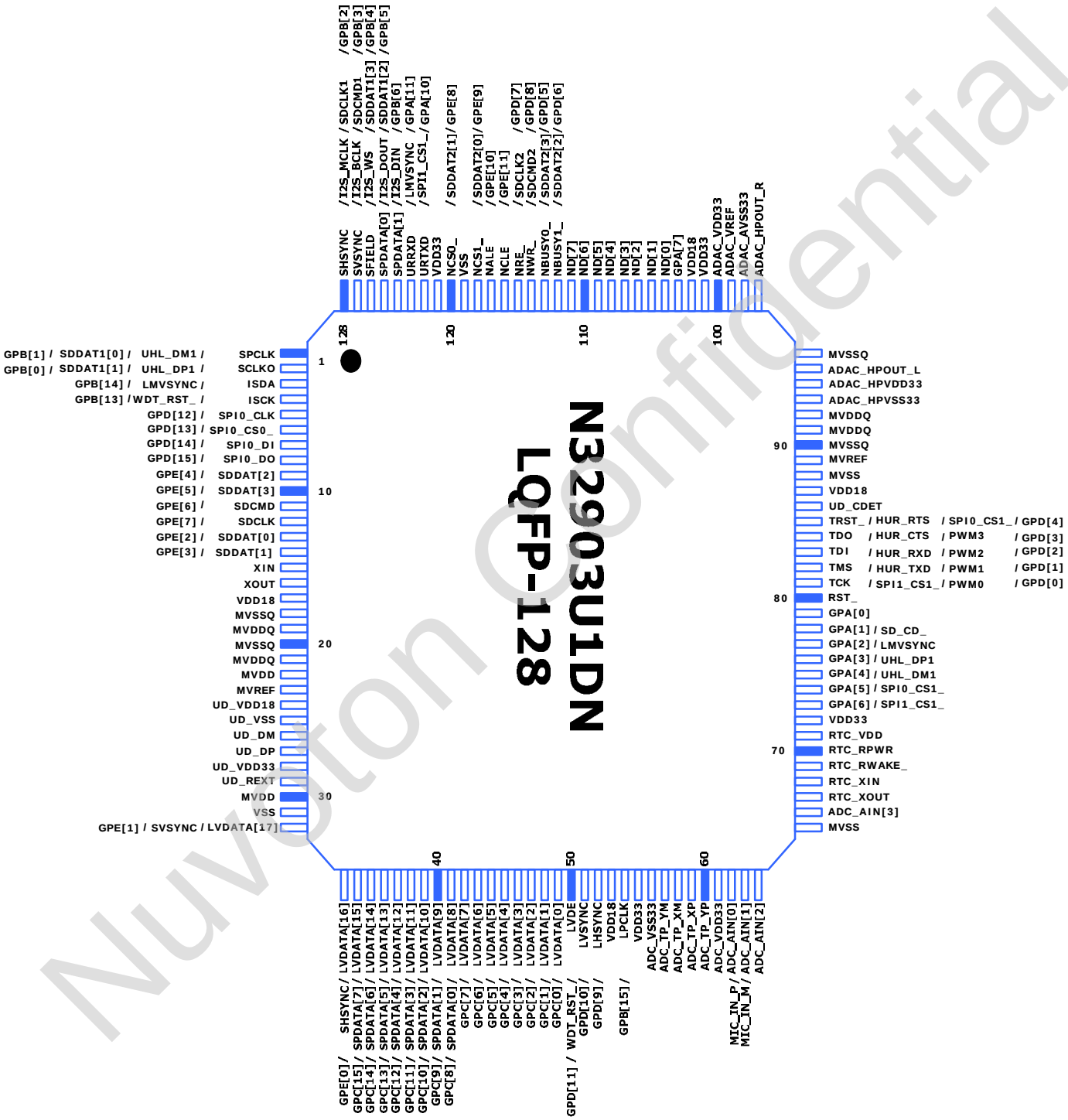
3.1 N32901U1DN (LQFP-128)



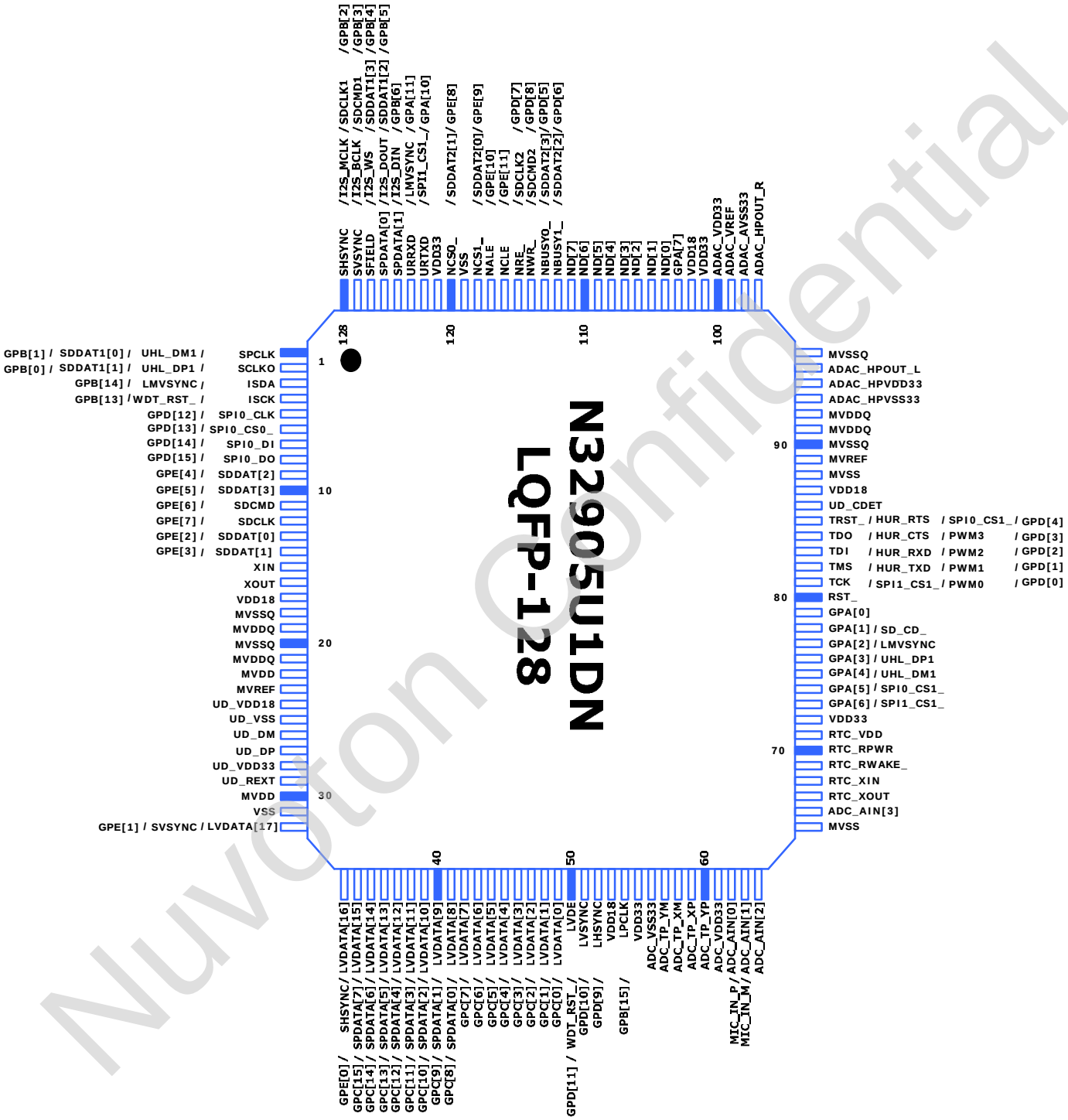
3.2 N32901U2DN (LQFP-128)



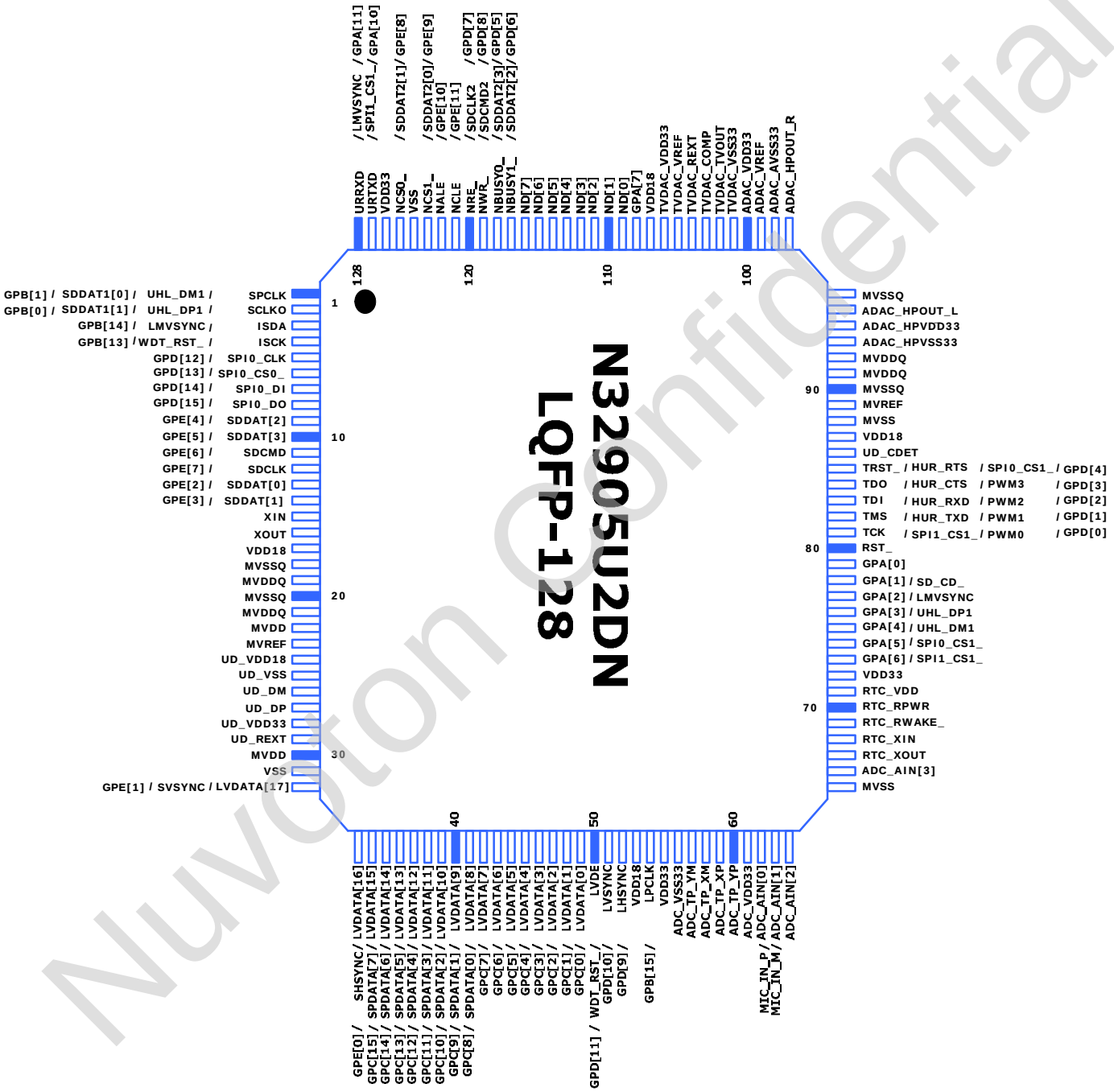
3.3 N32903U1DN (LQFP-128)



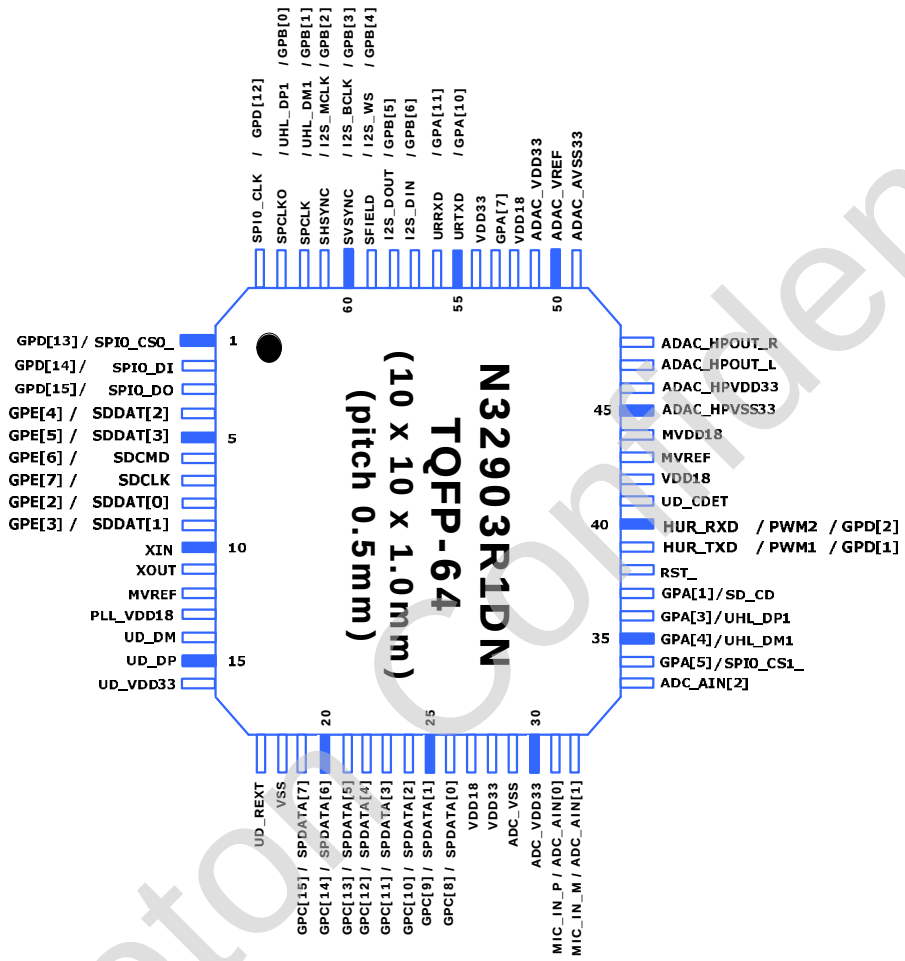
3.4 N32905U1DN (LQFP-128)



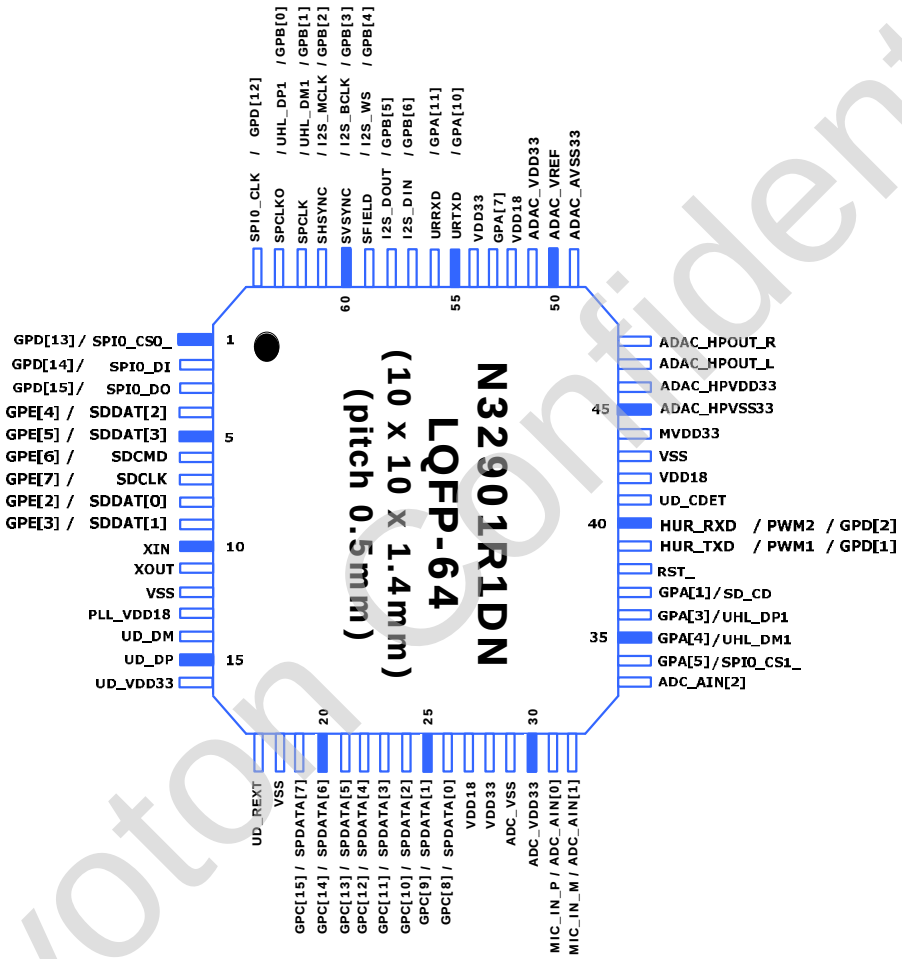
3.5 N32905U2DN (LQFP-128)



3.6 N32903R1DN (TQFP-64)



3.7 N32901R1DN (LQFP-64)



4. PIN DESCRIPTION

4.1 Pin Description & Cross Reference

Pin Name	I/O Type	Description	N32901U1DN	N32901U2DN	N32903U1DN	N32905U1DN	N32905U2DN	N32903R1DN	N32901R1DN
Clock & Reset									
XIN	I	27MHz/12MHz Crystal Input	•	•	•	•	•	•	•
XOUT	O	27MHz/12MHz Crystal Output	•	•	•	•	•	•	•
RST_	IOSU	System Reset, Input, Low Active Watch-Dog Reset, Output, Low Active	•	•	•	•	•	•	•
JTAG Interface									
TCK	IOD	JTAG Interface Test Clock, Input							
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active	•	•	•	•	•		
PWM0		PWM Channel 0							
GPD[0]		GPIO Port D Bit 0							
TMS	IOU	JTAG Interface Test Mode Select, Input							
HUR_TXD		High-Speed UART TX Data, Output							
PWM1		PWM Channel 1	•	•	•	•	•	•	•
GPD[1]		GPIO Port D Bit 1							
TDI	IOU	JTAG Interface Test Data In, Input							
HUR_RXD		High-Speed UART RX Data, Input							
PWM2		PWM Channel 2	•	•	•	•	•	•	•
GPD[2]		GPIO Port D Bit 2							
TDO	IOU	JTAG Interface Test Data Out, Output							
HUR_CTS		High-Speed UART Clear-To-Send, Input, Low Active							
PWM3		PWM Channel 3	•	•	•	•	•		
GPD[3]		GPIO Port D Bit 3							
TRST_	IOU	JTAG Interface Test Reset, Input, Low Active							
HUR_RTS		High-Speed UART Reset-To-Send, Output, Low Active							
SPI0_CS1_		SPI Port 0 Device Select 1, Output, Low Active	•	•	•	•	•		
GPD[4]		GPIO Port D Bit 4							
NAND Interface									

NCS0_	IOU	NAND Interface Chip Select 0, Output, Low Active	•	•	•	•	•		
SDDAT2[1]		SD Port 2 Data Bit 1							
GPE[8]		GPIO Port E Bit 8							
NCS1_	IOU	NAND Interface Chip Select 1, Output, Low Active	•	•	•	•	•		
SDDAT2[0]		SD Port 2 Data Bit 0							
GPE[9]		GPIO Port E Bit 9							
NALE	IOU	NAND Interface Address-Latch-Enable, Output, High Active	•	•	•	•	•		
GPE[10]		GPIO Port E Bit 10							
NCLE	IOU	NAND Interface Command-Latch-Enable, Output, High Active	•	•	•	•	•		
GPE[11]		GPIO Port E Bit 11							
NBUSY0_	IOU	NAND Interface Busy 0, Input, Low Active	•	•	•	•	•		
SDDAT2[3]		SD Port 2 Data Bit 3							
GPD[5]		GPIO Port D Bit 5							
NBUSY1_	IOU	NAND Interface Busy 1, Input, Low Active	•	•	•	•	•		
SDDAT2[2]		SD Port 2 Data Bit 2							
GPD[6]		GPIO Port D Bit 6							
NRE_	IOU	NAND Interface Read Enable, Output, Low Active	•	•	•	•	•		
SDCLK2		SD Port 2 Clock, Output							
GPD[7]		GPIO Port D Bit 7							
NWR_	IOU	NAND Interface Write Enable, Output, Low Active	•	•	•	•	•		
SDCMD2		SD Port 2 Command/Response							
GPD[8]		GPIO Port D Bit 8							
ND[7:0]	IOU	NAND Interface Data Bit [7:0]	•	•	•	•	•		
CHIPCFG[7:0]		Chip Power-On Configuration Bit [7:0], Input							
Sensor/Video-In Interface									
SCLKO	IOU	Clock to Sensor Module, Output	•	•	•	•	•	•	•
UHL_DP1		USB Host Like Interface, DP							
SDDAT1[1]		SD Port 1 Data Bit 1							
GPB[0]		GPIO Port B Bit 0							
SPCLK	IOU	Sensor Interface Pixel Clock, Input	•	•	•	•	•	•	•
UHL_DM1		USB Host Like Interface, DM							
SDDAT1[0]		SD Port 1 Data Bit 0							

GPB[1]		GPIO Port B Bit 1							
SVSYNC	IOU	Sensor Interface VSYNC, Input	•		•	•		•	•
I2S_BCLK		I2S Interface Clock, Input							
SDCMD1		SD Port 1 Command/Response							
GPB[3]		GPIO Port B Bit 3							
SFIELD	IOU	Sensor Interface Even/ODD Field Indicator, Input	•		•	•		•	•
I2S_WS		I2S Interface Word Select, Output							
SDDAT1[3]		SD Port 1 Data Bit 3							
GPB[4]		GPIO Port B Bit 4							
SPDATA[0]	IOU	Sensor Interface Data Bit 0, Input	•		•	•		•	•
I2S_DOUT		I2S Interface Data Output							
SDDAT1[2]		SD Port 1 Data Bit 2							
GPB[5]		GPIO Port B Bit 5							
SPDATA[1]	IOU	Sensor Interface Data Bit 1, Input	•		•	•		•	•
I2S_DIN		I2S Interface Data Input							
GPB[6]		GPIO Port B Bit 6							
I2C Interface									
ISCK	IOU	I2C Interface Clock, Output	•	•	•	•	•		
GPB[13]		GPIO Port B Bit 13							
ISDA	IOU	I2C Interface Data	•	•	•	•	•		
LMVSYNC		MPU Mode VSYNC, Output							
LFMARK		Frame Mark, Input							
GPB[14]		GPIO Port B Bit 14							
LCD/Display Interface									
LPCLK	IOU	LCD Interface Pixel Clock, Output	•	•	•	•	•		
GPB[15]		GPIO Port B Bit 15							
LHSYNC	IOU	LCD Interface HSYNC, Output, High Active	•	•	•	•	•		
GPD[9]		GPIO Port D Bit 9							
LVSYNC	IOU	LCD Interface VSYNC, Output, High Active	•	•	•	•	•		
GPD[10]		GPIO Port D Bit 10							
LVDE	IOU	LCD Interface Data Enable, Output, High Active	•	•	•	•	•		
GPD[11]		GPIO Port D Bit 11							
LVDATA[0]	IOU	LCD Interface Data Bit 0	•	•	•	•	•		
GPC[0]		GPIO Port C Bit 0							
LVDATA[1]	IOU	LCD Interface Data Bit 1	•	•	•	•	•		

GPC[1]		GPIO Port C Bit 1							
LVDATA[2]	IOU	LCD Interface Data Bit 2	•	•	•	•	•		
GPC[2]		GPIO Port C Bit 2							
LVDATA[3]	IOU	LCD Interface Data Bit 3	•	•	•	•	•		
GPC[3]		GPIO Port C Bit 3							
LVDATA[4]	IOU	LCD Interface Data Bit 4	•	•	•	•	•		
GPC[4]		GPIO Port C Bit 4							
CHIPCFG[8]		Chip Power-On Configuration Bit [8], Input							
LVDATA[5]	IOU	LCD Interface Data Bit 5	•	•	•	•	•		
GPC[5]		GPIO Port C Bit 5							
CHIPCFG[9]		Chip Power-On Configuration Bit [9], Input							
LVDATA[6]	IOU	LCD Interface Data Bit 6	•	•	•	•	•		
GPC[6]		GPIO Port C Bit 6							
CHIPCFG[10]		Chip Power-On Configuration Bit [10], Input							
LVDATA[7]	IOU	LCD Interface Data Bit 7	•	•	•	•	•		
GPC[7]		GPIO Port C Bit 7							
LVDATA[8]	IOU	LCD Interface Data Bit 8	•	•	•	•	•	•	•
KPI_SI[0]		KPI Scan In Bit 0							
SPDATA[0]		Sensor Interface Data Bit 0, Input							
GPC[8]		GPIO Port C Bit 8							
LVDATA[9]	IOU	LCD Interface Data Bit 9	•	•	•	•	•	•	•
KPI_SI[1]		KPI Scan In Bit 1							
SPDATA[1]		Sensor Interface Data Bit 1, Input							
GPC[9]		GPIO Port C Bit 9							
LVDATA[10]	IOU	LCD Interface Data Bit 10	•	•	•	•	•	•	•
KPI_SI[2]		KPI Scan In Bit 2							
SPDATA[2]		Sensor Interface Data Bit 2, Input							
GPC[10]		GPIO Port C Bit 10							
LVDATA[11]	IOU	LCD Interface Data Bit 11	•	•	•	•	•	•	•
KPI_SI[3]		KPI Scan In Bit 3							
SPDATA[3]		Sensor Interface Data Bit 3, Input							
GPC[11]		GPIO Port C Bit 11							
LVDATA[12]	IOU	LCD Interface Data Bit 12	•	•	•	•	•	•	•
KPI_SI[4]		KPI Scan In Bit 4							
SPDATA[4]		Sensor Interface Data Bit 4, Input							
GPC[12]		GPIO Port C Bit 12							

LVDATA[13]	IOU	LCD Interface Data Bit 13	•	•	•	•	•	•	•
KPI_SI[5]		KPI Scan In Bit 5							
SPDATA[5]		Sensor Interface Data Bit 5, Input							
GPC[13]		GPIO Port C Bit 13							
LVDATA[14]	IOU	LCD Interface Data Bit 14	•	•	•	•	•	•	•
KPI_SI[6]		KPI Scan In Bit 6							
SPDATA[6]		Sensor Interface Data Bit 6, Input							
GPC[14]		GPIO Port C Bit 14							
LVDATA[15]	IOU	LCD Interface Data Bit 15	•	•	•	•	•	•	•
KPI_SI[7]		KPI Scan In Bit 7							
SPDATA[7]		Sensor Interface Data Bit 7, Input							
GPC[15]		GPIO Port C Bit 15							
LVDATA[16]	IOU	LCD Interface Data Bit 16	•	•	•	•	•		
SHSYNC		Sensor Interface HSYNC, Input							
GPE[0]		GPIO Port E Bit 0							
LVDATA[17]	IOU	LCD Interface Data Bit 17	•	•	•	•	•		
SVSYNC		Sensor Interface VSYNC, Input							
GPE[1]		GPIO Port E Bit 1							
UART Interface									
URTXD	IOU	UART TX Data, Output	•	•	•	•	•	•	•
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active							
GPA[10]		GPIO Port A Bit 10							
URRXD	IOU	UART RX Data, Input	•	•	•	•	•	•	•
LMVSYNC		MPU Mode VSYNC, Output							
LFMARK		Frame Mark, Input							
GPA[11]		GPIO Port A Bit 11							
SPI 0 Interface									
SPI0_CLK	IOU	SPI Port 0 Clock Output in Master Mode Input in Slave Mode	•	•	•	•	•		
GPD[12]		GPIO Port D Bit 12							
SPI0_CS0_	IOU	SPI Port 0 Device Select 0, Low Active Output in Master Mode Input in Slave Mode	•	•	•	•	•	•	•
GPD[13]		GPIO Port D Bit 13							
SPI0_DI	IOU	SPI Port 0 Data Input	•	•	•	•	•	•	•

GPD[14]		GPIO Port D Bit 14							
SPI0_DO	IOU	SPI Port 0 Data Output	•	•	•	•	•	•	•
GPD[15]		GPIO Port D Bit 15							
SD Card Interface									
SDCLK	IOU	SD Port 0 Clock, Output	•	•	•	•	•	•	•
GPE[7]		GPIO Port E Bit 7							
SDCMD	IOU	SD Port 0 Command/Response	•	•	•	•	•	•	•
GPE[6]		GPIO Port E Bit 6							
SDDAT[0]	IOU	SD Port 0 Data Bit 0	•	•	•	•	•	•	•
GPE[2]		GPIO Port E Bit 2							
SDDAT[1]	IOU	SD Port 0 Data Bit 1	•	•	•	•	•	•	•
GPE[3]		GPIO Port E Bit 3							
SDDAT[2]	IOU	SD Port 0 Data Bit 2	•	•	•	•	•	•	•
GPE[4]		GPIO Port E Bit 4							
SDDAT[3]	IOU	SD Port 0 Data Bit 3	•	•	•	•	•	•	•
GPE[5]		GPIO Port E Bit 5							
GPIO A									
GPA[0]	IOU	GPIO Port A Bit 0	•	•	•	•	•		
GPA[1]	IOU	GPIO Port A Bit 1	•	•	•	•	•	•	•
SD_CD_		SD Card Detect, Input, Low Active							
GPA[2]	IOU	GPIO Port A Bit 2	•	•	•	•	•		
LMVSYNC		MPU Mode VSYNC, Output							
LFMARK		Frame Mark, Input							
KPI_SO[0]		KPI Scan Out Bit 0							
GPA[3]	IOU	GPIO Port A Bit 3	•	•	•	•	•	•	•
UHL_DP1		USB Host 1.0 Lite Port 1, D+							
KPI_SO[1]		KPI Scan Out Bit 1							
GPA[4]	IOU	GPIO Port A Bit 4	•	•	•	•	•	•	•
UHL_DM1		USB Host 1.0 Lite Port 1, D-							
KPI_SO[2]		KPI Scan Out Bit 2							
GPA[5]	IOU	GPIO Port A Bit 5	•	•	•	•	•	•	•
SPI0_CS1_		SPI Port 0 Device Select 1, Output, Low Active							
KPI_SO[3]		KPI Scan Out Bit 3							
GPA[6]	IOU	GPIO Port A Bit 6	•	•	•	•	•		
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active							

KPI_SO[4]		KPI Scan Out Bit 4							
GPA[7]	IOU	GPIO Port A Bit 7	•	•	•	•	•	•	•
KPI_SO[5]		KPI Scan Out Bit 5							
RTC (Real Time Clock)									
RTC_XIN (32768Hz)	I	32768Hz Crystal Input	•	•	•	•	•		
RTC_XOUT (32768Hz)	O	32768Hz Crystal Output	•	•	•	•	•		
RTC_RWAKE_	I	Wakeup Enable, Input, Low Active	•	•	•	•	•		
RTC_RPWR	OD	Power Enable, Open-Drain	•	•	•	•	•		
USB 2.0 Device Interface									
UD_CDET	I	USB Device Connect Detect, Input, High Active	•	•	•	•	•	•	•
UD_DP	IO	USB 2.0 Device D+	•	•	•	•	•	•	•
UD_DM	IO	USB 2.0 Device D-	•	•	•	•	•	•	•
UD_REXT	IO	External Resistor Connect Recommend to connect 12.1KW resistor to ground for USB 2.0 PHY	•	•	•	•	•	•	•
TV Out									
TVDAC_TVOUT	O	Composite/Chroma Output Connect an external 75W resistor to ground of TVDAC as TV terminal impedence		•			•		
TVDAC_REXT	IO	External Resistor Connection Recommend to connect 160W resistor to ground of TVDAC		•			•		
TVDAC_COMP	O	External Capacitor Connection Connect 0.1uF capacitor to VDD33 of TVDAC		•			•		
TVDAC_VREF	O	Reference Voltage Output Connect 0.1uF capacitor to ground of TVDAC		•			•		
ADC & Touch Panel									
ADC_AIN[3]	I	ADC Analog Input Channel 3	•	•	•	•	•		
ADC_AIN[2]	I	ADC Analog Input Channel 2	•	•	•	•	•	•	•
ADC_AIN[1]	I	ADC Analog Input Channel 1	•	•	•	•	•	•	•
MIC_IN_M	I	Microphone Negative Input							
ADC_AIN[0]	I	ADC Analog Input Channel 0	•	•	•	•	•	•	•
MIC_IN_P	I	Microphone Positive Input							
ADC_TP_YP	I	Touch Panel YP	•	•	•	•	•		
ADC_TP_XP	I	Touch Panel XP	•	•	•	•	•		

ADC_TP_XM	I	Touch Panel XM	•	•	•	•	•		
ADC_TP_YM	I	Touch Panel YM	•	•	•	•	•		
Audio DAC									
ADAC_HPOUT_R	O	Audio Headphone Right Channel Output	•	•	•	•	•	•	•
ADAC_HPOUT_L	O	Audio Headphone Left Channel Output	•	•	•	•	•	•	•
ADAC_VREF	O	Audio DAC Reference Voltage Output Recommend to connect 1uF capacitor to ground of Audio DAC	•	•	•	•	•	•	•
Power/Ground									
MVREF	P	Reference Voltage for SDRAM I/F Useless if SDR SDRAM used. It should be MVDD/2 if DDR/DDR2/LPDDR SDRAM used	•	•	•	•	•	•	•
MVREF_GND_SHIELDING	G	Ground Shielding for Reference Voltage	•		•				
MVDD18	P	SDRAM I/F Power (1.8V)	•		•	•	•	•	
MVDD33	P	SDRAM I/F Power (3.3V)		•					•
MVSS	G	SDRAM I/F Ground (0V)	•	•	•	•	•	•	•
MVDDQ	P	SDRAM I/F Power (1.8V)	•	•	•	•	•	•	•
MVSSQ	G	SDRAM I/F Ground (0V)	•	•	•	•	•	•	•
RTC_VDD	P	RTC Core, I/F & 32768Hz Crystal Power	•	•	•	•	•		
UD_VDD33	P	USB 2.0 PHY Power (3.3V)	•	•	•	•	•	•	•
UD_VSS33	G	USB 2.0 PHY Ground (0V)	•	•	•	•	•	•	•
UD_VDD18	P	USB 2.0 PHY Power (1.8V)	•	•	•	•	•	•	•
UD_VSS18	G	USB 2.0 PHY Ground (0V)	•	•	•	•	•	•	•
TVDAC_VDD33	P	TV DAC Power (3.3V)		•			•		
TVDAC_VSS33	G	TV DAC Ground (0V)		•			•		
ADC_VDD33	P	ADC Power (3.3V)	•	•	•	•	•	•	•
ADC_VSS33	G	ADC Ground (0V)	•	•	•	•	•	•	•
ADAC_HPVDD33	P	Audio DAC Headphone Driver Power (3.3V)	•	•	•	•	•	•	•
ADAC_HPVSS33	G	Audio DAC Headphone Driver Ground (0V)	•	•	•	•	•	•	•
ADAC_AVDD33	P	Audio DAC Power (3.3V)	•	•	•	•	•	•	•
ADAC_AVSS33	G	Audio DAC Ground (0V)	•	•	•	•	•	•	•
VDD33	P	I/O Power (3.3V)	•	•	•	•	•	•	•
VDD18	P	Core Logic Power (1.8V)	•	•	•	•	•	•	•
VSS	G	Ground (0V)	•	•	•	•	•	•	•

4.2 Pin Type Description

Type	Description
I	Input
O	Output
OD	Open Drain output
IO	Input / Output
IOD	Input with pull-Down / Output
IOU	Input with pull-Up / Output
IOSU	Input with Schmitt trigger & pull-Up/ Output
P	Power
G	Ground

5. ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Rating

Parameters	Values
Ambient Temperature	-20 °C ~ 85 °C
Storage Temperature	-40 °C ~ 125 °C
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 2.5V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA
Crystal Frequency	2MHz ~ 27MHz

5.2 DC Characteristics (Normal I/O)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
VDD33	I/O Buffer Post-Driver Voltage			3.0	3.3	3.6	V
MVDD33	SDRAM Operation Voltage			3.0	3.3	3.6	V
VDD18	Core Logic and I/O Buffer Pre-Driver Voltage	200MHz		1.62	1.8	1.98	V
MVDD18	DDR Operation Voltage	100MHz		1.7	1.8	1.9	V
MVDDQ/ MVDD	DDR Operation Voltage	100MHz		1.7	1.8	1.9	V
RTC_VDD	RTC Power Supply			1.2	-	1.8	V
I_{RTC_VDD}	RTC Supply Current		RTC_VDD<VDD18	-	4	-	uA
V_{IH}	Input High Voltage			2.0	-	5.5	V
V_{IL}	Input Low Voltage			-0.3	-	0.8	V
V_T	Threshold Point			1.45	1.58	1.74	V
V_{T+}	Schmitt Trigger Low to High Threshold Point			1.44	1.42	1.56	V
V_{T-}	Schmitt Trigger High to Low Threshold Point			0.89	1.06	0.99	V
I_{CC}	Core Power Supply Current		F_{CPU} = 200MHz, MCLK = 100MHz, VDD18 = 1.8V	-	160	-	mA

I_L	Input Leakage Current			-10	-	10	uA
I_{OZ}	Tri-State Output Leakage Current			-10	-	10	uA
R_{PU}	Pull-Up Resistor			39	65	116	kΩ
R_{PD}	Pull-Down Resistor			40	56	108	kΩ
V_{OL}	Output Low Voltage			-	-	0.4	V
V_{OH}	Output High Voltage			2.4	-	-	V
I_{OL}	Low Level Output Current	4mA I/O	V_{OL} = 0.4V	-	4.0	-	mA
I_{OH}	High Level Output Current	4mA I/O	V_{OH} = 2.4V	-	5.9	-	mA

5.3 Audio DAC Characteristics

Test conditions: RL = 10K / 50pF, BW = 20Hz ~ 20KHz, Freq.= 1KHz, Sample Rate = 48KHz.

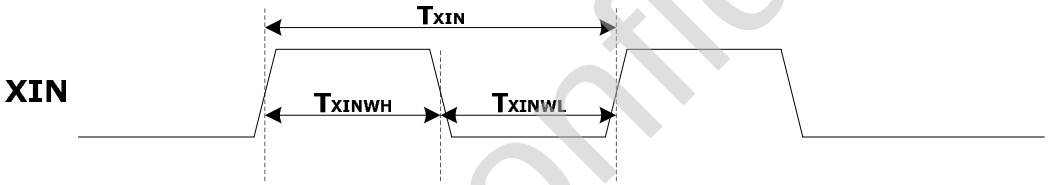
Parameter	Min	Typ	Max	Unit
Operating Voltage	3.0	3.3	3.6	V
Reference Voltage	-	DAC_VDD/2	-	V
Reference Capacitor	-	0.1	-	uF
Full Scale output voltage	-	1.32	-	Vrms
Maximum Output Power	-	-	52	mW
Maximum Output Power @ 32ohm load	-	-	46	mW
Maximum Output Power @ 16ohm load	-	-	41	mW
L-Channel SNR	-	86	-	dBV
R-Channel SNR	-	85	-	dBV
L-Channel THD+N	-	-64	-	dB
R-Channel THD+N	-	-64	-	dB
L-Channel THD+N @ 32ohm load	-	-63	-	dB
R-Channel THD+N @ 32ohm load	-	-63	-	dB
L-Channel THD+N @ 16ohm load	-	-62	-	dB
R-Channel THD+N @ 16ohm load	-	-62	-	dB

5.4 ADC Characteristics

Parameter	Min.	Typ.	Max.	Unit
SAR ADC Input Voltage Range	3.0	-	3.6	V
Resolution of ADC	-	-	10	bit
Signal-to-Noise Plus Distortion of ADC from Line In	-	TBD	-	dB
Integral Non-Linearity of ADC	-	±2.0	-	LSB
Differential Non-Linearity of ADC	-	±0.8	-	LSB
No Missing Code	-	10	-	bit
AD Conversion Rate=ADCCLK/16	-	-	400	KHz

5.5 AC Characteristics (Digital Interface)

5.5.1 Clock Input Characteristics

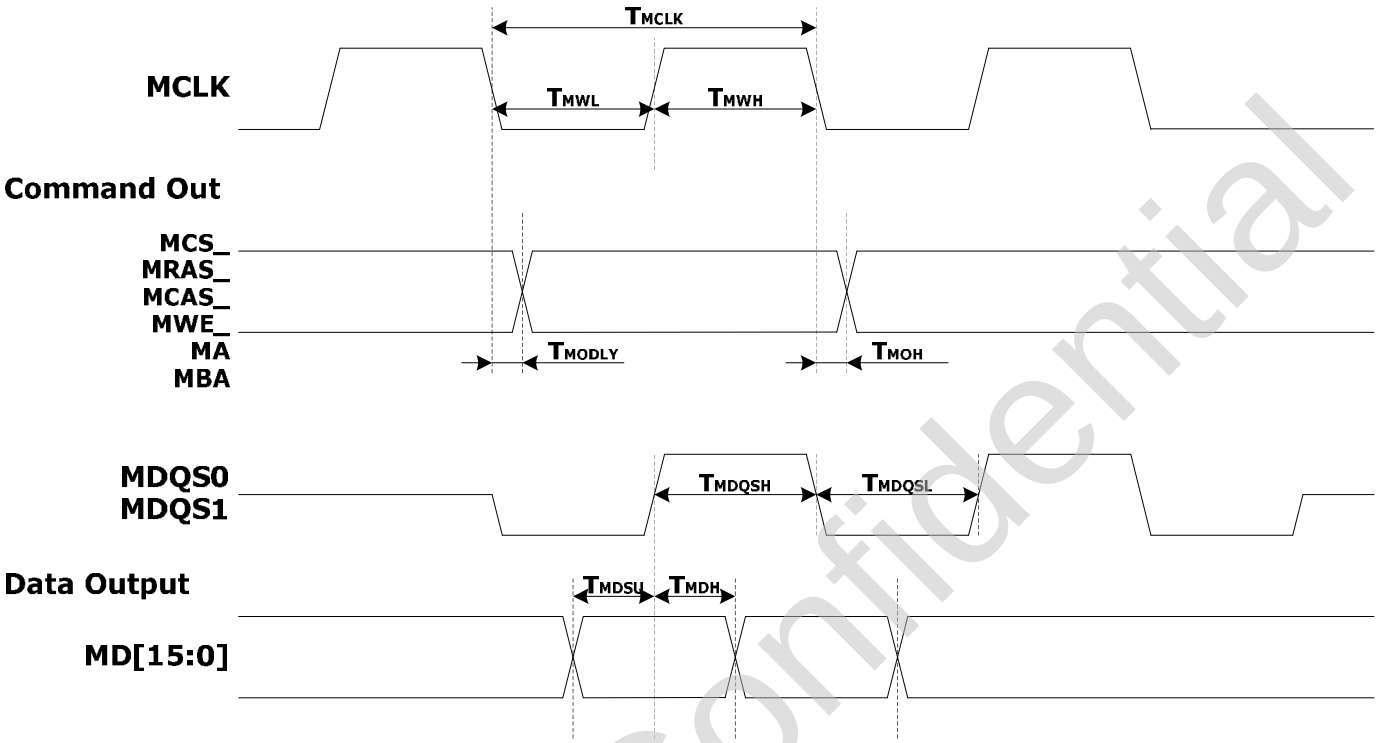


$F_{XIN} = 1 / T_{XIN}$

$XIN_{DUTY} = T_{XINWH} / (T_{XINWH} + T_{XINWL})$

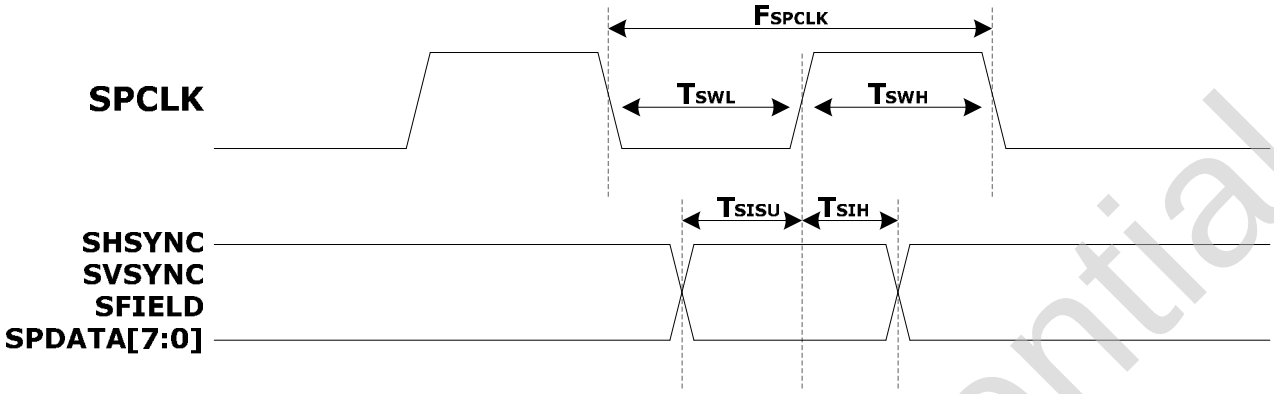
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{XIN}	Clock Input Frequency	-	12 / 27	-	MHz
XIN_{DUTY}	Clock Input Duty Cycle	45	50	55	%

5.5.2 SDRAM Interface



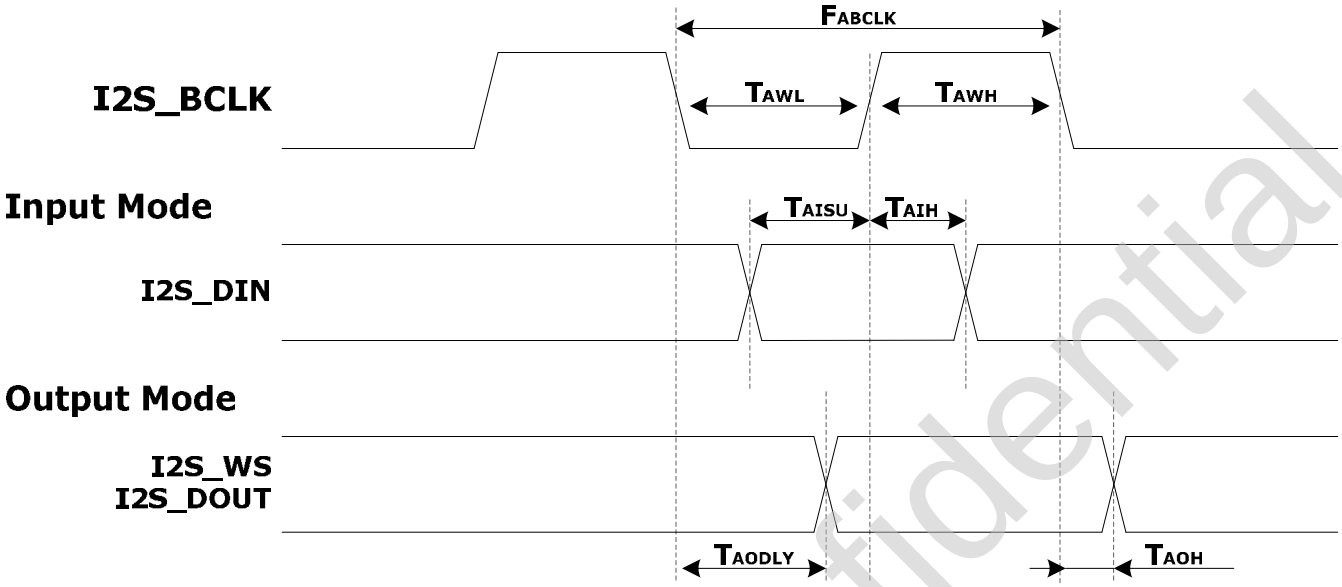
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{MCLK}	MCLK Clock Cycle Time	6	-	12	ns
T_{MWL}	MCLK Clock Low Time	0.45	-	0.55	T_{MCLK}
T_{SWH}	MCLK Clock High Time	0.45	-	0.55	T_{MCLK}
T_{MODLY}	Command and Address Output Delay Time	-	-	2	ns
T_{MOH}	Command and Address Output Hold Time	2	-	-	ns
T_{MDQSH}	MDQS0/MDQS1 High Time	0.4	-	0.6	T_{MCLK}
T_{MDQSL}	MDQS0/MDQS1 Low Time	0.4	-	0.6	T_{MCLK}
T_{MDSU}	MD to MDQS0/MDQS1 Setup Time	0.6	-	-	ns
T_{MDH}	MD to MDQS0/MDQS1 Hold Time	0.6	-	-	ns
VREF	IO reference voltage	0.49	-	0.51	VDD

5.5.3 Sensor/Video-In Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPCLK Clock Frequency	-	-	50	MHz
T_{SWL}	SPCLK Clock Low Time	10	-	-	ns
T_{SWH}	SPCLK Clock High Time	10	-	-	ns
T_{SISU}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Setup Time	1.0	-	-	ns
T_{SIH}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Hold Time	1.0	-	-	ns

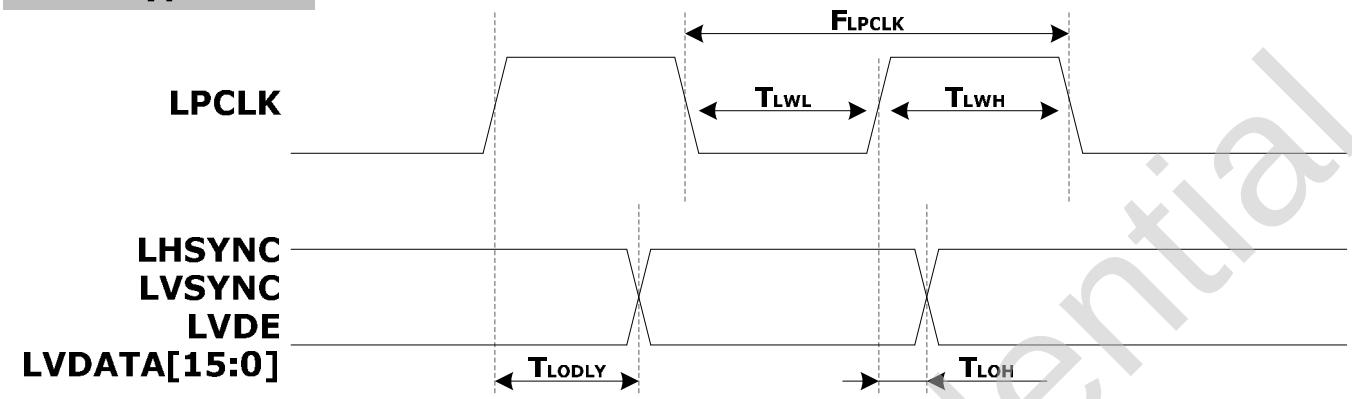
5.5.4 I2S Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{ABCLK}	I2S_BCLK Clock Frequency	-	-	16	MHz
T_{AWL}	I2S_BCLK Clock Low Time	31.25	-	-	ns
T_{AWH}	I2S_BCLK Clock High Time	31.25	-	-	ns
T_{AISU}	I2S_DIN Setup Time	10	-	-	ns
T_{AIH}	I2S_DIN Hold Time	10	-	-	ns
T_{AODLY}	I2S_DOUT Output Delay Time	-	-	0.5	ns
T_{AOH}	I2S_DOUT Output Hold Time	0.1	-	-	ns

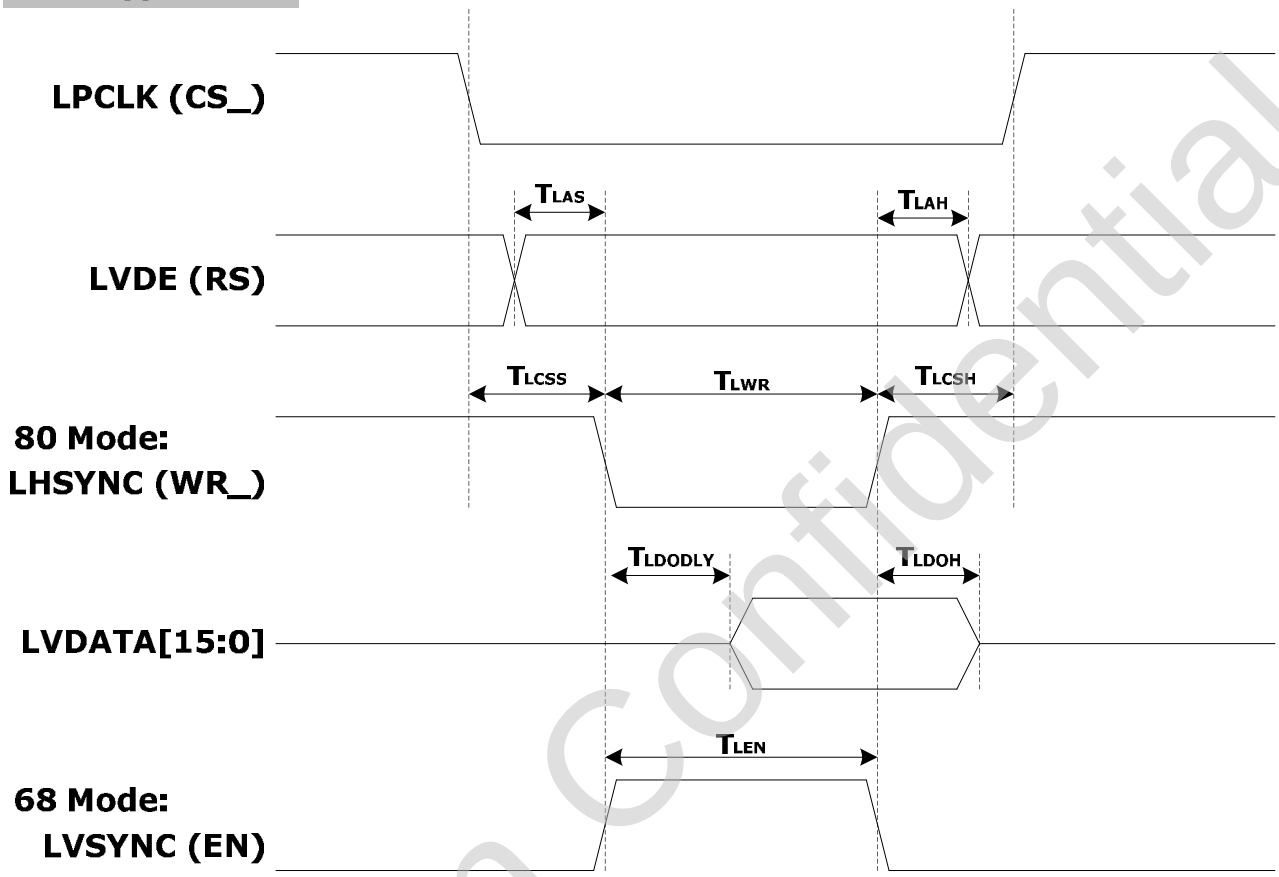
5.5.5 LCD / Display Interface

SYNC Type LCD



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPCLK}	LPCLK Clock Frequency	-	-	27	MHz
T_{LWL}	LPCLK Clock Low Time	18.5	-	-	ns
T_{LWH}	LPCLK Clock High Time	18.5	-	-	ns
T_{LODLY}	LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time	-	-	1.3	ns
T_{LOH}	LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time	0.67	-	-	ns

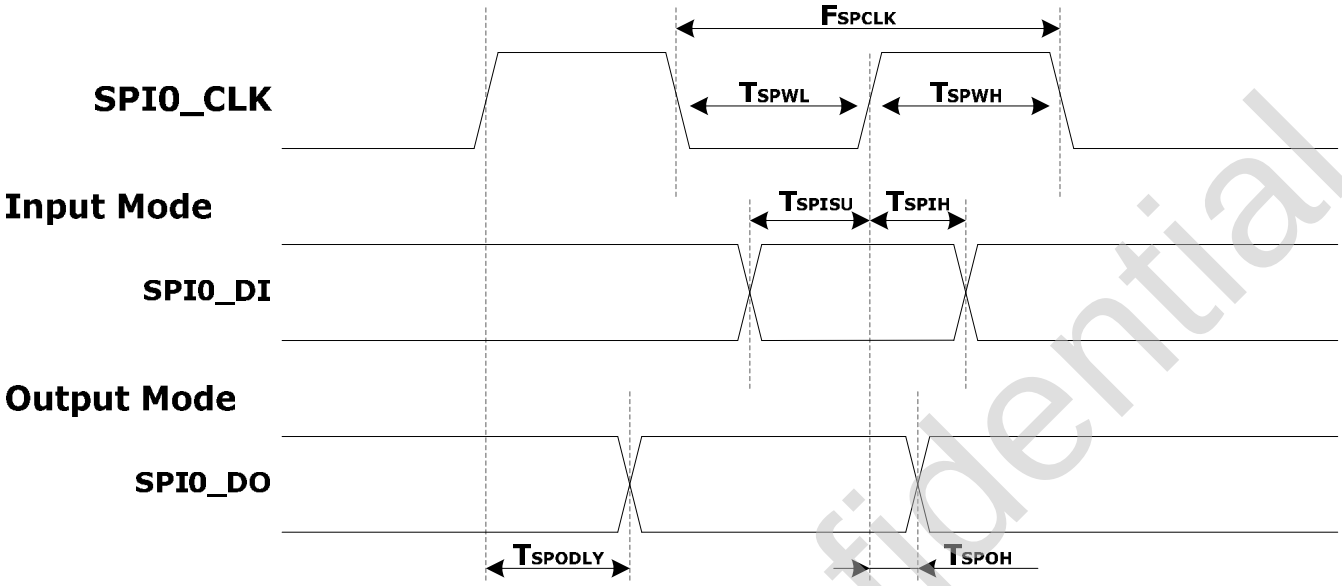
MPU Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LCSS}	CS_ to WR_ Setup Time		2	-	-	PCLK
T_{LCSH}	CS_ to WR_ Hold Time		1	-	-	PCLK
T_{LAS}	RS to WR_ Setup Time		1	-	-	PCLK
T_{LAH}	RS to WR_ Hold Time		1	-	-	PCLK
T_{LDODLY}	LVDATA Output Delay Time		-	-	1	PCLK
T_{LDOH}	LVDATA Output Hold Time		1	-	-	PCLK
T_{LWR}	WR_ Pulse Width	80 Mode	1	-	-	PCLK
T_{LEN}	EN Pulse Width	68 Mode	1	-	-	PCLK

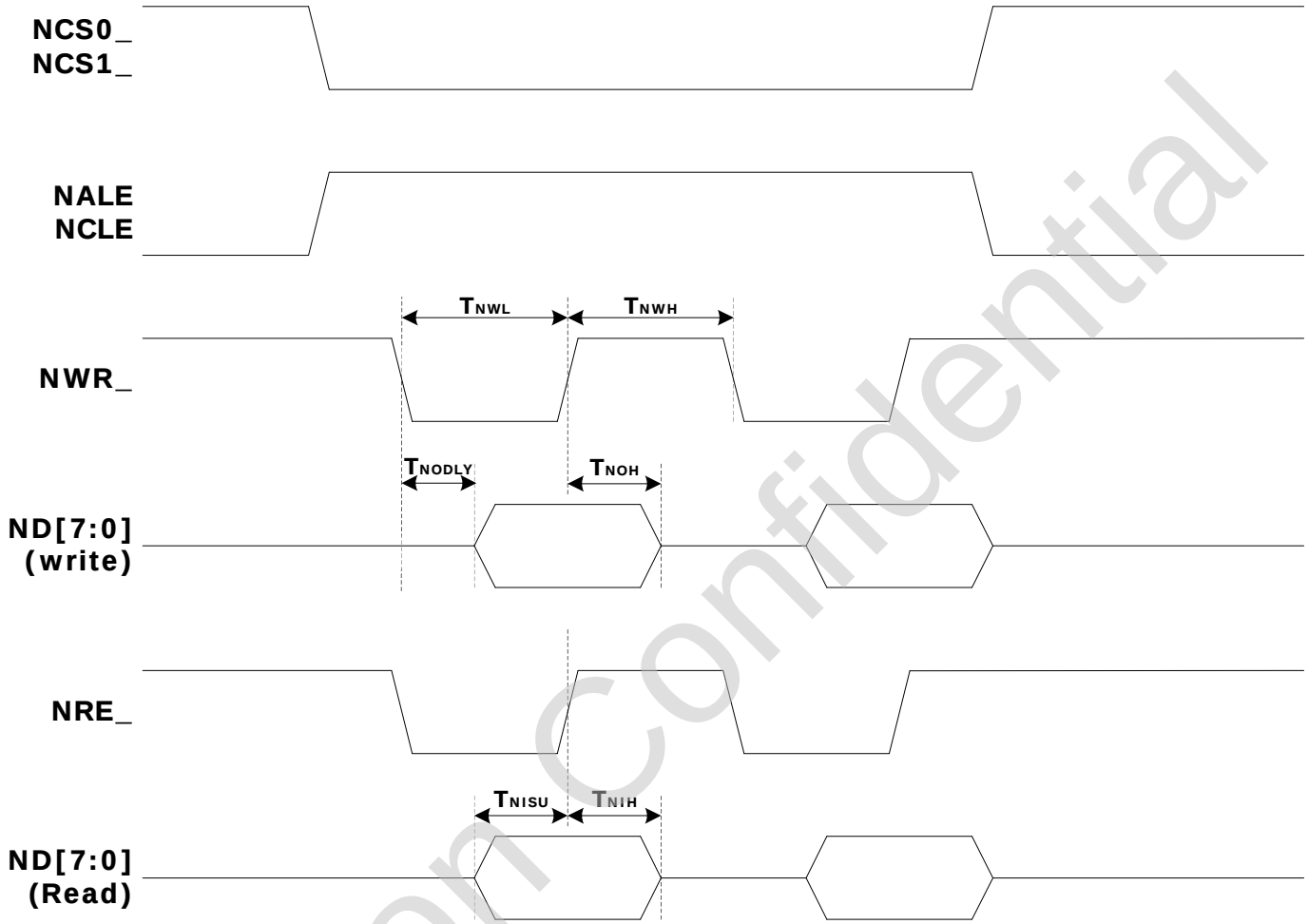
Note: PCLK is the period of one APB bus clock.

5.5.6 SPI Interface



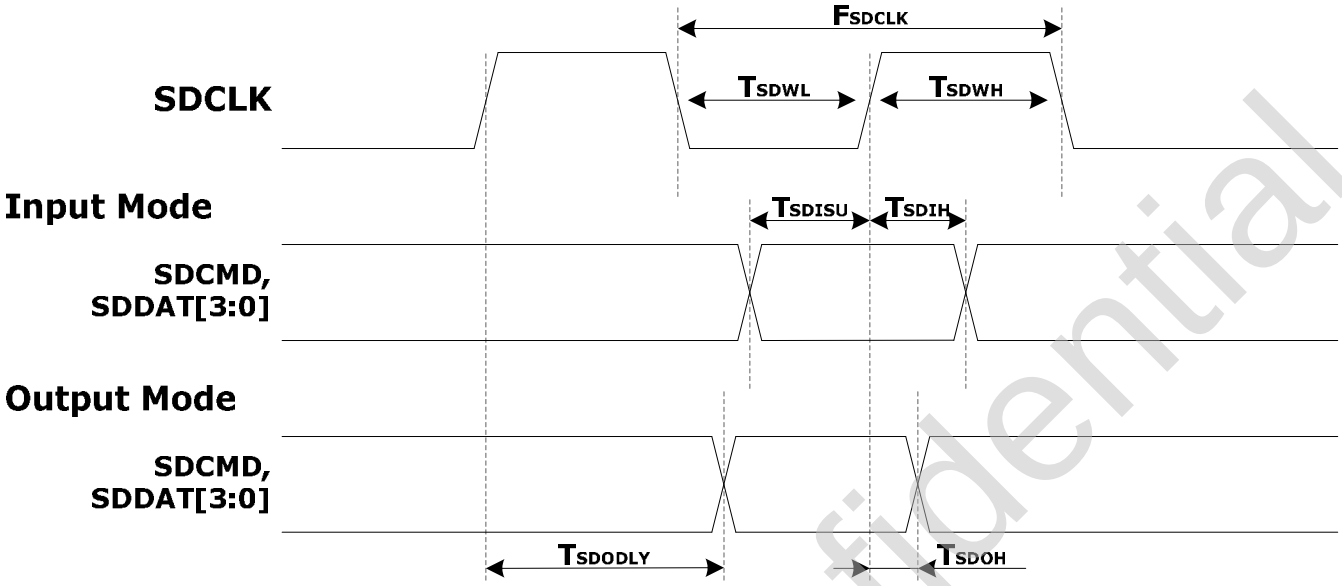
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPI0_CLK Clock Frequency	-	-	25	MHz
T_{SPWL}	SPI0_CLK Clock Low Time	20	-	-	ns
T_{SPWH}	SPI0_CLK Clock High Time	20	-	-	ns
T_{SPISU}	SPI0_DI Setup Time	10	-	-	ns
T_{SPIH}	SPI0_DI Hold Time	10	-	-	ns
T_{SPODLY}	SPI0_DO Output Delay Time	-	-	1	ns
T_{SPOH}	SPI0_DO Output Hold Time	0.2	-	-	ns

5.5.7 NAND Interface



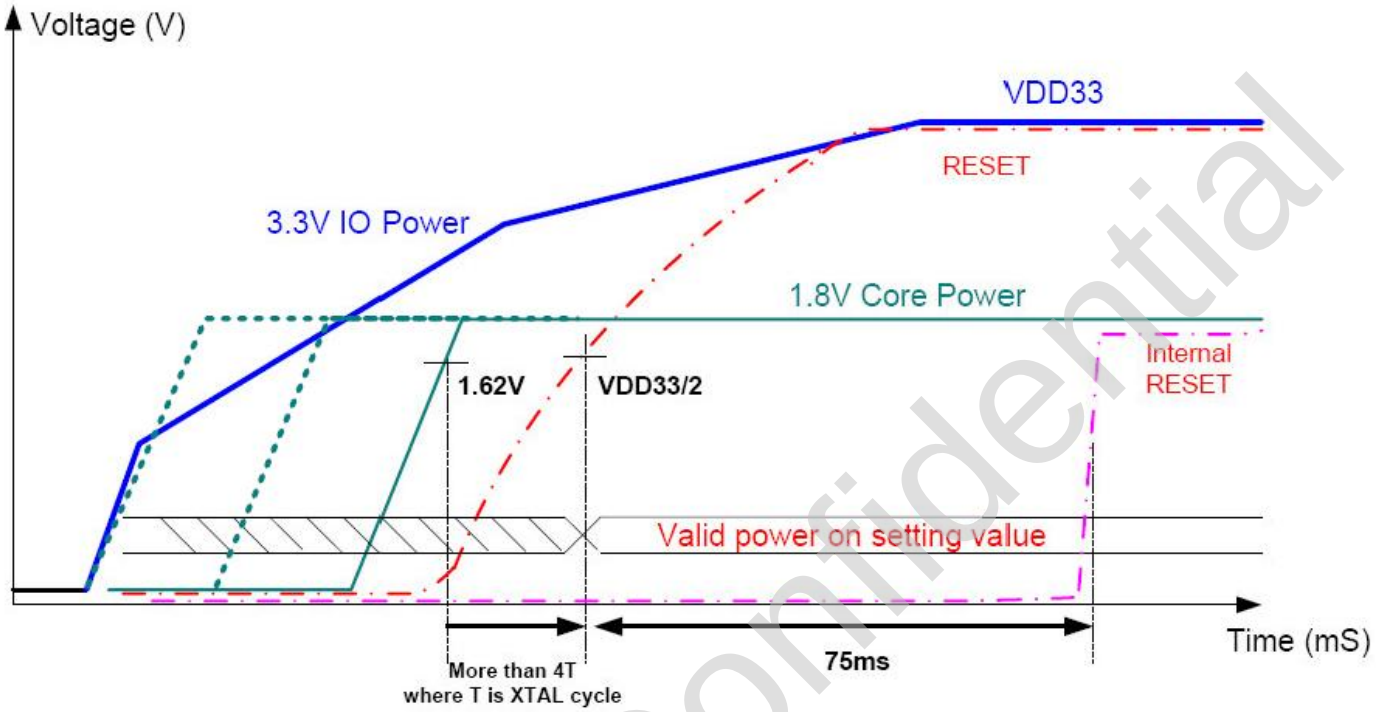
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{NWL}	Write Pulse Low Width	10	-	-	ns
T_{NWH}	NWR_ High Hold Time	10	-	-	ns
T_{NODLY}	ND[7:0] Output Delay Time	-	-	2.5	ns
T_{NOH}	ND[7:0] Output Hold Time	10	-	-	ns
T_{NISU}	ND[7:0] Data in Setup Time	3.2	-	-	ns
T_{NIH}	ND[7:0] Data in hold time	1	-	-	ns

5.5.8 SD Card Interface

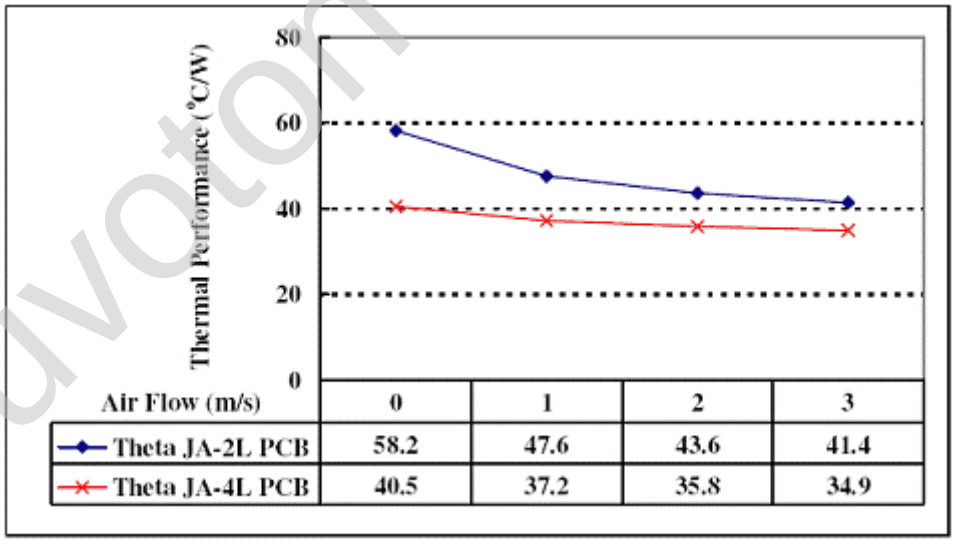


Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock SDCLK					
F_{SDCLK}	Clock Frequency in Data Transfer Mode	-	-	24	MHz
F_{SDCLK}	Clock Frequency in Identification Mode	100	-	400	KHz
T_{SDWL}	Clock Low Time	10	-	-	ns
T_{SDWH}	Clock High Time	10	-	-	ns
Input SDCMD, SDDAT[3:0] (referenced to SDCLK)					
T_{SDISU}	Input Setup Time	6	-	-	ns
T_{SDIH}	Input Hold Time	2	-	-	ns
Output SDCMD, SDDAT[3:0] (referenced to SDCLK)					
T_{SDODLY}	Output Delay Time	-	-	14	ns
T_{SDOH}	Output Hold Time	2.5	-	-	ns

5.6 Power-on Sequence



5.7 Thermal characteristics of LQFP-128 Package



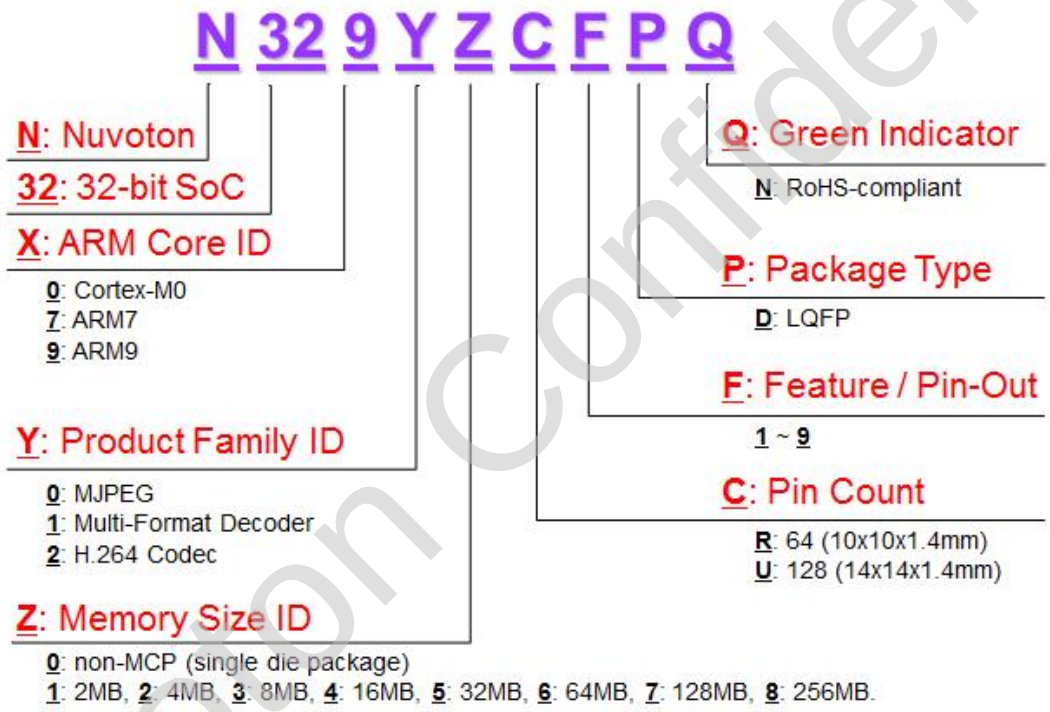
Air Flow (m/s)	0	1	2	3
Theta JA-2L PCB	58.2	47.6	43.6	41.4
Theta JA-4L PCB	40.5	37.2	35.8	34.9

Thermal Performance of LQFP-128 under Forced Convection

6. ORDERING INFORMATION

PART NO.	PACKAGE TYPE	DESCRIPTION
N32901U1DN	LQFP-128, MCP[1]	Stacked 1Mbit x16 SDR MCP with LCD, CIS and I2S interface.
N32903R1DN	TQFP-64, MCP	Stacked 4Mbit x 16 DDR MCP with CIS, SDHC and I2S interface
N32903U1DN	LQFP-128, MCP	Stacked 4Mbit x16 DDR MCP with LCD,CIS and I2S interface.
N32905U1DN	LQFP-128, MCP	Stacked 16Mbit x16 DDR MCP with LCD, CIS and I2S interface.
N32905U2DN	LQFP-128, MCP	Stacked 16Mbit x16 DDR MCP with LCD,CIS interface & TV output.

6.1 Part Number Definition



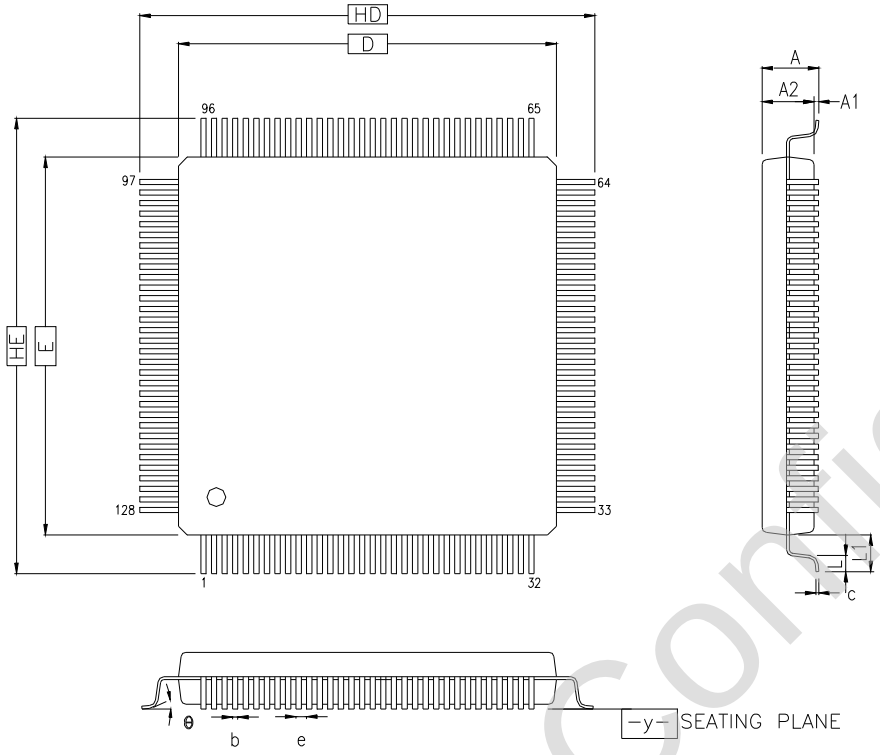
6.2 Difference between N32901U1DN, N32903U1DN, N32905U1DN and N32905U2DN

	MCPed SDRAM Type/Capacity	Analog Composite TV Output	I2S Interface
N32901U1DN	SDR/2MBytes	-	V
N32901U2DN	SDR/2MBytes	V	-
N32903U1DN	DDR/8MBytes	-	V
N32905U1DN	DDR/32MBytes	-	V
N32905U2DN	DDR/32MBytes	V	-

[1] MCP stands for Multi-Chip Package.

7. PACKAGE OUTLINE

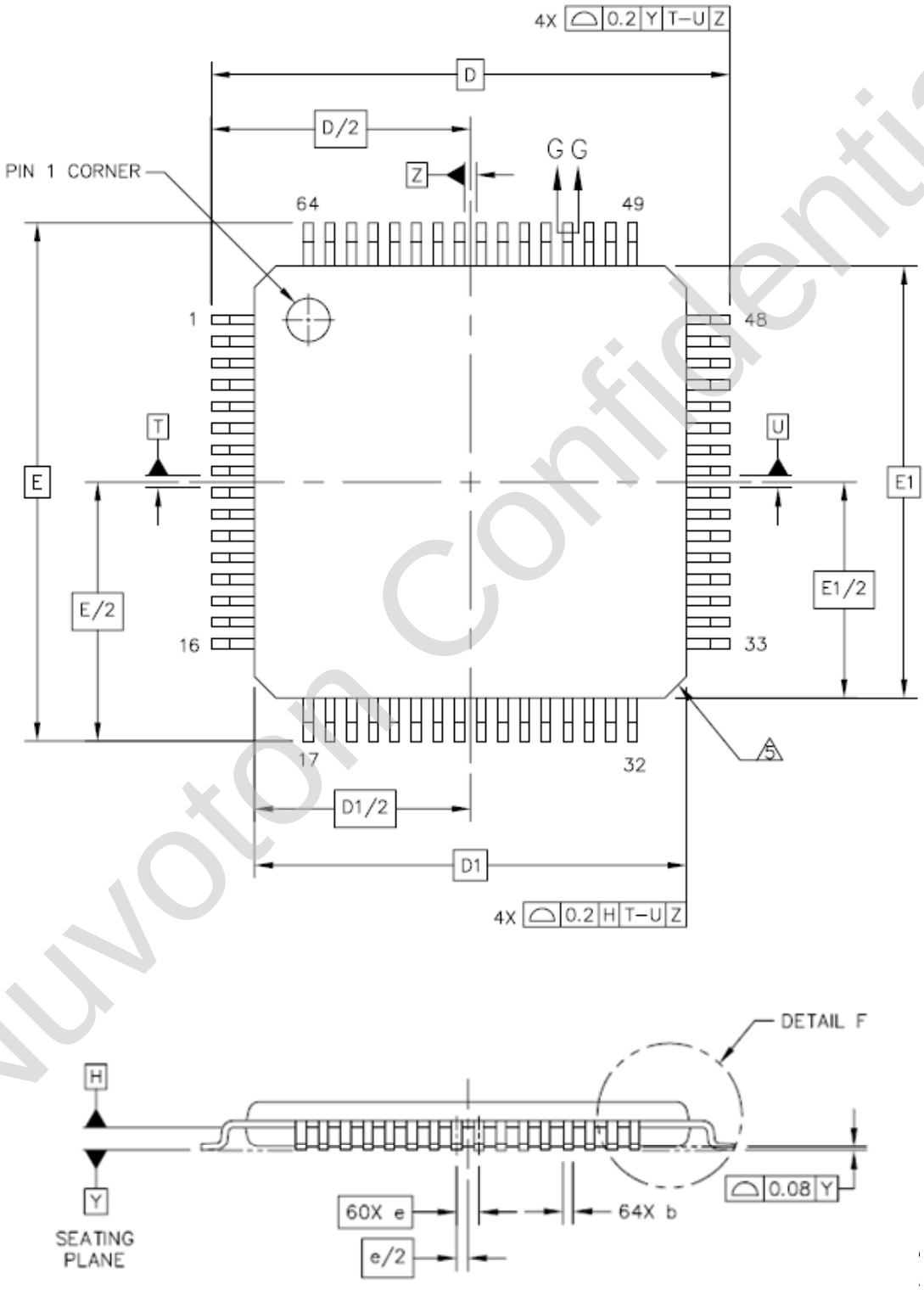
7.1 LQFP-128 (14X14X1.4mm body, 0.4mm pitch)

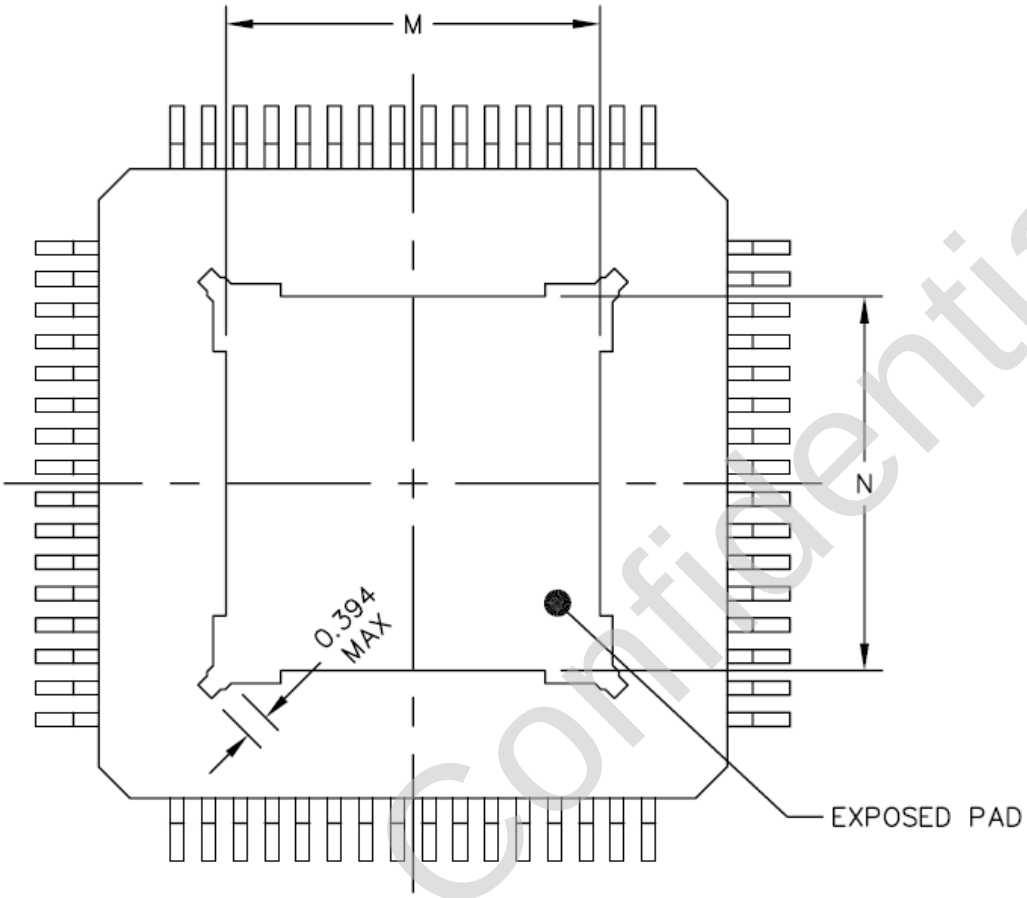


COTROL DIMENSIONS ARE IN MILLIMETERS.

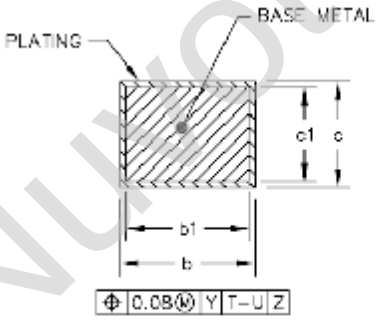
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

7.2 TQFP-64 (10X10X1.0mm body, 0.5mm pitch)

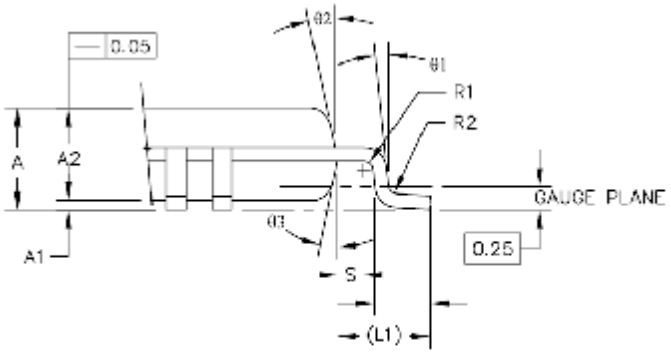




BOTTOM VIEW



SECTION C-C



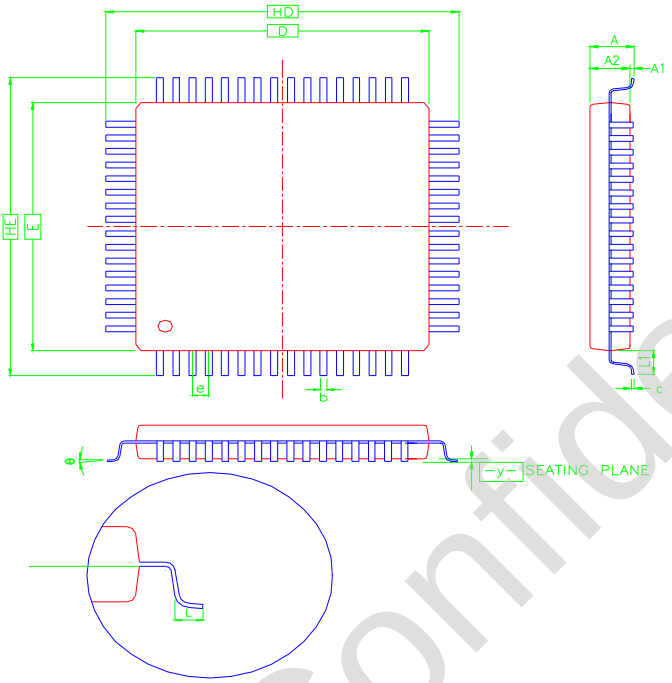
DETAIL F

DIM	MIN		MAX
A	---		1.2
A1	0.05		0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		12 BSC	
D1		10 BSC	
e		0.5 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.6	0.75

DIM	MIN		MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°
M	5.85		6.05
N	5.85		6.05

UNIT: mm

7.3 LQFP-64 (10X10X1.4mm body, 0.5mm pitch)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

8. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A0	Jul. 25, 2012	ALL	▪ Initial release.
A1	Aug. 1, 2012	36	▪ Add stacked DRAM size into order Information
A2	Aug. 30, 2012	ALL	▪ Add N32901U1DN Information ▪ Correct the N32905U2DN Pin Diagram
A2.1	Sept. 17, 2012	22	▪ 1Mx16 MVDD and MVDDQ are changed from 3.3V to 1.8V for consistence with N32905 and N32903
A3	Oct. 15, 2012	23,35	▪ Extend Operation Temperature Range ▪ Add Parts Feature Difference Table
A3.1	Oct. 26, 2012	35	▪ Add Part Number Definition
A3.2	Nov. 8, 2012	6,7,8,9	▪ Add CCIR Still Image and Video Recommanded Resolutions. ▪ Add LCD Display for Still Image and Video Recommanded Resolutions. ▪ Modify One SPI H/W Engine to Support Two SPI Devices by Two Chip Selection Signals when SPI0 is in Master Mode. For LQFP128 package, only SPI0 is active. ▪ Add USB 1.1 Host One H/W Controller, Three Different Pin Locations Information.
A3.3	Nov. 10, 2012	35	▪ Remove Adobe Flash Feature from Comparision Table.
A3.4	Jan. 21, 2013	4, 5, 10, 23	▪ Update the AC characteristics.
A4.0	Mar. 15, 2013	ALL	▪ Add N32903R1DN
A5.0	May. 1, 2013	ALL	▪ Add N32901R1DN Information. ▪ Add N32901U2DN Information.
A5.1	May. 3,2013	28	▪ Add SDRAM and DDR Operation Voltage Spec

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