MELSEC A/Q Series

Programmable Logic Controller Manual

Analog Input Module A68ADN

MITSUBISHI ELECTRIC EUROPE B.V.
FACTORY AUTOMATION

REVISIONS

*The manual number is given on the bottom left of the back cover.

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Jul., 1991	IB (NA) 66307-A	First edition
Jul., 1992	IB (NA) 66307-B	Correction Sections 3.2 (Table 3.2), 4.2, 5.3 , APPENDIX 2
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● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual. Also pay careful attention to safety and handle the module properly.

These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PC system safety precautions.

These ● SAFETY PRECAUTIONS ● classify the safety precautions into two categories: "DANGER" and "CAUTION".

DANGER	Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.
CAUTION	Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.

Depending on circumstances, procedures indicated by **CAUTION** may also be linked to serious results.

In any case, it is important to follow the directions for usage.

Store this manual in a safe place so that you can take it out and read it whenever necessary.
Always forward it to the end user.

[System Design Precautions]

DANGER

- Safety circuits should be installed external to the programmable controller to ensure that the system as a whole will continue to operate safely in the event of an external power supply malfunction or a programmable controller failure.
  Erroneous outputs and operation could result in an accident.
  1) The following circuitry should be installed outside the programmable controller:
     Interlock circuitry for the emergency stop circuit protective circuit, and for reciprocal operations such as forward/reverse, etc., and interlock circuitry for upper/lower positioning limits, etc., to prevent machine damage.
  2) When the programmable controller detects an abnormal condition, processing is stopped and all outputs are switched OFF. This happens in the following cases
     - When the power supply module's over-current or over-voltage protection device is activated
     - When an error (watchdog timer error, etc.) is detected at the PC CPU by the self-diagnosis function.

     Some errors, such as input/output control errors, cannot be detected by the PC CPU, and there may be cases when all outputs are turned ON when such errors occur. In order to ensure that the machine operates safely in such cases, a failsafe circuit or mechanism should be provided outside the programmable controller. Refer to the CPU module user's manual for an example of such a failsafe circuit.
  3) Outputs may become stuck at ON or OFF due to an output module relay or transistor failure. An external circuit should therefore be provided to monitor output signals whose incorrect operation could cause serious accidents.

- A circuit should be installed which permits the external power supply to be switched ON only after the programmable controller power has been switched ON. Accidents caused by erroneous outputs and motion could result if the external power supply is switched ON first.

- When a data link communication error occurs, the status shown below will be established at the faulty station. In order to ensure that the system operates safely at such times, an interlock circuit should be provided in the sequence program (using the communication status information).
  Erroneous outputs and operation could result in an accident.
  1) The data link data which existed prior to the error will be held.
  2) All outputs will be switched OFF at MELSECNET (II, /B, /10) remote I/Ostations.
  3) At the MELSECNET/MINI-S3 remote I/O stations, all outputs will be switched OFF or output statuses will be held, depending on the E.C. mode setting.

  For details on procedures for checking faulty stations, and for operation statuses when such errors occur, refer to the appropriate data link manual.

[System Design Precautions]

⚠ CAUTION

- Do not bundle control lines or communication wires together with main circuit or power lines, or lay them close to these lines.
  As a guide, separate the lines by a distance of at least 100 mm, otherwise malfunctions may occur due to noise.
  When file register R that are outside the range are read, e.g. by a MOV instruction, the file register data will become $FFFF_H$ and use of this data will cause malfunctions. Take care not to use file registers that are outside the range when designing programs
  For details on instructions, refer to the Programming Manual.

[Cautions on Mounting]

⚠ CAUTION

- Use the PC in an environment that conforms to the general specifications in the manual.
  Using the PC in environments outside the ranges stated in the general specifications will cause electric shock, fire, malfunction, or damage to/deterioration of the product.
- Make sure that the module fixing projection on the base of the module is properly engaged in the module fixing hole in the base unit before mounting the module.
  Failure to mount the module properly will result in malfunction or failure, or in the module falling.
- Extension cables should be securely connected to base unit and module connectors. Check for loose connection after installation
  A poor connection could result in contact problems and erroneous inputs/outputs.
- Plug the memory card firmly into the memory card mounting connector. Check for loose connection after installation. A poor connection could result in erroneous operation.

[Cautions on Wiring]

DANGER

- Switch off the external power supply before staring installation and wiring work
  Failure to do so could result in electrical shocks and equipment damage.
- After installation and wiring is completed, be sure to attach the terminal cover before switching the power ON and starting operation
  Failure to do so could result in electrical shocks.

CAUTION

- Be sure to ground the FG and LG terminals, carrying out at least class 3 grounding work with a ground exclusive to the PC.
  Otherwise there will be a danger of electric shock and malfunctions.
- Carry out wiring to the PC correctly, checking the rated voltage and terminal arrangement of the product.
  Using a power supply that does not conform to the rated voltage, or carrying out wiring incorrectly, will cause fire or failure.
- Outputs from multiple power supply modules should not be connected in parallel. Failure to do so could cause the power supply module to overheat, resulting in a fire or module failure.
- Tighten the terminal screws to the stipulated torque.
  Loose screws will cause short circuits, fire, or malfunctions.
- Make sure that no foreign matter such as chips or wiring offcuts gets inside the module. It will cause fire, failure or malfunction.
- Connectors for external connections should be crimped, pressure welded, or soldered in the correct manner using the correct tools
  For details regarding crimping and pressure welding tools, refer to the input/output module user's manual.
  A poor connection could cause shorts, fire, and erroneous operation.

[Cautions on Startup and Maintenance]

DANGER

- Do not touch terminals while the power is ON.
  This will cause malfunctions.
- Make sure that the battery is connected properly. Do not attempt to charge or disassemble the battery, do not heat the battery or place it in a flame, and do not short or solder the battery.
  Incorrect handling of the battery can cause battery heat generation and ruptures which could result in fire or injury.
- Switch the power off before cleaning or re-tightening terminal screws.
  Carrying out this work while the power is ON will cause failure or malfunction of the module.

CAUTION

- In order to ensure safe operation, read the manual carefully to acquaint yourself with procedures for program changes, forced outputs, RUN/STOP, and PAUSE operations, etc., while operation is in progress. Incorrect operation could result in machine failure and injury.
- Do not disassemble or modify any module.
  This will cause failure, malfunction, injuries, or fire.
- Switch the power OFF before mounting or removing the module.
  Mounting or removing it with the power ON can cause failure or malfunction of the module.
- When replacing fuses, be sure to use the prescribed fuse.
  A fuse of the wrong capacity could cause a fire.

[Cautions on Disposal]

CAUTION

- Dispose of this product as industrial waste.

CONTENTS

1. INTRODUCTION

This manual gives specifications, handling, programming procedures, etc. for the A68ADN analog to digital converter module (hereafter called the A68ADN) for use with MELSEC-A series PC CPU modules.

An A68ADN converts analog signals (voltage or current) into 16-bit, signed binary digital values, as shown in the following figure.

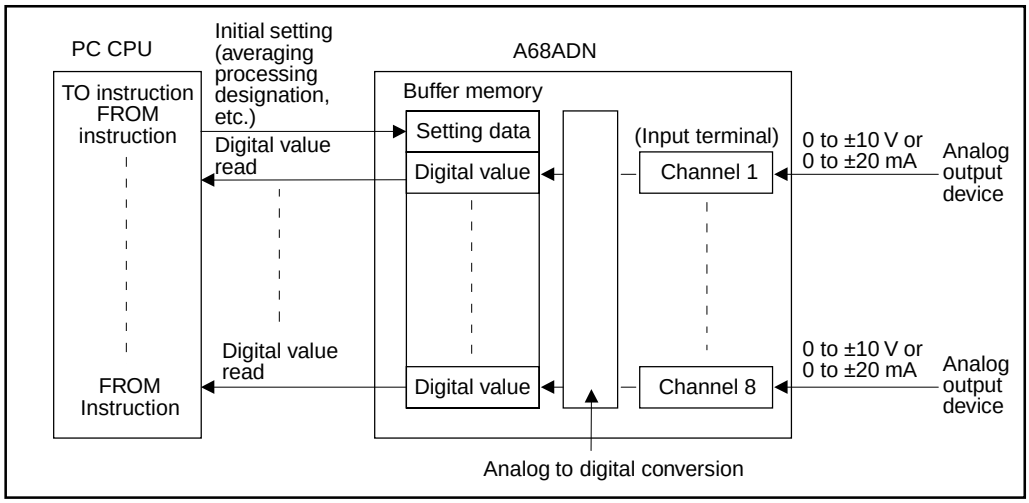


Figure 1.1 Analog to Digital Conversion

A chart showing differences between the A68ADN and the A68AD, A68AD-S2, and A616AD is given in Appendix 1.

1.1 Features

(1) 8-channel analog to digital (hereafter A-D) conversion is possible with a single module.

The A616ADN has 8-channel A-D conversion capability, with each channel selectable for voltage or current input.

(2) 1/12000 high resolution (all channels)

Resolution is selectable from 1/4000, 1/8000, and 1/12000. High resolution digital values can be obtained. Resolution setting applies to all channels.

(3) Averaging processing by designating time or frequency (for each channel)

In addition to sampling processing (in which the digital value obtained in A-D conversion is output each time the A-D conversion is executed) averaging processing can be done in a designated time or frequency. The A-D conversion mode is selectable for each channel.

(4) Conversion enable/disable setting (for each channel)

Whether A-D conversion is enabled or disabled can be set for each channel. By setting "disable" for the unused channels, conversion speed can be increased.

(5) Offset/gain adjustment without dials (for each channel)

Offset and gain can be set by simply inputting the required value (voltage or current) and turning the setting switch ON.

2. SYSTEM CONFIGURATIONS

2.1 Overall Configurations

(1) Figure 2.1 shows the overall system configuration when the A68ADN is used with a building block-type PC CPU

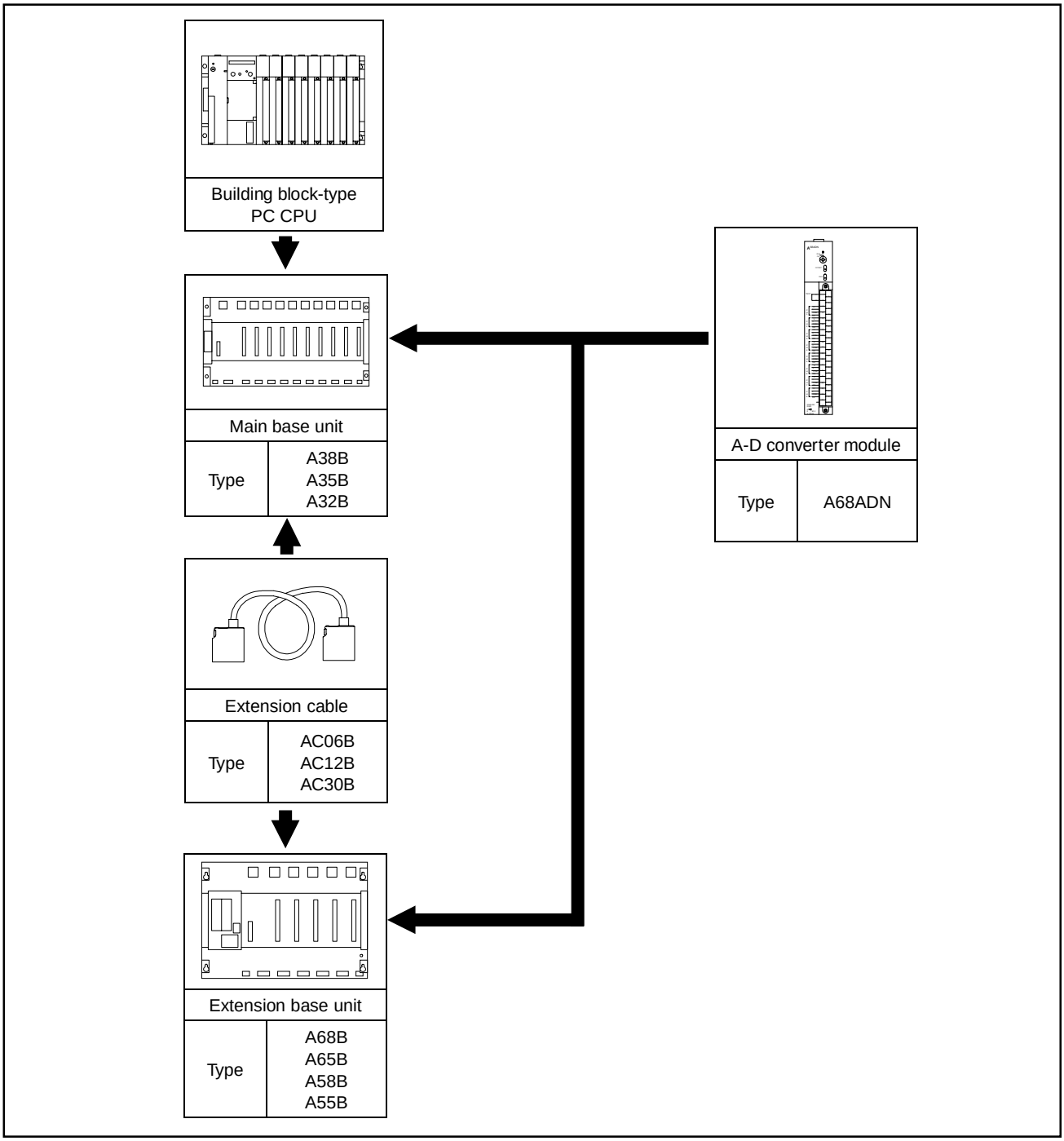


Fig.2.1 Overall Configuration Using a Building Block–Type PC CPU

(2) Figure 2.2 shows the overall system configuration when the A68ADN is used with a compact-type PC CPU

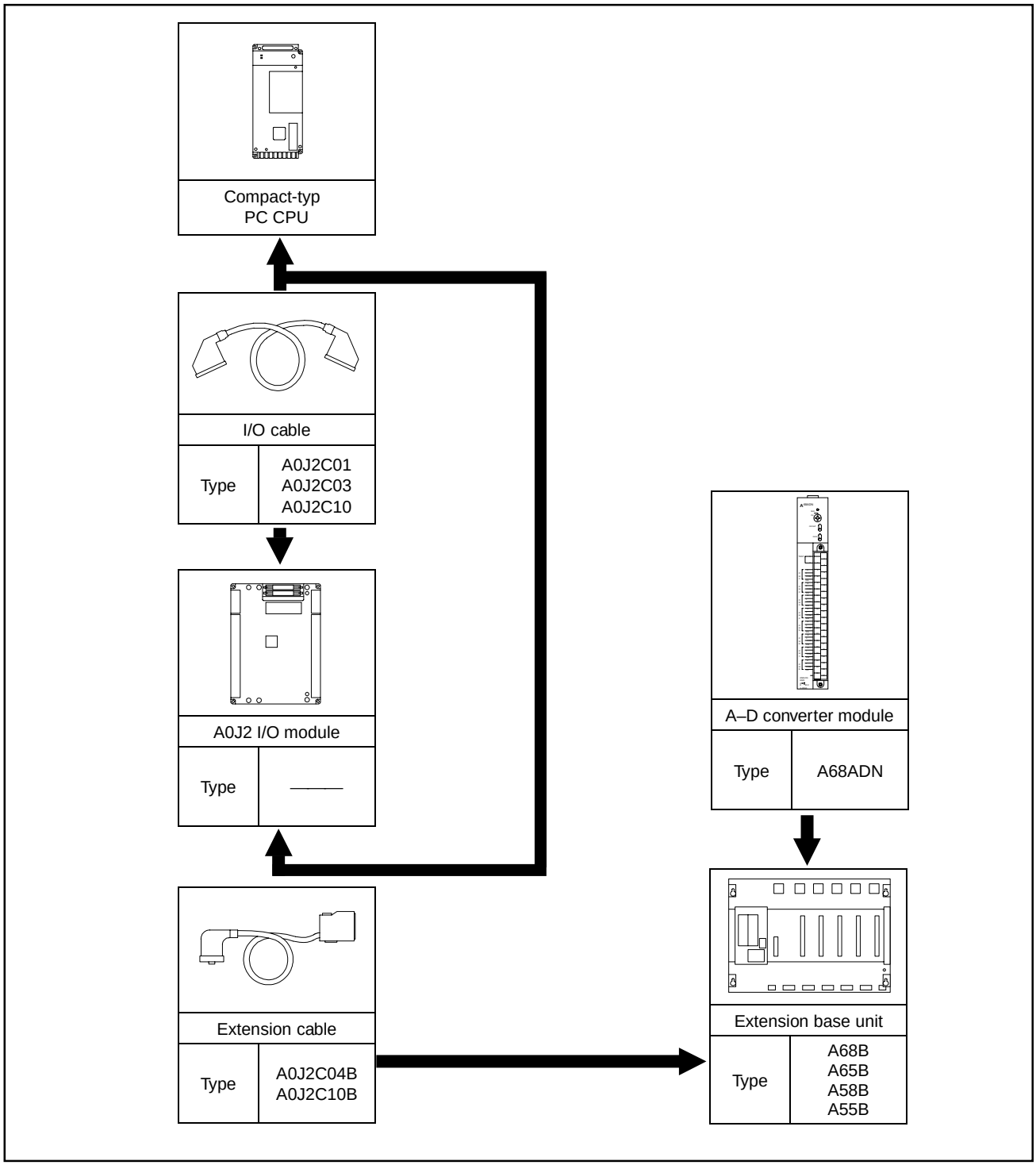


Fig. 2.2 Overall Configuration Using a Compact-Type PC CPU

2.2 Applicable Systems

The A68ADN can be used for the systems indicated below. Please note that installation of the A68ADN in other systems is not possible.

(1) The following PC CPU modules and remote I/O module can be used with an A68ADN:

Applicable models

A0J2CPU(P21/R21)	AOJ2CPU(P23/R23)	A2ASCPU-S1
A1NCPU(P21/R21)	A1CPU(P21/R21)	A52GCPU(T21B)
A2NCPU(P21/R21)	A2CPU(P21/R21)	A2ACPU(P21/R21)
A2NCPU(P21/R21)-S1	A2CPU(P21/R21)-S1	A2ACPU(P21/R21)-S1
A3NCPU(P21/R21)	A3CPU(P21/R21)	A3ACPU(P21/R21)
A3HCPU(P21/R21)	A1SCPU-S1	A2UCPU
A3MCPU(P21/R21)	A1SJCPU	A2UCPU-S1
A73CPU(P21/R21)	A2SCPU-S1	A3UCPU
		A4UCPU

Applicable remote I/O module

AJ71P25/R25

POINT

The A68ADN cannot be used with the A0J2P25/R25 (remote I/O station)

(2) The A68ADN can be attached to any slot of the base unit. However, the following precautions must be taken:

(a) The power supply capacity will be exceeded if the A68ADN is attached to an extension base unit (A55B and A58B) which contains no power supply. When attaching the A68ADN to an extension base unit not loaded with a power supply module, the voltage drop of the power capacity of a power supply module of a main base unit and the extension cable must be considered. Keep these factors in mind when selecting a power supply module and an extension cable.

The User's Manual for each PC CPU module gives details.

(b) In an A3CPU(P21/R21) system, do not use the final slot of the seventh extension unit to attach the A68ADN. (This restriction does not apply to the A3NCPU, A3HCPU, A3MCPU, and A3ACPU.)

3. SPECIFICATIONS

3.1 General Specifications

The following table shows the general specifications of the A68ADN.

Table 3.1 General Specifications

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55 °C</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">-20 to 75 °C</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90 %RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90 %RH, non-condensing</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms t
*JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 50 Hz</td><td>—</td><td>0.075 mm
(0.003 in)</td><td rowspan="2">10 times
*(1 octave/minute)</td></tr>
<tr><td>55 to 150 Hz</td><td>1 g</td><td>—</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to *JIS C 0912 (10 g × 3 times in 3 directions)</td></tr>
<tr><td>Noise Durability</td><td colspan="5">By noise simulator of 1500 Vpp noise voltage, 1 μs noise width and 25 to 60 Hz noise frequency.</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">1500 VAC for 1 minute across AC external terminals and ground
500 VAC for 1 minute across DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5 MΩ or larger by 500 VDC insulation resistance tester across AC external terminals and ground</td></tr>
<tr><td>Grounding</td><td colspan="5">Class 3 grounding; grounding is not required when it is impossible.</td></tr>
<tr><td>Operating ambience</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling metho</td><td colspan="5">Self-cooling</td></tr>
</table>

REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, 20 Hz to 40 Hz, 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.
* Japanese Industrial Standard

3.2 Performance Specifications

The following table gives the performance specifications of the A68ADN.

Table 3.2 Performance Specifications

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Analog input</td><td>Voltage : -10 to 0 to 10 VDC (Input resistance: 1 MΩ)
Current : -20 to 0 to 20 mA (Input resistance: 250 kΩ)
} Can be set with th input terminal</td></tr>
<tr><td>Digital output</td><td>Signed 16-bit binary
{ 1/4000 setting : -4096 to 4095
1/8000 setting : -8192 to 8191
1/12000 setting : -12287 to 12287 }</td></tr>
<tr><td>I/ O characteristics</td><td>
<table>
<tr><th rowspan="2">Analog Input</th><th colspan="3">Digital output value (gain : 5 V/20 mA, offset: 0 V/0 mA)</th></tr>
<tr><th>1/4000 setting</th><th>1/8000 setting</th><th>1/12000 setting</th></tr>
<tr><td>10 V</td><td>+4000</td><td>+8000</td><td>+12000</td></tr>
<tr><td>+5 V or +20 mA</td><td>+2000</td><td>+4000</td><td>+6000</td></tr>
<tr><td>0 V or 0 mA</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>+5 V or -20 mA</td><td>-2000</td><td>-4000</td><td>-6000</td></tr>
<tr><td>-10 V</td><td>-4000</td><td>-8000</td><td>-12000</td></tr>
</table>
(Factory setting: gain.....5 V, offset .... 0 V)
</td></tr>
<tr><td>Maximum resolution</td><td>
<table>
<tr><th></th><th>1/4000 setting</th><th>1/8000 setting</th><th>1/12000 setting</th></tr>
<tr><td>Voltage Input</td><td>2.5 mV</td><td>1.25 mV</td><td>0.83 mV</td></tr>
<tr><td>Current input</td><td>10 μA</td><td>5 μA</td><td>3.33 μA</td></tr>
</table>
</td></tr>
<tr><td>Overall accuracy</td><td>Within ±1 % (Accuracy with respect to the maximum value)</td></tr>
<tr><td>Maximum conversion speed</td><td>20 ms/1 channel</td></tr>
<tr><td>Absolute maximum input</td><td>Voltage: ±15 V Current: ±30 mA</td></tr>
<tr><td>Number of analo input device points</td><td>8 channels/1 module</td></tr>
<tr><td>Insulation</td><td>Between input terminals and PC CPU : Photocoupler insulation
Between channels : Not insulated</td></tr>
<tr><td>Number of occupied I/O points</td><td>32 device points (special)</td></tr>
<tr><td>Connection terminal</td><td>38-device point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG) (Applicable tightening torque 7 kg-cm (6.06 lb-in))</td></tr>
<tr><td>Applicable solder-less terminal</td><td>V1.25–3, V1.25–YS3A, V2–S3, V2–YS3A</td></tr>
<tr><td>Internal current consumption (5 V)</td><td>0.4 A</td></tr>
<tr><td>Weight kg (lb)</td><td>0.51 kg (1.13 lb)</td></tr>
<tr><td>External dimen-sions mm (in)</td><td>250 (9.84) (H) × 37.5 (1.48) (W × 131 (5.16) (D)</td></tr>
</table>

POINT

Analog input allowed for maximum resolution and overall accuracy is from –10 to 0 to 10 V or from –20 to 0 to 20 mA

3.3 I/O Conversion Characteristics

Input/output (hereafter I/O) conversion characteristics are expressed by the angle of the line connecting the offset value and gain value used to convert the analog signals, input to the PC CPU, into digital values. This is shown in Figure 3.1 below.

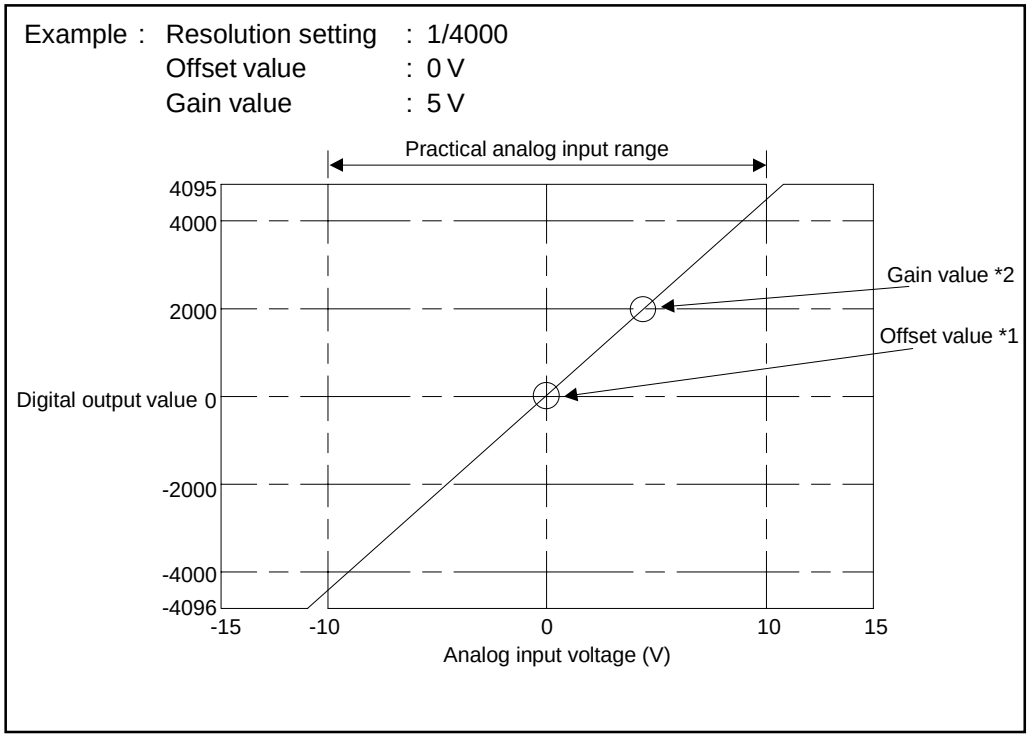


Fig.3.1 I/O Conversion Characteristics

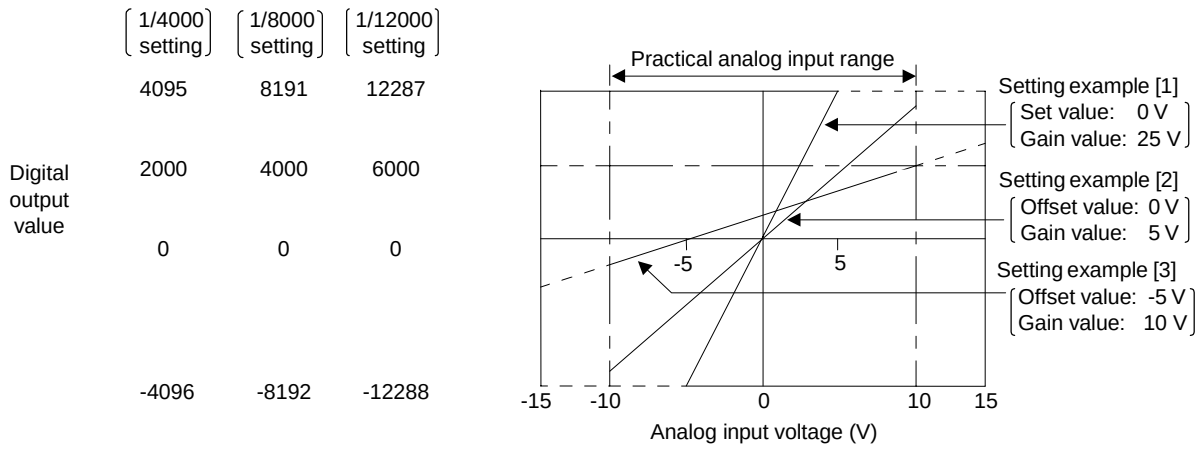
*1 Analog input value (voltage or current) corresponding to the digital output value of "0"

*2 Analog input value (voltage or current) corresponding to the following digital output values:

2000 with resolution setting of 1/4000
4000 with resolution setting of 1/8000
6000 with resolution setting of 1/12000

3.3.1 Voltage input characteristics

Figure 3.2 shows the voltage input characteristics for three different offset/gain combinations.



Setting Example No.	Offset Value	Gain value	Digital Output Value with +3 V Analog Input			Digital Output Value with -3 V Analog Input		
			1/4000 Setting	1/8000 Setting	1/12000 Setting	1/4000 Setting	1/8000 Setting	1/12000 Setting
1	0 V	2.5 V	2400	4800	7200	-2400	-4800	-7200
2	0 V	5 V	1200	2400	3600	-1200	-2400	-3600
3	-5 V	10 V	1066	2132	3198	266	532	798

Figure 3.2 Voltage Input Characteristics

POINTS

(1) If the input voltage is in the range of -10 to 0 to 10 V, the maximum resolution and overall accuracy are within the range of performance specifications. However, if the input voltage exceeds this range, resolution and accuracy will be impaired

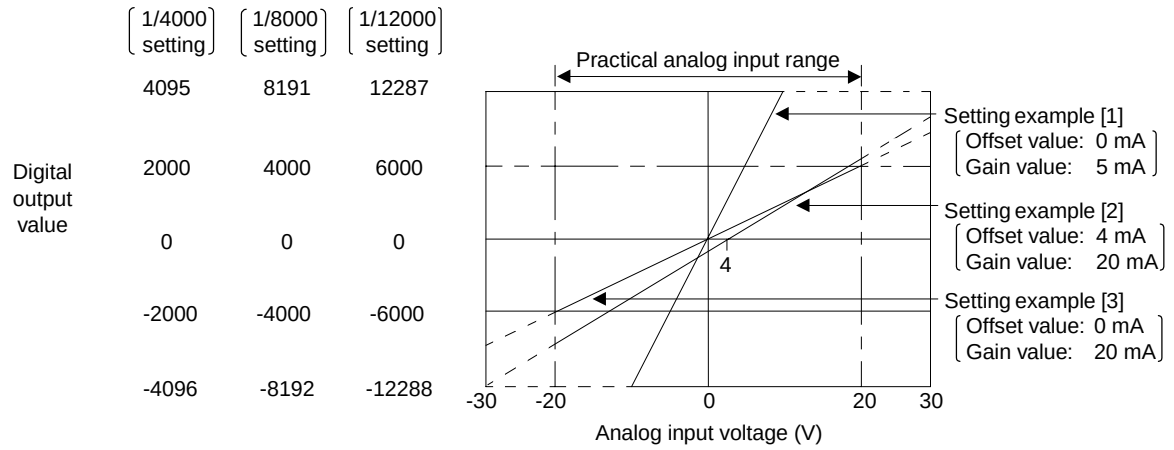
(2) Inputting an analog voltage that causes the digital output value to exceed the maximum value (4095/8191/12287) or to become smaller than the minimum value (-4096/-8192/-12288), locks the result of the A-D conversion (digital output value) at either the maximum value (4095/8191/12287) or the minimum value (-4096/-8192/-12288).

(3) Do not apply ± 15 V or more. This will damage the module.

(4) When setting the gain or offset, the following must be satisfied:
(Gain value) – (Offset value) ≥ 1 V (1/4000 setting)/1.5 V (1/8000 setting)/2 V (1/12000 setting)
If the set values do not satisfy the relationship stated above, the obtained digital output values will not be correct.

3.3.2 Current input characteristics

Figure 3.3 shows the voltage input characteristics for three different offset/gain combinations



Setting Example No.	Offset Value	Gain value	Digital Output Value with +7 mA Analog Input			Digital Output Value with -3 mA Analog Input		
			1/4000 Setting	1/8000 Setting	1/12000 Setting	1/4000 Setting	1/8000 Setting	1/12000 Setting
1	0 mA	5 mA	2800	5600	8400	-1200	-2400	-3600
2	4 mA	20 mA	374	748	1122	-874	-1748	-2622
3	0 mA	20 mA	700	1400	2100	-300	-600	-900

Figure 3.3 Current Input Characteristics

POINTS

(1) When the input voltage is in the range from -20 to 0 to +20 mA, the maximum resolution and overall accuracy are within the range of performance specifications. However, if input current exceeds this range, resolution and accuracy will be impaired

(2) Inputting an analog current that causes the digital output value to exceed the maximum value (4095/8191/12287) or to become smaller than the minimum value (-4096/-8192/-12288), locks the result of the A-D conversion (digital output value) at either the maximum value (4095/8191/12287) or the minimum value (-4096/8192/-12288).

(3) Do not apply ± 30 mA or more. This will damage the module.

(4) When setting the gain or offset, the following must be satisfied:
(Gain value) – (Offset value) ≥ 4 mA (1/4000 setting)/6 mA (1/8000 setting)/8 mA (1/12000 setting)
If the set values do not satisfy the relationship stated above, the obtained digital output values will not be correct.

3.3.3 Relationship between the offset/gain setting and the digital output values

(1) Resolution

Resolution is obtained using the following expression:

- Voltage input

$$\text{Resolution} = \frac{(\text{Gain value}) - (\text{Offset value})}{2000\ (\text{for 1/4000 setting})/4000\ (\text{for 1/8000 setting})/6000\ (\text{for 1/12000}} \times 1000\ (\text{mV})$$

- Current input

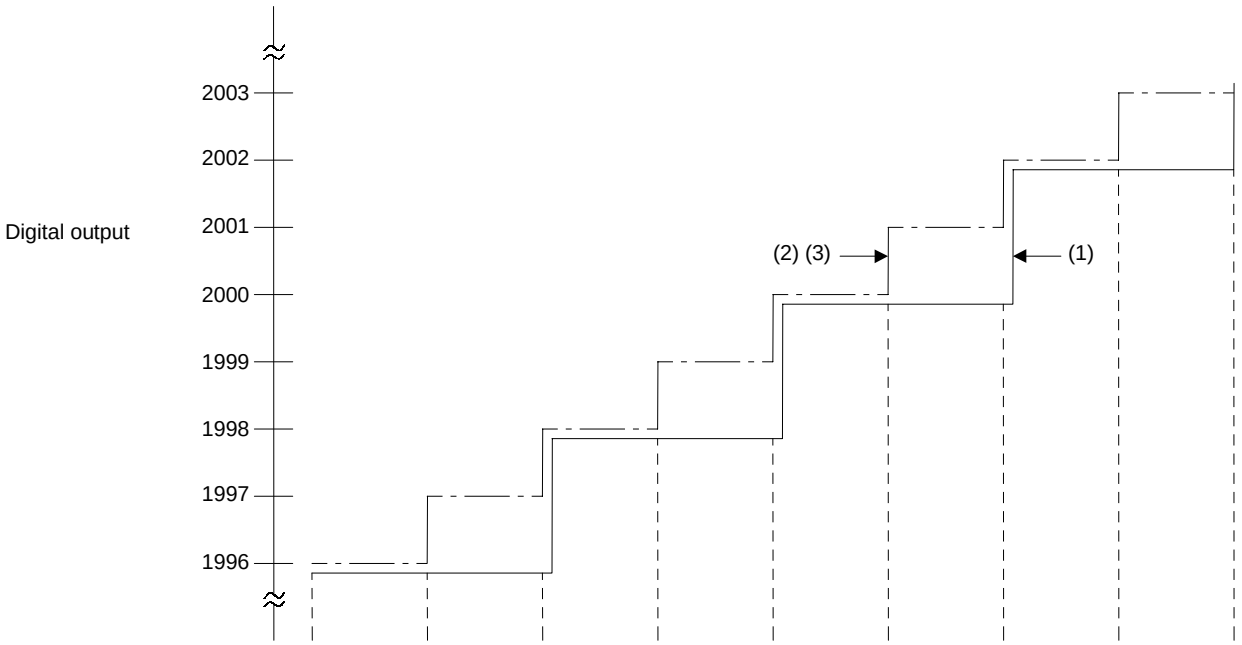
$$\text{Resolution} = \frac{(\text{Gain value}) - (\text{Offset value})}{2000\ (\text{for 1/4000 setting})/4000\ (\text{for 1/8000 setting})/6000\ (\text{for}} \times 1000\ (\mu\text{A})$$

(2) Relationship between the maximum resolution and the digital output value

If the setting of offset/gain values causes the following, the digital value does not change in increments of "1".

$$\frac{(\text{Gain value}) - (\text{Offset value})}{2000\ /4000\ /8000} < (\text{Maximum resolution})$$

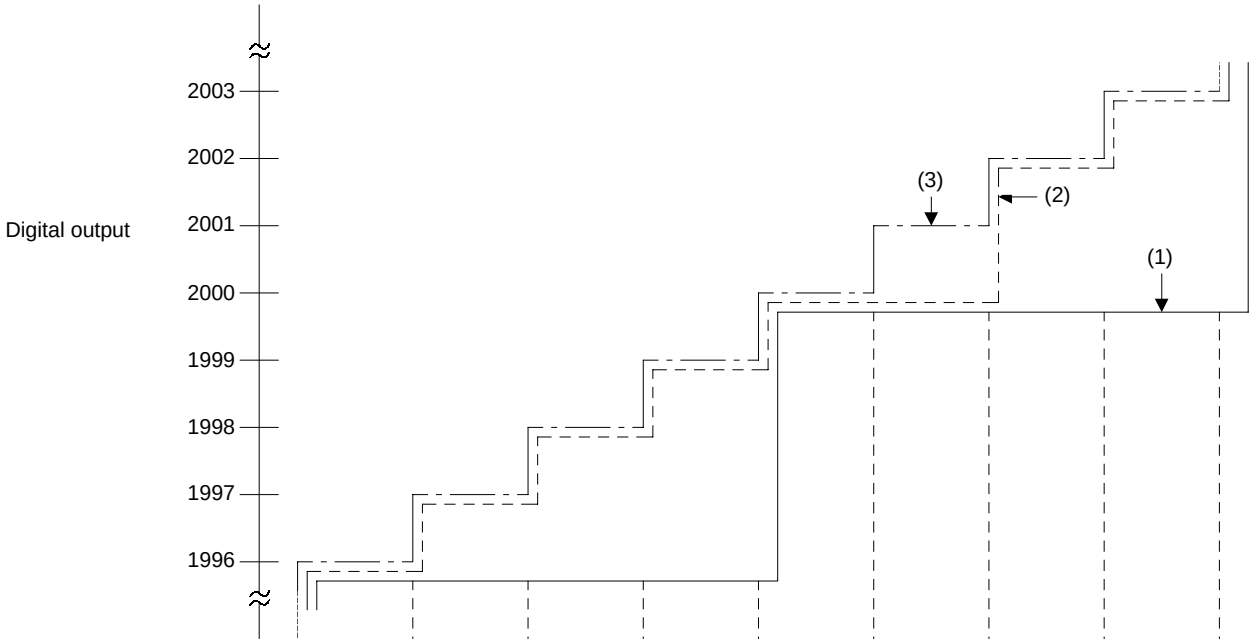
Figures 3.4 and 3.5 show the relationship between the offset/gain settings and the digital output values.
The offset and gain values in these figures are those in the voltage and current input characteristics figures in Sections 3.3.1 and 3.3.2.



No.	Offset Value	Gain Value	Reso-lution	Analog InputValue (V)							
1	0 V	2.5 V	1/4000	2.4950 to 2.4975		2.4975 to 2.5000		2.5000 to 2.5025		2.5025 to 2.5050	
			1/8000	1.2475 to 1.2488		1.2488 to 1.2500		1.2500 to 1.2513		1.2513 to 1.2525	
			1/12000	0.8317 to 0.8325		0.8325 to 0.8334		0.8334 to 0.8342		0.8342 to 0.8350	
2	0 V	5 V	1/4000	4.9900 to 4.9925	4.9925 to 4.9950	4.9950 to 4.9975	4.9975 to 5.0000	5.0000 to 5.0025	5.0025 to 5.0050	5.0050 to 5.0075	5.0075 to 5.0100
			1/8000	2.4950 to 2.4936	2.4936 to 2.4975	2.4975 to 2.4988	2.4988 to 2.5000	2.5000 to 2.5013	2.5013 to 2.5025	2.5025 to 2.5038	2.5038 to 2.5050
			1/12000	1.6634 to 1.6642	1.6642 to 1.6650	1.6650 to 1.6659	1.6659 to 1.6667	1.6667 to 1.6675	1.6675 to 1.6684	1.6684 to 1.6692	1.6692 to 1.6700
3	–5 V	10 V	1/4000	9.9700 to 9.9755	9.9755 to 9.9850	9.9980 to 9.9925	9.9925 to 10.0000	10.0000 to 10.0075	10.0075 to 10.0150	10.0150 to 10.0225	10.0225 to 10.0300
			1/8000	4.9850 to 4.98888	4.9888 to 4.9925	4.9925 to 4.9963	4.9963 to 5.0000	5.0000 to 5.0038	5.0038 to 5.0075	5.0075 to 5.0113	5.0113 to 5.0150
			1/12000	3.3234 to 3.3259	3.3259 to 3.3284	3.3284 to 3.3309	3.3334 to 3.3359	3.3359 to 3.3384	3.3359 to 3.3384	3.3384 to 3.3409	3.3409 to 3.3434

* With the gain and offset setting as in No. 1, the digital output values do not change in increments of "1" because the maximum resolution (see Section 3.2) is exceeded.

Figure 3.4 Voltage Input and Digital Output Values



No.	Offset Value	Gain Value	Reso-lution	Analog Input Value (mA)							
1	0 mA	5 mA	1/4000	4.9900 to 5.0000				5.0000 to 5.0100			
			1/8000	2.4950 to 2.5000				2.5000 to 2.5050			
			1/12000	1.6634 to 1.6667				1.6667 to 1.6700			
2	4 mA	20 mA	1/4000	19.9680 to 19.9760	19.9970 to 19.9840	19.9840 to 19.9920	19.9920 to 20.0000	20.0000 to 20.0160		20.0160 to 20.0240	20.0240 to 20.0320
			1/8000	9.9840 to 9.9880	9.9980 to 9.9920	9.9920 to 9.9960	9.9960 to 1.0000	10.0000 to 10.0080		10.0080 to 10.0120	10.0120 to 10.0160
			1/12000	6.6560 to 6.6587	6.6587 to 6.6614	6.6614 to 6.6640	6.6640 to 6.6667	6.6667 to 6.6720		6.6720 to 6.6747	6.6747 to 6.6774
3	0 mA	20 mA	1/4000	19.9600 to 19.9700	19.9700 to 19.9800	19.9800 to 19.9900	19.9900 to 20.0000	20.0000 to 20.0100	20.0100 to 20.0200	20.0200 to 20.0300	20.0300 to 20.0400
			1/8000	9.9980 to 9.9985	9.9985 to 9.9900	9.9900 to 9.9950	9.9950 to 10.0000	10.0000 to 10.0050	10.0050 to 10.0100	10.0100 to 10.0150	10.0150 to 10.0200
			1/12000	6.6534 to 6.6567	6.6567 to 6.6600	6.6600 to 6.6634	6.6634 to 6.6677	6.6667 to 6.6700	6.6700 to 6.6734	6.6734 to 6.6767	6.6767 to 6.6800

* With the gain and offset setting as in No. 1 and No. 2, the digital output values do not change in increments of "1" because the maximum resolution (see Section 3.2) is exceeded.

Figure 3.5 Current Input and Digital Output values

3.4 Functions

Table 3.1 A68ADN Functions

Item	Descriptions	Section Ref.
A-D conversion enable/disable setting	• Enable/disable setting is possible for each individual channel. (Default: Enable for all channels) • Sampling time can be shortened by setting "disable" for the unused channels.	3.7.1
Offset/gain setting	• Offset/gain setting is possible for each individual channel without a volume dial to change I/O conversion characteristics.	3.3
Averaging processing designation	• By designating the number of frequencies or time duration for each channel, A-D conversion data is averaged and the result is set to buffer memory as the digital output value.	3.7.2

3.5 Maximum Conversion Speed

Conversion speed is the period of time between channel switching and the writing of the digital value to buffer memory.

3.5.1 Conversion speed per channel

Conversion speed per channel is 20 ms.

If more than one channel is used, the sampling time will be "(20 ms) × (number of conversion-enabled channels)".

3.5.2 Influence of [FROM]/[TO] instruction executions on maximum conversion speed.

The maximum conversion speed indicated in 3.5.1 assumes that the [FROM]/[TO] instruction is not executed. If the [FROM]/[TO] instruction is executed:

(1) Digital value write to the buffer memory is suspended during [FROM]/[TO] processing until the [FROM]/[TO] processing is completed.

(2) Channel switching is suspended during [FROM]/[TO] processing until [FROM]/[TO] processing is completed.

(3) [FROM]/[TO] processing is suspended during digital value write to the buffer memory or channel switching until the write or channel switching process is completed.

(4) The [FROM]/[TO] instruction should be specified to transfer more than one data simultaneously. Processing is less influenced if the number of [FROM]/[TO] instructions is smaller.

3.6 I/O List for PC CPU

The A68ADN uses 32 input and 32 output device points for data communications with the PC CPU. I/O signal assignment and functions are shown in Table 5.1.

Device X indicates an input signal from the A68ADN to the PC CPU and device Y an output signal from the PC CPU to the A68ADN. I/O numbers (X, Y) and I/O addresses used in this manual assume that the A68ADN is located at slot 0 of the main base unit.

Table 3.2 I/O Signals

Signal Direction (A68ADN to PC CPU)		Signal Direction (PC CPU to A68ADN)	
Device No.	**Signal Name**	**Device No.**	**Signal Name**
X0	Watchdog timer error (Detected by A68ADN)	Y0 to YC	Unavailable
X1	A – D conversion ready		
X2	Error flag		
X3 to X1C	Unavailable	YD to YF	[RFRP] [RTOP] instruction interlock signals Only used when the A68ADN is used in a remote I/O station
		Y10 Y11	Unavailable
		Y12	Error reset
X1D to X1F	[RFRP] [RTOP] instruction interlock signals Only employed when the A68ADN is used in a remote I/O station	Y13 to Y1F	Unavailable

POINT

Outputs Y0 to YC, Y10 to Y11, and Y13 to Y1F are reserved. They cannot be used in the sequence program.
Y0 to Y1F (corresponding to X0 to X1F) cannot be used as internal relays.

(1) Watchdog timer error (X0)

The X0 signal goes ON when the A68ADN (using the self-diagnosis function) detects a watchdog timer error.

When a watchdog timer error occurs, the A68ADN stops A-D conversion.

A watchdog timer error indicates faulty A68ADN hardware.

(2) A – D conversion ready (X1)

The X1 signal goes ON when A-D conversion processing is ready in a normal (other than test) mode when the power supply to the PC CPU goes ON or the PC CPU is reset.

The signal goes OFF when the test terminals on the front panel are shorted.

This signal can be used as an interlock for buffer memory read/write operations.

REMARK

Definition of A-D conversion-ready status: When A-D conversion is completed in all eight channels and the digital output values are stored in buffer memory.

IMPORTANT

A FROM/TO instruction cannot be executed in the test mode. Use the D/A conversion ready signal (X1) as an interlock for any program that contains a FROM/TO instruction.
If a FROM/TO instruction is executed in the test mode, the preset offset and/or gain value might be lost, or a CPU error may occur causing the calculation to stop.

(3) Error flag (X2)

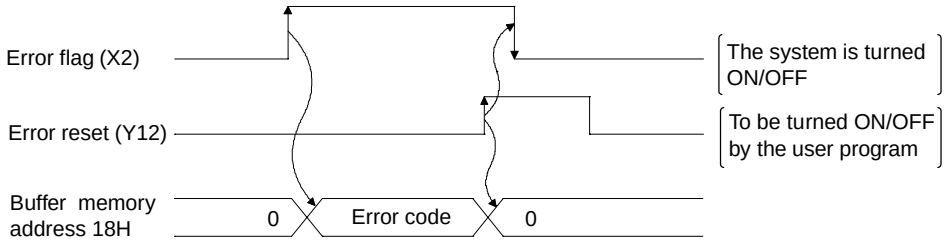
The X2 signal goes ON when an error (other than a watchdog timer error) is detected by the A68ADN. When the X2 signal is turned ON, an error code is stored in the error code storage area in buffer memory.

The signal goes OFF when the error reset signal (Y12) is turned ON.

(4) Error reset (Y12)

Turning Y12 ON causes the error flag (X2) to go OFF and writes "0" to the error code storing area (address 18H) in buffer memory, after clearing the error code stored there.

The RUN LED, which flashes on the front panel after an error is detected, stops flashing when the Y12 signal is turned ON (which indicates "normal operation").



3.7 Buffer Memory

The A68ADN uses the buffer memory (not battery-backed) for data communications with a PC CPU.

Buffer memory allocations are shown below.

Address (decimal)		Default value	
0	A-D conversion-enabled/disabled setting	00FFH (all channels enabled)	..... See section 3.7.1
1	Averaging processing specification	0 (sampling processing for all channels)	..... See section 3.7.2
2	CH1 averaging time, count	0	.....
3	CH2 averaging time, count		
4	CH3 averaging time, count		
5	CH4 averaging time, count		
6	CH5 averaging time, count		
7	CH6 averaging time, count		
8	CH7 averaging time, count		
9	CH8 averaging time, count		
10	CH1 digital output value	0	..... See section 3.7.3
11	CH2 digital output value		
12	CH3 digital output value		
13	CH4 digital output value		
14	CH5 digital output value		
15	CH6 digital output value		
16	CH7 digital output value		
17	CH8 digital output value		
18	Write data error code	0 (no error)	..... See section 3.7.4
19	A-D conversion-completion flag	00FFH (A-D conversion completed for all channels)	..... See section 3.7.5
20	Resolution setting	1 (1/4000)	..... See section 3.7.6

POINT

Since buffer memory addresses 10 to 17 are reserved for read only, data should not be written to them using a sequence program. If an attempt is made to write data to these addresses, the RUN LED begins flashing and an error code is stored in buffer memory address 18.

3.7.1 A-D conversion-enabled/disabled setting

Whether A-D conversion is to be executed or not is written to buffer memory address 0 for each channel ("1" for enable and "0" for disable).

The sampling cycle can be shortened by setting "disable" for the unused channels The default value for each channel is set as an A-D conversion.

Examples:

(1) Sampling cycle time when "enable" is set for all channels:

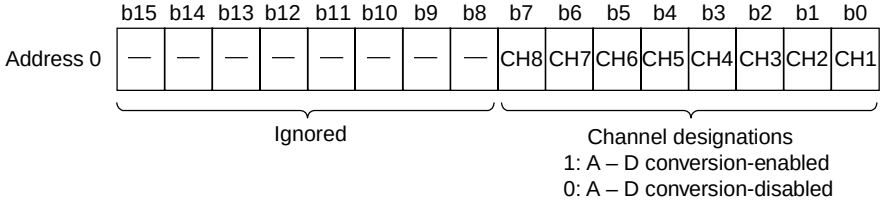
(number of enabled channels) 8 × (conversion speed per channel) 20 ms = 160 ms

(2) Sampling cycle time when "enable" is set for channels 1 and 3:

(number of enabled channels) 2 × (conversion speed per channel) 20 ms = 40 ms

(1) Enable/disable setting method

Enable or disable is set for each channel.



(2) Processing by the A68ADN for enable/disable setting

(a) Initialization for averaging processing

For averaging processing, the data stored in the work area by the A68ADN system software is initialized.

The data stored in buffer memory prior to the setting of enable/disable consists of digital values.

If conversion-enabled/disabled setting is made when 30 sampling times have been completed at a channel which is set for 50 averaging processing times, the sampling data collected in the 30 sampling times is cleared and averaging processing is executed from the beginning.

(b) Resetting the A – D conversion-completion flag

The A – D conversion-completion flag (address 19 in buffer memory) for channels 1 to 8 is reset.

3.7.2 Setting for sampling processing/averaging processing

(1) Digital value output in sampling processing and averaging processing

(a) Sampling processing

The analog values input to the channels are converted 1:1 to digital output values. These digital output values are then stored in buffer memory.

(b) Averaging processing

The A68ADN does the A-D conversion for any channels which the PC CPU has specified for averaging processing. Using a preset count or a preset period of time, an average is calculated (excluding the minimum and maximum values) and stored in buffer memory. If the specified processing count is two or less, sampling processing is executed instead of averaging processing.

When A-D conversion-enabled/disabled setting is made, data stored in the work area is initialized.

POINTS

(1) When sampling processing is designated:
As the A68ADN's PC CPU scans each channel, the value appearing at that instant is written to the buffer memory as a digital value. The timing of this sampling depends on the number of A-D conversion-enabled channels, and may be found by using the following formula:

(processing time) =
(number of A – D conversion – enabled channels) × 20 (ms/1 channel)
↑ Maximum conversion speed

Example: When conversion-enabled is set for channels 1, 2, 3, 5, and 6:
Processing time = 5 × 20 = 100 (ms)

(2) Averaging processing by specifying time

(a) The setting time is in 10 ms units. Values less than 10 ms are rounded down.

Example: If 1234 ms is set, it is processed as 1230 ms.

(b) The number of times set time processing is done varies with the number of A-D conversion-enabled channels.

$$\text{Processing count} = \frac{\text{Time setting}}{(\text{number of A – D conversion-enabled channels}) \times 20\ (\text{ms/channel})}$$

Maximum conversion speed

Example: Number of A-D conversion-enabled channels = 4, Time setting = 8000 ms
8000 ÷ (4 × 20) = 100 times

(3) Averaging processing by specifying a number of counts
The time in which the average value by this processing is stored in the buffer memory varies with the number of A-D conversion-enabled channels.

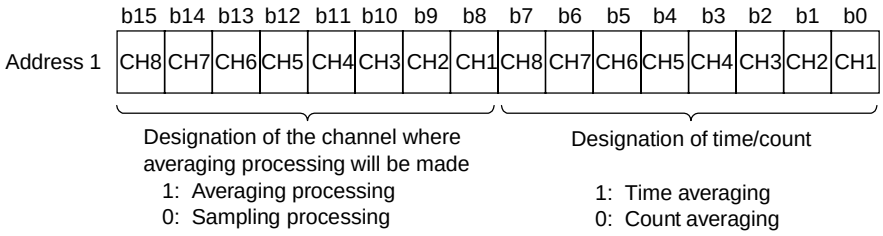
Processing time = (count setting) × (A-D conversion-enabled channels × 20 (ms/channel)
↑ Maximum conversion speed

Example: When A-D conversion-enabled is set for channels 1, 2, 3 and 4
50 × 4 × 20 = 4000 (ms)

(2) Designation of averaging processing and selection between time averaging and count averaging

(a) When the power is turned ON and the A68ADN A-D conversion-ready signal is ON, all channels are set for sampling processing.

(b) For selection of sampling processing or averaging processing, use address 1 of the buffer memory.



POINTS

(1) For averaging processing, "count" or "time" must be set in advance.
(2) When averaging processing is not designated, sampling processing is set without regard to the designation of time/count.

(3) Setting "time" or "count"

(a) For the channels designated for averaging processing, write the "time" or "count" to the buffer memory addresses (2 to 9) corresponding to those channels.

When the power is turned ON, the setting for "time" and "count" is "0".

(b) The setting ranges are as indicated below:

"Count" averaging processing: 1 to 500 times

"Time" averaging processing: 160 to 10000 ms

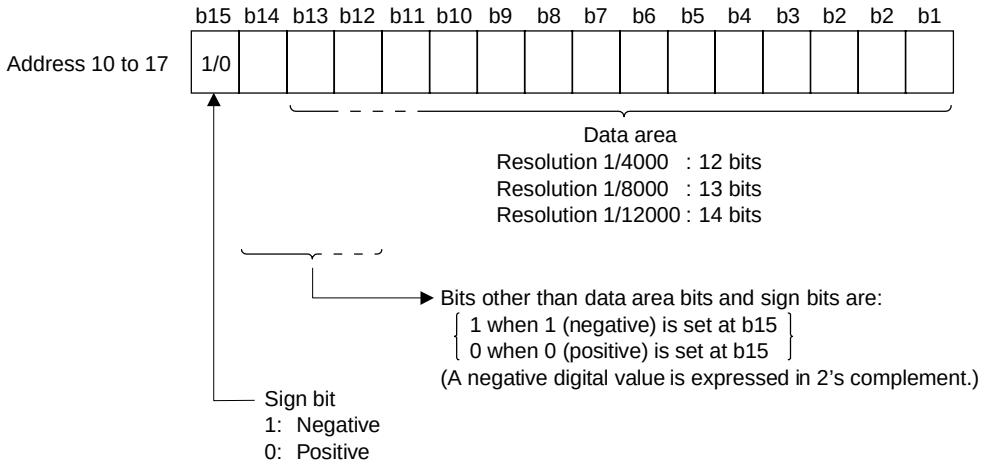
POINT

If a value outside the above ranges is written, a setting error occurs and the set value in buffer memory does not change. However, the A68ADN performs A – D conversion processing based on the averaging time or count previously set.

3.7.3 Digital output values

Digital values after A – D conversion are stored to buffer memory addresses 10 to 17 for each channel.

Digital output values are 16-bit, singed binary. The ranges vary depending on the resolution setting, as indicated below:



3.7.4 Write data error code

(1) When data is written to the A68ADN from the PC CPU, data range checks and read/write area access checks are only made once. If the written data is outside the designated range, an error code is stored (as a 16-bit binary value) in buffer memory address 18.

Section 6.1 gives error code details.

(2) If more than one type of error occurs, only the error code of the first error is stored in the A68ADN.

(3) To reset the error code, use the sequence program to turn Y12 ON (see Section 5.1).

(4) When an error is reset, the data error code is set to 0 and the RUN LED of the A68ADN stops flashing

3.7.5 A-D conversion-completion flag

(1) When the power is turned ON, the A – D conversion-ready signal (X1) goes ON This indicates that the A – D conversion-completion flag is ready for all channels from 1 to 8. OOFFH is stored in buffer memory.

(2) After the power is turned ON, A/D conversion-completion flag processing is only done once if the setting for A – D conversion-enabled/disabled at address 0 is changed.

- A – D conversion-disabled → enabled:

  When averaging processing is specified, averaging processing is executed a preset number of times or for a preset length of time of averaging. After the processing is completed, the digital value (obtained after A-D conversion) is then stored in buffer memory. The flag is then set to 1.

- A – D conversion-enabled → disabled:

  The relevant channel's A – D conversion-completion flag is set to 0.

(3) Each channel has an A-D conversion-completion flag.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Address 0	0	0	0	0	0	0	0	0	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

A – D conversion-completion flag
1: A – D conversion completed
0: A – D conversion not completed

(4) The A/D conversion-completion flag can be used for the interlock when reading the digital value of the channel for which averaging processing has been executed.

3.7.6 Setting resolution

(1) Set the digital output value resolution to "1/4000", "1/8000", or "1/12000". When the power is turned ON, the default is set at 1/4000.

(2) Write a number (1 to 3) to address 20 corresponding to the required resolution.

Setting	Resolution
1	1/4000
2	1/8000
3	1/12000

POINT

Only set the resolution once while the PC CPU is running and before the A-D conversion-enabled/disabled setting is made.
If the setting is changed while the A-D conversion is set for enabled, the correct digital output values will not be obtained.

4. PRE-OPERATION SETTINGS AND PROCEDURES

4.1 Handling Instructions

(1) Protect the A68ADN and the terminal block from impacts.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards.

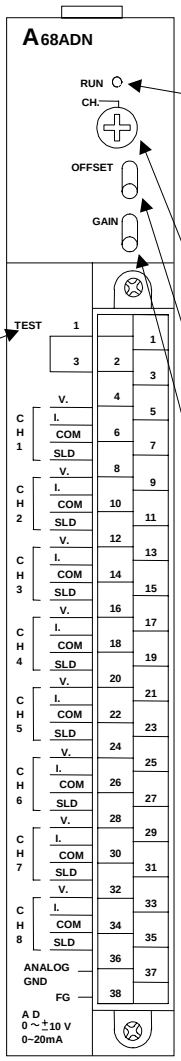
(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten terminal screws as specified below:

Screw	TighteningTorque Range (kg·cm) (lb·inch)
I/O terminal block terminal screws (M3)	5 (4.33) to 8 (6.93)
I/O terminal block installation screws (M4)	8 (6.93) to 14 (12.13)

(5) To load the module onto the base, press the module against the base so that the hook is securely locked. To unload the module, push the catch on top of the module, and, after the hook is disengaged from the base, pull the module toward you.

4.2 Nomenclature



Test mode terminals

Prior to offset/gain setting, connect terminals 1 and 3 together.

RUN LED

Indicates the operating status of the A68ADN.
(Normal mode)
ON : During normal operation
Flashing : Write data error
OFF : 5V power OFF or watchdog timer error
(Test mode)
ON : When the OFFSET switch or the GAI switch is in the ON position.
OFF : When both the OFFSET switch and the GAIN switch are in the OFF position.

Channel select switch

Used to select a channel for offset and gain adjustment (No processing at positions 0 and 9.)

OFFSET switch

At the ON position, the analog input value is stored as the offset value.

GAIN switch

At the ON position, the analog input value is stored as the gain value.

Switches marked [ ] are valid only in the test mode. Section 4.3 gives details

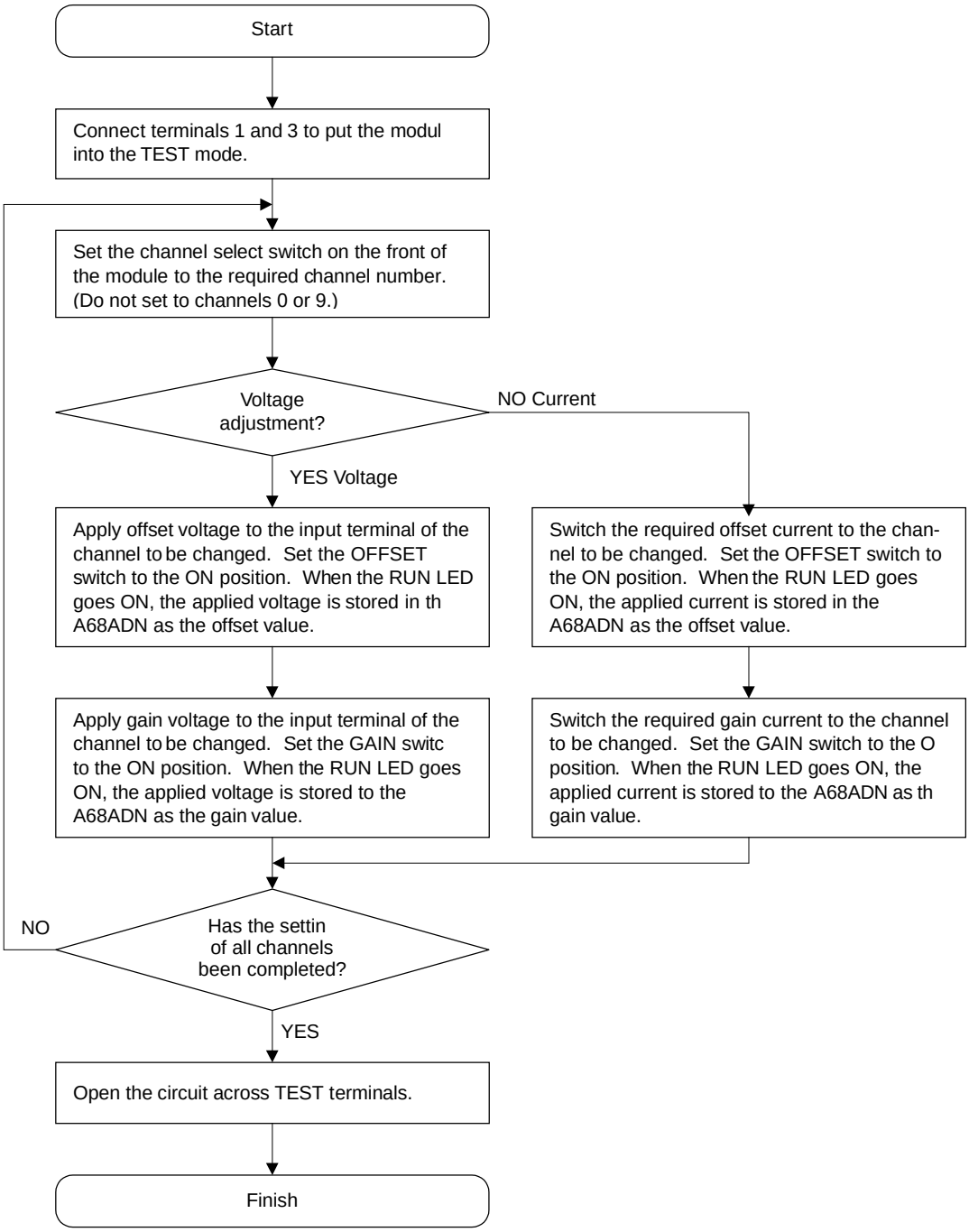
Terminal No.	Signal Name	Terminal No.	Signal Name	Terminal No.	Signal Name
1	TEST	13	CH3 V+	25	CH6 V+
2	Open	14	CH3 I+	26	CH6 I+
3	TEST	15	CH3 COM	27	CH6 COM
4	Open	16	CH3 SLD	28	CH6 SLD
5	CH1 V+	17	CH4 V+	29	CH7 V+
6	CH1 I+	18	CH4 I+	30	CH7 I+
7	CH1 COM	19	CH4 COM	31	CH7 COM
8	CH1 SLD	20	CH4 SLD	32	CH7 SLD
9	CH2 V+	21	CH5 V+	33	CH8 V+
10	CH2 I+	22	CH5 I+	34	CH8 I+
11	CH2 COM	23	CH5 COM	35	CH8 COM
12	CH2 SLD	24	CH5 SLD	36	CH8 SLD
				37	ANALOG GND
				38	FG

4.3 Offset/Gain Settings

To change the I/O characteristics, follow the chart below.

The factory settings are:

Voltage input ..... Offset value : 0 V
Gain value : 5 V
Current input ..... Offset value : 0 mA
Gain value : 20 mA



POINTS

(1) Set the offset and gain values under conditions of actual use.
(2) The offset and gain values are stored in the A68ADN and are not erased if the power is turned OFF.
(3) Do offset/gain setting with the PC CPU in the stop mode. If the module is set to the test mode, A-D conversion is stopped on all channels Therefore, use the A-D conversion ready signal as an interlock.
(4) Perform the offset/gain setting within the range of -10 to 0 to 10 VDC or –20 to 0 to 20 mA. If set outside these ranges, maximum resolution and overall accuracy may not be within the ranges specified.
(5) If grounding at the point marked with *5 described in Section 4.4.2 (no ground—ground, or ground—removal), redo offset/gain setting from the first step.

4.4 Wiring

4.4.1 Wiring instructions

Take the following precautions to protect external wiring from noise:

(1) Separate the AC and DC wiring.

(2) Separate the main circuit and/or high voltage wiring from the control and signal wiring.

(3) When applicable, ground the shielding of all wires to a common ground point.

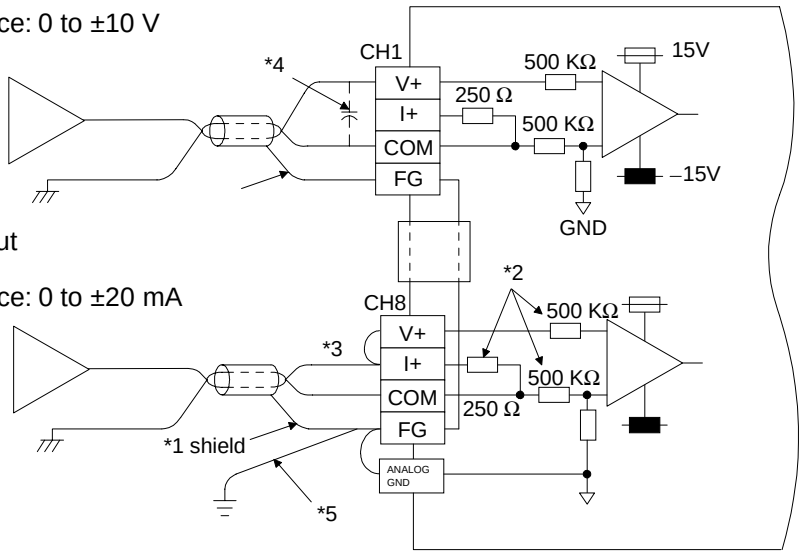
4.4.2 Module connection example

(1) Voltage input

Signal source: 0 to ±10 V

(2) Current input

Signal source: 0 to ±20 mA



*1: For the cable, use a two-core twisted shielded wire.

*2: Indicates the input resistance of the A68ADN.

*3: For current input, make sure to connect the terminals (V+) and (I+).

*4: If noise or ripple is generated at the external wiring, connect a capacitor of approximately 0.1 to 0.47 μF25WV between terminals V and COM.

*5: If there is excessive noise, ground the module. If any change has been made in grounding method (ground/no ground) after offset/gain setting, redo the setting.

4.5 Inspection and Maintenance

The A68ADN module does not require special inspections after installation However, to ensure that the system operates at its best, the module should be checked following the instructions in the User's Manual for the particular PC CPU.

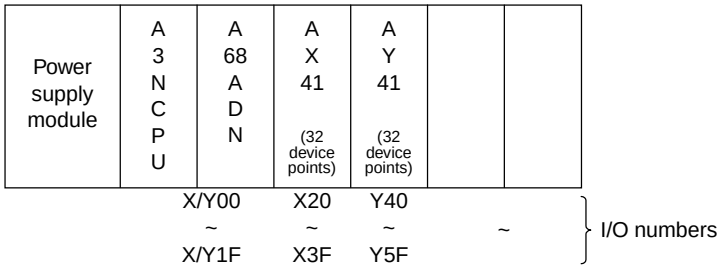
5. PROGRAMMING

Initial setting programs for using the A68ADN and digital output value read programs are explained below using sample programs.

5.1 Initial setting program and digital output value read program

[Sample Program Conditions]

(1) System configuration



(2) Initial setting

(a) A-D conversion-enabled channels.....Channels 1, 2, 3, and 5

(b) Averaging processing by count..... Channel 3 (setting: 50 times)

(c) Averaging processing by time.....Channel 2 (setting: 1000 ms)

(d) Resolution setting.....2 (1/8000)

(3) Devices to be used

(a) Initial setting write command input signal X20

(b) Write data error reset signal.....X21

(c) Digital output value read command input signal X22

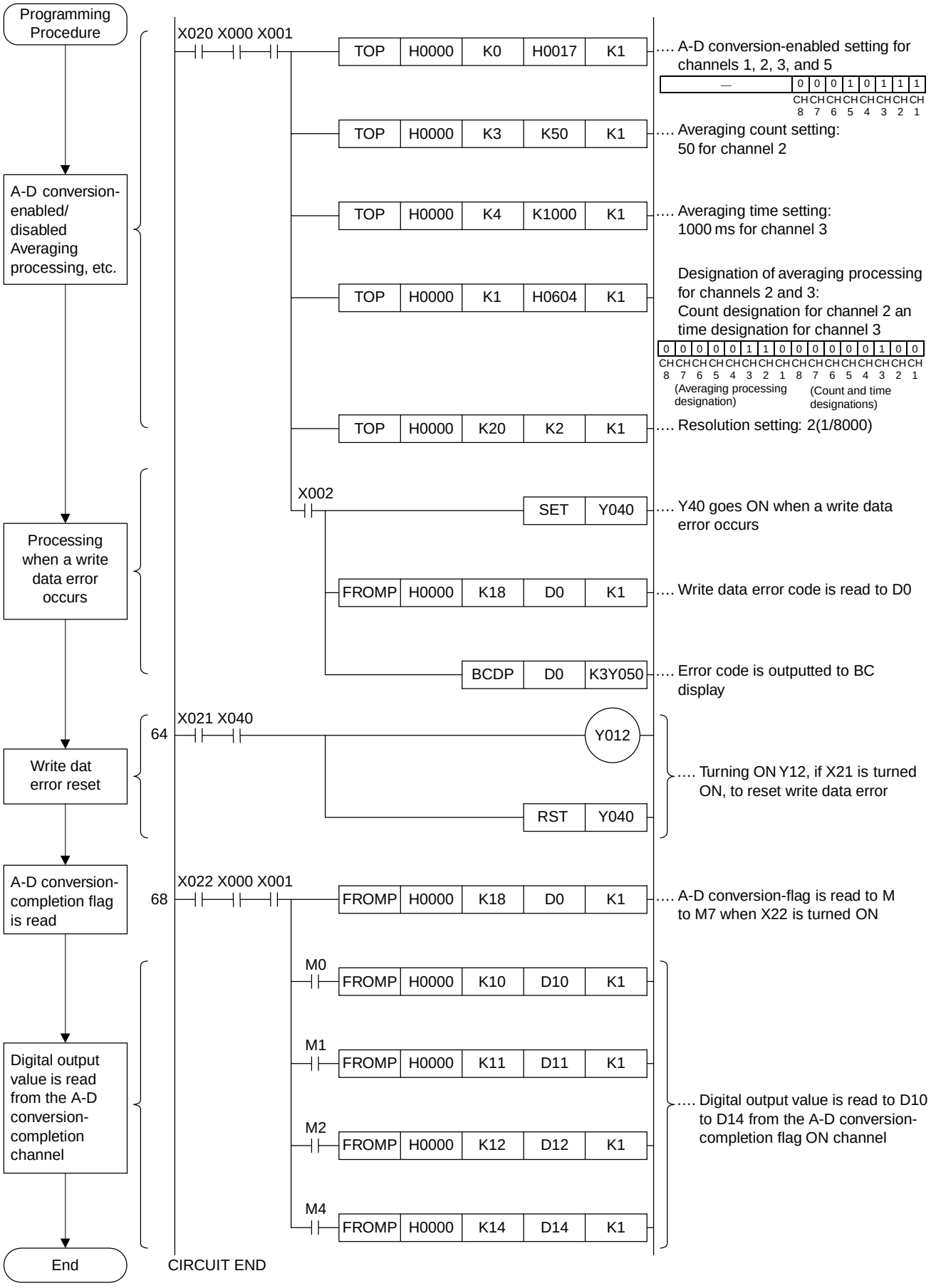
(d) Write data error occurrence external display Y40

(e) Write data error code BCD output.....Y50 to 5B

(f) Write data error code storage data register D0

(g) A-D conversion-completion flag storage devices ..... M0 to M7

(h) Digital output value read destination data registers .....D10 to D14


Programming Procedure
A-D conversion-enabled/ disabled Averaging processing, etc.
Processing when a write data error occurs
Write dat error reset
A-D conversion-completion flag is read
Digital output value is read from the A-D conversion-completion channel
End
X020 X000 X001
TOP H0000 K0 H0017 K1
.... A-D conversion-enabled setting for channels 1, 2, 3, and 5
— 0 0 0 1 0 1 1 1
CH8 CH7 CH6 CH5 CH4 CH3 CH2 CH1
TOP H0000 K3 K50 K1
.... Averaging count setting: 50 for channel 2
TOP H0000 K4 K1000 K1
.... Averaging time setting: 1000 ms for channel 3
TOP H0000 K1 H0604 K1
Designation of averaging processing for channels 2 and 3:
Count designation for channel 2 an time designation for channel 3
0 0 0 0 0 1 1 0 0 0 0 0 0 1 0 0
CH8 CH7 CH6 CH5 CH4 CH3 CH2 CH1 CH8 CH7 CH6 CH5 CH4 CH3 CH2 CH1
(Averaging processing designation)
(Count and time designations)
TOP H0000 K20 K2 K1
.... Resolution setting: 2(1/8000)
X002
SET Y040
.... Y40 goes ON when a write data error occurs
FROMP H0000 K18 D0 K1
.... Write data error code is read to D0
BCDP D0 K3Y050
.... Error code is outputted to BC display
64
X021 X040
Y012
RST Y040
.... Turning ON Y12, if X21 is turned ON, to reset write data error
68
X022 X000 X001
FROMP H0000 K18 D0 K1
.... A-D conversion-flag is read to M to M7 when X22 is turned ON
M0
FROMP H0000 K10 D10 K1
M1
FROMP H0000 K11 D11 K1
M2
FROMP H0000 K12 D12 K1
M4
FROMP H0000 K14 D14 K1
.... Digital output value is read to D10 to D14 from the A-D conversion-completion flag ON channel
CIRCUIT END

5.2 Sample programs when the A68ADN is loaded onto remote I/O station

[Precautions when writing programs]

(1) Data transmission/receive method

Data transmission/receive is made in the batch refresh mode after executing an END (FEND) instruction, even though the PC CPU I/O control mode is direct or refresh.

(2) Response delay

When transmitting/receiving control information between a master station P CPU and an A68ADN in a remote I/O station, a response delay is inevitable because control is made through a link module.

Pay attention to control timing.

(3) User instructions

The following instructions are used for data transmission/receive between a master station PC CPU and an A68ADN in a remote I/O station.

(a) Data write (master station → A68ADN): RTOP

(b) Data read (A68ADN → master station): RFRP

(4) Data transmission/receive device

Use link registers (W) for data transmission/receive between a master station PC CPU and an A68ADN in a remote I/O station.

Install the following program to the master station as needed:

(a) When writing data:

Transmit the data that is to be sent to the the remote I/O station A68ADN to the designated link register before executing an RTOP instruction.

(b) When reading data:

Transmit the link register data to another device before executing an RFRP instruction.

(5) Simultaneous execution of RTOP and RFRP instructions is not possible:

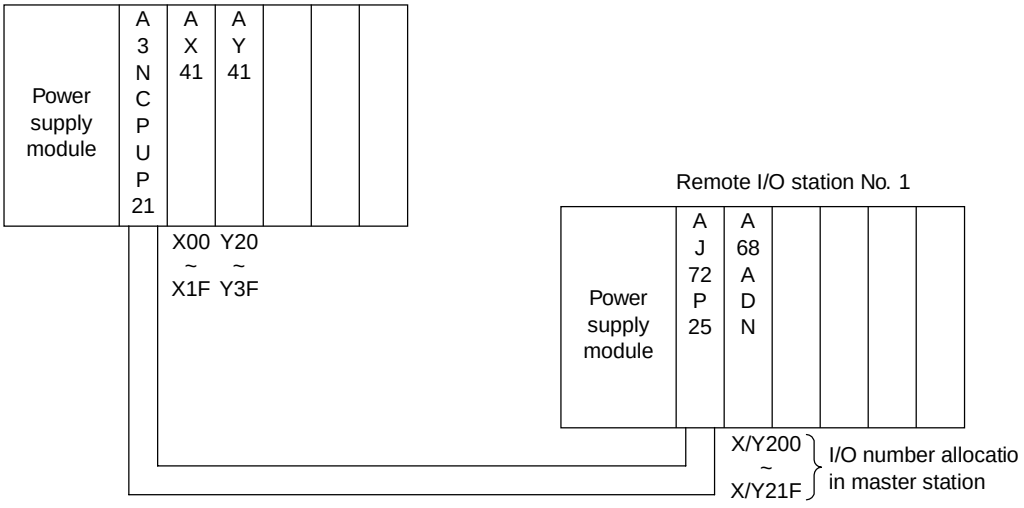
Simultaneous execution of an RTOP instruction and an RFRP instruction at the same time for the same A68ADN cannot be done. Therefore, the data link I/O signal must be added to the program as an interlock condition.

However, if two A68ADN modules are loaded in a remote I/O station, it is possible to execute an RTOP instruction for one A68ADN and an RFRP instruction for the other module at the same time.

(6) Control signals for the A68ADN

If the output signal (Y[ ][ ]) to a remote I/O station is PLS Y[ ][ ]), there are cases when it is not output to the A68ADN in accordance with the relationship between the master station scan time and the link scan time.

[Sample Program Conditions]



Because the data transmission/receive between a master station and remote I/O station is executed in the batch refresh mode after the execution of an END (FEND) instruction, a pulse output that uses an RST instruction after the execution of the SET instruction cannot be used.

[Sample Program Conditions]

(1) Initial setting

(a) A-D conversion-enabled channel ..... Channels 1, 2, 3, and 5

(b) Averaging processing by count ..... Channel 3 (setting: 50 times)

(c) Averaging processing by time ..... Channel 2 (setting: 1000 ms)

(d) Resolution setting 2 (1/8000)

(3) Devices to be used

(a) Intial setting write command input signal X0

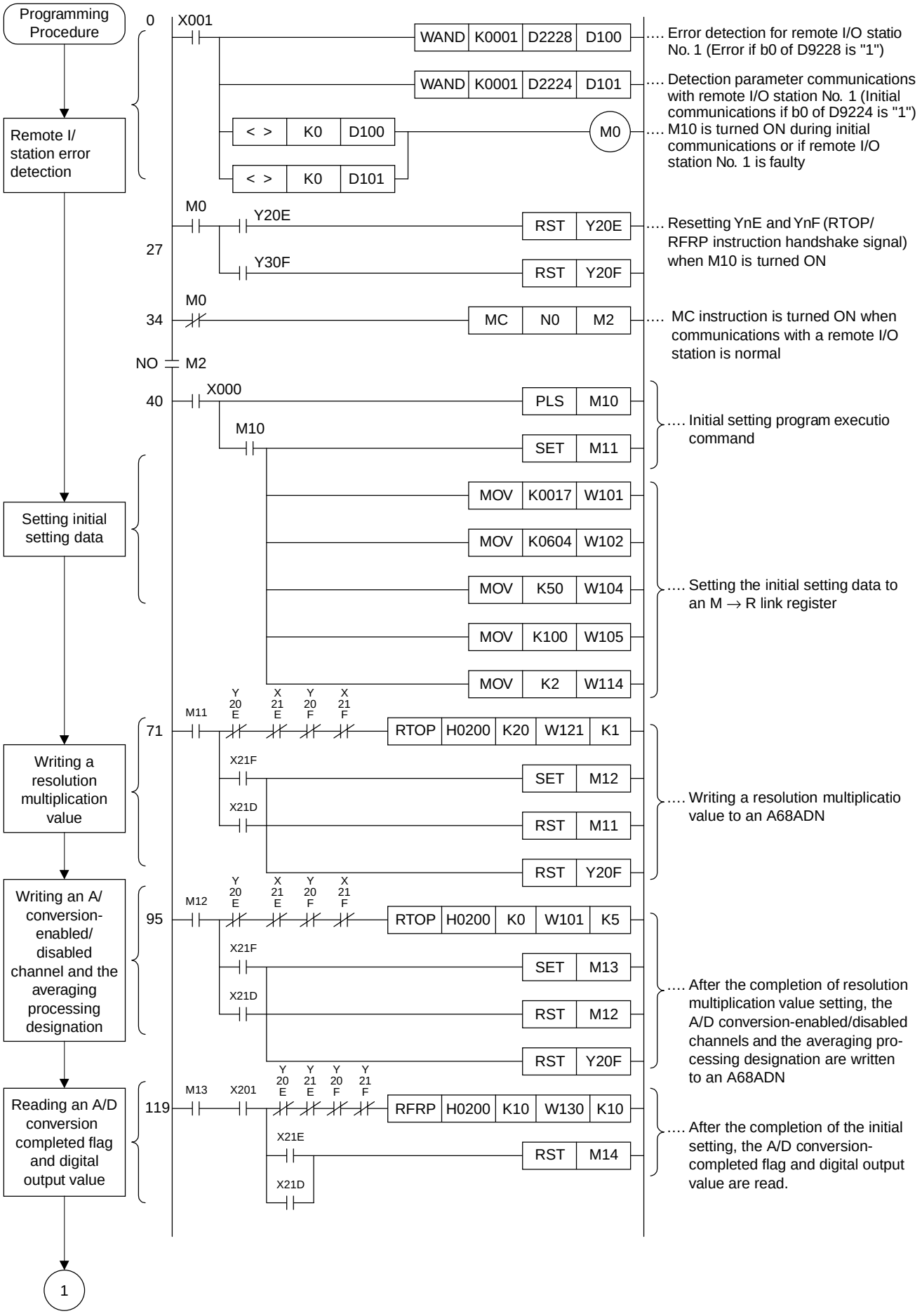
(b) Write data error reset signal X2

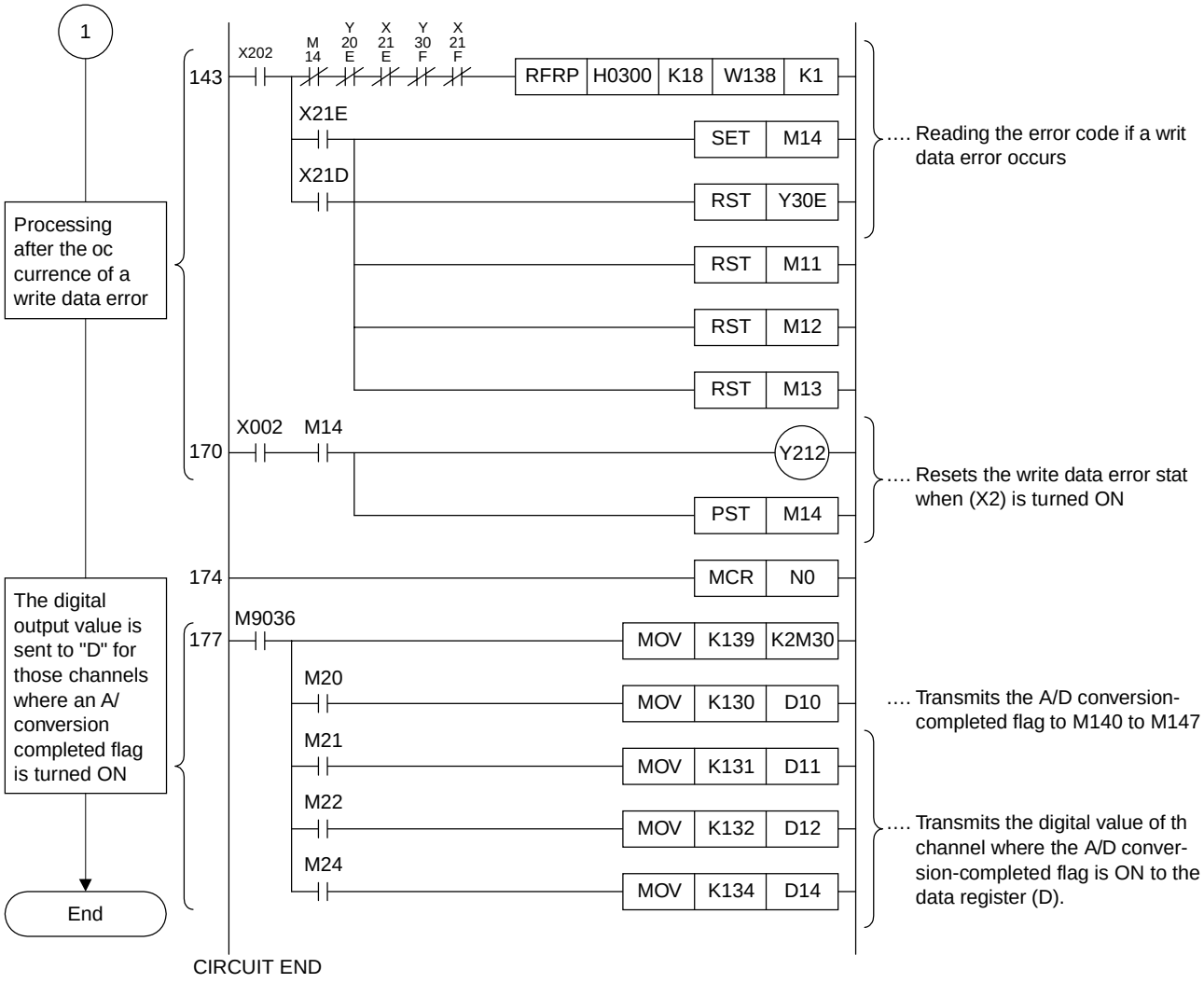
(c) Digital output value read command input signal X1

(d) Write data error flag Y20

(e) M → R link registers ..... W100 to W12F

(f) R → M link registers ..... W130 to W13F


Programming Procedure
Remote I/ station error detection
Setting initial setting data
Writing a resolution multiplication value
Writing an A/ conversion-enabled/ disabled channel and the averaging processing designation
Reading an A/D conversion completed flag and digital output value
1
0
X001
WAND K0001 D2228 D100
.... Error detection for remote I/O statio No. 1 (Error if b0 of D9228 is "1")
WAND K0001 D2224 D101
.... Detection parameter communications with remote I/O station No. 1 (Initial communications if b0 of D9224 is "1")
< > K0 D100
< > K0 D101
M0
.... M10 is turned ON during initial communications or if remote I/O station No. 1 is faulty
M0
Y20E
RST Y20E
27
Y30F
RST Y20F
.... Resetting YnE and YnF (RTOP/ RFRP instruction handshake signal) when M10 is turned ON
M0
34
MC N0 M2
.... MC instruction is turned ON when communications with a remote I/O station is normal
NO M2
X000
40
PLS M10
M10
SET M11
.... Initial setting program executio command
MOV K0017 W101
MOV K0604 W102
MOV K50 W104
MOV K100 W105
MOV K2 W114
.... Setting the initial setting data to an M → R link register
M11
Y20E X21E Y20F X21F
71
RTOP H0200 K20 W121 K1
X21F
SET M12
X21D
RST M11
RST Y20F
.... Writing a resolution multiplicatio value to an A68ADN
M12
Y20E X21E Y20F X21F
95
RTOP H0200 K0 W101 K5
X21F
SET M13
X21D
RST M12
RST Y20F
.... After the completion of resolution multiplication value setting, the A/D conversion-enabled/disabled channels and the averaging processing designation are written to an A68ADN
M13
X201
Y20E Y21E Y20F Y21F
119
RFRP H0200 K10 W130 K10
X21E
RST M14
X21D
.... After the completion of the initial setting, the A/D conversion-completed flag and digital output value are read.

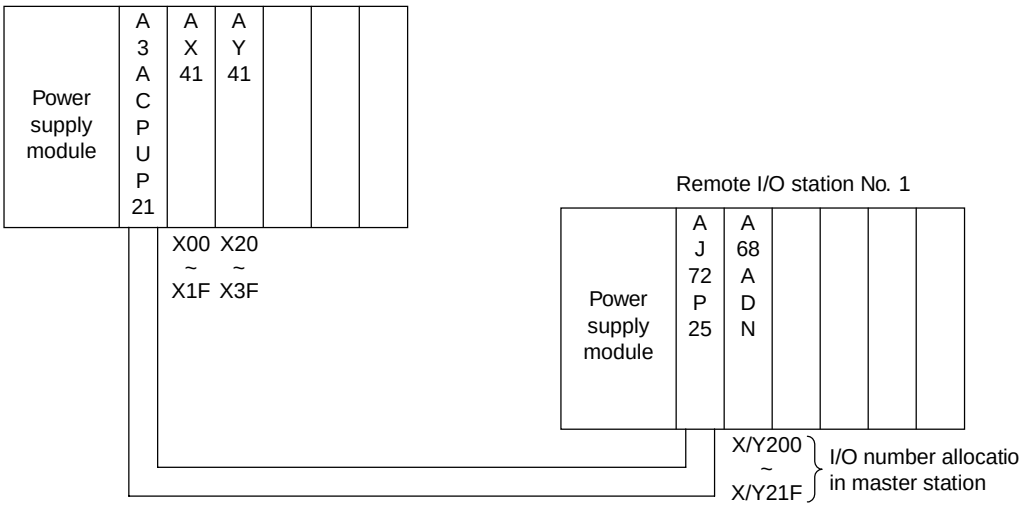

1
Processing after the oc currence of a write data error
The digital output value is sent to "D" for those channels where an A/ conversion completed flag is turned ON
End
143
X202
M 14
Y 20 E
X 21 E
Y 30 F
X 21 F
RFRP H0300 K18 W138 K1
X21E
SET M14
X21D
RST Y30E
RST M11
RST M12
RST M13
170
X002 M14
Y212
PST M14
174
MCR N0
177
M9036
MOV K139 K2M30
M20
MOV K130 D10
M21
MOV K131 D11
M22
MOV K132 D12
M24
MOV K134 D14
CIRCUIT END
.... Reading the error code if a writ data error occurs
.... Resets the write data error stat when (X2) is turned ON
.... Transmits the A/D conversion-completed flag to M140 to M147
.... Transmits the digital value of th channel where the A/D conver-sion-completed flag is ON to the data register (D).

5.3 Sample program when an A68ADN is loaded to a remote I/O station (using AnACPU dedicated instructions)

Sample program of initial setting and digital output value reading, using AnA dedicated instructions, is explained below for the MELSECNET in which A2A(S1) or A3ACPU functions as the master station and the A68ADN is loaded to a remote I/O station.

[Sample Program Conditions]

(1) System configuration



(2) Initial setting

(a) A-D conversion-enabled channel ..... Channels 1, 2, 3, and 5

(b) Averaging processing by count ..... Channel 3 (setting: 50 times)

(c) Averaging processing by time ..... Channel 2 (setting: 1000 ms)

(d) Resolution setting 2 (1/8000)

(3) Devices to be used

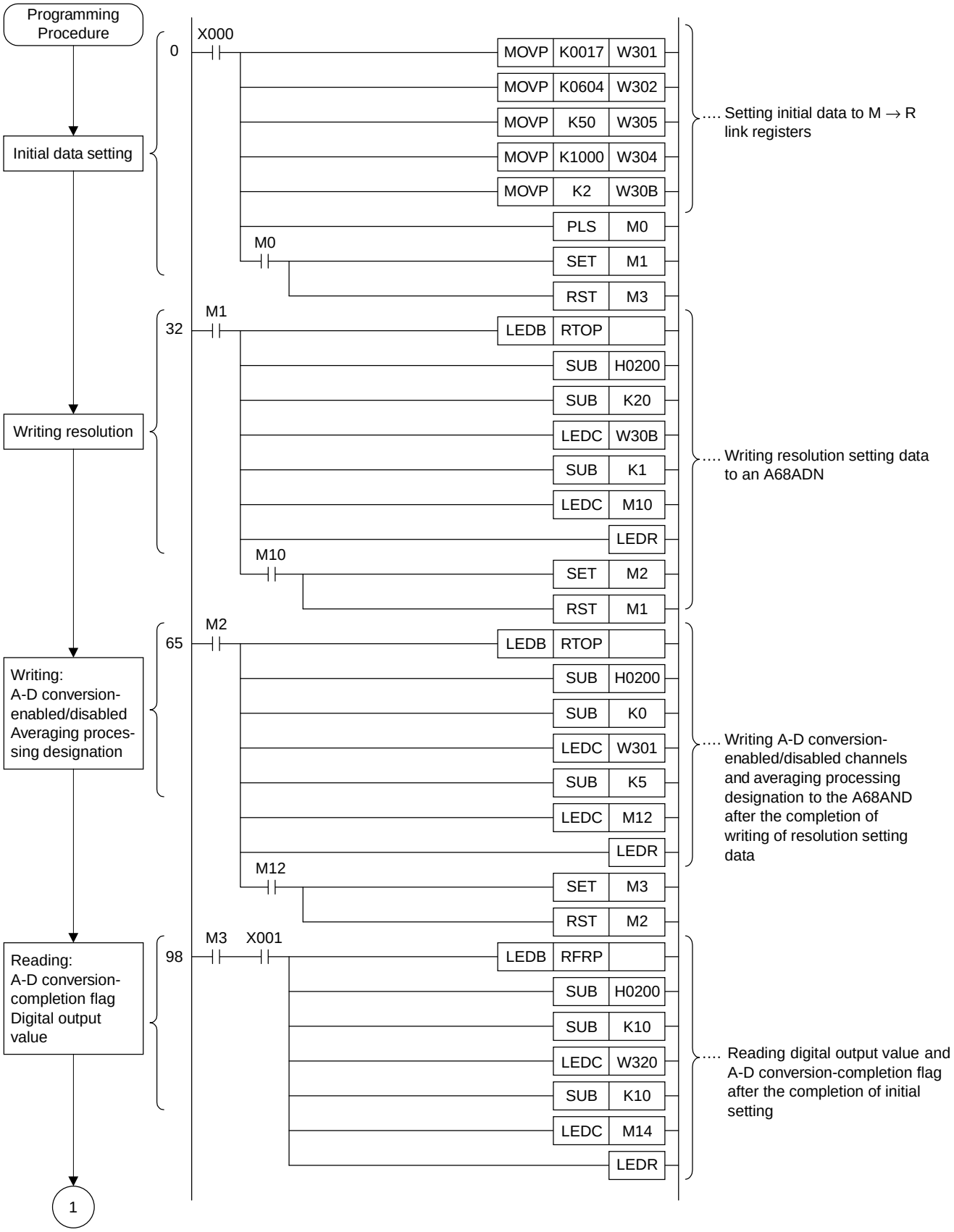
(a) Initial setting write command input signal X20

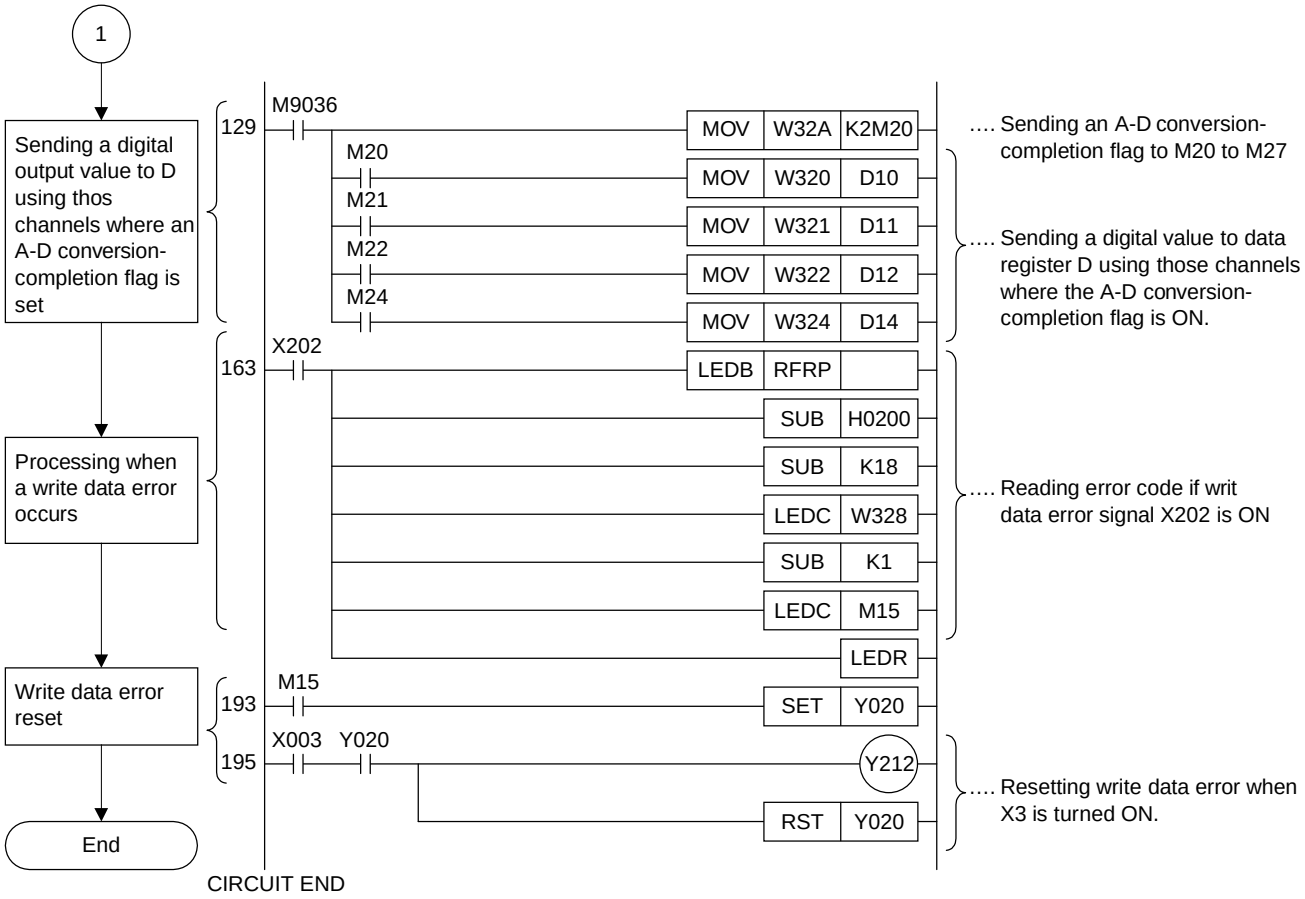
(b) Write data error reset signal X23

(c) Digital output value read command input signal X21

(d) M → R link registers ..... W300 to W31F

(e) R → M link registers ..... W320 to W32F


Programming Procedure
Initial data setting
Writing resolution
Writing:
A-D conversion-enabled/disabled
Averaging processing designation
Reading:
A-D conversion-completion flag
Digital output value
1
0
X000
MOVP K0017 W301
MOVP K0604 W302
MOVP K50 W305
MOVP K1000 W304
MOVP K2 W30B
PLS M0
M0
SET M1
RST M3
Setting initial data to M → R link registers
32
M1
LEDB RTOP
SUB H0200
SUB K20
LEDC W30B
SUB K1
LEDC M10
LEDR
M10
SET M2
RST M1
Writing resolution setting data to an A68ADN
65
M2
LEDB RTOP
SUB H0200
SUB K0
LEDC W301
SUB K5
LEDC M12
LEDR
M12
SET M3
RST M2
Writing A-D conversion-enabled/disabled channels and averaging processing designation to the A68AND after the completion of writing of resolution setting data
98
M3
X001
LEDB RFRP
SUB H0200
SUB K10
LEDC W320
SUB K10
LEDC M14
LEDR
Reading digital output value and A-D conversion-completion flag after the completion of initial setting


1
Sending a digital output value to D using thos channels where an A-D conversion-completion flag is set
Processing when a write data error occurs
Write data error reset
End
129
M9036
MOV W32A K2M20
M20
MOV W320 D10
M21
MOV W321 D11
M22
MOV W322 D12
M24
MOV W324 D14
163
X202
LEDB RFRP
SUB H0200
SUB K18
LEDC W328
SUB K1
LEDC M15
LEDR
193
M15
SET Y020
195
X003 Y020
Y212
RST Y020
CIRCUIT END
.... Sending an A-D conversion-completion flag to M20 to M27
.... Sending a digital value to data register D using those channels where the A-D conversion-completion flag is ON.
.... Reading error code if writ data error signal X202 is ON
.... Resetting write data error when X3 is turned ON.

6. TROUBLESHOOTING

6.1 Error Code Table

If an error occurs during PC CPU read/write data operations, the following error codes are stored in the A68ADN buffer memory (address 18).

Table 6.1 Error Code Table (Error Detected by the A68ADN)

Error Code	Causes	Corrective Action
100	• A number other than 1 to 3 is set for resolution setting.	• Correct the resolution setting.
102	• Data is written to the read-only area (addresses 10 to 17)	• Correct the program that specifies the read-only area.
[ ] 0 to 4	• A value outside the range of 160 to 10000 (ms) is set for averaging time setting. • [ ] indicates the channel where an error is detected. • 0 to 4 : A value in this field has no special meaning. Any number can indicate the averaging time setting error.	• Correct the setting.
[ ] 5 to 8	• A value outside the range of 1 to 500 (times) is set for averaging count setting. • [ ] indicates the channel where an error is detected. • 5 to 8 : A value in this field has no special meaning. Any number can indicate the averaging time setting error.	• Correct the setting.

(1) If more than one type of error occurs, only the error code of the first error is stored in the A68ADN.

(2) To reset the error code, use the sequence program to turn Y12 ON (see Section 5.1).

6.2 Troubleshooting

This section deals with troubleshooting related to the A68ADN. For troubleshooting related to the PC CPU, see the appropriate PC CPU User's Manual.

6.2.1 RUN LED (A68ADN) is flashing

Check Point	Corrective Action
Data which disables write or read is written to the A68ADN.	Check the error code table (see Section 6.1) for the cause, and correct the sequence program.

6.2.2 RUN LED (A68ADN) is OFF

Check Point	Corrective Action
Are the TEST terminals open?	After offset/gain setting, open the TEST terminals.
Is the X2 signal (watchdog timer error) ON?	Reset the PC CPU. If the RUN LED is not ON even after the PC CPU is reset, the hardware is faulty. Consult the nearest Mitsubishi representative.

6.2.3 Digital output value cannot be read

Check Point	Corrective Action
Is the RUN LED (A68ADN) either flashing o OFF?	See Section 6.2.1 or 6.2.2.
Is the ERROR LED (PC CPU) ON?	See the appropriate PC CPU User's Manual.
Is the RUN LED (PC CPU) either flashing or OFF?	See the appropriate PC CPU User's Manual.
Have conditions to execute a FROM instructio been met?	Monitor the conditions with a peripheral device (like a GPP) to see if they have been met.
Is the buffer memory address designated by a FROM instruction the address for the digital output value from the channel to be read?	Check the sequence program.
Is the channel designated by a FROM instruction A-D conversion enabled?	Read buffer memory address 0 to check th enable/disable setting for the channel in question.
Is A-D conversion completed for the channel designated by a FROM instruction?	Read buffer memory address 19 to see whether or not the A-D conversion-completion flag is set.
Is the analog input signal cable broken or disconnected	Find the defect, using both visual inspection and a continuity check.
Disconnect the analog input cable from the A68ADN, and apply a test voltage (using either stabilized power supply or a battery) to measure digital output value.	If the digital output value is correct, it means that the module is influenced by external noise, etc Check cable connections and grounding.

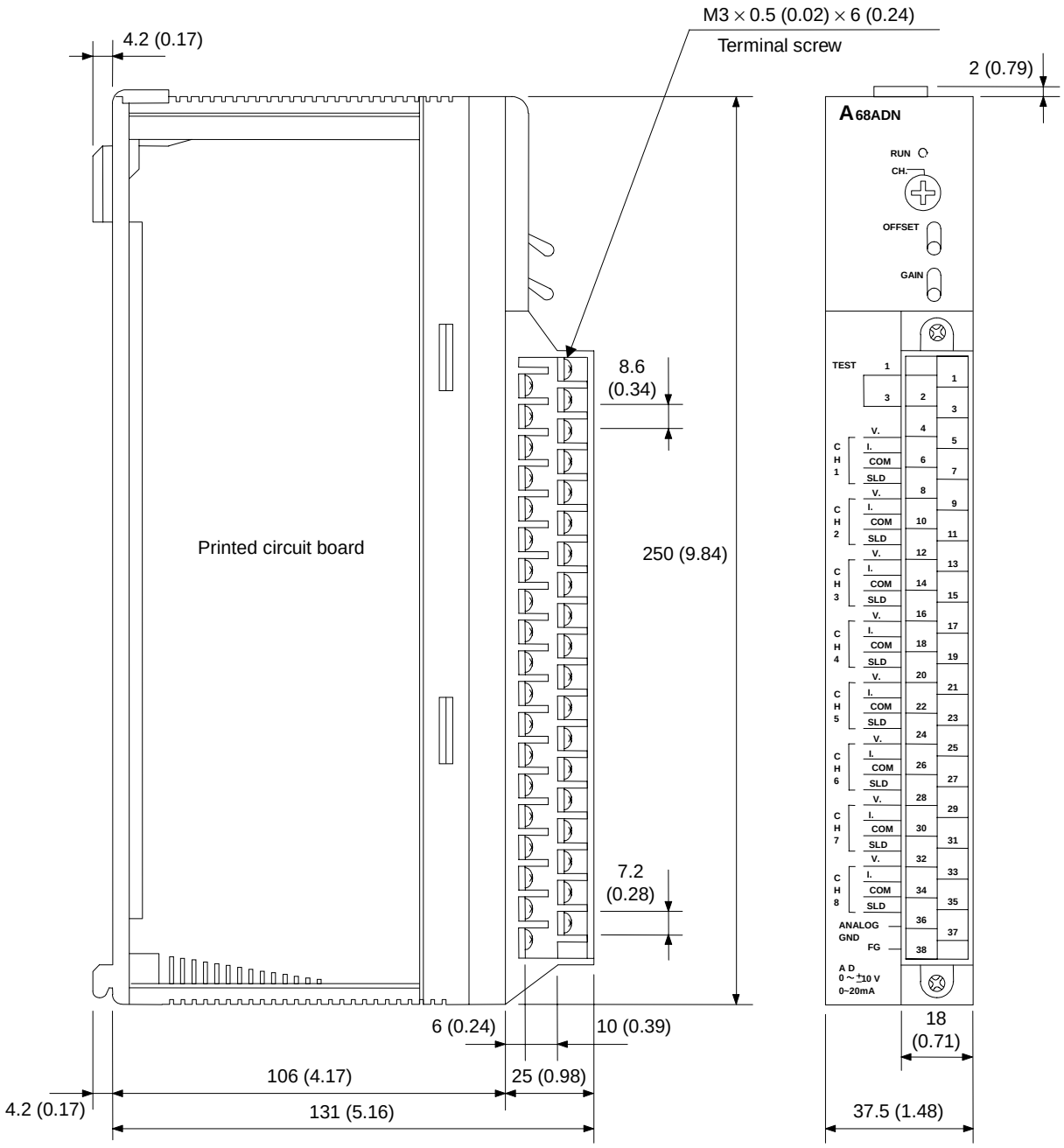
APPENDICES

APPENDIX 1 Comparison of A68ADN and A68AD/A68AD-S2/A616AD Functions

Table A1 Function Comparison

Item		Specifications								
		A68AD	A68AD-S2	A616AD			A68ADN			
Analog input	Voltage	–10 to 0 to 10 VDC (input resistance 30 KΩ)		–10 to 0 to 10 VDC (input resistance 1 MΩ)						
	Current	–20 to 20 mADC (input resistance 250 W)								
Digital output	ACPU	16-bit signed binary (–2048 to 2047)		16-bit signed binary (–48 to 4047, –2048 to 2047)			16-bit signed binary (–4096 to 4095, –8192 to 8191, –12288 to 12287)			
	K2ACPU	16-bit signed binary (±2047)		(Unavailable)						
Maximum resolution	Voltage	5 mV (1/2000)		1.0 mV (1 to 5 V), 1.25 mV (0 to 5 V), 2.5 mV (0 to 10 V), 5.0 mV (-10 to 10 V)	(1/4000)	Selected with a setting pin	2.5 mV 1.25 mV 0.83 mV	(1/4000) (1/8000) (1/12000)	Selectable	
	Current	20 μA (1/1000)		10 μA (0 to 20 mA), 20 μ A (-20 to 20 mA)	(1/2000)	Selected with a setting pin	10 μA 5 μA 3.3 μA	(1/4000) (1/8000) (1/12000)	Selectable	
				4 μA (4 to 20 mA), 5 μA (0 to 20 mA), 10 μA (-20 to 20 mA)	(1/4000)					
Overall accuracy		Within ±1 %		Within ±0.6 %			Within ±1 %			
Maximum conversion speed		Max. 2.5 ms/channel		1 ms/channel			20 ms/channel			
Absolute maximum input	Voltage	±15 V								
	Current	±30 mA								
Number of analog input device points		8 channels/module		16 channels/modul (extendable)			8 channels/module			
Conversion method		Scannings per channel								
Offset/gain adjustment		Use offset/gain adjustment knobs		Switched with a setting pin			Use offset/gain adjustment knobs			
Average processing		Enabled		Disabled			Enabled			
Insulation method	Between input terminal an PC CPU	Photocoupler insulation								
	Between channels	No insulation								
Specification of A-D conversion channel		Set serial channel numbers beginning with CH 1		A-D conversion-enabled/disabled setting						
A-D conversion-completion flag		Not provided		When A-D conversion is specified, after A-D conversion is completed, and the digital value is written to buffermemory, the A-D conversion-completion flag is set						

APPENDIX 2 External Dimensions



Unit: mm (inch)