

0.5 Ω CMOS 1.65 V TO 3.6 V **4-Channel Multiplexer**

ADG804

FEATURES

 0.5Ω typical on resistance 0.8 Ω maximum on resistance at 125°C 1.65 V to 3.6 V operation Automotive temperature range: -40°C to +125°C High current carrying capability: 300 mA continuous Rail-to-rail switching operation Fast switching times <25 ns Typical power consumption (<0.1 μW)

APPLICATIONS

MP3 players Power routing Battery-powered systems PCMCIA cards **Cellular phones** Modems Audio and video signal routing **Communication systems**

GENERAL DESCRIPTION

The ADG804 is a low voltage 4-channel CMOS multiplexer comprising four single channels. This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range. The digital inputs can handle 1.8 V logic with a 2.7 V to 3.6 V supply.

The ADG804 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. A Logic 0 on the EN pin disables the device. The ADG804 has break-before-make switching.

The ADG804 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation. It is available in a 10-lead MSOP package.

FUNCTIONAL BLOCK DIAGRAM

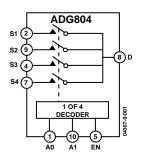


Figure 1.

PRODUCT HIGHLIGHTS

- $<0.8 \Omega$ over full temperature range of -40° C to $+125^{\circ}$ C.
- Single 1.65 V to 3.6 V operation.
- Operational with 1.8 V CMOS logic.
- High current handling capability (300 mA continuous current at 3.3 V).
- Low THD + N (0.02% typ).
- Small 10-lead MSOP package.

TABLE OF CONTENTS

Specifications3	Typical Performance Characteristics	8
Absolute Maximum Ratings 6	••	11
ESD Caution	Outline Dimensions	13
Pin Configurations7	Ordering Guide	13

REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

 $V_{\rm DD}$ = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.¹

Table 1.

Parameter	+25°C	−40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0VtoV_{DD}$	V	
On Resistance (Ron)	0.5			Ωtyp	$V_{DD} = 2.7 \text{ V}$; $V_S = 0 \text{ V to } V_{DD}$, $I_S = 10 \text{ mA}$; Figure 18
	0.65	0.75	0.8	Ω max	
On Resistance Match between	0.04			Ωtyp	$V_{DD} = 2.7 \text{ V}; V_S = 0.65 \text{ V}, I_S = 10 \text{ mA}$
Channels (ΔR _{ON})		0.075	0.08	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	0.1			Ωtyp	$V_{DD} = 2.7 \text{ V; } V_S = 0 \text{ V to } V_{DD},$
(12.1(6.1))		0.15	0.16	Ω max	$I_S = 10 \text{ mA}$
LEAKAGE CURRENTS				-	V _{DD} = 3.6 V
Source Off Leakage Is (OFF)	±0.1			nA typ	$V_S = 0.6 \text{ V/3.3 V; } V_D = 3.3 \text{ V/0.6 V; Figure 19}$
Jource on Leanage 13 (or 17	±1			nA max	75 6.6 7/5.5 7/76 5.5 7/6.6 7/1.gaic 15
Drain Off Leakage I _D (OFF)	±0.1			nA typ	$V_S = 0.6 \text{ V/3.3 V; } V_D = 3.3 \text{ V/0.6 V; Figure 19}$
Drain on Leakage in (Or 1)	±1			nA max	V ₃ = 0.0 V/3.3 V, V ₀ = 3.3 V/0.0 V, Figure 19
Channel On Leakage I _D , I _S (ON)	±0.1			nA typ	$V_S = V_D = 0.6 \text{ V or } 3.3 \text{ V; Figure } 20$
Charmer Off Leakage 10, 15 (ON)	±1			nA max	VS = VB = 0.0 V 01 3.3 V, 1 igure 20
DIGITAL INPUTS	Σ1			TIA IIIax	
			2	V min	
Input High Voltage, V			2 0.8	V max	
Input Low Voltage, V _{INL}	0.005		0.8		W W 55W
Input Current I _{INL} or I _{INH}	0.005		.01	μA typ	$V_{IN} = V_{INL} \text{ or } V_{INH}$
c			±0.1	μA max	
C _{IN} , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS ²	2.4				D 500 C 35 5
t transistion	24	22	25	ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
. FNARIE	30	32	35	ns max	$V_S = 1.5 \text{ V/O V}$; Figure 21
t _{on} ENABLE	23	20	24	ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
	29	30	31	ns max	$V_S = 1.5 \text{ V/O V}$; Figure 23
t _{OFF} ENABLE	5			ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
	6	7	8	ns max	$V_{S} = 1.5 \text{ V}$; Figure 23
Break-Before-Make Time Delay (t _{BBM})	20			ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$; Figure 22
Charge Injection	28			pC typ	$V_S = 1.5 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF}; Figure 24$
Off Isolation	-67			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; Figure 25
Channel-to-Channel Crosstalk	-75			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; Figure 27
Total Harmonic Distortion (THD+N)	0.02			%	$R_L = 32 \Omega$, $f = 20 Hz$ to 20 kHz, $V_S = 2 V p-p$
Insertion Loss	0.06			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$
–3 dB Bandwidth	33			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Figure 26
C _S (OFF)	24			pF typ	
C _D (OFF)	105			pF typ	
C _D , C _S (ON)	125			pF typ	
POWER REQUIREMENTS					$V_{DD} = 3.6 \text{ V}$
I _{DD}	0.003			μA typ	Digital inputs = 0 V or 3.6 V
		1.0	4	μA max	

 $^{^1}$ Temperature range, Y version: -40°C to $+125^\circ\text{C}.$ 2 Guaranteed by design, not subject to production test.

 $V_{\rm DD}$ = 2.5 V \pm 0.2 V, GND = 0 V, unless otherwise noted. 1

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0 V to V_{DD}$	V	
On Resistance (RoN)	0.65			Ωtyp	$V_{DD} = 2.3 \text{ V}$; $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$; Figure 18
	0.77	0.8	0.88	Ω max	
On Resistance Match between	0.4			Ωtyp	$V_{DD} = 2.3 \text{ V}; V_S = 0.7 \text{ V}; I_S = 10 \text{ mA}$
Channels (ΔR _{ON})		0.08	0.085	Ω max	
On Resistance Flatness (RFLAT(ON))	0.16			Ωtyp	$V_{DD} = 2.3 \text{ V}; V_S = 0 \text{ V to } V_{DD}; I_S = 10 \text{ mA}$
		0.23	0.24	Ωmax	
LEAKAGE CURRENTS					$V_{DD} = 2.7 \text{ V}$
Source Off Leakage I _S (OFF)	±0.1			nA typ	$V_S = 0.6 \text{ V/2.4 V}, V_D = 2.4 \text{ V/0.6 V};$ Figure 19
_	±1			nA max	
Drain Off Leakage I _D (OFF)	±0.1			nA typ	$V_S = 0.6/2.4 \text{ V}, V_D = 2.4/0.6 \text{ V}; Figure 19$
-	±1			nA max	
Channel On Leakage ID, IS (ON)	±0.1			nA typ	$V_S = V_D = 0.6 \text{ V or } 2.4 \text{ V; Figure } 20$
5	±1			nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			1.7	V min	
Input Low Voltage, V _{INL}			0.7	V max	
Input Current I _{INL} or I _{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			±0.1	μA max	
C _{IN} , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS ²					
T _{TRANSISTION}	-25 -			ns typ	$R_L = 50 \Omega, C_L = 35 pF$
	31	33	35	ns max	$V_S = 1.5 \text{ V/O V}$; Figure 21
t _{on} ENABLE	25			ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
	30	32	34	ns max	V _s = 1.5 V/0 V; Figure 22
t _{OFF} ENABLE	5			ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
	7	8	9	ns max	$V_S = 1.5 \text{ V}$; Figure 22
Break-Before-Make Time Delay (t _{BBM})	20			ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$; Figure 22
Charge Injection	20			pC typ	$V_S = 1.25 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF; Figure 24}$
Off Isolation	-67			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; Figure 25
Channel-to-Channel Crosstalk	-75			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; Figure 27
Total Harmonic Distortion (THD $+$ N)	0.022			%	$R_L = 32 \Omega$, $f = 20 Hz$ to 20 kHz, $V_S = 1.5 V p-p$
Insertion Loss	-0.06			dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$
–3 dB Bandwidth	33			MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Figure 26
C _S (OFF)	25			pF typ	
C _D (OFF)	110			pF typ	
C_D, C_S (ON)	128			pF typ	
POWER REQUIREMENTS					V _{DD} = 2.7 V
I _{DD}	0.003			μA typ	Digital inputs = 0 V or 2.7 V
		1	4	μA max	

 $^{^1}$ Temperature range, Y version: -40°C to +125°C. 2 Guaranteed by design, not subject to production test.

 V_{DD} = 1.65 V \pm 1.95 V, GND = 0 V, unless otherwise noted. 1

Table 3.

ANALOG SWITCH 0 V to V _D Analog Signal Range 0 V to V _D On Resistance (RoN) 1 1.4 2.2 2.2 2.2 4 4 On Resistance Match between Channels (ΔRoN) 0.1 LEAKAGE CURRENTS 5 ±0.1 Source Off Leakage Is (OFF) ±0.1 ±1 Drain Off Leakage ID (OFF) ±0.1 ±1 Channel On Leakage ID, Is (ON) ±0.1 ±1 DIGITAL INPUTS Input High Voltage, ViNH 0.65 V _{DD} Input Low Voltage, ViNL 0.35 V _{DD} Input Current InL or InNH 0.005 ±0.1 CIN, Digital Input Capacitance 4 4 DYNAMIC CHARACTERISTICS ² ±0.1 40 42 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12 5	D V Ω typ Ω max Ω max Ω typ NA typ NA max	$V_{DD} = 1.8 \text{ V; } V_S = 0 \text{ V to V}_{DD}, I_S = 10 \text{ m.}$ $V_{DD} = 1.65 \text{ V, V}_S = 0 \text{ V to V}_{DD},$ $I_S = 10 \text{ mA; Figure 18}$ $V_{DD} = 1.65 \text{ V, V}_S = 0.7 \text{ V, I}_S = 10 \text{ mA}$ $V_{DD} = 1.95 \text{ V}$ $V_S = 0.6 \text{ V/1.65 V, V}_D = 1.65 \text{ V/0.6 V;}$ $Figure 19$ $V_S = 0.6/1.65 \text{ V, V}_D = 1.65/0.6 \text{ V;}$ $Figure 19$ $V_S = V_D = 0.6 \text{ V or 1.65 V;}$ $Figure 20$ $V_{IN} = V_{INL} \text{ or V}_{INH}$
On Resistance (Ron) 1 1.4 2.2 2.2 2.2 2.2 4 4 On Resistance Match between Channels (ΔRon) 0.1 LEAKAGE CURRENTS 5 ±0.1 Source Off Leakage Is (OFF) ±0.1 ±1 Drain Off Leakage Ib (OFF) ±0.1 Channel On Leakage Ib (ON) ±0.1 DIGITAL INPUTS Input High Voltage, VINH 0.65 VDD 0.35 VDD Input Low Voltage, VINL 0.005 ±0.1 Input Current IINL or IINH 0.005 ±0.1 CIN, Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² 40 42 44 ton ENABLE 34 ton ENABLE 39 40 41 toff ENABLE 8 Total Time Delay (t _{BBM}) 22 Charge Injection 12	Ω typ Ω max Ω max Ω typ nA typ nA max nA typ nA max nA typ nA max V min V max μA typ μA max	$V_{DD} = 1.65 \text{ V}, V_S = 0 \text{ V to V}_{DD}, \\ I_S = 10 \text{ mA}; Figure 18 \\ V_{DD} = 1.65 \text{ V}, V_S = 0.7 \text{ V}, I_S = 10 \text{ mA} \\ \\ V_{DD} = 1.95 \text{ V} \\ V_S = 0.6 \text{ V}/1.65 \text{ V}, V_D = 1.65 \text{ V}/0.6 \text{ V}; \\ Figure 19 \\ V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V}; \\ Figure 19 \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figur$
1.4 2.2	Ω max Ω max Ω typ nA typ nA max nA typ nA max nA typ nA max v max	$V_{DD} = 1.65 \text{ V}, V_S = 0 \text{ V to V}_{DD}, \\ I_S = 10 \text{ mA}; Figure 18 \\ V_{DD} = 1.65 \text{ V}, V_S = 0.7 \text{ V}, I_S = 10 \text{ mA} \\ \\ V_{DD} = 1.95 \text{ V} \\ V_S = 0.6 \text{ V}/1.65 \text{ V}, V_D = 1.65 \text{ V}/0.6 \text{ V}; \\ Figure 19 \\ V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V}; \\ Figure 19 \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ \\ V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figure 20 \\ \\ V_S = 0.6 \text{ V or } 1.65 \text{ V}; Figur$
On Resistance Match between Channels (\(\text{\(\text{LRON} \))} \) LEAKAGE CURRENTS Source Off Leakage \(\text{Ls} \) (OFF) Drain Off Leakage \(\text{Ls} \) (OFF) Channel On Leakage \(\text{Ls} \) (ON) DIGITAL INPUTS Input High Voltage, V_{INH} Input Low Voltage, V_{INL} Input Current \(\text{InNL} \) or \(\text{InNH} \) C_{IN}, Digital Input Capacitance DYNAMIC CHARACTERISTICS ² t_{TRANSISTION} 22 40 42 44 toff ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t_{BBM}) 22 5 Charge Injection	Ω max Ω max Ω typ nA typ nA max nA typ nA max nA typ nA max v max	$I_{S} = 10 \text{ mA; Figure 18}$ $V_{DD} = 1.65 \text{ V, } V_{S} = 0.7 \text{ V, } I_{S} = 10 \text{ mA}$ $V_{DD} = 1.95 \text{ V}$ $V_{S} = 0.6 \text{ V/1.65 V, } V_{D} = 1.65 \text{ V/0.6 V;}$ Figure 19 $V_{S} = 0.6/1.65 \text{ V, } V_{D} = 1.65/0.6 \text{ V;}$ Figure 19 $V_{S} = V_{D} = 0.6 \text{ V or 1.65 V;}$ Figure 20
On Resistance Match between Channels (\(\text{\(\Delta \text{RON} \))} \) LEAKAGE CURRENTS Source Off Leakage Is (OFF) Drain Off Leakage ID (OFF) Channel On Leakage ID, Is (ON) DIGITAL INPUTS Input High Voltage, VINH Input Low Voltage, VINL Input Current INL or INH CIN, Digital Input Capacitance DYNAMIC CHARACTERISTICS ² trransistion 4 Toff ENABLE 10 11 13 Break-Before-Make Time Delay (tabus) Charge Injection 0.1 \$\frac{\pmathrm{1}}{\pmathrm{2}} \text{\(\text{tabus}\)}{\pmathrm{2}} \(\text{tabus	nA typ nA max nA typ nA max nA typ nA max V min V max μA typ μA max	$I_{S} = 10 \text{ mA; Figure 18}$ $V_{DD} = 1.65 \text{ V, } V_{S} = 0.7 \text{ V, } I_{S} = 10 \text{ mA}$ $V_{DD} = 1.95 \text{ V}$ $V_{S} = 0.6 \text{ V/1.65 V, } V_{D} = 1.65 \text{ V/0.6 V;}$ Figure 19 $V_{S} = 0.6/1.65 \text{ V, } V_{D} = 1.65/0.6 \text{ V;}$ Figure 19 $V_{S} = V_{D} = 0.6 \text{ V or 1.65 V;}$ Figure 20
LEAKAGE CURRENTS ±0.1	nA typ nA max nA typ nA max nA typ nA max V min V max µA typ µA max	$V_{DD} = 1.65 \text{ V}, V_S = 0.7 \text{ V}, I_S = 10 \text{ mA}$ $V_{DD} = 1.95 \text{ V}$ $V_S = 0.6 \text{ V}/1.65 \text{ V}, V_D = 1.65 \text{ V}/0.6 \text{ V};$ Figure 19 $V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V};$ Figure 19 $V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V};$ Figure 20
Source Off Leakage Is (OFF) ±0.1 ±1 ±0.1 ±1 ±0.1 ±1 ±0.1 Channel On Leakage ID, Is (ON) ±0.1 ±1 ±1 DIGITAL INPUTS 0.65 VDD Input High Voltage, VINH 0.005 Input Current INL or INH 0.005 ±0.1 ±0.1 CIN, Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² ±0.1 ±0.1 40 40 42 44 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 ±0.1 <	nA max nA typ nA max nA typ nA max V min V max µA typ µA max	$V_S = 0.6 \text{ V}/1.65 \text{ V}, V_D = 1.65 \text{ V}/0.6 \text{ V};$ Figure 19 $V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V};$ Figure 19 $V_S = V_D = 0.6 \text{ V}$ or 1.65 V; Figure 20
Drain Off Leakage I₀ (OFF) ±1 ±0.1 ±1 Channel On Leakage I₀, I₅ (ON) ±0.1 ±1 ±1 DIGITAL INPUTS 0.65 V₀₀ Input High Voltage, Vᵢ⋈L 0.35 V₀₀ Input Low Voltage, Vᵢ⋈L 0.35 V₀₀ Input Current Iᵢ⋈L or Iᵢ⋈H 0.005 ★0.1 ★0.1 CIŊ, Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² ★0.42 trransistion 32 40 42 44 ★1 ton ENABLE 34 39 40 41 toff ENABLE 8 Break-Before-Make Time Delay (t₀Խм) 22 Charge Injection 12	nA max nA typ nA max nA typ nA max V min V max µA typ µA max	Figure 19 $V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V};$ Figure 19 $V_S = V_D = 0.6 \text{ V} \text{ or } 1.65 \text{ V};$ Figure 20
Drain Off Leakage I₀ (OFF) ±0.1 ±1 ±0.1 ±0.1 ±1 DIGITAL INPUTS 0.65 V₀₀ Input High Voltage, Vᵢ⋈H 0.35 V₀₀ Input Low Voltage, Vᵢ⋈L 0.35 V₀₀ Input Current Iᵢ⋈Lor Iᵢ⋈H 0.005 ±0.1 ±0.1 Cᵢӎ, Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² 32 transistion 32 40 42 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (tଃBM) 22 5 Charge Injection 12 5	nA typ nA max nA typ nA max V min V max µA typ µA max	$V_S = 0.6/1.65 \text{ V}, V_D = 1.65/0.6 \text{ V};$ Figure 19 $V_S = V_D = 0.6 \text{ V} \text{ or } 1.65 \text{ V};$ Figure 20
Channel On Leakage I _D , I _S (ON) ±1 ±0.1 ±1 DIGITAL INPUTS 0.65 V _{DD} Input High Voltage, V _{INH} 0.35 V _{DD} Input Current I _{INL} or I _{INH} 0.005 ±0.1 ±0.1 C _{IN} , Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² ±0.1 t _{TRANSISTION} 32 40 42 44 t _{ON} ENABLE 34 39 40 41 t _{OFF} ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12 5	nA max nA typ nA max V min V max µA typ µA max	Figure 19 $V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V; Figure } 20$
Channel On Leakage I _D , I _S (ON) ±1 ±0.1 ±1 DIGITAL INPUTS 0.65 V _{DD} Input High Voltage, V _{INH} 0.35 V _{DD} Input Current I _{INL} or I _{INH} 0.005 ±0.1 ±0.1 C _{IN} , Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² ±0.1 t _{TRANSISTION} 32 40 42 44 t _{ON} ENABLE 34 39 40 41 t _{OFF} ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12 5	nA typ nA max V min V max μA typ μA max	Figure 19 $V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V; Figure } 20$
DIGITAL INPUTS Input High Voltage, V _{INH} Input Low Voltage, V _{INL} Input Current I _{INL} or I _{INH} O.005 **D.1** **C_IN, Digital Input Capacitance DYNAMIC CHARACTERISTICS2* **t_TRANSISTION** **T_ANSISTION** **T_ANSISTOON** **T_ANSISTOO	NA max V min V max μA typ μA max	$V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V; Figure 20}$
DIGITAL INPUTS Input High Voltage, V _{INH} 0.65 V _{DD} Input Low Voltage, V _{INL} 0.35 V _{DD} Input Current I _{INL} or I _{INH} 0.005 ±0.1 ±0.1 C _{IN} , Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² ±0.1 t _{TRANSISTION} 32 40 42 44 ton ENABLE 34 39 40 41 t _{OFF} ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12	NA max V min V max μA typ μA max	
DIGITAL INPUTS 0.65 V _{DD} Input High Voltage, V _{INL} 0.35 V _{DD} Input Current I _{INL} or I _{INH} 0.005 ±0.1 ±0.1 C _{IN} , Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS² 32 t _{TRANSISTION} 32 40 42 44 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12	V min V max μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Input High Voltage, V _{INH} 0.65 V _{DD} 0.35 V _{DD} 0.35 V _{DD} 0.005 ±0.1	V max μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V _{INL} 0.35 V _{DD} 1	V max μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Input Current I _{INL} or I _{INH}	μΑ typ μΑ max	$V_{IN} = V_{INL}$ or V_{INH}
#0.1 CIN, Digital Input Capacitance DYNAMIC CHARACTERISTICS ² trransistion 32 40 42 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12	μA max	VIN — VINL OF VINH
CIN, Digital Input Capacitance 4 DYNAMIC CHARACTERISTICS2 32 tTRANSISTION 32 40 42 44 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (tBBM) 22 Charge Injection 12	•	
DYNAMIC CHARACTERISTICS2 32 40 42 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12 5	ргтур	
tTRANSISTION 32 40 42 44 ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12 5		
ton ENABLE top En	I .	D 500 C 35 5
ton ENABLE 34 39 40 41 toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12	ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
39 40 41	ns max	$V_S = 1.5 \text{ V/O V}$; Figure 21
toff ENABLE 8 10 11 13 Break-Before-Make Time Delay (tbbb) 22 5 Charge Injection 12	ns typ	$R_L = 50 \Omega$, $C_L = 35 pF$
10	ns max	$V_S = 1.5 \Omega/0 V$; Figure 22
Break-Before-Make Time Delay (t _{BBM}) 22 5 Charge Injection 12	ns typ	$R_L = 50 \Omega, C_L = 35 pF$
Charge Injection 12	ns max	$V_S = 1.5 \text{ V}$; Figure 22
Charge Injection 12	ns typ	$R_L = 50 \Omega, C_L = 35 pF$
	ns min	$V_{S1} = V_{S2} = 1 \text{ V; Figure 22}$
	pC typ	$V_S = 1 \text{ V}, R_S = 0 \text{ V}, C_L = 1 \text{ nF}; Figure 24$
Off Isolation –67	dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$; Figure 25
Channel-to-Channel Crosstalk –75	dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$, Figure 27
Total Harmonic Distortion (THD + N)) 0.14	%	$R_L = 32 \Omega$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, $V_S = 1.2 \text{ V p-p}$
Insertion Loss 0.08	dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 100 kHz$
-3 dB Bandwidth 30	MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Figure 26
C _S (OFF) 26	pF typ	, , p.,,g 3
C _D (OFF) 115	pF typ	
C _D , C _S (ON) 130	pF typ	
POWER REQUIREMENTS	P. 0P	V _{DD} = 1.95 V
I _{DD} 0.003	1	Digital inputs = 0 V or 1.95 V
1.0 4	μA typ	Digital hipats = 0 v Ol 1.93 v

 $^{^1}$ Temperature range, Y version: –40°C to +125°C. 2 Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25$ °C, unless otherwise noted.

Table 4

Table 4.	
Parameter	Rating
V _{DD} to GND	−0.3 V to +4.6 V
Analog Inputs ¹	$-0.3 \text{ V to V}_{DD} + 0.3 \text{ V}$
Digital Inputs ¹	−0.3 V to +4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	(Pulsed at 1 ms, 10% Duty Cycle Max)
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
IR Reflow, Peak Temperature <20 sec	235°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 5. ADG804 Truth Table

A 1	A0	EN	ON Switch
Х	Х	0	None
0	0	1	S1
0	1	1	S2
1	0	1	S3
1	1	1	S4

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATION

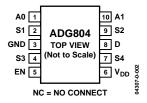


Figure 2. 10-Lead MSOP (RM-10)

Table 6. Terminology

V_{DD}	Most positive power supply potential.
I _{DD}	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or an output.
D	Drain terminal. May be an input or an output.
EN	Active high logic control input.
A0, A1	Logic control inputs. Used to select which source terminal, S1 to S4, is connected to the drain, D.
V_D , V_S	Analog voltage on terminals D, S.
Ron	Ohmic resistance between D and S.
R _{FLAT} (ON)	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
ΔR_{ON}	On resistance match between any two channels.
Is (OFF)	Source leakage current with the switch off.
I _D (OFF)	Drain leakage current with the switch off.
I_D , I_S (ON)	Channel leakage current with the switch on.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I _{INL} (I _{INH})	Input current of the digital input.
Cs (OFF)	Off switch source capacitance. Measured with reference to ground.
C _D (OFF)	Off switch drain capacitance. Measured with reference to ground.
C_D , C_S (ON)	On switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
ton (EN)	Delay time between the 50% and the 90% points of the digital input and switch on condition.
t _{OFF} (EN)	Delay time between the 50% and the 90% points of the digital input and switch off condition.
t transition	Delay time between the 50% and the 90% points of the digital input and switch on condition when switching from one address state to the other.
t _{BBM}	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
–3 dB Bandwidth	The frequency at which the output is attenuated by 3 dB.
On Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on resistance of the switch.
THD + N	The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

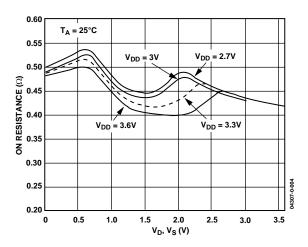


Figure 3. On Resistance vs. V_D (V_S) $V_{DD} = 2.7 \text{ V}$ to 3.6 V

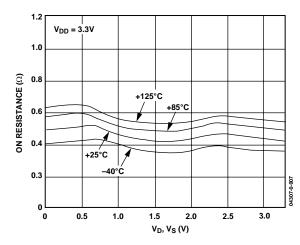


Figure 6. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 3.3 \text{ V}$

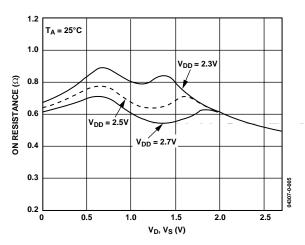


Figure 4. On Resistance vs. V_D (V_S) V_{DD} = 2.5 $V \pm 0.2 V$

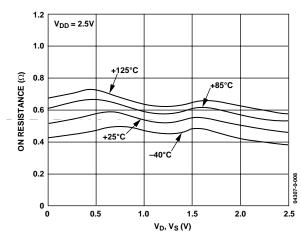


Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 2.5 \text{ V}$

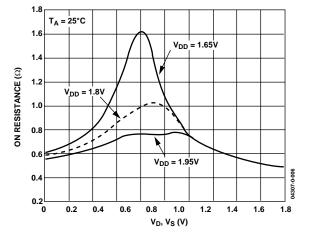


Figure 5. On Resistance vs. V_D (V_S) V_{DD} = 1.8 \pm 0.15 V

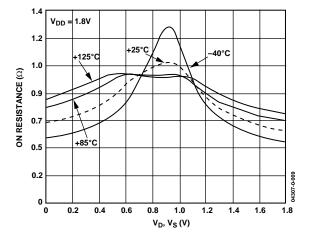


Figure 8. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 1.8 \text{ V}$

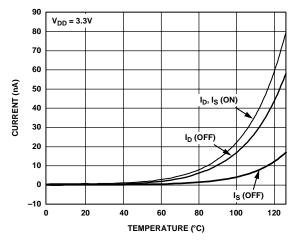


Figure 9. Leakage Current vs. Temperature, $V_{DD} = 3.3 \text{ V}$

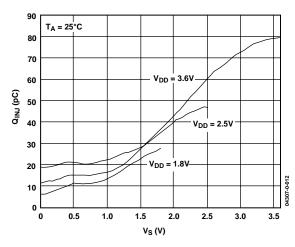


Figure 12. Charge Injection vs. Source Voltage, $V_{DD} = 1.8 \text{ V}$

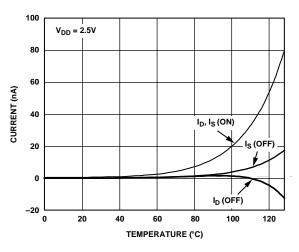


Figure 10. Leakage Current vs. Temperature, $V_{DD} = 2.5 \text{ V}$

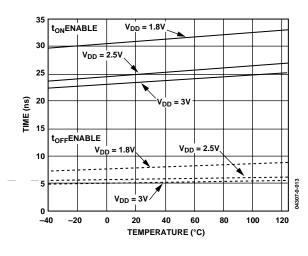


Figure 13. ton/toff Times vs. Temperature

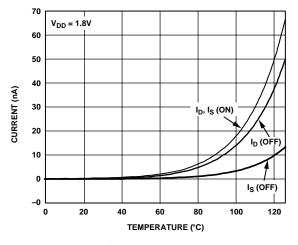


Figure 11. Leakage Current vs. Temperature, $V_{\text{DD}} = 1.8 \text{ V}$

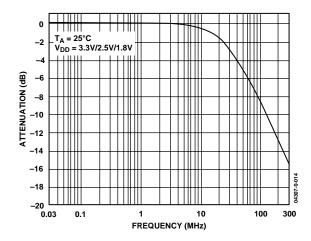


Figure 14. Bandwidth

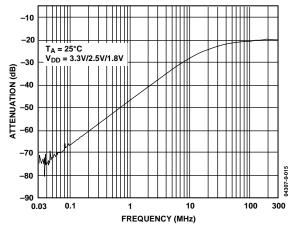


Figure 15. Off Isolation vs. Frequency

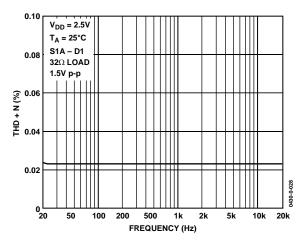


Figure 17. Total Harmonic Distortion + Noise

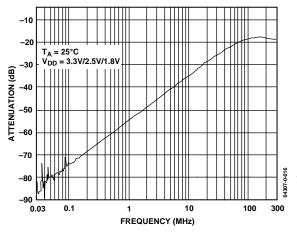


Figure 16. Crosstalk vs. Frequency

TEST CIRCUITS

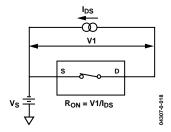
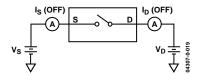
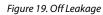


Figure 18. On Resistance





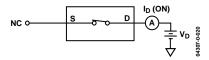


Figure 20. On Leakage

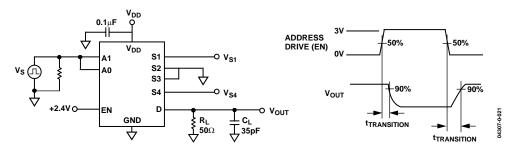


Figure 21. Switching Time of Multiplexer, ttransition

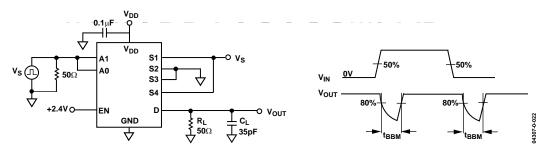


Figure 22. Break-Before-Make Time Delay, tbbm

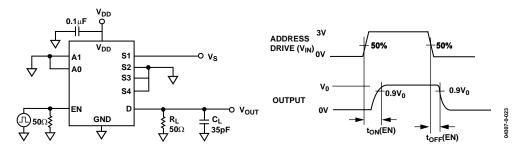


Figure 23. Enable Delay, ton(EN), toff(EN)

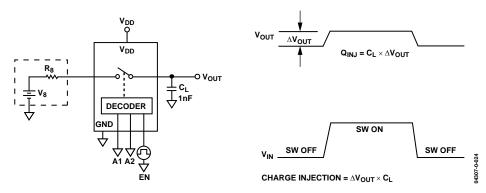


Figure 24. Charge Injection

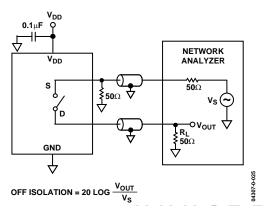


Figure 25. Off Isolation

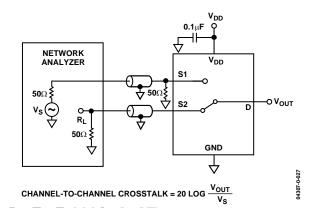


Figure 27. Channel-to-Channel Crosstalk

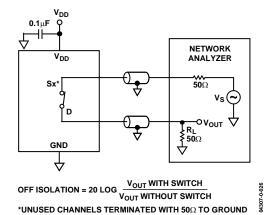
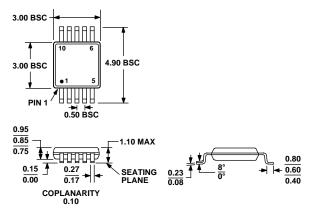


Figure 26. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187BA

Figure 28. 10-Lead Mini Small Outline Package [MSOP] (RM-10) Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding ¹
ADG804YRM	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S1A
ADG804YRM-REEL	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S1A
ADG804YRM-REEL7	−40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S1A

 $^{^{\}mbox{\tiny 1}}$ Branding on this package is limited to three characters due to space constraints.

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