FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13707-3E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90520A/520B Series

# MB90522A/523A/522B/523B/F523B/V520A

## ■ DESCRIPTION

The MB90520A/520B series is a general-purpose 16-bit microcontroller designed for process control applications in consumer products that require high-speed real-time processing.

The microcontroller instruction set is based on the AT architecture of the F²MC* family with additional instructions for high-level languages, extended addressing modes, enhanced multiplication and division instructions, and a complete range of bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word (32-bit) data.

The MB90520A/520B series peripheral resources include an 8/10-bit A/D converter, 8-bit D/A converter, UART (SCI) , extended I/O serial interfaces 0 and 1, 8/16-bit up/down counter/timers 0 and 1, 8/16-bit PPG timers 0 and 1, a range of I/O timers (16-bit free-run timers 1 and 2, input capture (ICU) 0 and 1, and output compare (OCU) 0 and 1) , an LCD controller/driver, 8 external interrupt inputs, and 8 wakeup interrupts.

* : F²MC stands for FUJITSU Flexible MicroController, a registered trademark of FUJITSU LIMITED.

## ■ FEATURES

- **Clock**
- Internal PLL clock multiplication circuit
- Selectable machine clock (PLL clock) : Base oscillation divided by two or multiplied by one to four
  (For a 4 MHz base oscillation, the machine clock range is 4 MHz to 16 MHz) .

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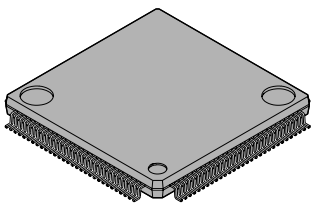
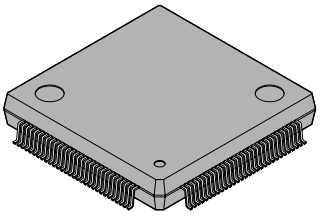
## ■ PACKAGES

| 120-pin, Plastic, LQFP | 120-pin, Plastic, QFP |
|---|---|
|  |  |
| (FPT-120P-M05) | (FPT-120P-M13) |

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- Sub-clock (32.768 KHz) operation available
  Minimum instruction execution time : 62.5 ns (for oscillation = 4 MHz, PLL clock setting = ×4, $V_{CC}$ = 5.0 V)
- **16MB CPU memory space**
  Internal 24-bit addressing
- **Instruction set optimized for controller applications**
  Rich data types (bit, byte, word, long-word)
  Extended addressing modes (23 types)
  Enhanced signed multiplication and division instructions and RETI instruction
  Enhanced calculation precision using a 32-bit accumulator
- **Instruction set designed for high-level language** (**C**) **and multi-tasking**
  System stack pointer
  Enhanced pointer-indirect instructions and barrel shift instructions
- **Faster execution speed**
  4-byte instruction queue
  ROM mirror function (48 Kbytes of bank FF is mirrored in bank 00)
- **Program patch function** : **An address match detection function** (**2** × **addresses**)
- **Interrupt function**
  32 programmable interrupts with 8 levels
- **Automatic data transmission function independent of CPU operation**
  Extended intelligent I/O service function ($EI^2OS$) : Up to 16 channels
- **Low-power consumption** (**stand-by**) **modes**
  Sleep mode (CPU operating clock stops, peripherals continue to operate.)
  Pseudo-clock mode (Only oscillation clock and timebase timer continue to operate.)
  Clock mode (Main oscillation clock stops, sub-clock and clock timer continue to operate.)
  Stop mode (Main oscillation and sub-clock both stop.)
  CPU intermittent operation mode
  Hardware stand-by mode (Change to stop mpde by operating hardware stand-by pins.)
- **Process**
  CMOS technology
- **I/O ports**
  General-purpose I/O ports (CMOS input/output) : 53 ports
  General-purpose I/O ports (inputs with pull-up resistors) : 24 ports
  General-purpose I/O ports (Nch open-drain outputs) : 8 ports
- **Timers**
  Timebase timer, clock timer, watchdog timer : 1 channel each
  8/16-bit PPG timers 0 and 1 : 8-bit × 2 channels or 16-bit × 1 channel
  16-bit reload timers 0 and 1 : 2 channels
  16-bit I/O timers :
    16-bit free-run timers 0 and 1 : 2 channels
    16-bit input capture 0 : 2 channels (2 channels per unit)
    16-bit output compare 0 and 1 : 8 channels (4 channels per unit)
  8/16-bit up/down counter/timers 0 and 1 : 8-bit × 2 channels or 16-bit × 1 channel
  Clock output function : 1 channel
- **Communications macro** (**communication interface**)
  Extended I/O serial interfaces 0 and 1 : 2 channels
  UART (full-duplex, double-buffered, SCI : Can also be used for synchronous serial transfer) : 1 channel

- **External event interrupt control function**
  DTP/external interrupts : 8 channels (Can be set to detect rising edges, falling edges, “H” levels, or “L” levels)
  Wake-up interrupts : 8 channels (Detects “L” levels only)
  Delayed interrupt generation module : 1 channel (for task switching)
- **Analog/digital conversion**
  8/10-bit A/D converter : 8 channels (Can be initiated by an external trigger. Minimum conversion time = 10.2 μs for a 16 MHz machine clock)
  8-bit D/A converter : 2 channels (R-2R type. Settling time = 12.5 μs for a 16 MHz machine clock)
- **Display function**
  LCD controller/driver : 32 × segment drivers + 4 × common drivers
- **Other**
  Supports serial writing to flash memory. (Only on versions with on-board flash memory.)

Note : The MB90520A and 520B series cannot be used in external bus mode. Always set these devices to single-chip mode.

## ■ PRODUCT LINEUP

| Parameter \ Part Number | MB90522A | MB90523A | MB90522B | MB90523B | MB90F523B | MB90V520A |
|---|---|---|---|---|---|---|
| Classification | Mask ROM | | | | Flash ROM | Evaluation product |
| ROM size | 64 Kbytes | 128 Kbytes | 64 Kbytes | 128 Kbytes | 128 Kbytes | — |
| RAM size | 4 Kbytes | | | | | 6 Kbytes |
| Separate emulator power supply[*1] | — | — | — | — | — | No |
| Process | CMOS | | | | | |
| Operating power supply voltage[*2] | 3.0 V to 5.5 V | | 2.7 V to 5.5 V | | 3.0 V to 5.5 V | |
| Internal regulator circuit | not mounted | | | | mounted | |
| CPU functions | Number of instructions : 340<br>Instruction sizes : 8-bit, 16-bit<br>Instruction length : 1 byte to 7 bytes<br>Data sizes : 1-bit, 8-bit, 16-bit | | | | | |
| | Minimum instruction execution time : 62.5 ns (for a 16 MHz machine clock) | | | | | |
| | Interrupt processing time : 1.5 µs min. (for a 16 MHz machine clock) | | | | | |
| Low power operation (standby modes) | Sleep mode, clock mode, pseudo-clock mode, stop mode, hardware standby mode, and CPU intermittent operation mode | | | | | |
| I/O ports | General-purpose I/O ports (CMOS outputs) : 53<br>General-purpose I/O ports (inputs with pull-up resistors) : 24<br>General-purpose I/O ports (Nch open drain outputs) : 8<br>Total : 85 | | | | | |
| Timebase timer | 18-bit counter<br>Interrupt interval : 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms<br>(for a 4 MHz base oscillation) | | | | | |
| Watchdog timer | Reset trigger period<br>• For a 4 MHz base oscillation : 3.58, 14.33, 57.23, 458.75 ms<br>• For 32.768 sub-clock operation : 0.438, 3.500, 7.000, 14.000 s | | | | | |
| 16-bit I/O timers — 16-bit freerun timer | Number of channels : 2<br>Generates an interrupt on overflow | | | | | |
| 16-bit I/O timers — 16-bit output compare | Number of channels : 8<br>Pin change timing : Free run timer register value equals output compare register value. | | | | | |
| 16-bit I/O timers — 16-bit input capture | Number of channels : 2<br>Saves the value of the freerun timer register when a pin input occurs (rising edge, falling edge, either edge) . | | | | | |
| 16-bit reload timer | Number of channels : 2<br>Count clock frequency : 0.125, 0.5, or 2.0 µs for a 16 MHz machine clock<br>Can be used to count an external event clock. | | | | | |

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| Parameter \ Part Number | MB90522A | MB90523A | MB90522B | MB90523B | MB90F523B | MB90V520A |
|---|---|---|---|---|---|---|
| Clock timer | 15-bit timer<br>Interrupt interval : 0.438, 0.5, or 2.0 μs for sub-clock frequency = 32.768 kHz | | | | | |
| 8/16-bit PPG timer | Number of channels : 1 (Can be used in 2 × 8-bit channel mode)<br>Can generate a pulse waveform output with specified period and 0 to 100% duty ratio. | | | | | |
| 8/16 -bit up/down counter/timers | Number of channels : 1 (Can be used in 2 × 8-bit channel mode)<br>External event inputs : 6 channels<br>Reload/compare function : 8-bit × 2 channels | | | | | |
| Clock monitor | Clock output frequency : Machine clock/$2^1$ to machine clock/$2^8$ | | | | | |
| Delayed interrupt generation module | Interrupt generation module for task switching. (Used by REALOS.) | | | | | |
| DTP/External interrupts | Input channels : 8<br>Generates interrupts to the CPU on rising edges, falling edges with input “H” level, or “L” level.<br>Can be used for external event interrupts and to activate $EI^2OS$. | | | | | |
| Wakeup interrupts | Input channels : 8<br>Triggered by “L” level. | | | | | |
| 8/10-bit A/D converter (successive approximation type) | Number of channels : 8<br>Resolution : 8-bit or 10-bit selectable<br>Conversion can be performed sequentially for multiple consecutive channels.<br>• Single-shot conversion mode : Converts specified channel once only.<br>• Continuous conversion mode : Repeatedly converts specified channel.<br>• Intermittent conversion mode : Converts specified channel then halts temporarily. | | | | | |
| 8-bit D/A converter (R-2R type) | Number of channels : 2<br>Resolution : 8-bit | | | | | |
| UART (SCI) | Number of channels : 1<br>Clock synchronous transfer : 62.5 Kbps to 1 Mbps<br>Clock asynchronous transfer : 1202 bps to 31250 bps<br>Supports bi-directional and master-slave communications. | | | | | |
| Extended I/O serial interface | Number of channels : 2<br>Clock synchronous transfer : 31.25 Kbps to 1 Mbps (Using internal shift clock)<br>Transmission format : Selectable LSB-first or MSB-first | | | | | |
| LCD controller/driver | Number of common outputs : 4<br>Number of segment outputs : 32<br>Number of power supply pins for LCD drive : 4<br>LCD display memory : 16 bytes<br>Divider resistor for LCD drive : Internal | | | | | |

*1 : As for the necessity of a DIP switch setting (S2) when using the emulation pod (MB2145-507) . Refer to the hardware manual for the emulation pod (MB2145-507) fomr details.

*2 : Take note of the maximum operating frequency and A/D converter precision restrictions when operating at 3.0 V to 3.6 V. See the “Electrical Characteristics” section for details.

## ■ PACKAGES AND CORRESPONDING PRODUCTS

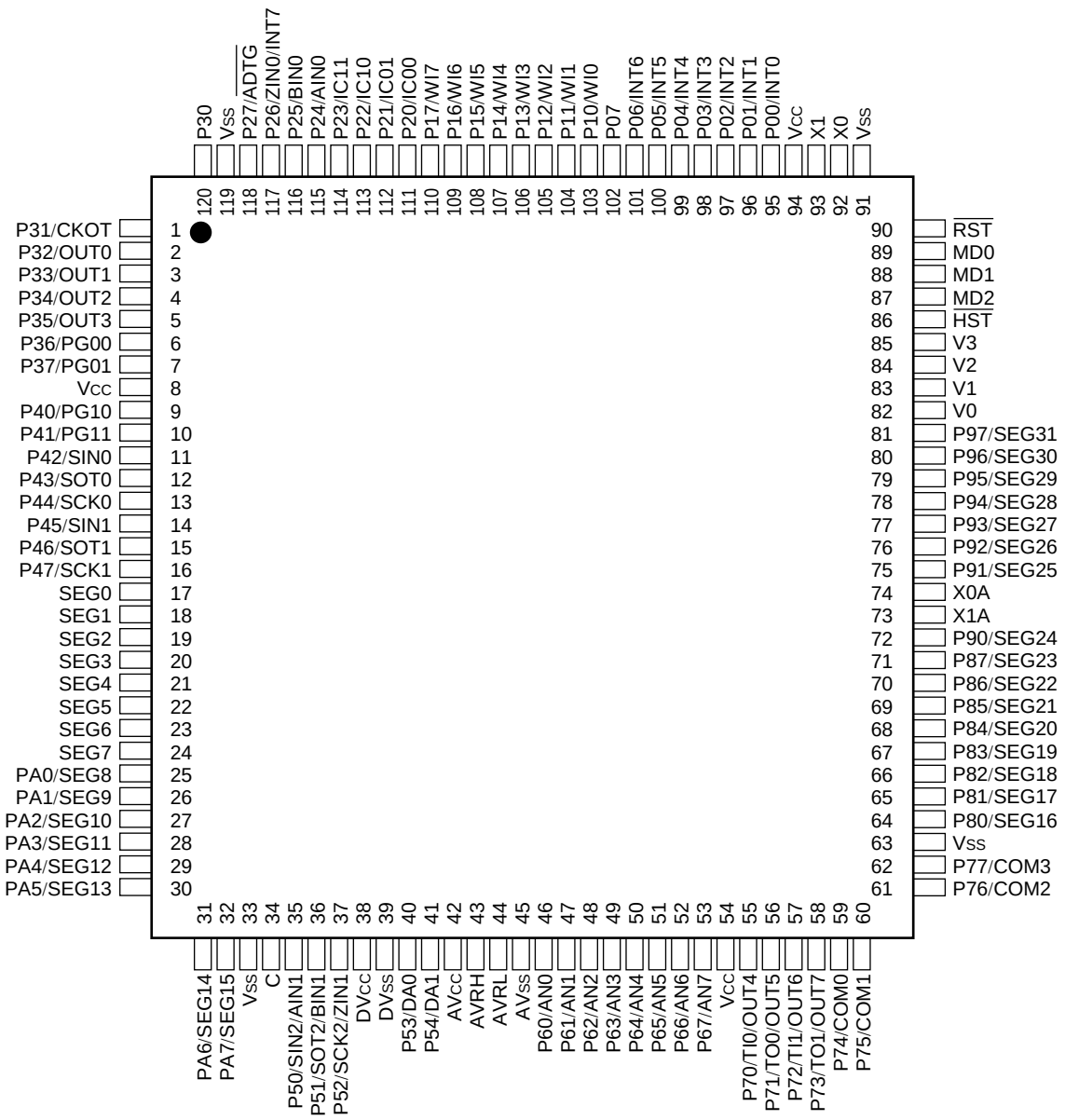
| Package | MB90522A | MB90523A | MB90522B | MB90523B | MB90F523B | MB90V520A |
|---|---|---|---|---|---|---|
| FPT-120P-M05 (LQFP) | ○ | ○ | ○ | ○ | ○ | × |
| FPT-120P-M13 (QFP) | ○ | ○ | ○ | ○ | ○ | × |
| PGA-256C-A01 (PGA) | × | × | × | × | × | ○ |

○ : Available, × : Not available

Note : See the “■ PACKAGE DIMENSIONS” section for more details.

## ■ PIN ASSIGNMENT

(TOP VIEW)




(FPT-120P-M05)
(FPT-120P-M13)

## ■ PIN DESCRIPTIONS

| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 92, 93 | X0, X1 | A | Oscillator pin |
| 74, 73 | X0A, X1A | B | Sub-oscillator pin |
| 89 to 87 | MD0 to MD2 | C | Input pins for setting the operation mode.<br>Connect directly to $V_{CC}$ or $V_{SS}$. |
| 90 | $\overline{RST}$ | C | External reset input pin |
| 86 | $\overline{HST}$ | C | Hardware standby input pin |
| 95 to 101 | P00 to P06 | D | General-purpose I/O ports<br>The settings in the pull-up resistor setup register (RDR0) are enabled when ports are set as inputs.<br>The RDR0 settings are ignored when ports are set as outputs. |
| | INT0 to INT6 | | Event input pins for ch.0 to ch.6 of the DTP/external interrupt circuit |
| 102 | P07 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR0) are enabled when ports are set as inputs.<br>The RDR0 settings are ignored when ports are set as outputs. |
| 103 to 110 | P10 to P17 | D | General-purpose I/O ports<br>The settings in the pull-up resistor setup register (RDR1) are enabled when ports are set as inputs.<br>The RDR1 settings are ignored when ports are set as outputs. |
| | WI0 to WI7 | | Event input pins for the wakeup interrupts. |
| 111, 112, 113, 114 | P20, P21, P22, P23 | E | General-purpose I/O ports |
| | IC00, IC01, IC10, IC11 | | Trigger input pins for input capture units (ICU) 0 and 1.<br>Input operates continuously when channels 0 and 1 of input capture units (ICU) 0 and 1 are operating. Accordingly, output to the pins from other functions that share this pin must be suspended unless performed intentionally. |
| 115 | P24 | E | General-purpose I/O port |
| | AIN0 | | Also can be used as the count clock A input to 8/16-bit up/down counter/timer 0. |
| 116 | P25 | E | General-purpose I/O port |
| | BIN0 | | Also can be used as the count clock B input to 8/16-bit up/down counter/timer 0. |
| 117 | P26 | E | General-purpose I/O port |
| | ZIN0 | | Also can be used as the control clock Z input to 8/16-bit up/down counter/timer 0. |
| | INT7 | | Event input pin for ch.7 of the DTP/external interrupt circuit |

*1 : FPT-120P-M05

*2 : FPT-120P-M13

*(Continued)*

| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 118 | P27 | E | General-purpose I/O port |
| | $\overline{\text{ADTG}}$ | | External trigger input to the 8/10-bit A/D converter<br>Input operates continuously when the 8/10-bit A/D converter is performing input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally. |
| 120 | P30 | E | General-purpose I/O port |
| 1 | P31 | E | General-purpose I/O port |
| | CKOT | | Output pin for clock monitor function<br>The clock monitor is output when clock monitor output is enabled. |
| 2 | P32 | E | General-purpose I/O port<br>Only available when waveform output from output compare 0 is disabled. |
| | OUT0 | | Event output pin for ch.0 of output compare unit 0 (OCU)<br>Only available when event output is enabled for output compare unit 0. |
| 3 | P33 | E | General-purpose I/O port<br>Only available when waveform output from output compare 1 is disabled. |
| | OUT1 | | Event output pin for ch.1 of output compare unit 0 (OCU)<br>Only available when event output is enabled for output compare unit 0. |
| 4 | P34 | E | General-purpose I/O port<br>Only available when waveform output from output compare 2 is disabled. |
| | OUT2 | | Event output pin for ch.2 of output compare unit 0 (OCU)<br>Only available when event output is enabled for output compare unit 0. |
| 5 | P35 | E | General-purpose I/O port<br>Only available when waveform output from output compare 3 is disabled. |
| | OUT3 | | Event output pin for ch.3 of output compare unit 0 (OCU)<br>Only available when event output is enabled for output compare unit 0. |
| 6 | P36 | E | General-purpose I/O port<br>Only available when waveform output from PG00 is disabled. |
| | PG00 | | Output pin for 8/16-bit PPG timer 0<br>Only available when waveform output is enabled for PG00. |
| 7 | P37 | E | General-purpose I/O port<br>Only available when waveform output from PG01 is disabled. |
| | PG01 | | Output pin for 8/16-bit PPG timer 0<br>Only available when waveform output is enabled for PG01. |

*1 : FPT-120P-M05

*2 : FPT-120P-M13

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| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 9, 10 | P40, P41 | D | General-purpose I/O ports<br>Only available when waveform outputs from PG10 and PG11 are disabled.<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | PG10, PG11 | | Output pins for 8/16-bit PPG timer 1<br>Only available when waveform output is enabled for PG10 and PG11. |
| 11 | P42 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | SIN0 | | UART (SCI) serial data input pin<br>Input operates continuously when the UART is performing input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally. |
| 12 | P43 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | SOT0 | | UART (SCI) serial data output pin<br>Only available when serial data output is enabled for the UART (SCI) . |
| 13 | P44 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | SCK0 | | UART (SCI) serial clock input/output pin<br>Only available when serial clock output is enabled for the UART (SCI) . |
| 14 | P45 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports set as inputs. The RDR4 settings are ignored when ports set are as outputs. |
| | SIN1 | | Data input pin for extended I/O serial interface 1<br>Input operates continuously when the performing serial input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally. |
| 15 | P46 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | SOT1 | | Data output pin for extended I/O serial interface 1<br>Only available when serial data output is enabled for SOT1. |

*1 : FPT-120P-M05

*2 : FPT-120P-M13

*(Continued)*

| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 16 | P47 | D | General-purpose I/O port<br>The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs. |
| | SCK1 | | Serial clock input/output pin for extended I/O serial interface 1<br>Only available when serial clock output is enabled for SCK1. |
| 35 | P50 | E | General-purpose I/O port |
| | SIN2 | | Data input pin for extended I/O serial interface 2<br>Input operates continuously when the performing serial input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally. |
| | AIN1 | | Also can be used as the count clock A input to 8/16-bit up/down counter/timer 1. |
| 36 | P51 | E | General-purpose I/O port |
| | SOT2 | | Data output pin for extended I/O serial interface 2<br>Only available when serial data output is enabled for SOT2. |
| | BIN1 | | Also can be used as the count clock B input to 8/16-bit up/down counter/timer 1. |
| 37 | P52 | E | General-purpose I/O port |
| | SCK2 | | Serial clock input/output pin for extended I/O serial interface 2<br>Only available when serial clock output is enabled for SCK2. |
| | ZIN1 | | Also can be used as the control clock Z input to 8/16-bit up/down counter/timer 1. |
| 40, 41 | P53, P54 | I | General-purpose I/O ports |
| | DA0, DA1 | | Analog output pins for ch.0 and ch.1 of the 8-bit D/A converter |
| 46 to 53 | P60 to P67 | K | General-purpose I/O ports<br>Port input is enabled when the analog input enable register (ADER) is set to the ports. |
| | AN0 to AN7 | | Analog inputs for the 8/10-bit A/D converter<br>Analog input is enabled when the analog input enable register (ADER) is set. |
| 55, 57 | P70, P72 | E | General-purpose I/O ports |
| | TI0, TI1 | | Event input pins for 16-bit reload timers 0 and 1<br>Input operates continuously when 16-bit reload timers 0 and 1 input an external clock. Accordingly, output to these pins from other functions that share the pins must be suspended unless performed intentionally. |
| | OUT4, OUT6 | | Event output pins for ch. 4 and ch. 6 of output compare unit 1 (OCU)<br>Only available when event output from output compare 1 is enabled. |

*1 : FPT-120P-M05

*2 : FPT-120P-M13

*(Continued)*

| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 56, 58 | P71, P73 | E | General-purpose I/O ports<br>Only available when event outputs from 16-bit reload timers 0 and 1 are disabled. |
| | TO0, TO1 | | Output pins for 16-bit reload timers 0 and 1.<br>Only available when output is enabled for 16-bit reload timers 0 and 1. |
| | OUT5, OUT7 | | Event output pins for ch. 5 and ch. 7 of output compare unit 1 (OCU)<br>Only available when event output from output compare 1 is enabled. |
| 59 to 62 | P74 to P77 | L | General-purpose I/O ports<br>Only available when the LCD controller/driver control register is set to the ports. |
| | COM0 to COM3 | | Common pins for the LCD controller/driver<br>Only available when the LCD controller/driver control register is set to the common outputs. |
| 64 to 71 | P80 to P87 | L | General-purpose I/O ports<br>Only available when the LCD controller/driver control register is set to the ports. |
| | SEG16 to SEG23 | | LCD segment output pins for the LCD controller/driver<br>Only available when the LCD controller/driver control register is set to the segment outputs. |
| 72, 75 to 81 | P90, P91 to P97 | M | General-purpose I/O ports (Support up to $I_{OL}$ = 10 mA)<br>Only available when the LCD controller/driver control register is set to the ports. |
| | SEG24, SEG25 to SEG31 | | LCD segment output pins for the LCD controller/driver<br>Only available when the LCD controller/driver control register is set to the segment outputs. |
| 17 to 24 | SEG0 to SEG7 | F | LCD segment 00 to 07 pins for the LCD controller/driver |
| 25 to 32 | PA0 to PA7 | L | General-purpose I/O ports<br>Only available when the LCD controller/driver control register is set up to the ports. |
| | SEG8 to SEG15 | | LCD segment 08 to 15 pins for the LCD controller/driver<br>Only available when the LCD controller/driver control register is set to the segment outputs. |

*1 : FPT-120P-M05

*2 : FPT-120P-M13

*(Continued)*

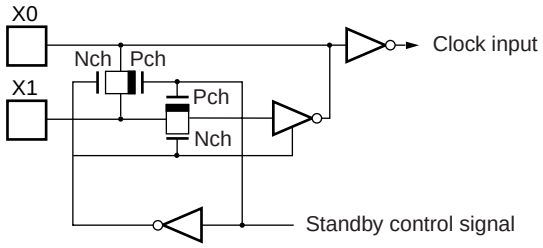
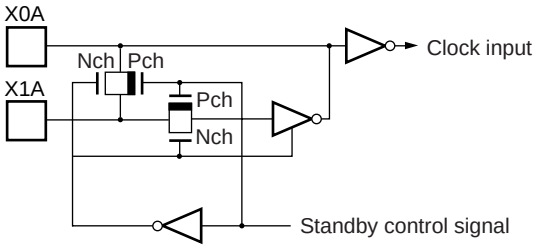
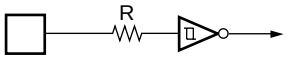
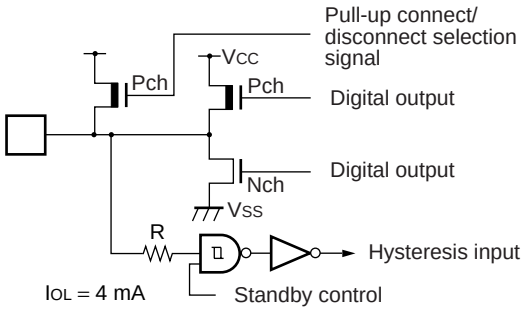
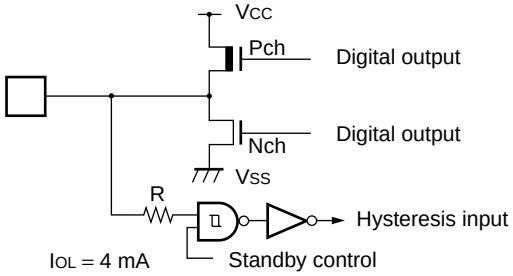
*(Continued)*

| Pin No. LQFP-120*1 QFP-120*2 | Pin Name | Circuit Type | Function |
|---|---|---|---|
| 34 | C | G | Capacitor connection pin for stabilizing power supply<br>Connect an external ceramic capacitor of approximately 0.1 μF. If operating at 3.3 V or lower, connect to $V_{CC}$. |
| 82 to 85 | V0 to V3 | N | Power supply input pins for the LCD controller/driver |
| 8, 54, 94 | $V_{CC}$ | Power supply | Power supply input pins for the digital circuit |
| 33, 63, 91, 119 | $V_{SS}$ | Power supply | GND level power supply input pins for the digital circuit |
| 42 | $AV_{CC}$ | H | Power supply input for the analog circuit<br>Ensure that a voltage greater than $AV_{CC}$ is applied to $V_{CC}$ before turning the analog power supply on or off. |
| 43 | AVRH | J | “H” reference voltage for the A/D converter<br>Ensure that a voltage greater than AVRH is applied to $AV_{CC}$ before turning the power supply to this pin on or off. |
| 44 | AVRL | H | “L” reference voltage for the A/D converter |
| 45 | $AV_{SS}$ | H | GND level power supply input pin for the analog circuit |
| 38 | $DV_{CC}$ | H | “H” reference voltage for the D/A converter<br>Ensure that this voltage does not exceed $V_{CC}$. |
| 39 | $DV_{SS}$ | H | “L” reference voltage for the D/A converter<br>Apply the same voltage level as $V_{SS}$. |

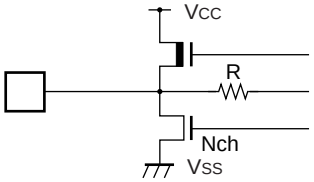
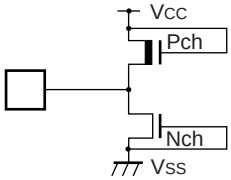
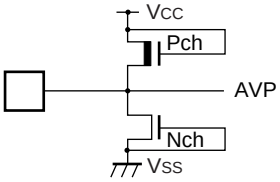
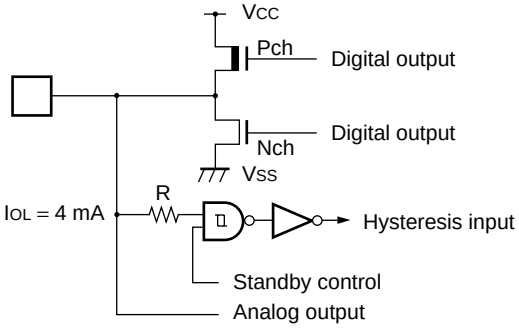
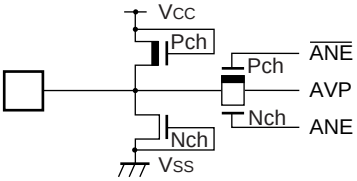
*1 : FPT-120P-M05

*2 : FPT-120P-M13

## ■ I/O CIRCUIT TYPE

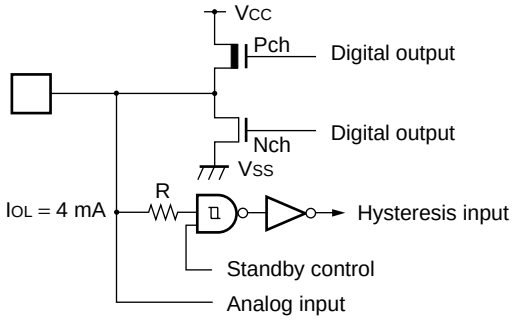
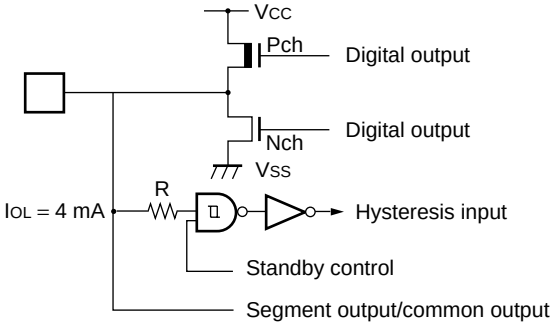
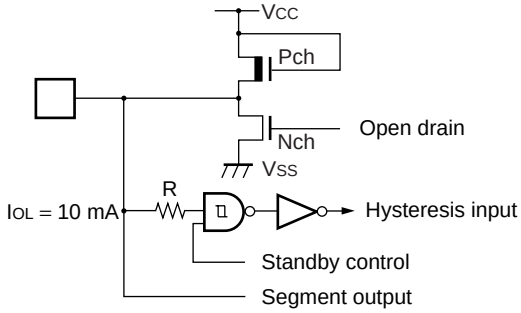
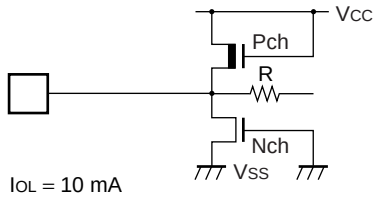
| Type | Circuit | Remarks |
|---|---|---|
| A |  | • High-speed oscillation feedback resistor<br>Approx. 1 MΩ |
| B |  | • Low-speed oscillation feedback resistor<br>Approx. 10 MΩ |
| C |  | • Hysteresis input |
| D |  | • Selectable pull-up option<br>• CMOS hysteresis input<br>• CMOS level output<br>• With standby control |
| E |  | • CMOS hysteresis input<br>• CMOS level output<br>• With standby control |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| F |  | • Segment output pins |
| G |  | • Capacitor connection pin (This is an N.C. pin on the MB90522A and MB90523A.) |
| H |  | • Analog power supply input protection circuit |
| I |  | • CMOS hysteresis input<br>• CMOS level output (CMOS output is not available when analog output is operating.)<br>• Also used as analog output (Analog output has priority)<br>• With standby control |
| J |  | • A/D converter ref+ power supply input pin (Incorporates power supply protection circuit.) |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| K |  | • CMOS hysteresis input<br>• CMOS level output<br>• Also used as analog input.<br>• With standby control |
| L |  | • CMOS hysteresis input<br>• CMOS level output<br>• Also used as segment output pin.<br>• With standby control<br>(only available when segment output is not operating.) |
| M |  | • CMOS hysteresis input<br>• N-ch open-drain output<br>• Also used as segment output pin.<br>• With standby control<br>(only available when segment output is not operaing.) |
| N |  | • Reference voltage pin for LCD controller |

## ■ HANDLING DEVICES

Take note of the following points when handling devices :

- Do not exceed maximum rated voltage (to prevent latch-up)
- Supply voltage stability
- Power-on precautions
- Power supply pins
- Crystal oscillator circuit
- Notes on using an external clock
- Precautions when not using sub-clock mode
- Treatment of unused pins
- Treatment of N.C. pins
- Treatment of pins when A/D converter is not used
- Sequence for connecting and disconnecting the A/D converter power supply and analog input pins
- Shared use of general-purpose I/O ports and LCD controller/driver SEG/COM pins
- Conditions when output from ports 0 and 1 is undefined
- Initialization
- Notes on using the DIV A, Ri and DIVW A, RWi instructions
- Notes on using REALOS

**Device Handling Precautions**

- **Do not exceed maximum rated voltage** (**to prevent latch-up**)
  Latch-up occurs in CMOS ICs if a voltage greater than $V_{CC}$ or less than $V_{SS}$ is applied to an input or output pin (other than a high or medium withstand voltage pin) or if the voltage applied between $V_{CC}$ and $V_{SS}$ exceeds the rating. If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.
  Similarly, when turning the analog power supply on or off, ensure the analog power supply voltages ($AV_{CC}$, AVRH, $DV_{CC}$) and analog input voltages do not exceed the digital voltage ($V_{CC}$) .
  Also ensure that the voltages applied to the LCD power supply pins (V3 to V0) do not exceed the power supply voltage ($V_{CC}$) .

- **Supply voltage stability**
  Rapid changes in supply voltage may cause the device to misoperate, even if the voltage remains within the allowed operating range. Accordingly, ensure that the $V_{CC}$ supply is stable.
  The standard for power supply voltage stability is a peak-to-peak $V_{CC}$ ripple voltage at the mains supply frequency (50 to 60 Hz) of 10% or less of $V_{CC}$ and a transient voltage change rate of 0.1 V/ms or less when turning the power supply on or off.

- **Power-on precautions**
  To prevent misoperation of the internal regulator circuit at power-on, ensure that the power supply rising time (0.2 V to 2.7 V) is at least 50 µs.

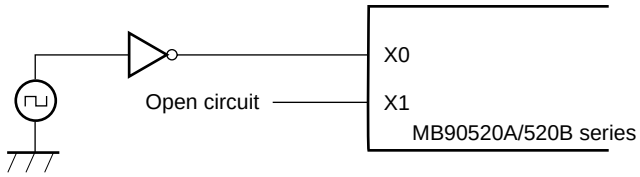
- **Power supply pins**
  When multiple $V_{CC}$ and $V_{SS}$ pins are provided, connect all $V_{CC}$ and $V_{SS}$ pins to power supply or ground externally. Although pins at the same potential are connected together in the internal device design so as to prevent misoperation such as latch-up, connecting all $V_{CC}$ and $V_{SS}$ pins appropriately minimizes unwanted radiation, prevents misoperation of strobe signals due to increases in the ground level, and keeps the overall output current rating.
  Also, ensure that the impedance of the $V_{CC}$ and $V_{SS}$ connections to the power supply are as low as possible.

Connection of a bypass capacitor of approximately 0.1 µF between $V_{CC}$ and $V_{SS}$ is recommended to prevent power supply noise. Connect the capacitor close to the $V_{CC}$ and $V_{SS}$ pins.

- **Crystal oscillator circuit**
  Noise on the X0 and X1 pins can be a cause of device misoperation. Place the X0 and X1 pins, crystal oscillator (or ceramic oscillator) , and bypass capacitor to ground as close together as possible. Also, design the circuit board so that the X0 and X1 pin wiring does not cross other wiring.
  Surrounding the X0/X1 and X0A/X1A pins with ground in the printed circuit board design is recommended to ensure stable operation.

- **Notes on using an external clock**
  When using an external clock, drive the X0 pin only and leave the X1 pin open.
  The figure below shows an example of how to use an external clock.

**Example of how to use an external clock**




- **Precautions when not using sub-clock mode**
  Connect an oscillator to X0A and X1A, even if not using sub-clock mode.

- **Treatment of unused pins**
  Leaving unused input pins unconnected can cause misoperation or permanent damage to the device due to latchup. Always pull-up or pull-down unused pins using a 2 kΩ or larger resistor.
  If some I/O pins are unused, either set as outputs and leave open circuit or set as inputs and treat in the same way as input pins.

- **Treatment of N.C. pins**
  Always leave N.C. (non connect) pins open circuit.

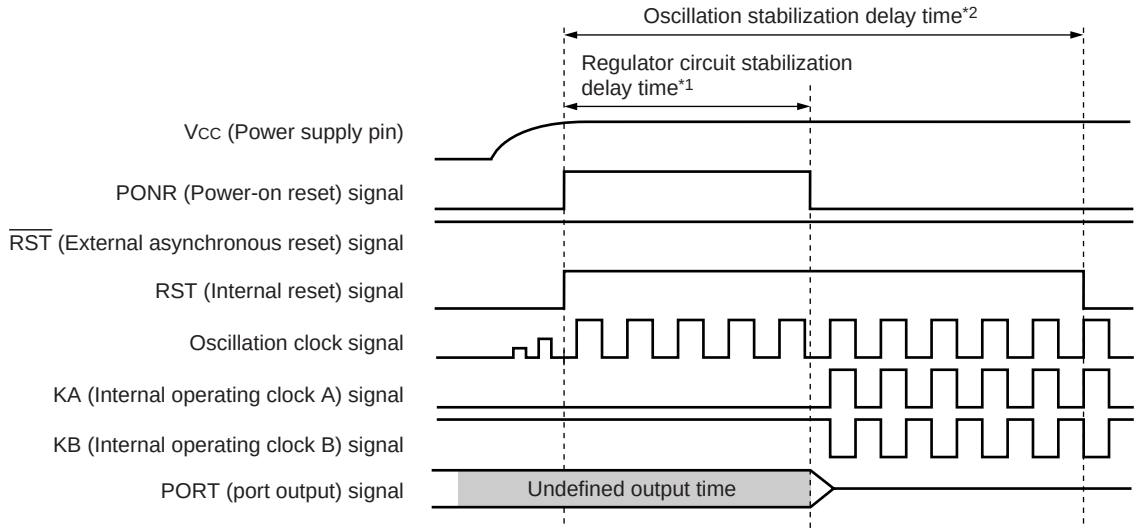
- **Treatment of pins when A/D converter not used**
  When not using the A/D converter and D/A converter, always connect $AV_{CC}$ = $DV_{CC}$ = AVRH = $V_{CC}$ and $AV_{SS}$ = AVRL = $V_{SS}$.

- **Sequence for connecting and disconnecting the A/D converter power supply and analog input pins**
  Do not apply voltage to the A/D and D/A converter power supply ($AV_{CC}$, AVRH, AVRL, $DV_{CC}$, $DV_{SS}$) or analog inputs (AN0 to AN7) until the digital power supply ($V_{CC}$) is turned on.
  When turning the device off, turn off the digital power supply after disconnecting the A/D converter power supply and analog inputs. When turning the power on or off, ensure that AVRH and $DV_{CC}$ do not exceed $AV_{CC}$ (turning the analog and digital power supplies on and off simultaneously is OK) .

- **Shared use of general-purpose I/O ports and LCD controller/driver SEG/COM pins**
  The SEG08 to SEG31 and COM0 to COM3 pins are shared with general-purpose I/O ports. The electrical ratings for SEG08 to SEG23 and COM0 to COM3 are the same as for CMOS outputs and the electrical ratings for SEG24 to SEG31 are the same as for N-ch open-drain ports.

- **Conditions when output from ports 0 and 1 is undefined**
  After turning on the power supply, the outputs from ports 0 and 1 are undefined during the oscillation stabilization delay time controlled by the regulator circuit (during the power-on reset) . The figure below shows the timing.
  Note that this undefined output period does not occur on products without an internal regulator circuit as these products do not have an oscillation stabilization delay time.

**Timing chart for undefined output from ports 0 and 1**




*1 : Regulator circuit oscillation stabilization delay time : $2^{17}$/Oscillation clock frequency
(approx. 8.19 ms for a 16 MHz oscillation clock frequency)

*2 : Oscillation stabilization delay time : $2^{18}$/Oscillation clock frequency
(approx. 16.38 ms for a 16 MHz oscillation clock frequency)

Note : See the "■ PRODUCT LINEUP" section for details of which MB90520A/520B series products have an internal regulator circuit.

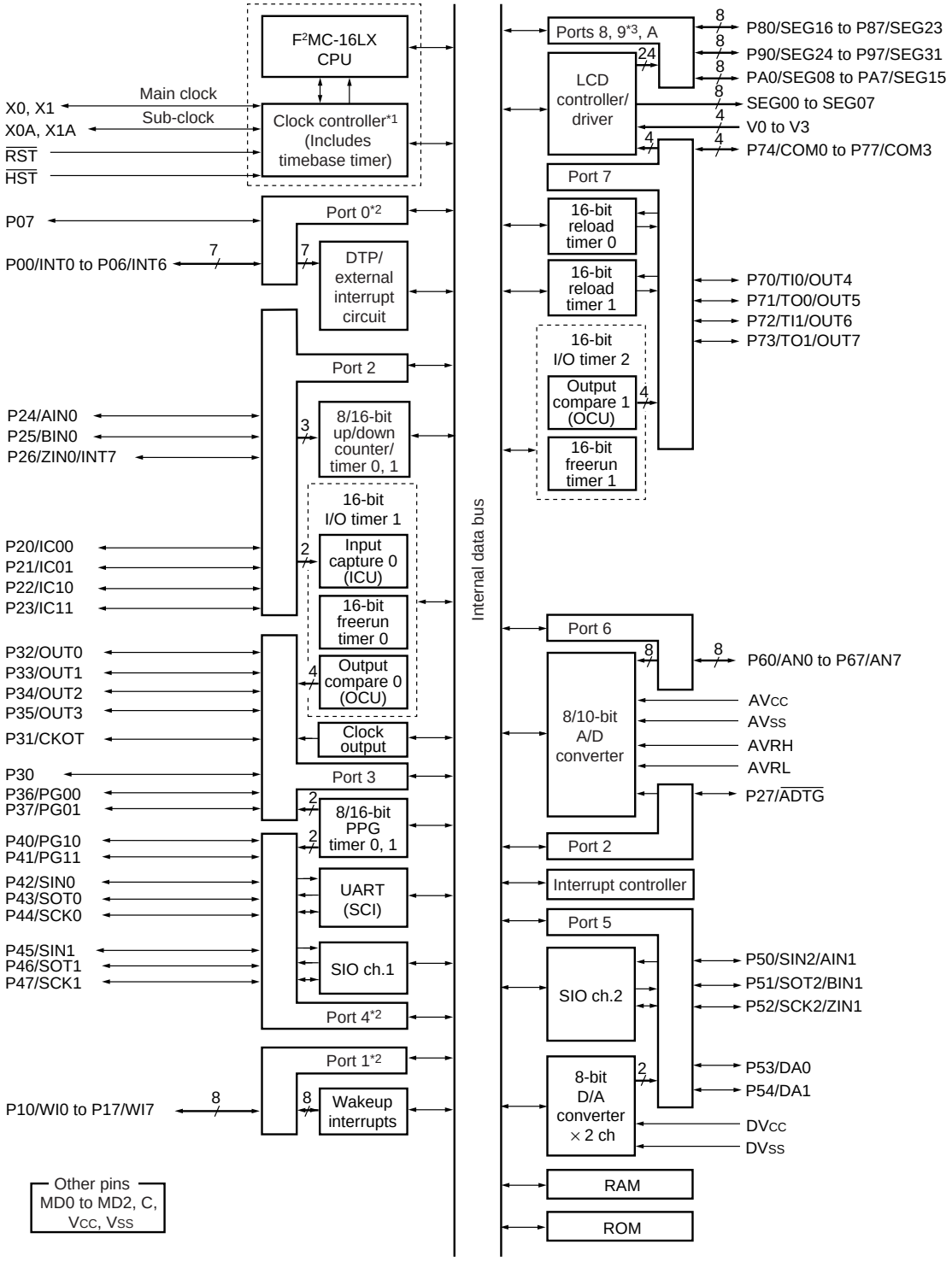
- **Initialization**
  The device contains internal registers that are only initialized by a power-on reset. To initialize these registers, restart the power supply.

- **Notes on using the DIV A, Ri and DIVW A, RWi instructions**
  Set the corresponding bank registers (DTB, ADB, USB, SSB) to "$00_H$" when using the signed division instructions "DIV A, Ri" and "DIVW A, RWi".
  If the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "$00_H$", the remainder value produced by the instruction is not stored in the instruction operand register.

- **Notes on using REALOS**
  The extended intelligent I/O service (EI$^2$OS) cannot be used when using REALOS.

**Caution on Operations during PLL Clock Mode**
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

• BLOCK DIAGRAM



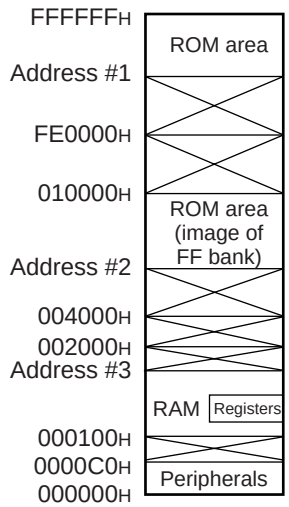

*1 : The clock control circuit includes the watchdog timer and timebase timer low power consumption control circuits.

*2 : Incorporates a pull-up register setting register. CMOS level input and output.

*3 : As this port shares pins with the LCD output, the port uses N-ch open-drain circuits.

## ■ MEMORY MAP

Single chip mode with mirror function




| Part No. | Address #1* | Address #2* | Address #3* |
|---|---|---|---|
| MB90522A/B | FF0000H | 004000H | 001100H |
| MB90523A/B | FE0000H | 004000H | 001100H |
| MB90F523B | FE0000H | 004000H | 001100H |
| MB90V520A | — | — | 001900H |

: Internal memory access

: Access prohibited

* : The values of addresses #1, #2, and #3 vary by product.

Note : The upper part of 00 bank contains a mirror of the ROM data in FF bank. This is called the mirror ROM function and enables use of the C compiler's small memory model. As the lower 16 bits of the FF bank and 00 bank addresses are the same, tables located in ROM can be referenced without needing to declare far pointers.

For example, accessing 00C000H actually accesses the contents of ROM at FFC000H. Note that, as the FF bank ROM area exceeds 48 KBytes, the entire ROM image cannot be mirrored in 00 bank. Accordingly, as ROM data from FF4000H to FFFFFFH is mirrored in 004000H to 00FFFFH, always locate ROM data tables in the range FF4000H to FFFFFFH.

## ■ I/O MAP

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 000000H | PDR0 | Port 0 data register | Port 0 | XXXXXXXXB |
| 000001H | PDR1 | Port 1 data register | Port 1 | XXXXXXXXB |
| 000002H | PDR2 | Port 2 data register | Port 2 | XXXXXXXXB |
| 000003H | PDR3 | Port 3 data register | Port 3 | XXXXXXXXB |
| 000004H | PDR4 | Port 4 data register | Port 4 | XXXXXXXXB |
| 000005H | PDR5 | Port 5 data register | Port 5 | XXXXXXXXB |
| 000006H | PDR6 | Port 6 data register | Port 6 | XXXXXXXXB |
| 000007H | PDR7 | Port 7 data register | Port 7 | XXXXXXXXB |
| 000008H | PDR8 | Port 8 data register | Port 8 | XXXXXXXXB |
| 000009H | PDR9 | Port 9 data register | Port 9 | XXXXXXXXB |
| 00000AH | PDRA | Port A data register | Port A | XXXXXXXXB |
| 00000BH | LCDCMR | Port 7/COM pin selection register | Port 7, LCD controller/driver | XXXX0000B |
| 00000CH | OCP4 | OCU compare register ch.4 | 16-bit I/O timer | XXXXXXXXB |
| 00000DH | | | | XXXXXXXXB |
| 00000EH | (Access prohibited) | | | |
| 00000FH | EIFR | Wakeup interrupt flag register | Wakeup interrupts | XXXXXXX0B |
| 000010H | DDR0 | Port 0 direction register | Port 0 | 00000000B |
| 000011H | DDR1 | Port 1 direction register | Port 1 | 00000000B |
| 000012H | DDR2 | Port 2 direction register | Port 2 | 00000000B |
| 000013H | DDR3 | Port 3 direction register | Port 3 | 00000000B |
| 000014H | DDR4 | Port 4 direction register | Port 4 | 00000000B |
| 000015H | DDR5 | Port 5 direction register | Port 5 | XXX00000B |
| 000016H | DDR6 | Port 6 direction register | Port 6 | 00000000B |
| 000017H | DDR7 | Port 7 direction register | Port 7 | 00000000B |
| 000018H | DDR8 | Port 8 direction register | Port 8 | 00000000B |
| 000019H | DDR9 | Port 9 direction register | Port 9 | 00000000B |
| 00001AH | DDRA | Port A direction register | Port A | 00000000B |
| 00001BH | ADER | Analog input enable register | Port 6, A/D converter | 11111111B |
| 00001CH | OCP5 | OCU compare register ch.5 | 16-bit I/O timer | XXXXXXXXB |
| 00001DH | | | | XXXXXXXXB |
| 00001EH | (Access prohibited) | | | |
| 00001FH | EICR | Wakeup interrupt enable register | Wakeup interrupts | 00000000B |

*(Continued)*

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 000020H | SMR | Serial mode register | UART (SCI) | 00000000B |
| 000021H | SCR | Serial control register | | 00000100B |
| 000022H | SIDR/ SODR | Serial input data register/ Serial output data register | | XXXXXXXXB |
| 000023H | SSR | Serial status register | | 00001X00B |
| 000024H | SMCS1 | Serial mode control status register 1 | Extended I/O serial interface 1 | XXXX0000B |
| 000025H | | | | 00000010B |
| 000026H | SDR1 | Serial data register 1 | | XXXXXXXXB |
| 000027H | CDCR | Communication prescaler control register | Communication prescaler register | 0XXX1111B |
| 000028H | SMCS2 | Serial mode control status register 2 | Extended I/O serial interface 2 | XXXX0000B |
| 000029H | | | | 00000010B |
| 00002AH | SDR2 | Serial data register 2 | | XXXXXXXXB |
| 00002BH | (Access prohibited) | | | |
| 00002CH | OCS45 | OCU control status register ch.45 | 16-bit I/O timer | 0000XX00B |
| 00002DH | | | | XXX00000B |
| 00002EH | OCS67 | OCU control status register ch.67 | | 0000XX00B |
| 00002FH | | | | XXX00000B |
| 000030H | ENIR | DTP/interrupt enable register | DTP /external interrupt circuit | 00000000B |
| 000031H | EIRR | DTP/interrupt request register | | XXXXXXXXB |
| 000032H | ELVR | Request level setting register | | 00000000B |
| 000033H | | | | 00000000B |
| 000034H | OCP6 | OCU compare register ch.6 | 16-bit I/O timer | XXXXXXXXB |
| 000035H | | | | XXXXXXXXB |
| 000036H | ADCS | A/D control status register | 8/10-bit A/D converter | 00000000B |
| 000037H | | | | 00000000B |
| 000038H | ADCR | A/D data register | | XXXXXXXXB |
| 000039H | | | | 00001XXXB |
| 00003AH | DADR0 | D/A converter data register ch.0 | 8-bit D/A converter | XXXXXXXXB |
| 00003BH | DADR1 | D/A converter data register ch.1 | | XXXXXXXXB |
| 00003CH | DACR0 | D/A control register 0 | | XXXXXXX0B |
| 00003DH | DACR1 | D/A control register 1 | | XXXXXXX0B |
| 00003EH | CLKR | Clock output enable register | Clock monitor function | XXXX0000B |

*(Continued)*

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 00003F$_H$ | (Access prohibited) | | | |
| 000040$_H$ | PRLL0 | PPG0 reload register L | 8/16-bit PPG timer 0, 1 | XXXXXXXX$_B$ |
| 000041$_H$ | PRLH0 | PPG0 reload register H | | XXXXXXXX$_B$ |
| 000042$_H$ | PRLL1 | PPG1 reload register L | | XXXXXXXX$_B$ |
| 000043$_H$ | PRLH1 | PPG1 reload register H | | XXXXXXXX$_B$ |
| 000044$_H$ | PPGC0 | PPG0 operation mode control register | | 0X000XX1$_B$ |
| 000045$_H$ | PPGC1 | PPG1 operation mode control register | | 0X000001$_B$ |
| 000046$_H$ | PPGOE | PPG0, 1 output control register | | 00000000$_B$ |
| 000047$_H$ | (Access prohibited) | | | |
| 000048$_H$ | TMCSR0 | Timer control status register ch.0 | 16-bit reload timer 0 | 00000000$_B$ |
| 000049$_H$ | | | | XXXX0000$_B$ |
| 00004A$_H$ | TMR0/ TMRLR0 | 16-bit timer register ch.0/ 16-bit reload register ch.0 | | XXXXXXXX$_B$ |
| 00004B$_H$ | | | | XXXXXXXX$_B$ |
| 00004C$_H$ | TMCSR1 | Timer control status register ch.1 | 16-bit reload timer 1 | 00000000$_B$ |
| 00004D$_H$ | | | | XXXX0000$_B$ |
| 00004E$_H$ | TMR1/ TMRLR1 | 16-bit timer register ch.1/ 16-bit reload register ch.1 | | XXXXXXXX$_B$ |
| 00004F$_H$ | | | | XXXXXXXX$_B$ |
| 000050$_H$ | IPCP0 | ICU data register ch.0 | 16-bit I/O timer | XXXXXXXX$_B$ |
| 000051$_H$ | | | | XXXXXXXX$_B$ |
| 000052$_H$ | IPCP1 | ICU data register ch.1 | | XXXXXXXX$_B$ |
| 000053$_H$ | | | | XXXXXXXX$_B$ |
| 000054$_H$ | ICS01 | ICU control status register | | 00000000$_B$ |
| 000055$_H$ | (Access prohibited) | | | |
| 000056$_H$ | TCDT0 | Freerun timer data register 0 | 16-bit I/O timer | 00000000$_B$ |
| 000057$_H$ | | | | 00000000$_B$ |
| 000058$_H$ | TCCS0 | Freerun timer control status register 0 | | 00000000$_B$ |
| 000059$_H$ | (Access prohibited) | | | |
| 00005A$_H$ | OCP0 | OCU compare register ch.0 | 16-bit I/O timer | XXXXXXXX$_B$ |
| 00005B$_H$ | | | | XXXXXXXX$_B$ |
| 00005C$_H$ | OCP1 | OCU compare register ch.1 | | XXXXXXXX$_B$ |
| 00005D$_H$ | | | | XXXXXXXX$_B$ |
| 00005E$_H$ | OCP2 | OCU compare register ch.2 | | XXXXXXXX$_B$ |
| 00005F$_H$ | | | | XXXXXXXX$_B$ |

*(Continued)*

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 000060H | OCP3 | OCU compare register ch.3 | 16-bit I/O timer | XXXXXXXXB |
| 000061H | | | | XXXXXXXXB |
| 000062H | OCS01 | OCU control status register ch.0, ch.1 | | 0000XX00B |
| 000063H | | | | XXX00000B |
| 000064H | OCS23 | OCU control status register ch.2, ch.3 | | 0000XX00B |
| 000065H | | | | XXX00000B |
| 000066H | TCDT1 | Freerun timer data register 1 | 16-bit I/O timer | 00000000B |
| 000067H | | | | 00000000B |
| 000068H | TCCS1 | Freerun timer control status register 1 | | 00000000B |
| 000069H | (Access prohibited) | | | |
| 00006AH | LCR0 | LCDC control register 0 | LCD controller/driver | 00010000B |
| 00006BH | LCR1 | LCDC control register 1 | | 00000000B |
| 00006CH | OCP7 | OCU compare register ch.7 | 16-bit I/O timer | XXXXXXXXB |
| 00006DH | | | | XXXXXXXXB |
| 00006EH | (Access prohibited) | | | |
| 00006FH | ROMM | ROM mirror function selection register | ROM mirror function selection module | XXXXXXX1B |
| 000070H to 00007FH | VRAM | Data memory for LCD display | LCD controller/driver | XXXXXXXXB |
| 000080H | UDCR0 | Up/down count register 0 | 8/16-bit up/down counter/timer 0, 1 | 00000000B |
| 000081H | UDCR1 | Up/down count register 1 | | 00000000B |
| 000082H | RCR0 | Reload compare register 0 | | 00000000B |
| 000083H | RCR1 | Reload compare register 1 | | 00000000B |
| 000084H | CSR0 | Counter status register 0 | | 00000000B |
| 000085H | (Reserved) *3 | | | |
| 000086H | CCR0 | Counter control register 0 | 8/16-bit up/down counter/timer 0, 1 | X0000000B |
| 000087H | | | | 00000000B |
| 000088H | CSR1 | Counter status register 1 | | 00000000B |
| 000089H | (Reserved) *3 | | | |
| 00008AH | CCR1 | Counter control register 1 | 8/16-bit up/down counter/timer 0, 1 | X0000000B |
| 00008BH | | | | X0000000B |
| 00008CH | RDR0 | Port 0 input pull-up resistor setup register | Port 0 | 00000000B |
| 00008DH | RDR1 | Port 1 input pull-up resistor setup register | Port 1 | 00000000B |

*(Continued)*

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 00008E$_H$ | RDR4 | Port 4<br>input pull-up resistor setup register | Port 4 | 00000000$_B$ |
| 00008F$_H$<br>to<br>00009D$_H$ | (Access prohibited)<br>(Area reserved for system use) *4 | | | |
| 00009E$_H$ | PACSR | Address detection control register | Address match detection function | 00000000$_B$ |
| 00009F$_H$ | DIRR | Delayed interrupt request output/clear register | Delayed interrupt generation module | XXXXXXX0$_B$ |
| 0000A0$_H$ | LPMCR | Low power consumption mode control register | Low power consumption (standby) mode | 00011000$_B$ |
| 0000A1$_H$ | CKSCR | Clock selection register | | 11111100$_B$ |
| 0000A2$_H$<br>to<br>0000A7$_H$ | (Access prohibited) | | | |
| 0000A8$_H$ | WDTC | Watchdog timer control register | Watchdog timer | XXXXXXXX$_B$ |
| 0000A9$_H$ | TBTC | Timebase timer control register | Timebase timer | 1XX00000$_B$ |
| 0000AA$_H$ | WTC | Clock timer control register | Clock timer | 1X001000$_B$ |
| 0000AB$_H$<br>to<br>0000AD$_H$ | (Access prohibited) | | | |
| 0000AE$_H$ | FMCS | Flash memory control status register | 1 Mbit flash memory | 000X0000$_B$ |
| 0000AF$_H$ | (Access prohibited) | | | |
| 0000B0$_H$ | ICR00 | Interrupt control register 00 | Interrupt controller | 00000111$_B$ |
| 0000B1$_H$ | ICR01 | Interrupt control register 01 | | 00000111$_B$ |
| 0000B2$_H$ | ICR02 | Interrupt control register 02 | | 00000111$_B$ |
| 0000B3$_H$ | ICR03 | Interrupt control register 03 | | 00000111$_B$ |
| 0000B4$_H$ | ICR04 | Interrupt control register 04 | | 00000111$_B$ |
| 0000B5$_H$ | ICR05 | Interrupt control register 05 | | 00000111$_B$ |
| 0000B6$_H$ | ICR06 | Interrupt control register 06 | | 00000111$_B$ |
| 0000B7$_H$ | ICR07 | Interrupt control register 07 | | 00000111$_B$ |
| 0000B8$_H$ | ICR08 | Interrupt control register 08 | | 00000111$_B$ |
| 0000B9$_H$ | ICR09 | Interrupt control register 09 | | 00000111$_B$ |
| 0000BA$_H$ | ICR10 | Interrupt control register 10 | | 00000111$_B$ |
| 0000BB$_H$ | ICR11 | Interrupt control register 11 | | 00000111$_B$ |
| 0000BC$_H$ | ICR12 | Interrupt control register 12 | | 00000111$_B$ |
| 0000BD$_H$ | ICR13 | Interrupt control register 13 | | 00000111$_B$ |

*(Continued)*

*(Continued)*

| Address | Abbreviated Register Name | Register Name | Peripheral Name | Initial Value |
|---|---|---|---|---|
| 0000BE$_H$ | ICR14 | Interrupt control register 14 | Interrupt controller | 00000111$_B$ |
| 0000BF$_H$ | ICR15 | Interrupt control register 15 | | 00000111$_B$ |
| 0000C0$_H$ to 0000FF$_H$ | (Access prohibited) *1 | | | |
| 000100$_H$ to 00####$_H$ | (RAM area) *2 | | | |
| 00####$_H$ to 001FEF$_H$ | (Reserved area) *3 | | | |
| 001FF0$_H$ | PADR0 | Detection address setting register 0 (low byte) | Address match detection function | XXXXXXXX$_B$ |
| 001FF1$_H$ | | Detection address setting register 0 (middle byte) | | XXXXXXXX$_B$ |
| 001FF2$_H$ | | Detection address setting register 0 (high byte) | | XXXXXXXX$_B$ |
| 001FF3$_H$ | PADR1 | Detection address setting register 1 (low byte) | | XXXXXXXX$_B$ |
| 001FF4$_H$ | | Detection address setting register 1 (middle byte) | | XXXXXXXX$_B$ |
| 001FF5$_H$ | | Detection address setting register 1 (high byte) | | XXXXXXXX$_B$ |
| 001FF6$_H$ to 001FFF$_H$ | (Reserved area) *3 | | | |

Initial value notation

0 : Initial value of bit is “0”.

1 : Initial value of bit is “1”.

X : Initial value of bit is undefined.

*1 : Access is prohibited to the address range 0000C0$_H$ to 0000FF$_H$. See the “■ MEMORY MAP” section.

*2 : See the “■ MEMORY MAP” section for details of the “ (RAM area) ”.

*3 : “ (Reserved areas) ” are addresses used internally by the system and may not be used.

*4 : The “ (Area reserved for system use) ” contains setting registers used by the evaluation tools.

Notes : • LPMCR, CKSCR, and WDTC are initialized by some types of reset and not by others. The initial values listed are for the case when the registers are initialized.

• The boundary address “####$_H$” between the “ (RAM area) ” and “ (Reserved area) ” differs depending on the product. See the “■ MEMORY MAP” section for details.

• OCU compare registers ch.0 to ch.3 use 16-bit freerun timer 0 and OCU compare registers ch.4 to ch.7 use 16-bit freerun timer 1. Note that 16-bit freerun timer 0 is also used by input capture 0 and 1 (ICU) .

## ■ INTERRUPTS, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt | EI²OS Support | Interrupt Vector | | Interrupt Control Register | | Priority |
|---|---|---|---|---|---|---|
| | | No. | Address | ICR | Address | |
| Reset | × | #08 | FFFFDC$_H$ | — | — | High |
| INT 9 instruction | × | #09 | FFFFD8$_H$ | — | — | |
| Exception | × | #10 | FFFFD4$_H$ | — | — | |
| 8/10-bit A/D converter | ○ | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ | |
| Timebase timer | × | #12 | FFFFCC$_H$ | | | |
| DTP0/DTP1 (external interrupt 0/external interrupt 1) | ○ | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ | |
| 16-bit freerun timer 0 overflow | × | #14 | FFFFC4$_H$ | | | |
| Extended I/O serial interface 1 | ○ | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ | |
| Wakeup interrupt | × | #16 | FFFFBC$_H$ | | | |
| Extended I/O serial interface 2 | ○ | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ | |
| DTP2/DTP3 (external interrupt 2/external interrupt 3) | ○ | #18 | FFFFB4$_H$ | | | |
| 8/16-bit PPG timer 0 counter borrow | × | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ | |
| DTP4/DTP5 (external interrupt 4/external interrupt 5) | ○ | #20 | FFFFAC$_H$ | | | |
| 8/16-bit up/down counter/timer 0 compare match | ○ | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ | |
| 8/16-bit up/down counter/timer 0 overflow, up/down direction change | ○ | #22 | FFFFA4$_H$ | | | |
| 8/16-bit PPG timer 1 counter borrow | × | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ | |
| DTP6/DTP7 (external interrupt 6/external interrupt 7) | ○ | #24 | FFFF9C$_H$ | | | |
| Output compare 1 (OCU) ch.4, ch.5 match | ○ | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ | |
| Clock timer | × | #26 | FFFF94$_H$ | | | |
| Output compare 1 (OCU) ch.6, ch.7 match | ○ | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ | |
| 16-bit freerun timer 1 overflow | × | #28 | FFFF8C$_H$ | | | |
| 8/16-bit up/down counter/timer 1 compare match | ○ | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ | |
| 8/16-bit up/down counter/timer 1 overflow, up/down direction change | ○ | #30 | FFFF84$_H$ | | | |
| Input capture 0 (ICU) capture | ○ | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ | |
| Input capture 1 (ICU) capture | ○ | #32 | FFFF7C$_H$ | | | |
| Output compare 0 (OCU) ch.0 match | ○ | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ | |
| Output compare 0 (OCU) ch.1 match | ○ | #34 | FFFF74$_H$ | | | |

*(Continued)*

*(Continued)*

| Interrupt | EI²OS Support | Interrupt Vector | | Interrupt Control Register | | Priority |
|---|---|---|---|---|---|---|
| | | No. | Address | ICR | Address | |
| Output compare 0 (OCU) ch.2 match | ○ | #35 | FFFF70H | ICR12 | 0000BCH | ↓ |
| Output compare 0 (OCU) ch.3 match | ○ | #36 | FFFF6CH | | | |
| UART (SCI) receive complete | ◎ | #37 | FFFF68H | ICR13 | 0000BDH | |
| 16-bit reload timer 0 | ○ | #38 | FFFF64H | | | |
| UART (SCI) send complete | ◎ | #39 | FFFF60H | ICR14 | 0000BEH | |
| 16-bit reload timer 1 | ○ | #40 | FFFF5CH | | | |
| Flash memory | × | #41 | FFFF58H | ICR15 | 0000BFH | |
| Delayed interrupt generation module | × | #42 | FFFF54H | | | Low |

○ : Supported

× : Not supported

◎ : Supported, includes EI²OS stop function

## ■ PERIPHERAL RESOURCES

### 1. I/O Ports

- The I/O ports can be used as general-purpose I/O ports (parallel I/O ports) . The MB90520A and 520B series have 11 ports (85 pins) . The ports share pins with the inputs and outputs of the peripheral functions.
- The port data registers (PDR) are used to output data to the I/O pins and capture the input signals from the I/O ports.
  Similarly, the port direction registers (DDR) set the I/O direction (input or output) for each individual port bit.
- The following tables list the I/O ports and peripheral functions with which they share pins.

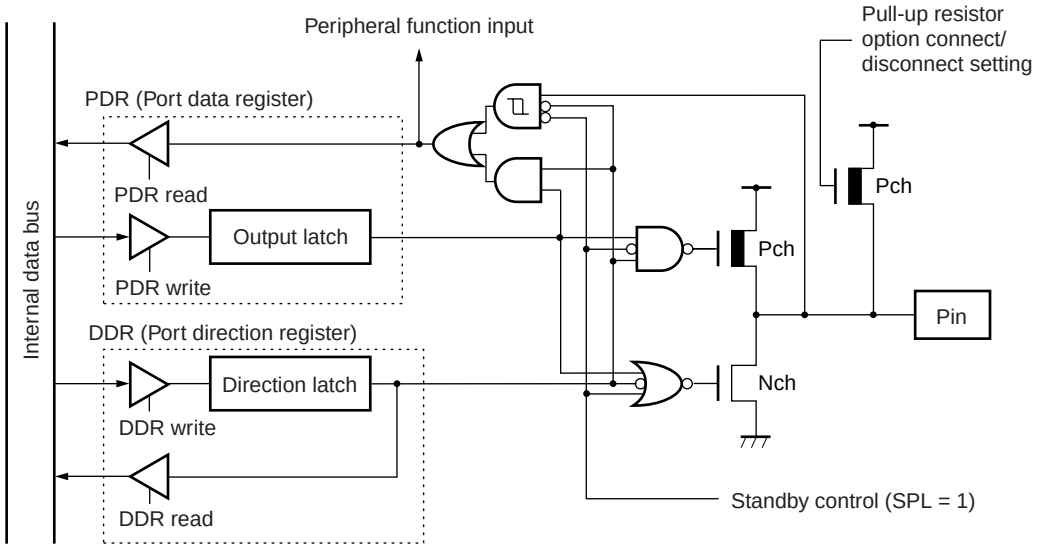
| | Pin Name (Port) | Pin Name (Peripheral) | Peripheral Function that Shares Pin |
|---|---|---|---|
| Port 0 | P00 – P06 | INT0 – INT6 | External interrupts |
| | P07 | — | Not shared |
| Port 1 | P10 – P17 | WI0 – WI7 | Wakeup interrupts |
| Port 2 | P20 – P23 | IN00 – IN11 | Input capture (unit 0) |
| | P24, P25 | AIN0, BIN0 | 8/16-bit up/down counter/timer 0 |
| | P26 | ZIN0/INT7 | 8/16-bit up/down counter/timer 0, external interrupt |
| Port 3 | P30 | — | Not shared |
| | P31 | CKOT | Clock monitor function |
| | P32 – P35 | OUT0 – OUT3 | Output compare (unit 0) |
| | P36, P37 | PPG00, PPG01 | 8/16-bit PPG timer 0 |
| Port 4 | P40, P41 | PPG10, PPG11 | 8/16-bit PPG timer 1 |
| | P42 – P44 | SIN0, SOT0, SCK0 | UART (SCI) |
| | P45 – P47 | SIN1, SOT1, SCK1 | Extended I/O serial interface 0 |
| Port 5 | P50 – P52 | SIN2/AIN1,<br>SOT1/BIN1,<br>SCK1/ZIN1 | 8/16-bit up/down counter/timer 0<br>Extended I/O serial interface 1 |
| | P53, P54 | DA0, DA1 | 8-bit D/A converter |
| Port 6 | P60 – P67 | AN0 – AN7 | 8/16-bit A/D converter |
| Port 7 | P70 – P73 | TIN0/OUT4,<br>TOT0/OUT5,<br>TIN1/OUT6,<br>TOT1/OUT7 | 16-bit reload timers 0, 1<br>Output compare (unit 1) |
| | P74 – P77 | COM0 – COM3 | LCD control driver common output |
| Port 8 | P80 – P87 | SEG16 – SEG23 | LCD control driver segment output |
| Port 9 | P90 – P97 | SEG24 – SEG31 | LCD control driver segment output |
| Port A | PA0 – PA7 | SEG8 – SEG15 | LCD control driver segment output |

Notes

- Port 9 contains general-purpose I/O ports with N-ch open-drain output circuits.
- Connect an external pull-up resistor when using port 9 pins as outputs.
- Port 6 shares pins with the analog inputs. When using port 6 as a general-purpose port, ensure that the corresponding analog input enable register (ADER) bits are set to “0”. ADER is initialized to “$FF_H$” after a reset.

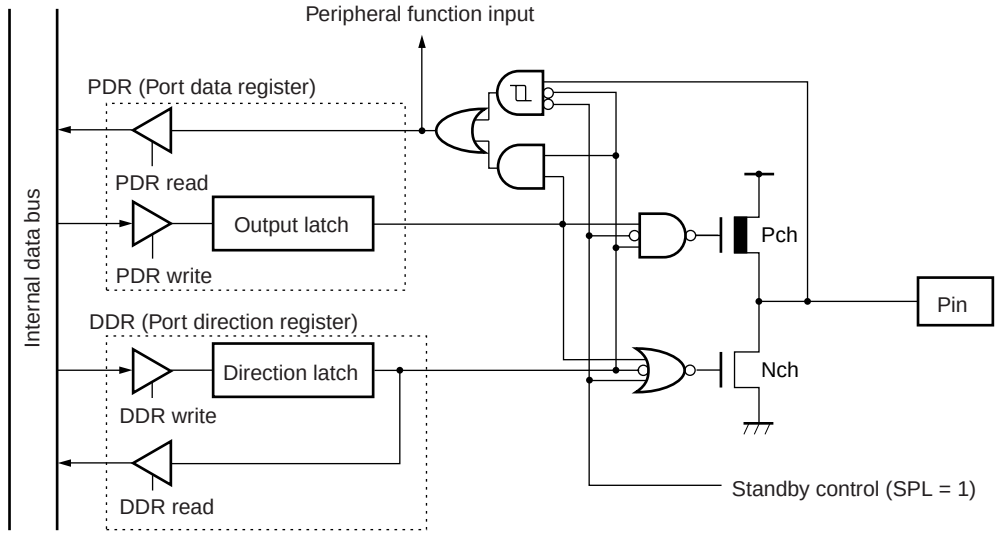
• **Block diagrams**

**P00 to P07, P10 to P17**



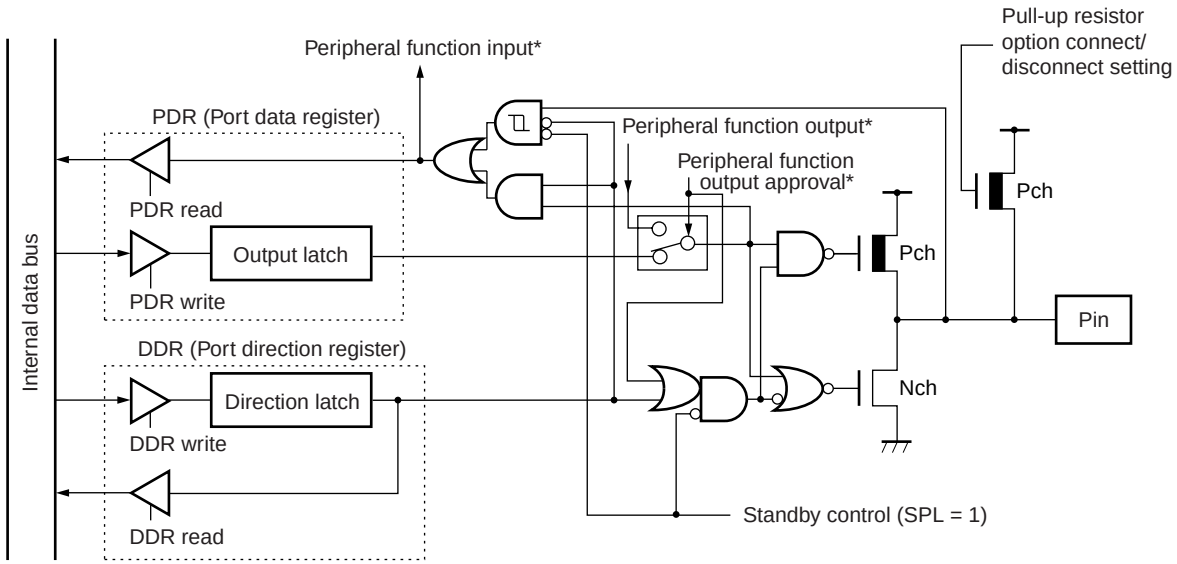

Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

**P20 to P27**




Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

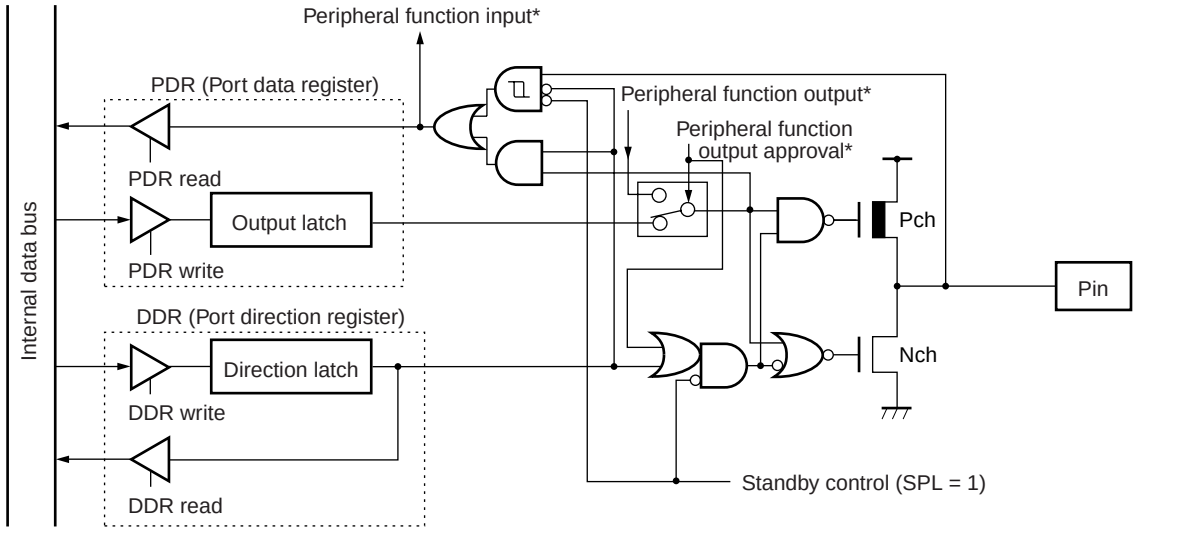
**P40 to P47**




Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

* : Peripheral function I/O is equivalent to I/O of peripheral function.

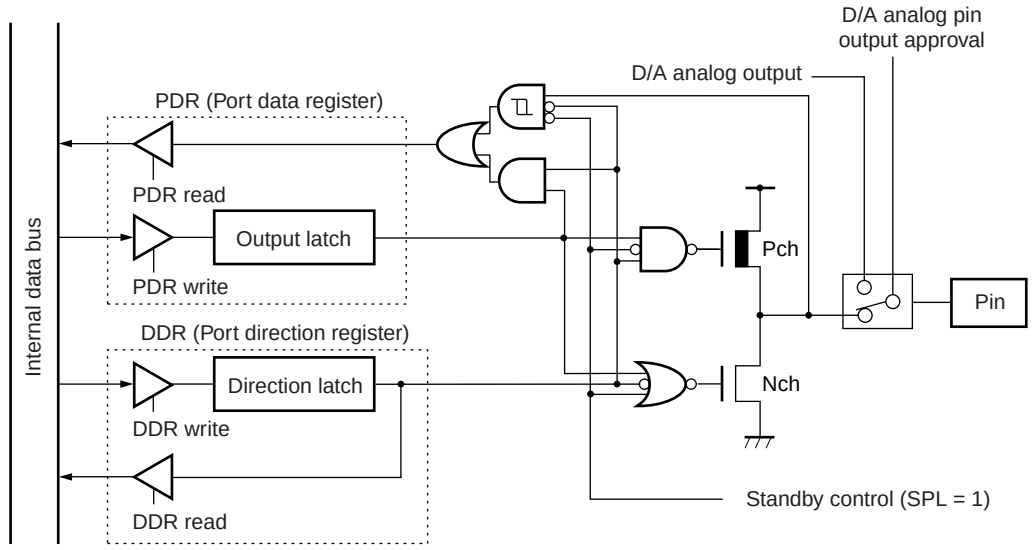
**P30 to P37, P50 to P52, P70 to P73**




Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

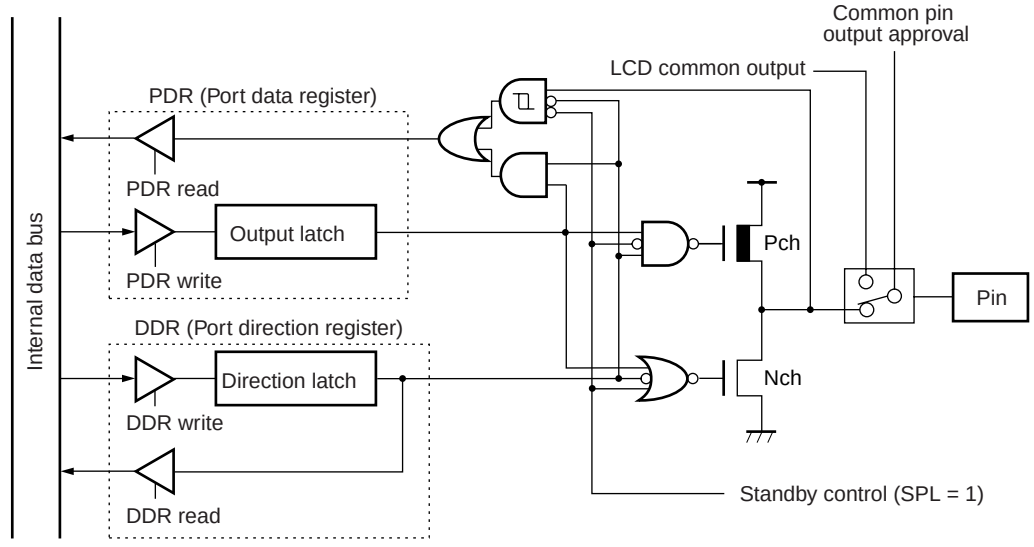
* : Peripheral function I/O is equivalent to I/O of peripheral function.

**P53, P54**



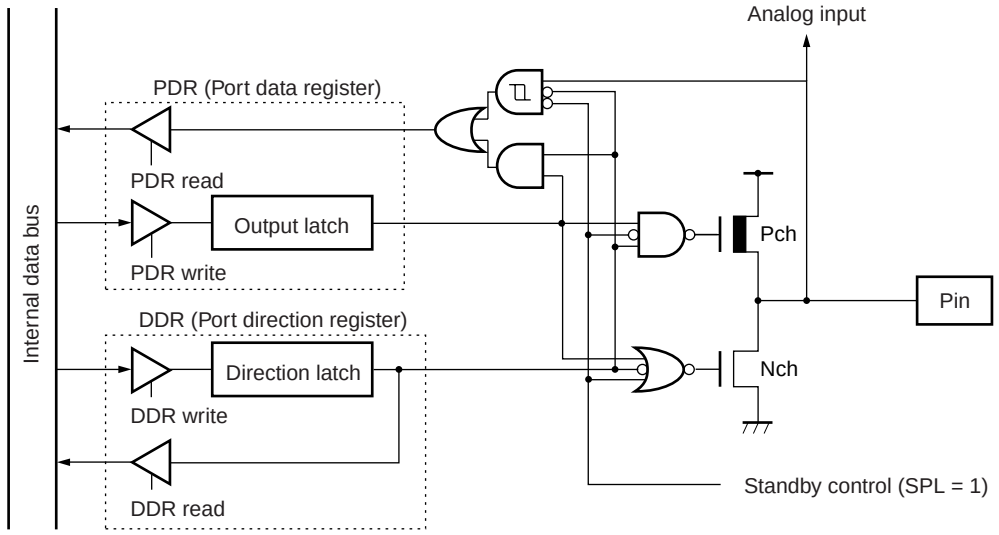

Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

**P74 to P77**



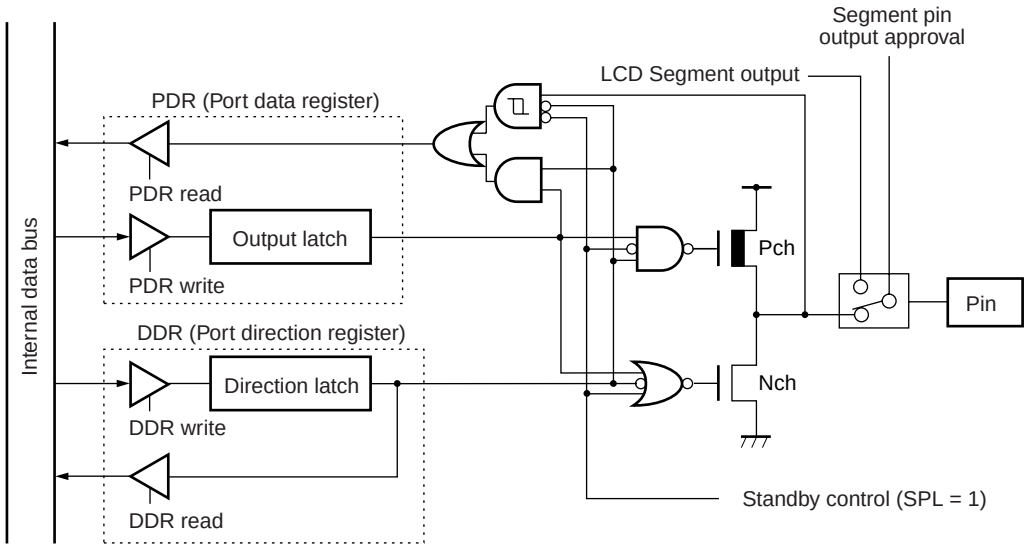

Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

**P60 to P67**



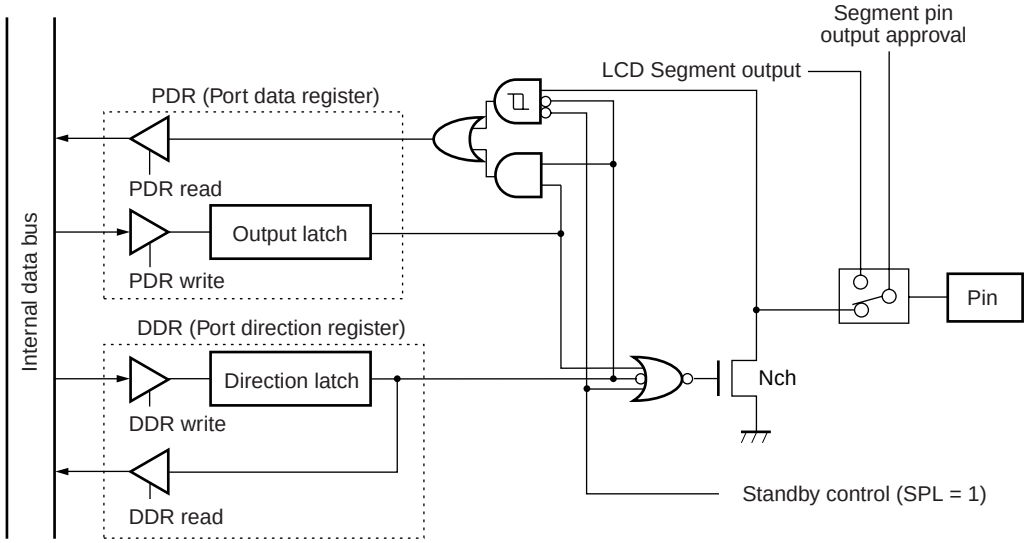

Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

**P80 to P87, PA0 to PA7**




Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

**P90 to P97**




Standby control : Controls stop mode (SPL = 1) , time-base-timer mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode

## 2. Timebase Timer

- The timebase timer is an 18-bit freerun timer (timebase timer/counter) that counts up synchronized with the main clock (oscillation clock : HCLK divided by 2) .
- The timer can generate interrupt requests at a specified interval, with four different interval time settings available.
- The timer supplies the operating clock for peripheral functions including the oscillation stabilization delay timer and watchdog timer.

**• Timebase timer interval settings**

| Internal Count Clock Period | Interval Time |
|---|---|
| 2/HCLK (0.5 µs) | $2^{12}$/HCLK (approx. 1.024 ms) |
| | $2^{14}$/HCLK (approx. 4.096 ms) |
| | $2^{16}$/HCLK (approx. 16.384 ms) |
| | $2^{19}$/HCLK (approx. 131.072 ms) |

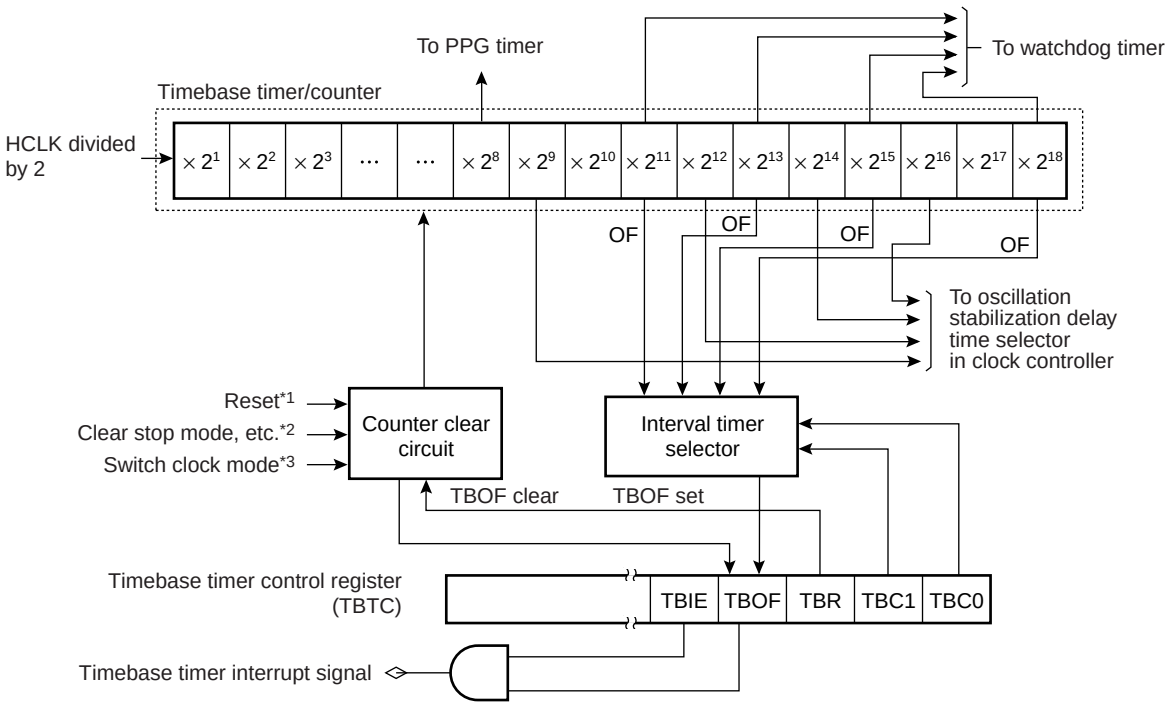
- HCLK : Oscillation clock frequency
- The values enclosed in ( ) indicate the times for a clock frequency of 4 MHz.

**• Period of clocks supplied from timebase timer**

| Peripheral Function | Clock Period |
|---|---|
| Oscillation stabilization delay for the main clock | $2^{10}$/HCLK (approx. 0.256 ms) |
| | $2^{13}$/HCLK (approx. 2.048 ms) |
| | $2^{15}$/HCLK (approx. 8.192 ms) |
| | $2^{17}$/HCLK (approx. 32.768 ms) |
| Watchdog timer | $2^{12}$/HCLK (approx. 1.024 ms) |
| | $2^{14}$/HCLK (approx. 4.096 ms) |
| | $2^{16}$/HCLK (approx. 16.384 ms) |
| | $2^{19}$/HCLK (approx. 131.072 ms) |
| PPG timer | $2^{9}$/HCLK (approx. 0.128 ms) |

- HCLK : Oscillation clock frequency
- The values enclosed in ( ) indicate the times for a clock frequency of 4 MHz.

• **Block diagram**




OF : Overflow
HCLK : Oscillation clock frequency
*1 : Power-on reset, release of hardware standby mode, watchdog reset
*2 : Clear stop mode, main clock mode, PLL clock mode, and pseudo-clock mode
*3 : Main → PLL clock, Sub → main clock, Sub → PLL clock

The actual interrupt request number for the timebase timer is :

Interrupt request number : #12 ($0C_H$)

## 3. Watchdog Timer

- The watchdog timer is a timer/counter used to detect faults such as program runaway.
- The watchdog timer is a 2-bit counter that counts the clock signal from the timebase timer or clock timer.
- Once started, the watchdog timer must be cleared before the 2-bit counter overflows. If an overflow occurs, the CPU is reset.

**• Interval time for the watchdog timer**

| HCLK : Oscillation Clock (4 MHz) | | | SCLK : Sub-Clock (8.192 kHz) | | |
|---|---|---|---|---|---|
| **Min** | **Max** | **Clock Period** | **Min** | **Max** | **Clock Period** |
| Approx. 3.58 ms | Approx. 4.61 ms | $2^{14} \pm 2^{11}$ / HCLK | Approx. 0.438 s | Approx. 0.563 s | $2^{12} \pm 2^{9}$ / SCLK |
| Approx. 14.33 ms | Approx. 18.30 ms | $2^{16} \pm 2^{13}$ / HCLK | Approx. 3.500 s | Approx. 4.500 s | $2^{15} \pm 2^{12}$ / SCLK |
| Approx. 57.23 ms | Approx. 73.73 ms | $2^{18} \pm 2^{15}$ / HCLK | Approx. 7.000 s | Approx. 9.000 s | $2^{16} \pm 2^{13}$ / SCLK |
| Approx. 458.75 ms | Approx. 589.82 ms | $2^{21} \pm 2^{18}$ / HCLK | Approx. 14.00 s | Approx. 18.00 s | $2^{17} \pm 2^{14}$ / SCLK |

* : The difference between the maximum and minimum watchdog timer interval times is due to the timing when the counter is cleared.

* : As the watchdog timer is a 2-bit counter that counts the carry-up signal from the timebase timer or clock timer, clearing the timebase timer (when operating on HCLK) or the clock timer (when operating on SCLK) lengthens the time until the watchdog timer reset is generated.

**• Watchdog timer count clock**

| WTC : WDCS | HCLK : Oscillation clock<br>PCLK : PLL clock | SCLK : Sub-clock |
|---|---|---|
| “0” | Count the clock timer output. | Count the clock timer output. |
| “1” | Count the timebase timer output. | |

**• Events that stop the watchdog timer**

1 : Stop due to a power-on reset

2 : Reset due to recovery from hardware standby mode

3 : Watchdog reset

**• Events that clear the watchdog timer**

1 : External reset input from the RST pin.

2 : Writing “0” to the software reset bit.

3 : Writing “0” to the watchdog control bit (second and subsequent times) .

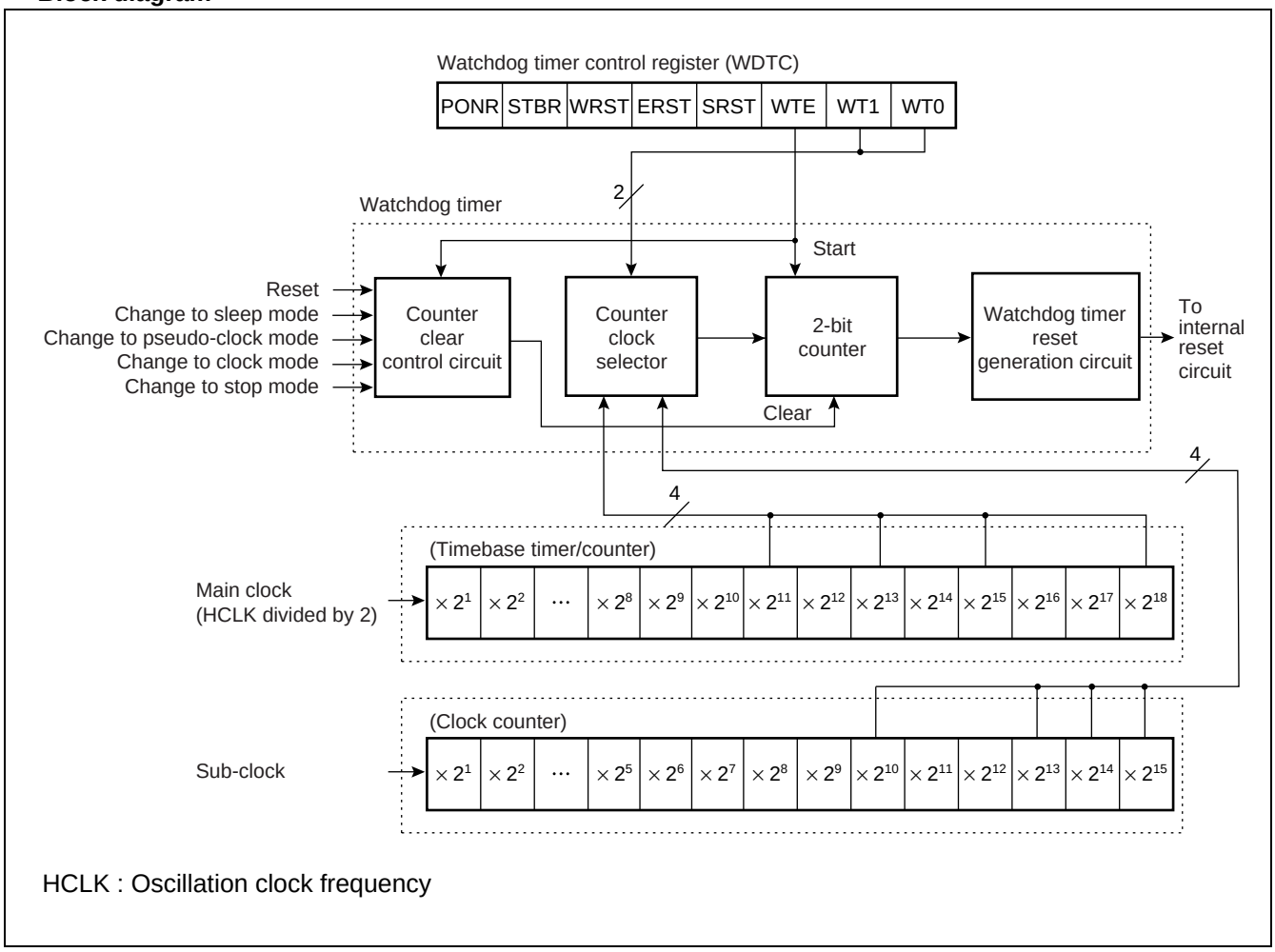
4 : Changing to sleep mode (clears the watchdog timer and temporarily halts the count) .

5 : Changing to pseudo-clock mode (clears the watchdog timer and temporarily halts the count) .

6 : Changing to clock mode (clears the watchdog timer and temporarily halts the count) .

7 : Changing to stop mode (clears the watchdog timer and temporarily halts the count) .

• **Block diagram**




HCLK : Oscillation clock frequency

### 4. 8/16-bit PPG (Programmable Pulse Generator) Timers 0 and 1

The 8/16-bit PPG timer is a two-channel reload timer module (PPG0 and PPG1) that can generate pulse outputs with the periods specified in the table below and with duty ratios between 0 and 100%. Note that the pulse periods are different depending on the operation mode.

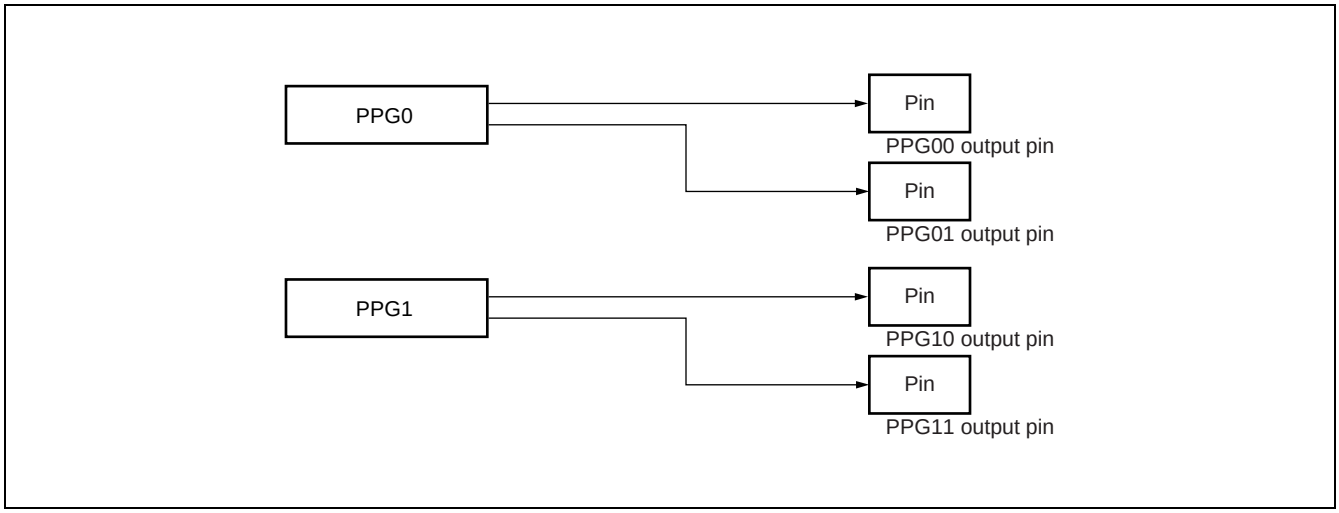
| Operation Mode | Count Clock*2 | PPG00, PPG01 (PPG ch0) | | PPG10, PPG11 (PPG ch1) | |
|---|---|---|---|---|---|
| | | Interval Time | Output Pulse Width | Interval Time | Output Pulse Width |
| 8-bit PPG output Independent 2ch operation mode | φ/1 (62.5 ns) | 1/φ to $2^8$/φ | 1/φ to $2^9$/φ | 1/φ to $2^8$/φ | 1/φ to $2^9$/φ |
| | φ/2 (125 ns) | 2/φ to $2^9$/φ | $2^2$/φ to $2^{10}$/φ | 2/φ to $2^9$/φ | $2^2$/φ to $2^{10}$/φ |
| | φ/4 (250 ns) | $2^2$/φ to $2^{10}$/φ | $2^3$/φ to $2^{11}$/φ | $2^2$/φ to $2^{10}$/φ | $2^3$/φ to $2^{11}$/φ |
| | φ/8 (500 ns) | $2^3$/φ to $2^{11}$/φ | $2^4$/φ to $2^{12}$/φ | $2^3$/φ to $2^{11}$/φ | $2^4$/φ to $2^{12}$/φ |
| | φ/16 (1000 ns) | $2^4$/φ to $2^{12}$/φ | $2^5$/φ to $2^{13}$/φ | $2^4$/φ to $2^{12}$/φ | $2^5$/φ to $2^{13}$/φ |
| | HCLK/512 (128 µs) | $2^9$/HCLK to $2^{17}$/HCLK | $2^{10}$/HCLK to $2^{18}$/HCLK | $2^9$/HCLK to $2^{17}$/HCLK | $2^{10}$/HCLK to $2^{18}$/HCLK |
| 16-bit PPG output operation mode | φ/1 (62.5 ns) | 1/φ to $2^{16}$/φ | 1/φ to $2^{17}$/φ | 1/φ to $2^{16}$/φ | 1/φ to $2^{17}$/φ |
| | φ/2 (125 ns) | 2/φ to $2^{17}$/φ | $2^2$/φ to $2^{18}$/φ | 2/φ to $2^{17}$/φ | $2^2$/φ to $2^{18}$/φ |
| | φ/4 (250 ns) | $2^2$/φ to $2^{18}$/φ | $2^3$/φ to $2^{19}$/φ | $2^2$/φ to $2^{18}$/φ | $2^3$/φ to $2^{19}$/φ |
| | φ/8 (500 ns) | $2^3$/φ to $2^{19}$/φ | $2^4$/φ to $2^{20}$/φ | $2^3$/φ to $2^{19}$/φ | $2^4$/φ to $2^{20}$/φ |
| | φ/16 (1000 ns) | $2^4$/φ to $2^{20}$/φ | $2^5$/φ to $2^{21}$/φ | $2^4$/φ to $2^{20}$/φ | $2^5$/φ to $2^{21}$/φ |
| | HCLK/512 (128 µs) | $2^9$/HCLK to $2^{25}$/HCLK | $2^{10}$/HCLK to $2^{26}$/HCLK | $2^9$/HCLK to $2^{25}$/HCLK | $2^{10}$/HCLK to $2^{26}$/HCLK |
| 8 + 8-bit PPG output operation mode*1 | φ/1 (62.5 ns) | 1/φ to $2^6$/φ | 1/φ to $2^9$/φ | 1/φ to $2^{16}$/φ | 1/φ to $2^{17}$/φ |
| | φ/2 (125 ns) | 2/φ to $2^9$/φ | $2^2$/φ to $2^{10}$/φ | 2/φ to $2^{17}$/φ | $2^2$/φ to $2^{18}$/φ |
| | φ/4 (250 ns) | $2^2$/φ to $2^{10}$/φ | $2^3$/φ to $2^{11}$/φ | $2^2$/φ to $2^{18}$/φ | $2^3$/φ to $2^{19}$/φ |
| | φ/8 (500 ns) | $2^3$/φ to $2^{11}$/φ | $2^4$/φ to $2^{12}$/φ | $2^3$/φ to $2^{19}$/φ | $2^4$/φ to $2^{20}$/φ |
| | φ/16 (1000 ns) | $2^4$/φ to $2^{12}$/φ | $2^5$/φ to $2^{13}$/φ | $2^4$/φ to $2^{20}$/φ | $2^5$/φ to $2^{21}$/φ |
| | HCLK/512 (128 µs) | $2^9$/HCLK to $2^{17}$/HCLK | $2^{10}$/HCLK to $2^{18}$/HCLK | $2^9$/HCLK to $2^{25}$/HCLK | $2^{10}$/HCLK to $2^{26}$/HCLK |

*1 : 8 + 8-bit PPG output operation mode consists of using the lower 8 bits as a prescaler for the PPG timer.

*2 : The values enclosed in ( ) indicate the times for a machine clock frequency of 16 MHz.

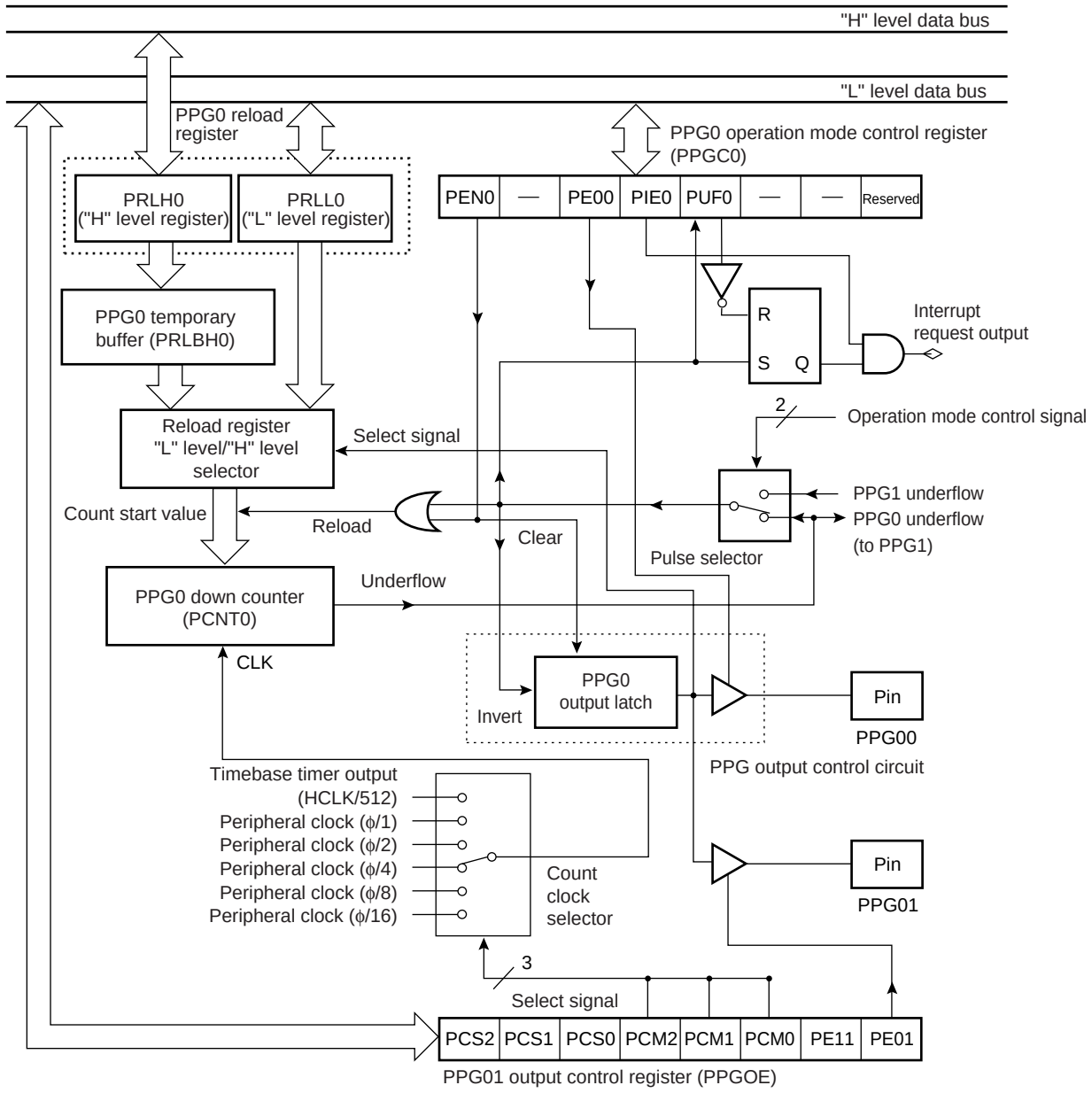
- **PPG timer channels and PPG pins**

The figure below shows the relationship between the 8/16-bit PPG channels and PPG pins on the MB90520A/520B series.



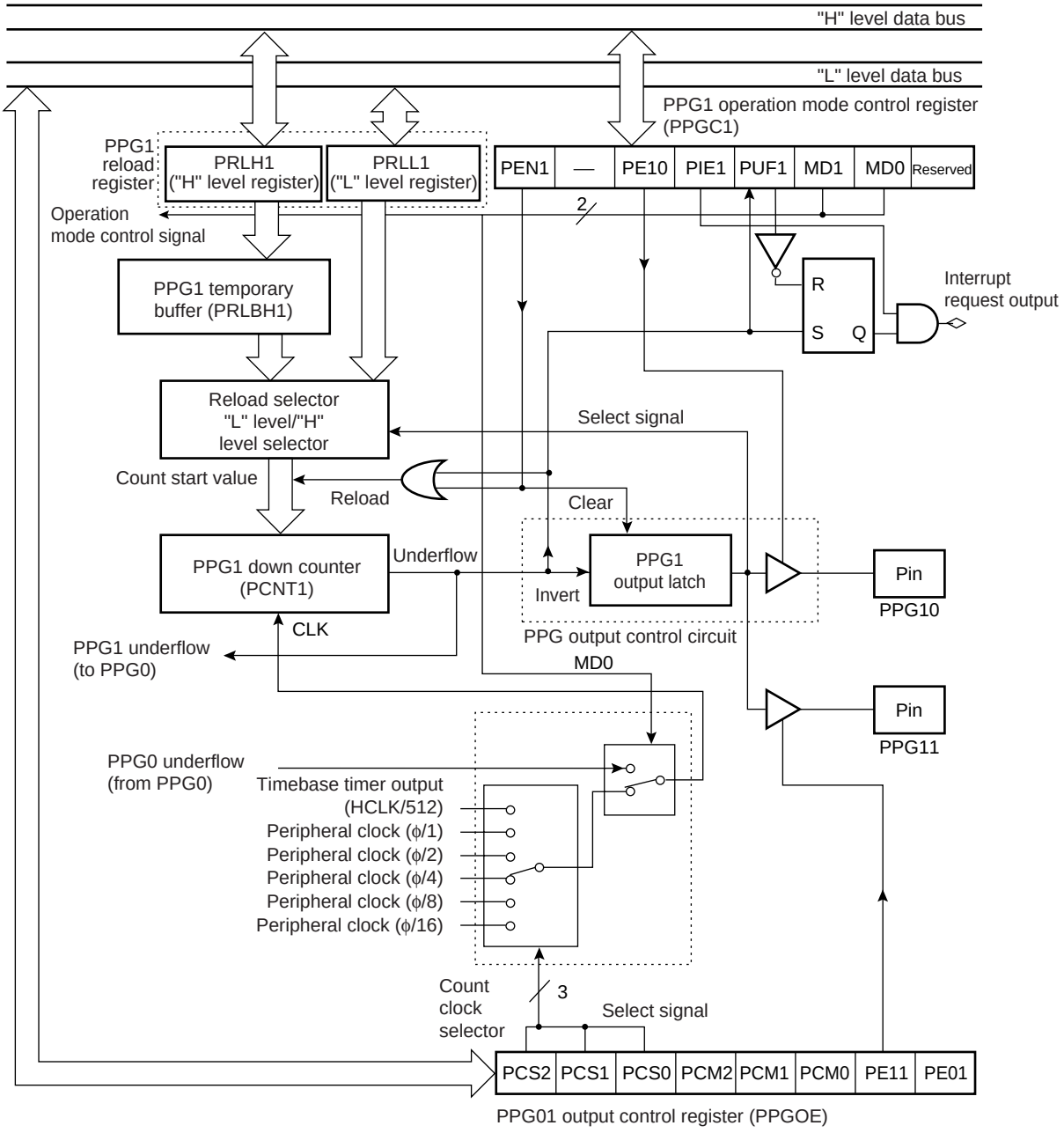
• **Block diagram**

**8/16-bit PPG timer 0**




— : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency

**8/16-bit PPG timer 1**




— : Undefined
Reserved : Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency

## 5. 16-bit Reload Timers 0 and 1 (With Event Count Function)

The 16-bit reload timers have the following functions.

- The count clock can be selected from three internal clock and the external event clock.
- Either software trigger or external trigger can be selected as the start signals for 16-bit reload timers 0 and 1.
- An interrupt to the CPU can be generated when an underflow occurs on 16-bit reload timer 0 and 1. This interrupt allows the timers to be used as interval timers.
- Two different operation modes can be selected when an underflow occurs on 16-bit reload timer 0 and 1 : one-shot mode in which timer operation halts when an underflow occurs or reload mode in which the reload register value is loaded into the timer and counting continues.
- Extended intelligent I/O service (EI$^2$OS) is supported.
- The MB90520A/520B series contains two 16-bit reload timer channels.

**• 16-bit reload timer operation modes**

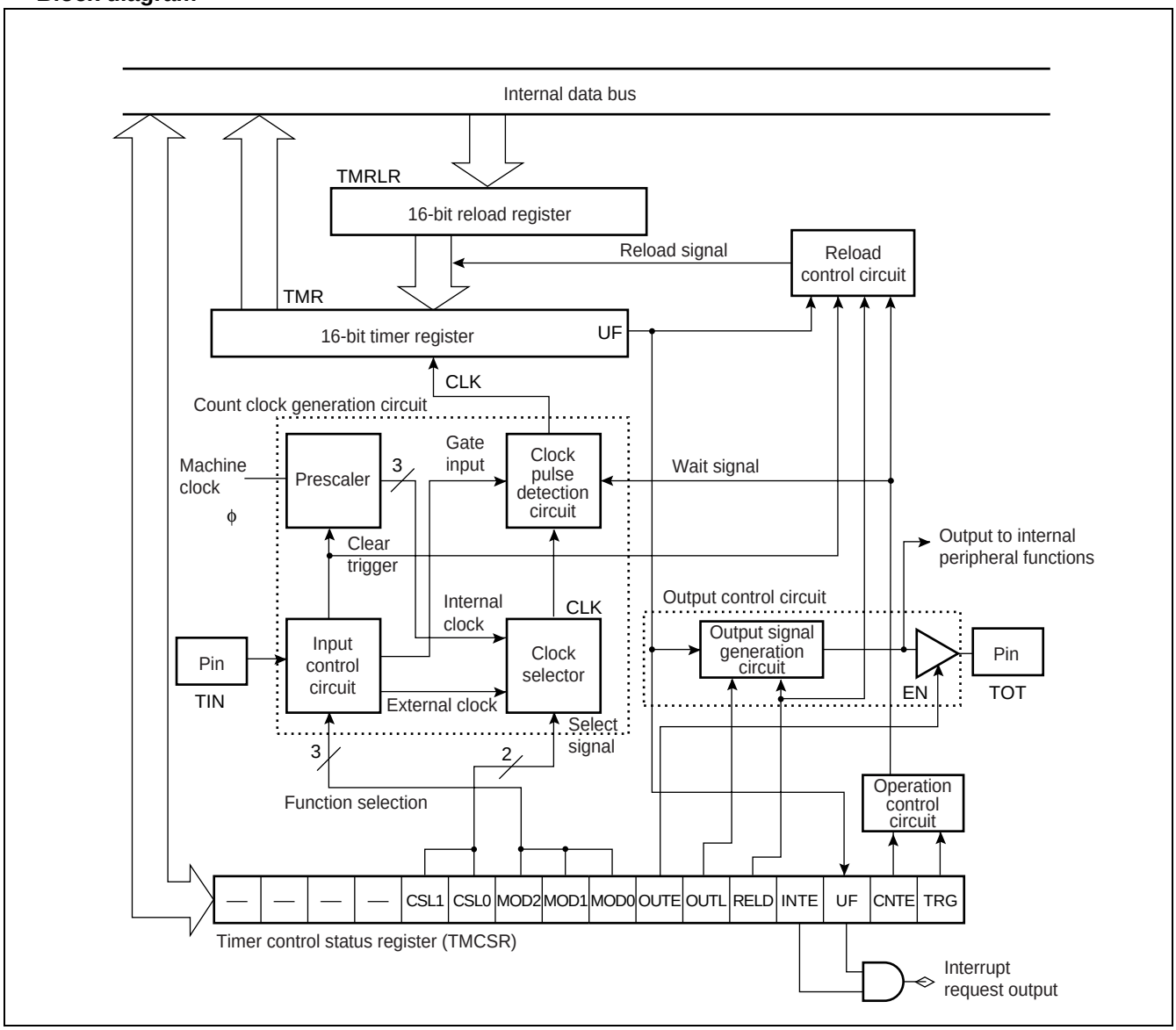
| Count Clock | Start Trigger | Operation when an Underflow Occurs |
|---|---|---|
| Internal clock (3 clocks available) | Software trigger | One-shot mode |
| | | Reload mode |
| | External trigger | One-shot mode |
| | | Reload mode |
| Event clock | Software trigger | One-shot mode |
| | | Reload mode |
| | External trigger | One-shot mode |
| | | Reload mode |

**• Interval times for the 16-bit reload timers**

| Count Clock | Count Clock Period | Example Interval Times |
|---|---|---|
| Internal clock | $2^1$T (0.125 µs) | 0.125 µs to 8.192 ms |
| | $2^3$T (0.5 µs) | 0.5 µs to 32.768 ms |
| | $2^5$T (2.0 µs) | 2.0 µs to 131.1 ms |
| Event clock | $2^3$T or longer | 0.5 µs or longer |

Note : The values enclosed in ( ) and the example interval times are for a machine clock frequency of 16 MHz.
"T" is the machine cycle and is 1/ (machine clock frequency) .

• **Block diagram**



## 6. 16-bit I/O Timers

The 16-bit I/O timers consist of a two-channel 16-bit freerun timer, two-channel input capture, and eight-channel output compare. The output compare channels can be used to generate eight independent waveform outputs based on the 16-bit freerun timer. The input capture channels can be used to measure input pulse widths and external clock periods.

**• Structure of I/O timers in the MB90520A/520B series**

| | 16-bit Freerun Timer | Output Compare | Input Capture |
|---|---|---|---|
| 16-bit I/O timer (unit 0) | 16-bit freerun timer 0 | Output compare 0 to 3 (unit 0) | Input capture 0 and 1 (unit 0) |
| 16-bit I/O timer (unit 1) | 16-bit freerun timer 1 | Output compare 4 to 8 (unit 1) | — |

**• 16-bit freerun timer functions**

- The count value for the 16-bit freerun timer sets the base time for the input capture and output compare functions.
- An interrupt can be generated when the 16-bit freerun timer overflows.
- Extended intelligent I/O service (EI$^2$OS) can be generated.
- 16-bit freerun timers 0 and 1 can be cleared to "$0000_H$" when an external reset is input, on setting the timer clear bit (TCCS : CLR = 1) , and when a compare match occurs on output compare 0 to 4.
- The count clock frequency can be selected from the following four clocks :
  4/$\phi$ (250 ns) , 16/$\phi$ (1.0 µs) , 64/$\phi$ (4.0 µs) , 256/$\phi$ (16.0 µs)

Note : $\phi$ is the machine clock frequency. The values in ( ) are for 16 MHz machine clock.

**• Input capture functions**

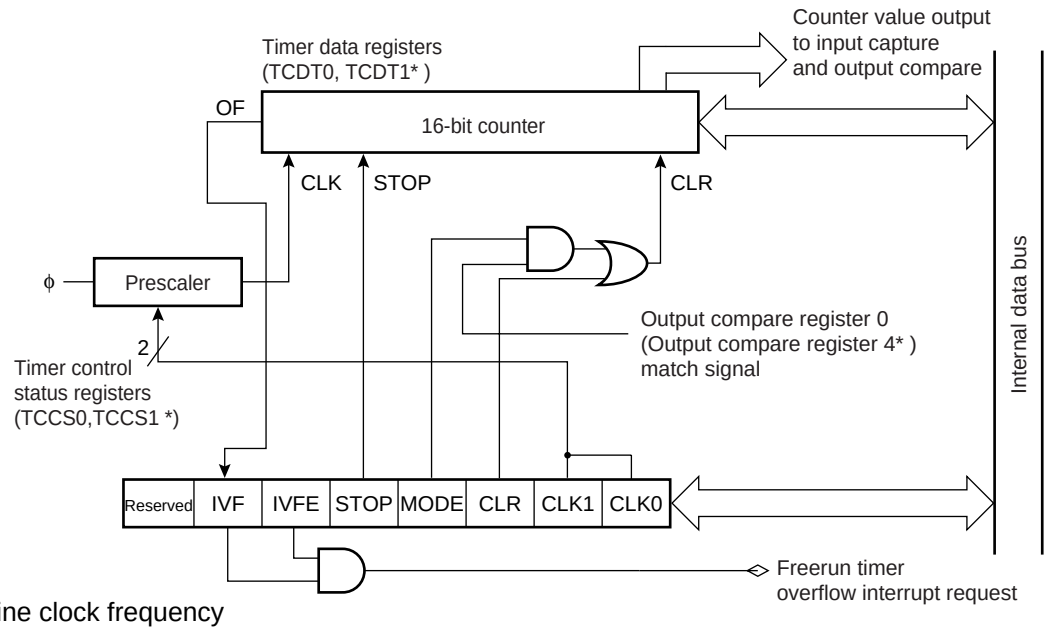
- The input capture saves the value of the 16-bit freerun timer and generates an interrupt request when the specified edge is detected on the trigger input from the external trigger input pin (IC00 or IC01/IC10 or IC11) .
- Input capture channels 0 and 1 can perform input capture and generate interrupt request independently.
- Extended intelligent I/O service (EI$^2$OS) can be generated.
- Detection of rising edges, falling edges, or either edge can be selected as the trigger edge.
- When using input capture 0, either the IC00 or IC01 pin can be used. Note, however, that masking one pin only is not possible.
- When using input capture 1, either the IC10 or IC11 pin can be used. Note, however, that masking one pin only is not possible.

**• Output compare functions**

- The output compare channels compare the values set in output compare registers 0 to 7 with the 16-bit freerun timers 0 and 1 count values and invert the level of the corresponding output compare pin and clear the 16-bit freerun timer to "$0000_H$" when a match is detected.
- Extended intelligent I/O service (EI$^2$OS) can be generated.
- The initial output levels at the output compare pins can be set after the microcontroller boots.
- The output levels from the eight output compare channels are controlled independently. Similarly, interrupt requests are also generated independently by each channel.

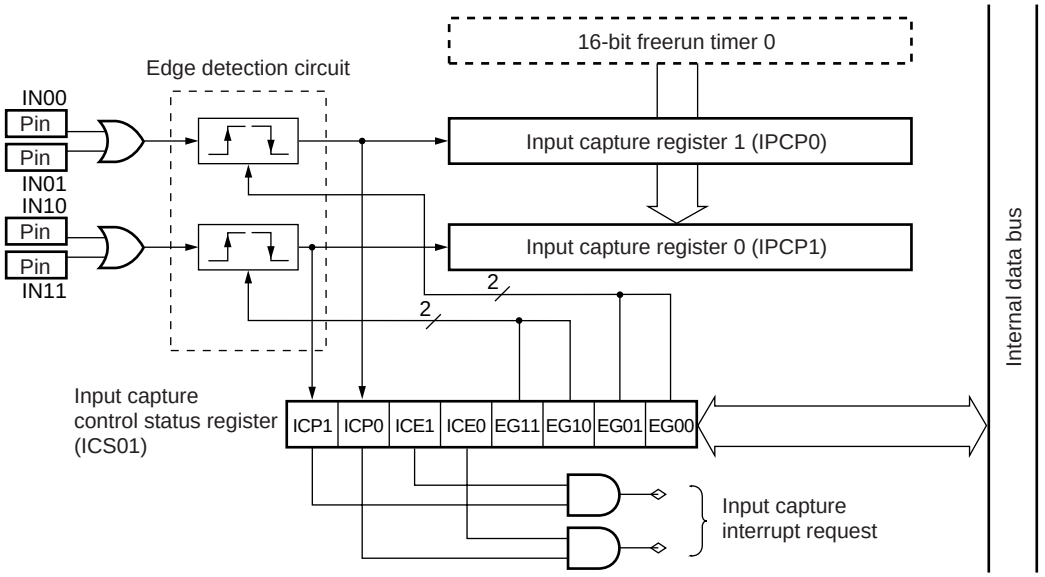
- **Block diagram**

**16-bit freerun timer**

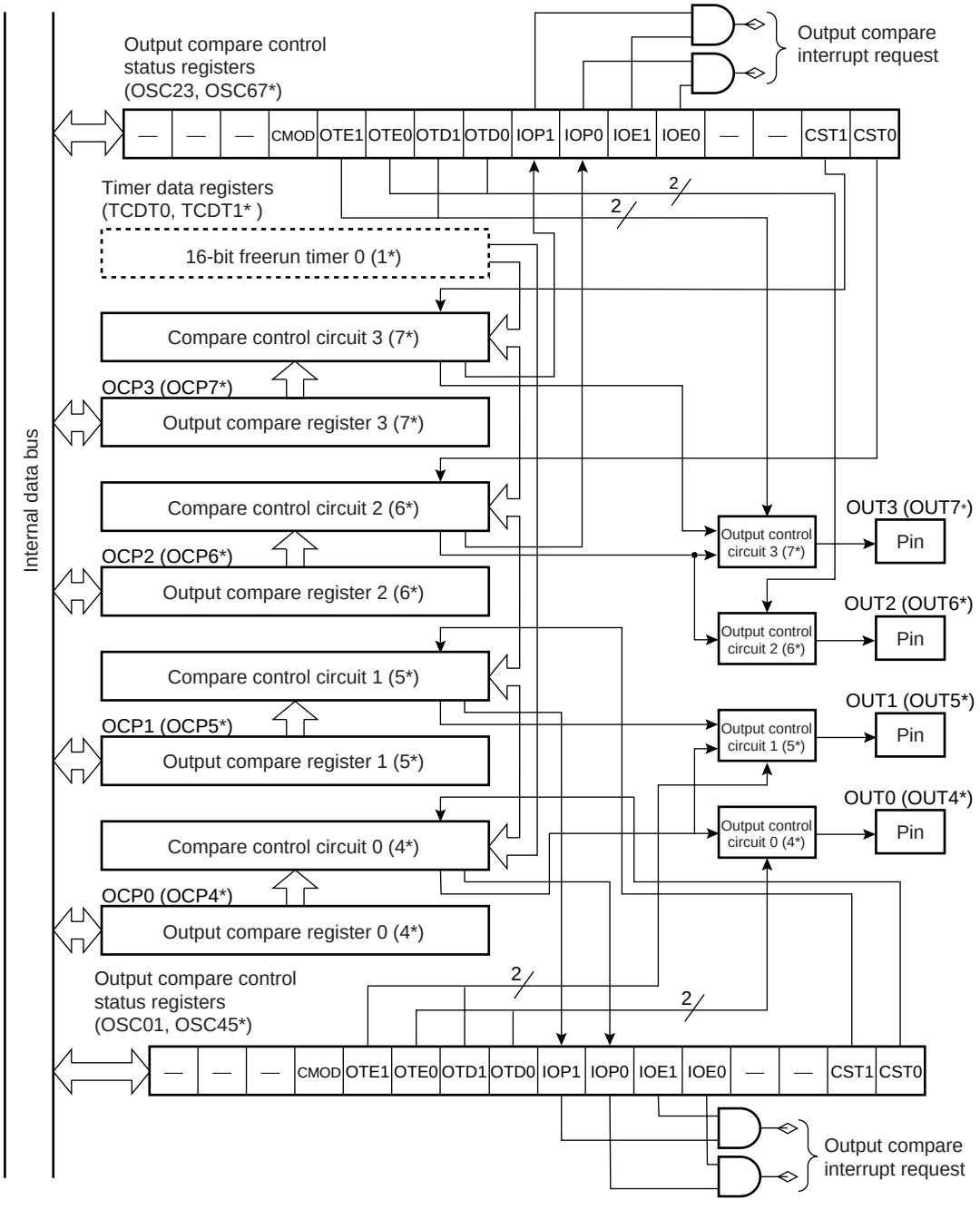



ϕ : Machine clock frequency
OF : Overflow
* : Name for 16-bit freerun timer channel 1

**Input capture**



**Output compare**




* : Name for output compare unit 1

## 7. 8/16-bit Up/Down Counter/Timers 0 and 1

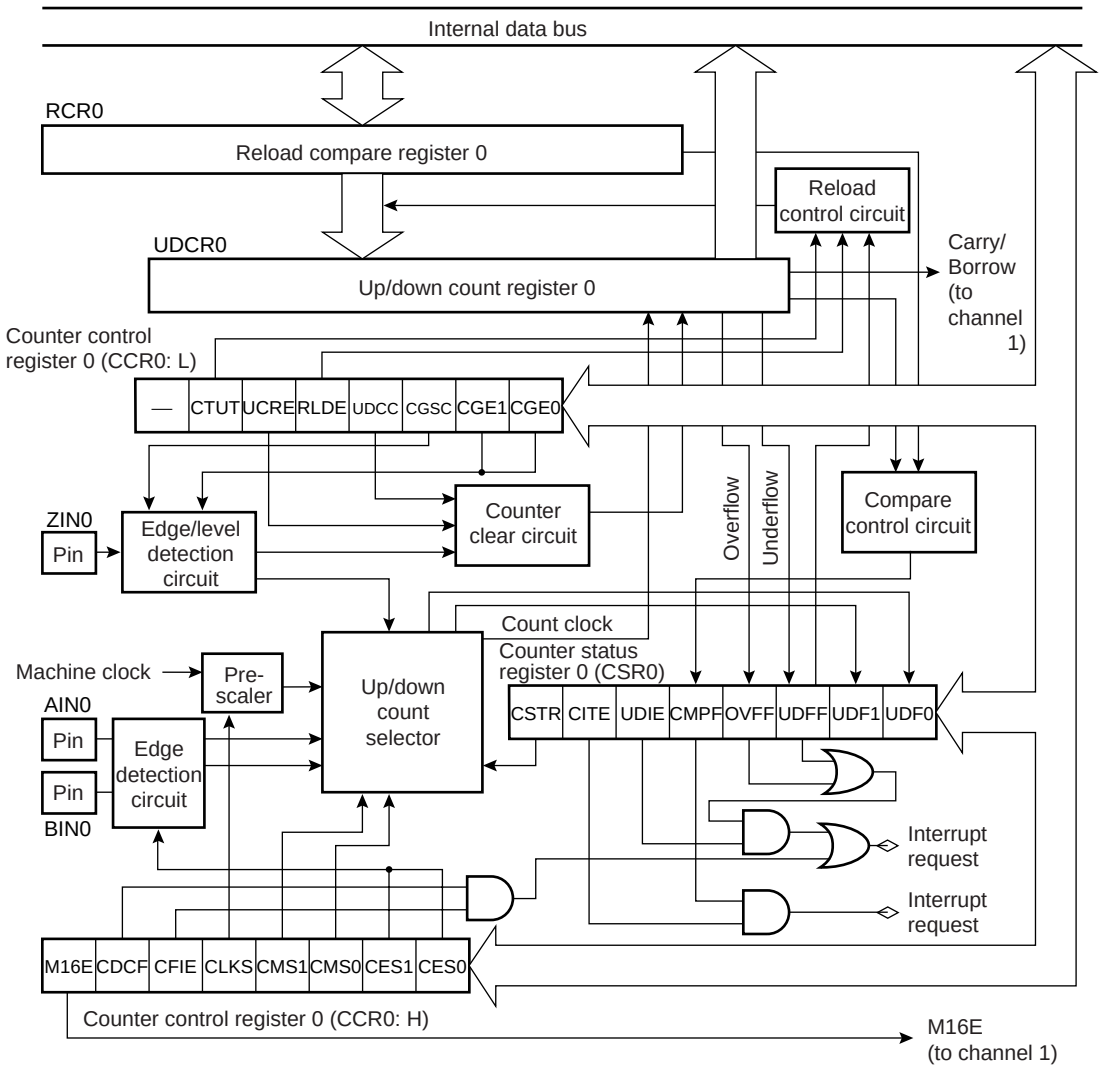
- The 8/16-bit up/down counter/timers can operate in timer mode, up/down count mode, and phase difference count mode.
- The unit can be used as either a 2-channel × 8-bit or 1-channel × 16-bit up/down counter/timer.

**• 8/16-bit up/down counter/timer functions**

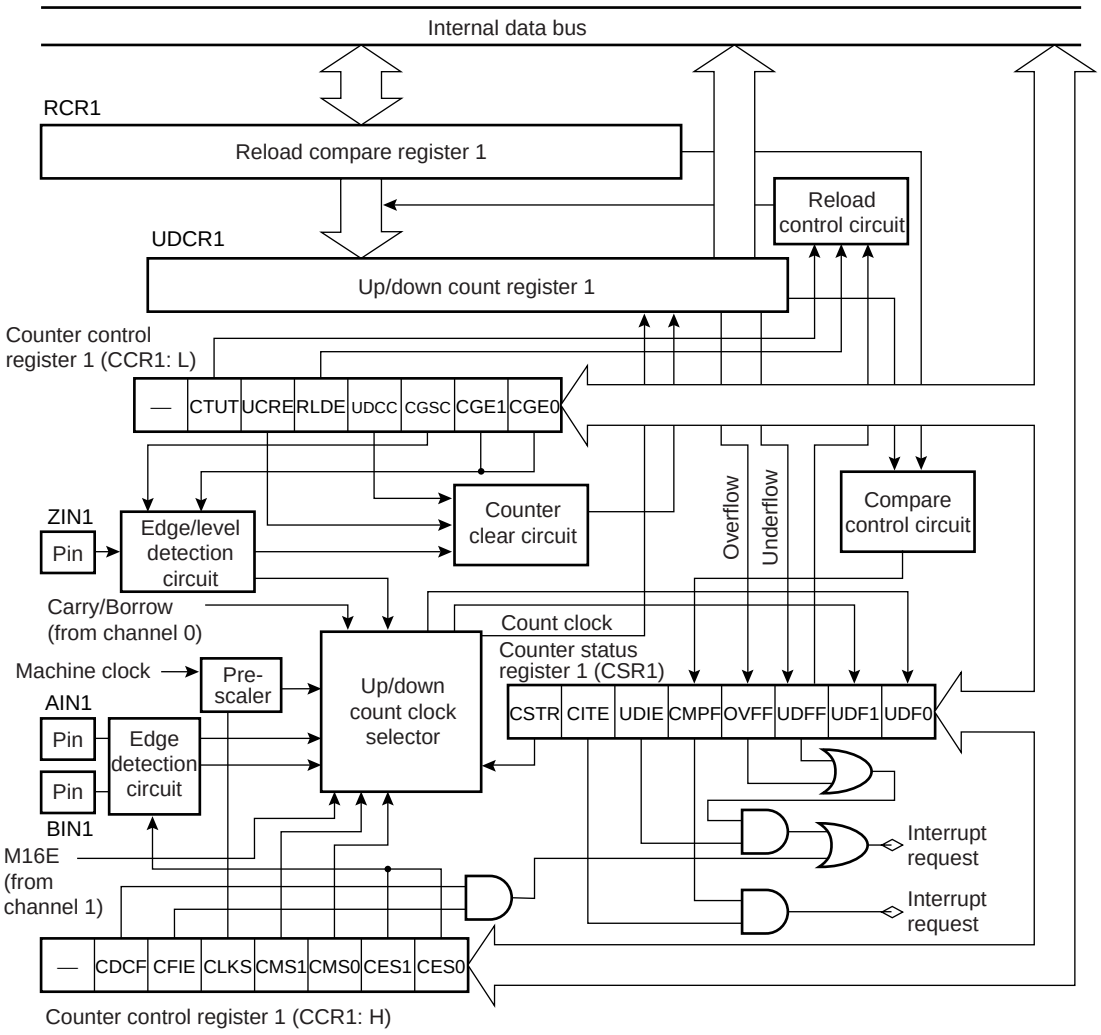
| Operation Mode | Count Mode | Count Clock (Count Edge) | Function of ZIN Pin | Other Functions |
|---|---|---|---|---|
| 8-bit × 2-channel mode | Timer mode | 2/ϕ, 4/ϕ (ϕ : Machine clock frequency) | — | • Compare function<br>• Reload function<br>• Compare/reload function<br>• Compare/reload prohibit<br>• The direction of the previous count can be determined from the up/down flag.<br>• Interrupt requests can be generated on the following conditions :<br>1 : Compare match<br>2 : Underflow or overflow<br>3 : Count direction change |
| | Up/down count mode | Counts up on detecting specified edge on the AIN pin. Counts down on detecting specified edge on the BIN pin. | Counter clear function | |
| | | | Gate function | |
| | Phase difference count mode (multiply by 2) | Reads the AIN pin input level on detecting a rising or falling edge on the BIN pin and counts up or counts down. | Counter clear function | |
| | | | Gate function | |
| | Phase difference count mode (multiply by 4) | Reads the AIN pin input level on detecting a rising or falling edge on the BIN pin and counts up or counts down. Similarly, reads the BIN pin input level on detecting a rising or falling edge on the AIN pin and counts up or counts down. | Counter clear function | |
| | | | Gate function | |
| 16-bit × 1-channel mode | Timer mode | 2/ϕ, 4/ϕ (ϕ : Machine clock frequency) | — | |
| | Up/down count mode | Counts up on detecting specified edge on the AIN pin. Counts down on detecting specified edge on the BIN pin. | Counter clear function | |
| | | | Gate function | |
| | Phase difference count mode (multiply by 2) | Reads the AIN pin input level on detecting a rising or falling edge on the BIN pin and counts up or counts down. | Counter clear function | |
| | | | Gate function | |
| | Phase difference count mode (multiply by 4) | Reads the AIN pin input level on detecting a rising or falling edge on the BIN pin and counts up or counts down. Similarly, reads the BIN pin input level on detecting a rising or falling edge on the AIN pin and counts up or counts down. | Counter clear function | |
| | | | Gate function | |

- **Block diagram**

**8/16-bit up/down counter/timer 0**



**8/16-bit up/down counter/timer 1**




- **Pins and interrupt numbers**

8/16-bit up/down counter/timer 0
AIN0 pin : P24/AIN0
BIN0 pin : P25/BIN0
ZIN0 pin : P26/ZIN0
Compare match interrupt number : #21 ($15_H$)
Interrupt number for underflow/overflow interrupt, count direction change interrupt : #2 ($16_H$)

8/16-bit up/down counter/timer 1
AIN1 pin : P50/AIN1
BIN1 pin : P51/BIN1
ZIN1 pin : P52/ZIN1
Compare match interrupt number : #29 ($1D_H$)
Interrupt number for underflow/overflow interrupt, count direction change interrupt : #3 ($1E_H$)

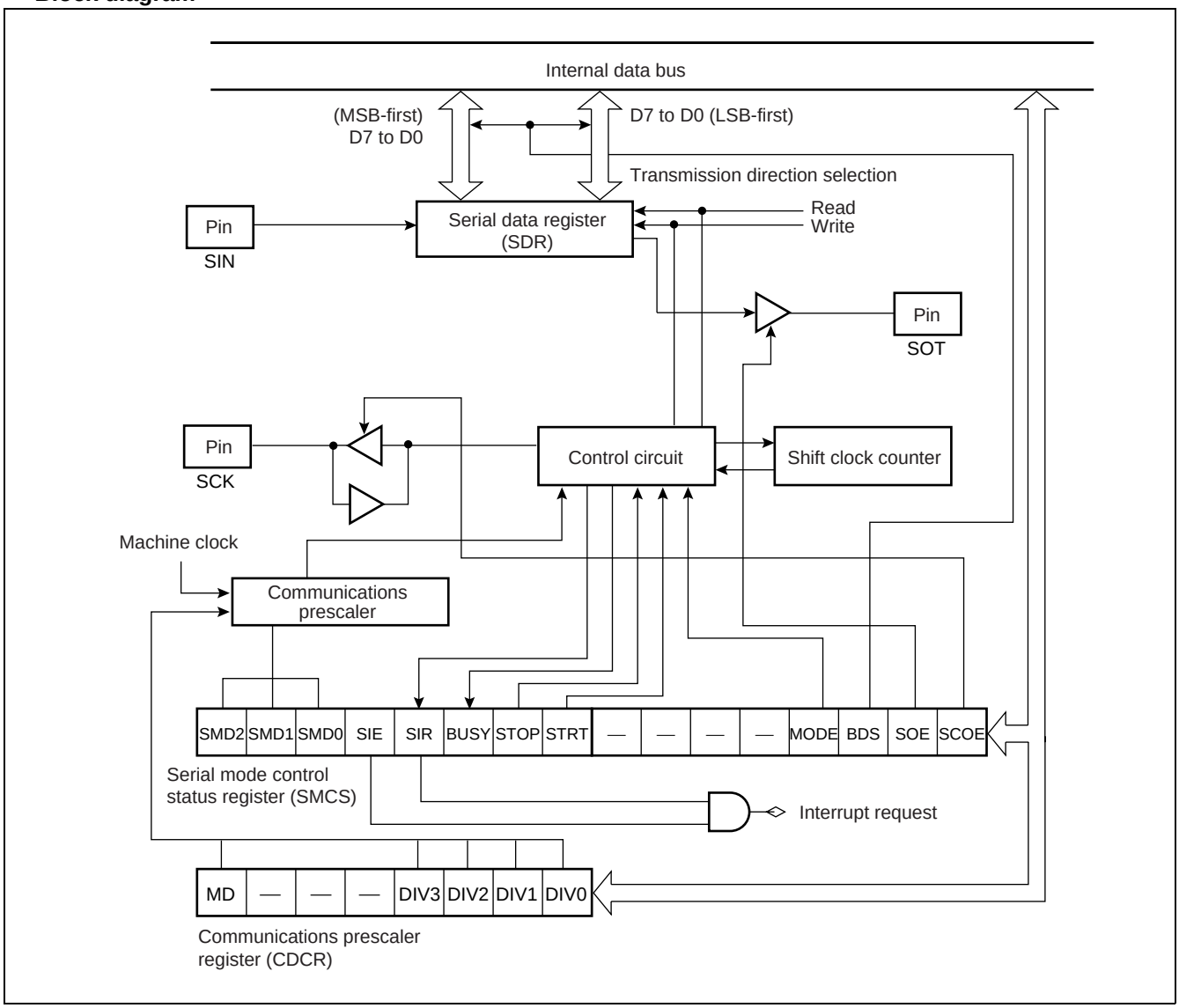
## 8. Extended I/O Serial Interfaces 0 and 1

- The extended I/O serial interfaces are serial I/O interfaces that perform clock-synchronized data transfer.
- The MB90520A/520B series contain two internal extended I/O serial interface channels.
- Either LSB-first or MSB-first data transmission format can be selected.

**• Extended I/O serial interface functions**

| | Function |
|---|---|
| Transmission direction | • Transmit and receive can be handled simultaneously. (A setting is required to select transmit or receive.) |
| Transmission mode | • Clock synchronous (data transfer only) |
| Transmission clock | • Internal shift clock mode (Uses the communications prescaler output clock.)<br>• External shift clock mode (Inputs the clock signal from SCK1 and SCK2.) |
| Transmission speed | • When using internal shift clock :<br>Up to 1 MHz operation can be achieved (for a 16 MHz machine clock with the divisor setting for the communication prescaler set to 8) . Speeds faster than 1 MHz are not possible.<br>• When using an external shift clock :<br>As a minimum of 5 machine cycles are required, when the machine clock is 16 MHz the maximum input frequency for the external shift clock is 16 MHz / 5 = 3.2 MHz. |
| Data transmission format | • LSB-first or MSB-first, selectable<br>• Data transfer only<br>• Number of data bits = 8 (fixed) |
| Interrupt request generation | • Interrupt generated when transfer completes |
| EI²OS support | • Supports use of the extended intelligent I/O service. |

• **Block diagram**



## 9. UART (SCI : Serial Communication Interface)

- The UART (SCI) is a general-purpose serial communications interface for performing synchronous or asynchronous communications with external devices.
- The interface provides bi-directional communications in both clock synchronous and clock asynchronous modes.
- Includes a master-slave communication function (multi-processor mode) .
- Can generate interrupt requests at receive complete, receive error detected, and transmit complete timings. Also supports EI$^2$OS.

**• UART (SCI) functions**

| | Function |
|---|---|
| Data buffer | • Full-duplex double-buffered |
| Transmission modes | • Clock synchronous (with no start/stop bit, no parity bit)<br>• Clock asynchronous (start-stop sync) |
| Baud rate | • Can use dedicated baud rate generator.<br>• Can use external clock input.<br>• Can use clock supplied by 16-bit reload timer 0.<br>• For machine clock speeds of 6 MHz, 8 MHz, 10 MHz, 12 MHz, and 16 MHz :<br>Available speeds for asynchronous communications : 31250 bps, 9615 bps, 4808 bps, 2404 bps, and 1202 bps<br>Available speeds for synchronous communications : 1 Mbps, 500 Kbps, 250 Kbps, 125 Kbps, and 62.5 Kbps |
| Number of data bits | • 7 bits (when parity is used for asynchronous normal mode)<br>• 8 bits (when parity is not used) |
| Signal format | • Non return to zero (NRZ) format |
| Receive error detection | • Framing errors (not available in clock synchronous mode)<br>• Overrun errors<br>• Parity errors (not available in clock synchronous mode and multi-processor mode) |
| Interrupt requests | • Receive interrupt (Receive complete or receive error detected)<br>• Transmit interrupt (Transmission complete)<br>• Both transmit and receive support the extended intelligent I/O service (EI$^2$OS) . |
| Master/slave communication function (multi-processor mode) | • Used for 1 (master) to n (slave) communications. (Can only be used as master) |
| EI$^2$OS support | • Supports the extended intelligent I/O service (EI$^2$OS) |

• **UART (SCI) operation modes**

| Operation Mode | | | No. of Data Bits | | Parity Bit | | No. of Stop Bits | |
|---|---|---|---|---|---|---|---|---|
| | | | 7 bits | 8 bits | None | Use | 1 bit | 2 bits |
| Mode 0 | Asynchronous | Normal mode (1-to-1) | ○ | ○ | ○ | ○ | ○ | ○ |
| Mode 1 | Asynchronous | Multi-processor mode (1-to-n) | × | ○ (+1) | ○ | × | ○ | ○ |
| Mode 2 | Clock synchronous | Clock synchronous mode (one-to-one) | × | ○ | ○ | × | × | × |

○ : Available

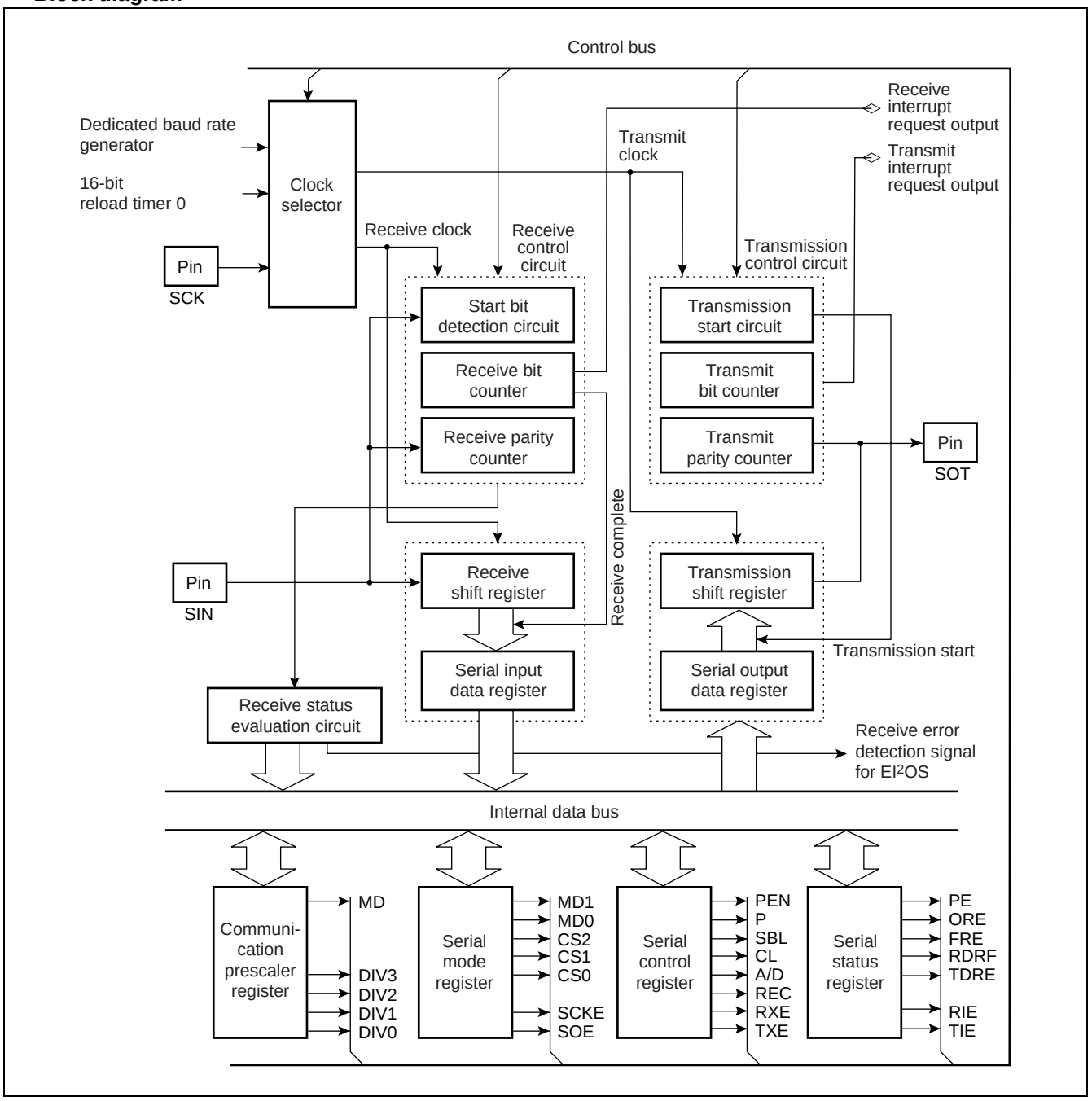
× : Not available

+1 : Address/data bit used for communication control

Notes :

- The number of data bits must be set to eight for multi-processor and clock synchronous modes.
- A parity bit cannot be used in multi-processor and clock synchronous modes.
- Only data can be transferred in clock synchronous mode. Start and stop bits cannot be added to the transmission data.

• **Block diagram**



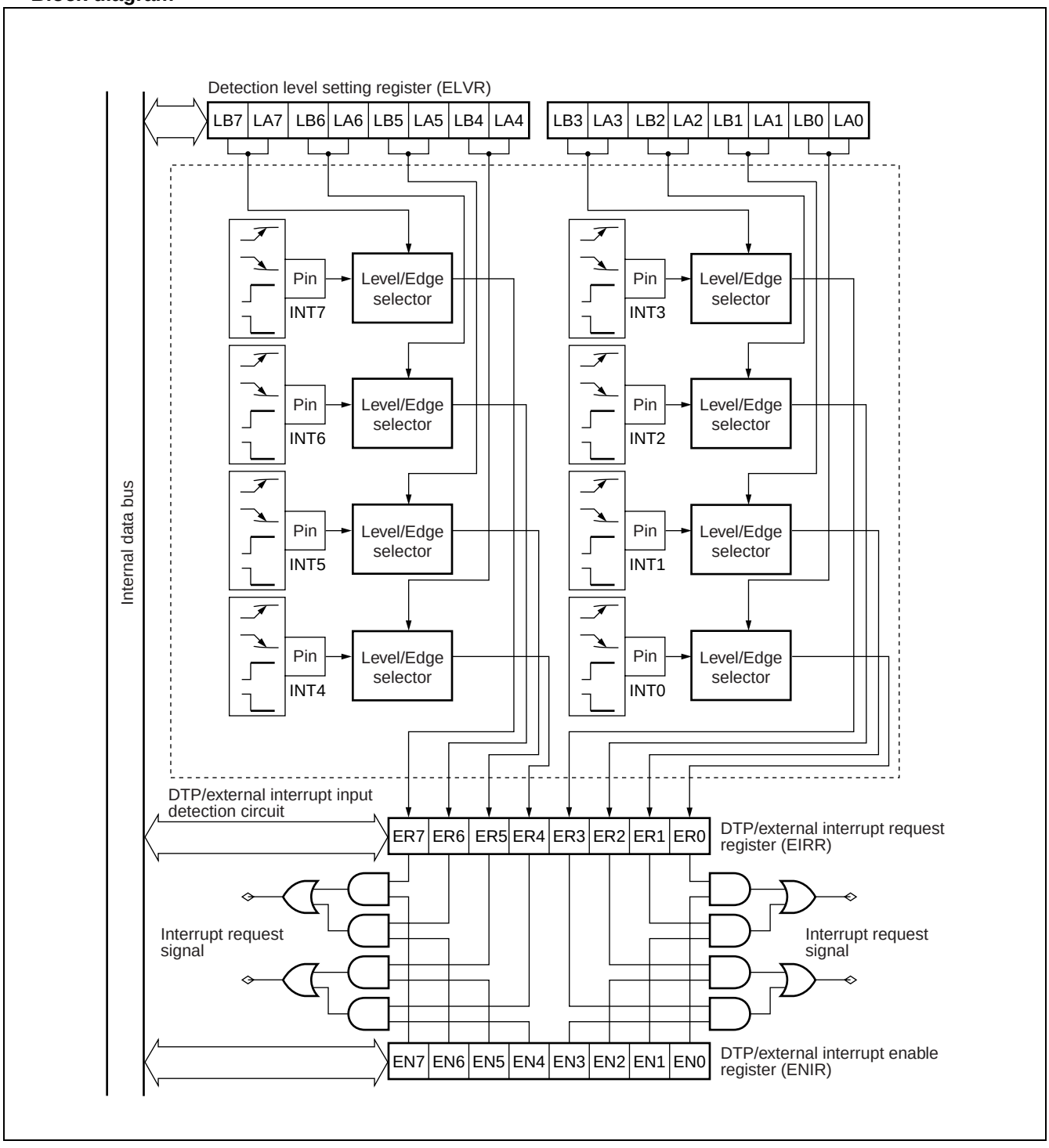
## 10. DTP (Data Transfer Peripheral) /External Interrupt Circuit

The DTP/external interrupt function detects interrupt requests and data transfer requests input from external devices and passes these to the CPU as external interrupt requests. This block can also activate the extended intelligent I/O service (EI$^2$OS) .

**• DTP/external interrupt functions**

| | External Interrupt | DTP Function |
|---|---|---|
| Input pins | • 8 channels (INT0 to INT7) | |
| Interrupt conditions | • Can be set independently for each channel (each pin) in the detection level setup register (ELVR) . | |
| | • “H” level, “L” level, rising edge, or falling edge input | “H” level or “L” level input |
| Interrupt control | • Interrupts can be enabled or disabled in the DTP/external interrupt enable register (ENIR) . | |
| Interrupt flag | • The DTP/external interrupt request register (EIRR) stores interrupt requests. | |
| Processing selection | • Set EI$^2$OS to be disabled (ICR : ISE = 0) | • Set EI$^2$OS to be enabled (ICR : ISE = 1) |
| Interrupt execution | • Jumps to interrupt handler routine | • Jumps to interrupt handler routine after automatic data transfer by EI$^2$OS completes. |
| EI$^2$OS support | • Supports the extended intelligent I/O service (EI$^2$OS) | |

• **Block diagram**



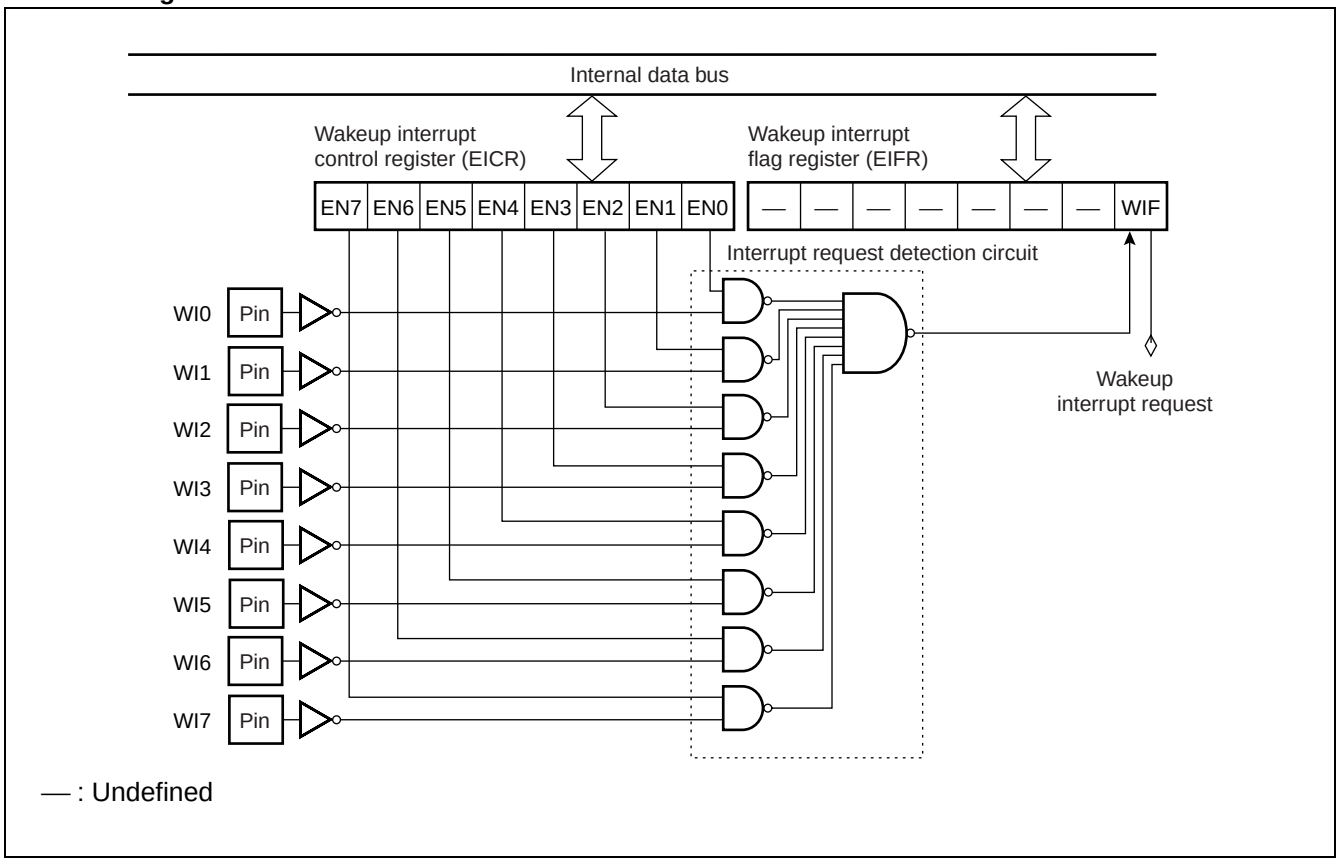
## 11. Wakeup Interrupts

- The wakeup interrupt function detects wakeup interrupt requests from external devices by detecting “L” levels input to the wakeup interrupt input pins (WI0 to WI7) and passes these to the CPU for interrupt processing.
- Wakeup interrupts can be used to wakeup the microcontroller from standby mode. (However, wakeup interrupts cannot be used to recover from hardware standby mode.)
- Not supported by the extended intelligent I/O service (EI²OS) .

**• Wakeup interrupt functions**

| | Function and Control |
|---|---|
| Input pins | • 8 channels (8 pins : WI0 to WI7) |
| Interrupt trigger | • “L” level inputs. One interrupt flag is shared by all eight channels. |
| Interrupt control | • Interrupt requests can be enabled or disabled in the wakeup interrupt control register (EICR) . |
| Interrupt flag | • Interrupt requests are stored in the wakeup interrupt flag register (EIFR) . |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Block diagram**




— : Undefined

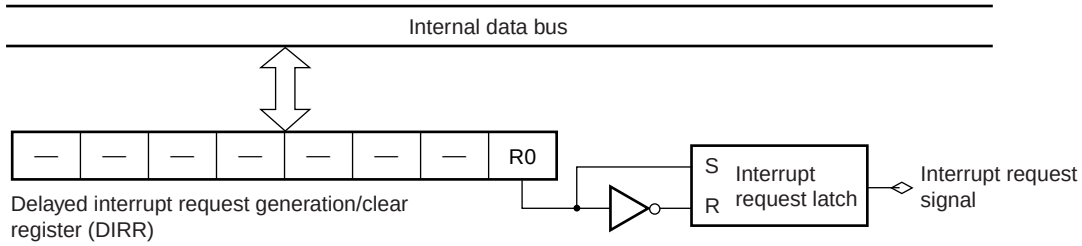
## 12. Delayed Interrupt Generation Module

The delayed interrupt generation module is used to generate the task switching interrupt. Generation of this hardware interrupt can be specified by software.

**• Delayed interrupt generation module functions**

| | Function and Control |
|---|---|
| Interrupt trigger | • Writing “1” to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 1) generates an interrupt request.<br>• Writing “0” to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 0) clears the interrupt request. |
| Interrupt control | • No enable/disable register is provided for this interrupt. |
| Interrupt flag | • Set in bit R0 of the delayed interrupt request generation/clear register (DIRR : R0) . |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Block diagram**




— : Undefined

## 13. 8/10-bit A/D Converter

- The 8/10-bit A/D converter uses RC successive approximation to convert analog input voltages to an 8-bit or 10-bit digital value.
- The input signals can be selected from the eight analog input pin channels.
- Either a software trigger, internal timer output, or external pin trigger can be selected to trigger the start of A/D conversion.

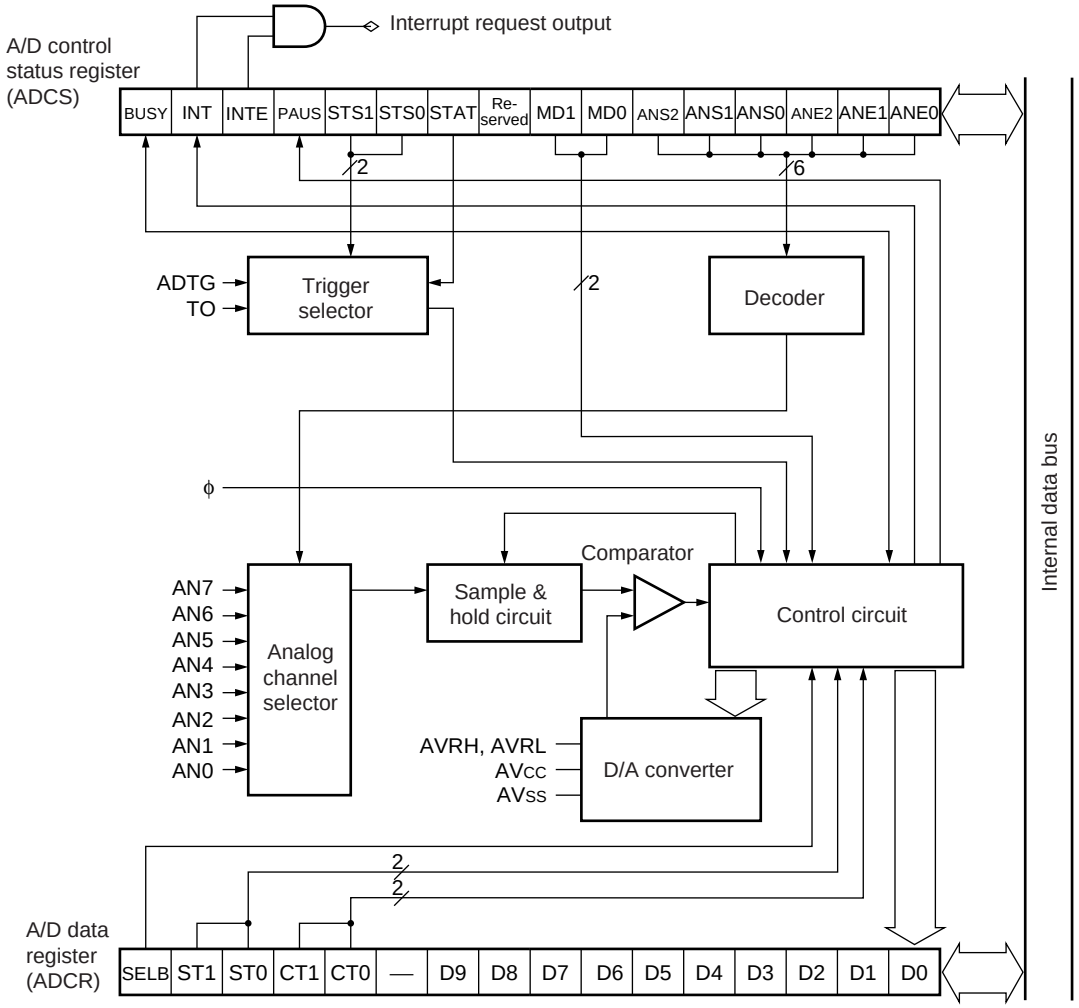
**• 8/10-bit A/D converter functions**

| | Function |
|---|---|
| A/D conversion time | • Sampling time : Can be selected from 64, 128, or 4096 machine cycles. The minimum is 4 μs.<br>• Compare time : Can be selected from 44, 99, or 176 machine cycles. The minimum is 4.4 μs.<br>• A/D conversion time = sampling time + conversion time. The minimum A/D conversion time is 10.2 μs. |
| Conversion method | • RC successive approximation with sample & hold circuit |
| Resolution | • 8-bit or 10-bit, selectable |
| Analog input pins | • Up to eight channels can be used. However, two or more channels cannot be used simultaneously. |
| Interrupts | • An interrupt request can be generated when A/D conversion completes. |
| A/D conversion start trigger | • Selectable : software, internal timer output, or falling edge on input from external pin |
| EI²OS support | • Supported by the extended intelligent I/O service (EI²OS) . |

**• 8/10-bit A/D converter conversion modes**

| | Description |
|---|---|
| Single-shot conversion mode | Performs A/D conversion sequentially from the start channel to the end channel. A/D conversion halts after conversion completes for the end channel. |
| Continuous conversion mode | Performs A/D conversion sequentially from the start channel to the end channel. A/D conversion starts again from the start channel after conversion completes for the end channel. |
| Incremental conversion mode | A/D conversion is performed for one channel then halts until the next trigger. After conversion is performed for the end channel, the next conversion is performed for the start channel, and repeated this operation. |

• **Block diagram**




TO : Internal timer output
— : Undefined
Reserved : Always set to “0”.
ϕ : Machine clock

## 14. 8-bit D/A Converter

- The 8-bit D/A converter performs R-2R D/A conversion with 8-bit resolution.
- Two D/A converter channels with independent analog outputs are provided.

**• D/A converter functions**

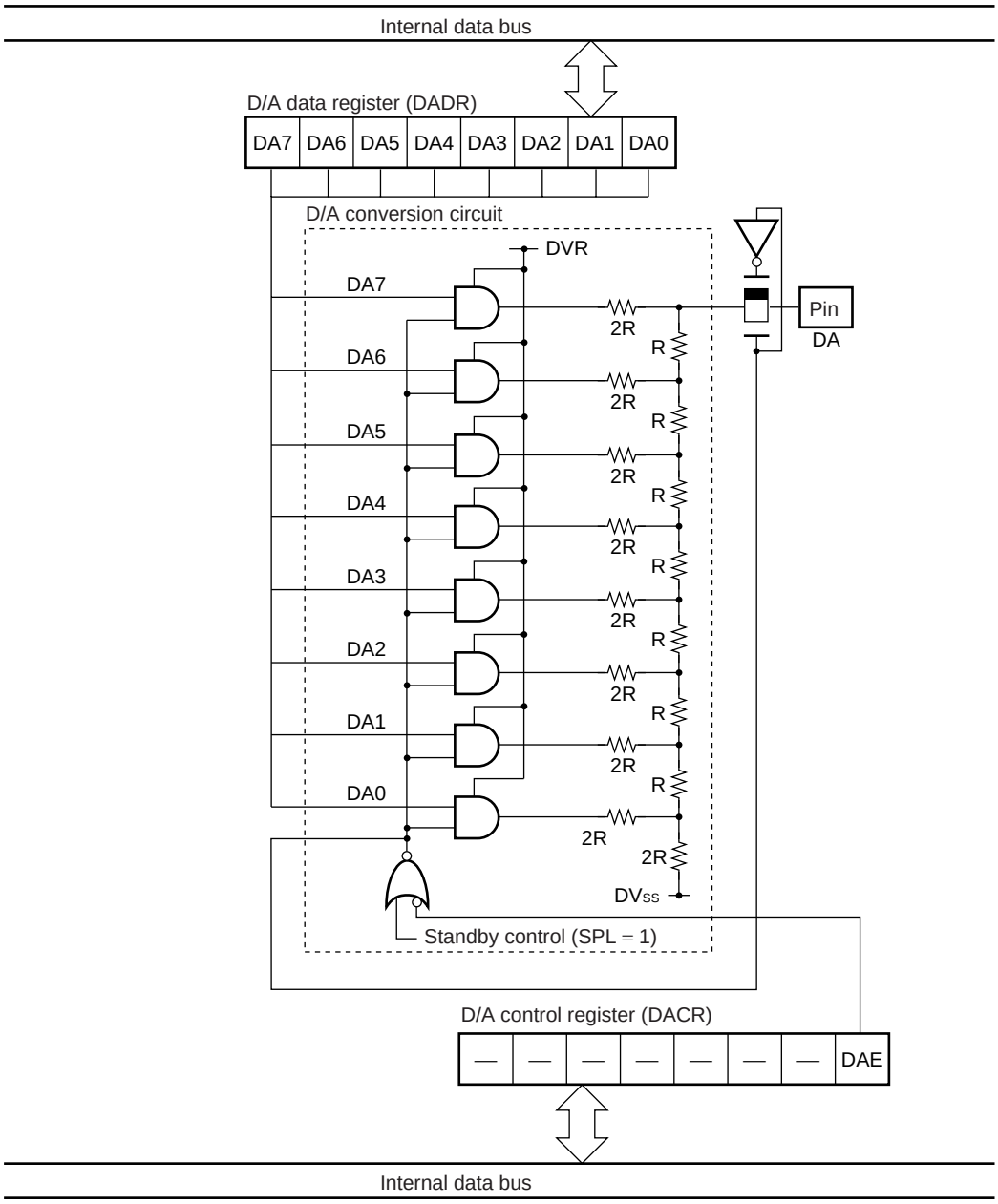
| | Function |
|---|---|
| D/A conversion time | •The settling time is 12.5 μs. This is independent of the machine clock. |
| Conversion method | • R-2R conversion |
| Resolution | • 8-bit |
| Analog output pins | • Two output pins are provided. Both pins can be used simultaneously. |
| Interrupts | • None |
| D/A conversion trigger | • Set the digital value in the D/A data register (DADR) , then enable D/A output in the D/A control register (DACR) to start analog output from the D/A output pin. |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• D/A converter theoretical output voltage**

| D/A Data Register Setting | Theoretical Output Voltage Value |
|---|---|
| $00_H$ | 0 / 256 × $DV_{CC}$ voltage ( = 0 V) |
| $00_H$ | 1 / 256 × $DV_{CC}$ voltage |
| ••• | ••• |
| $FE_H$ | 254 / 256 × $DV_{CC}$ voltage |
| $FF_H$ | 255 / 256 × $DV_{CC}$ voltage |

Note : $DV_{CC}$ voltage : D/A converter reference voltage. This must not exceed $V_{CC}$.
Also, always ensure that $DV_{SS}$ is equipotential to $V_{SS}$.

• **Block diagram**




Standby control : Controls stop mode (SPL = 1) , pseudo-clock mode (SPL = 1) , clock mode (SPL = 1) , and hardware standby mode.

## 15. Clock Timer

- The clock timer is a 15-bit freerun timer that counts up synchronized with the sub-clock.
- Seven different interval time settings are available.
- This timer provides the clock for the sub-clock's oscillation stabilization delay timer and the watchdog timer.
- This timer always counts the sub-clock, regardless of the settings in the clock selection register (CKSC) .

**• Clock timer functions**

| | Function |
|---|---|
| Interval time | • Selectable from the seven settings shown in the table below. |
| Clock timer size | • 15-bit |
| Clock supply | • Oscillation stabilization delay timer for sub-clock and watchdog timer |
| Source clock | • Sub-oscillation clock divided by four. (SCLK : Sub-clock) |
| Interrupts | • Interval time overflow |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Clock timer interval times**

| Sub-Clock Period | Interval Time |
|---|---|
| SCLK (122 µs) | $2^9$/SCLK (approx. 62.5 ms) |
| | $2^{10}$/SCLK (approx. 125.0 ms) |
| | $2^{11}$/SCLK (approx. 250.0 ms) |
| | $2^{12}$/SCLK (approx. 500.0 ms) |
| | $2^{13}$/SCLK (approx. 1.0 s) |
| | $2^{14}$/SCLK (approx. 2.0 s) |
| | $2^{16}$/SCLK (approx. 4.0 s) |

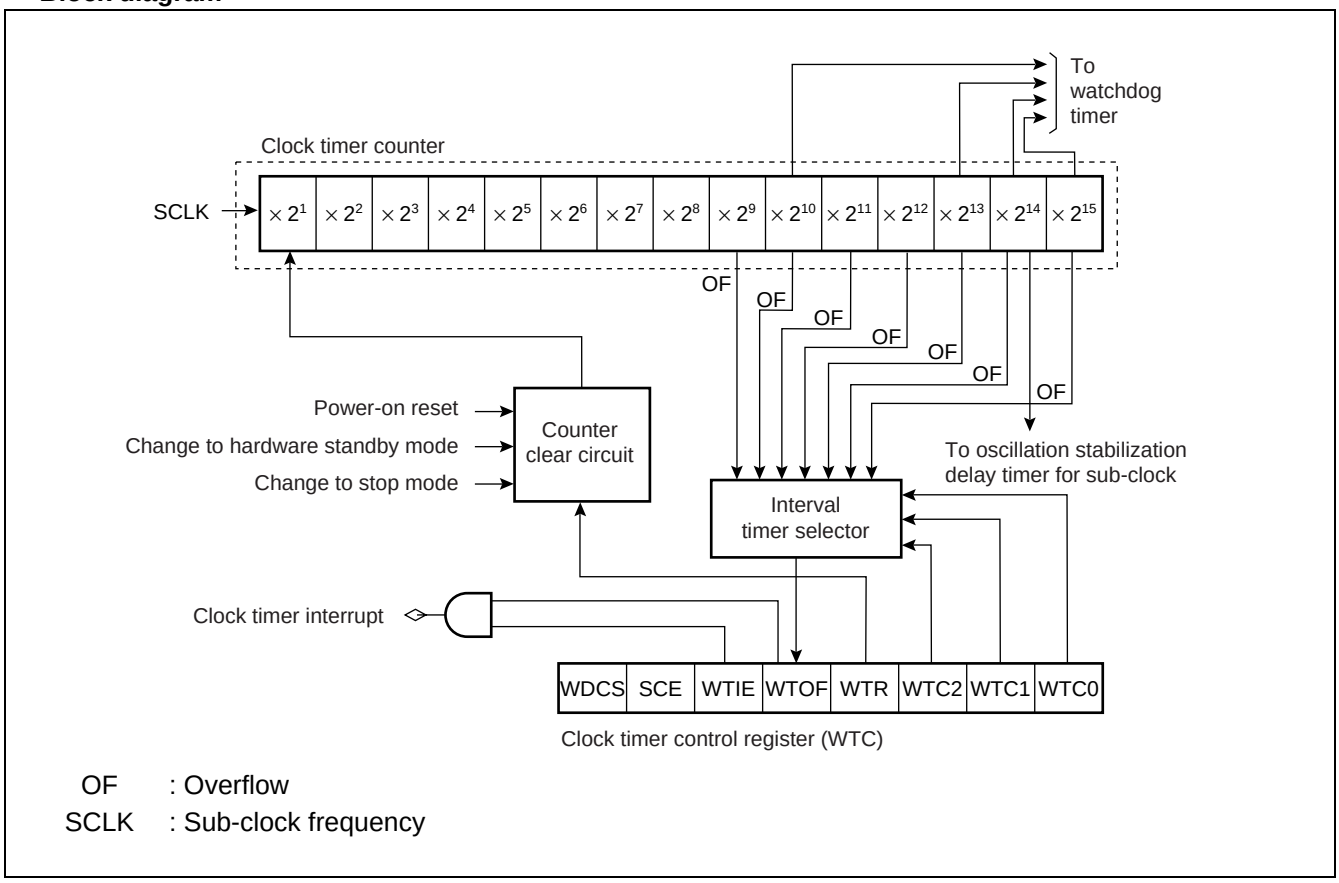
SCLK : Sub-clock frequency
The values enclosed in ( ) are the times for a sub-clock frequency of 8.192 kHz.
Note that the sub-oscillation clock is divided by four to generate the sub-clock frequency. The sub-oscillation clock operates at 32.768 kHz.

**• Clock periods generated by clock timer**

| Clock Supply | Clock Period |
|---|---|
| Oscillation stabilization delay timer for sub-clock | $2^{14}$/SCLK (approx. 2.0 s) |
| Watchdog timer | $2^{10}$/SCLK (approx. 125.0 ms) |
| | $2^{13}$/SCLK (approx. 1.0 s) |
| | $2^{14}$/SCLK (approx. 2.0 s) |
| | $2^{16}$/SCLK (approx. 4.0 s) |

SCLK : Sub-clock frequency
The values enclosed in ( ) are the times for a sub-clock frequency of 8.192 kHz.
Note that the sub-oscillation clock is divided by four to generate the sub-clock frequency. The sub-oscillation clock operates at 32.768 kHz.

• **Block diagram**




OF : Overflow
SCLK : Sub-clock frequency

## 16. LCD Controller/Driver

- The LCD controller/driver can drive an LCD (Liquid Crystal Display) directly.
- The LCD is driven by 4 common outputs and 32 segment outputs.
- The output mode can be set to 1/2, 1/3, or 1/4 duty.

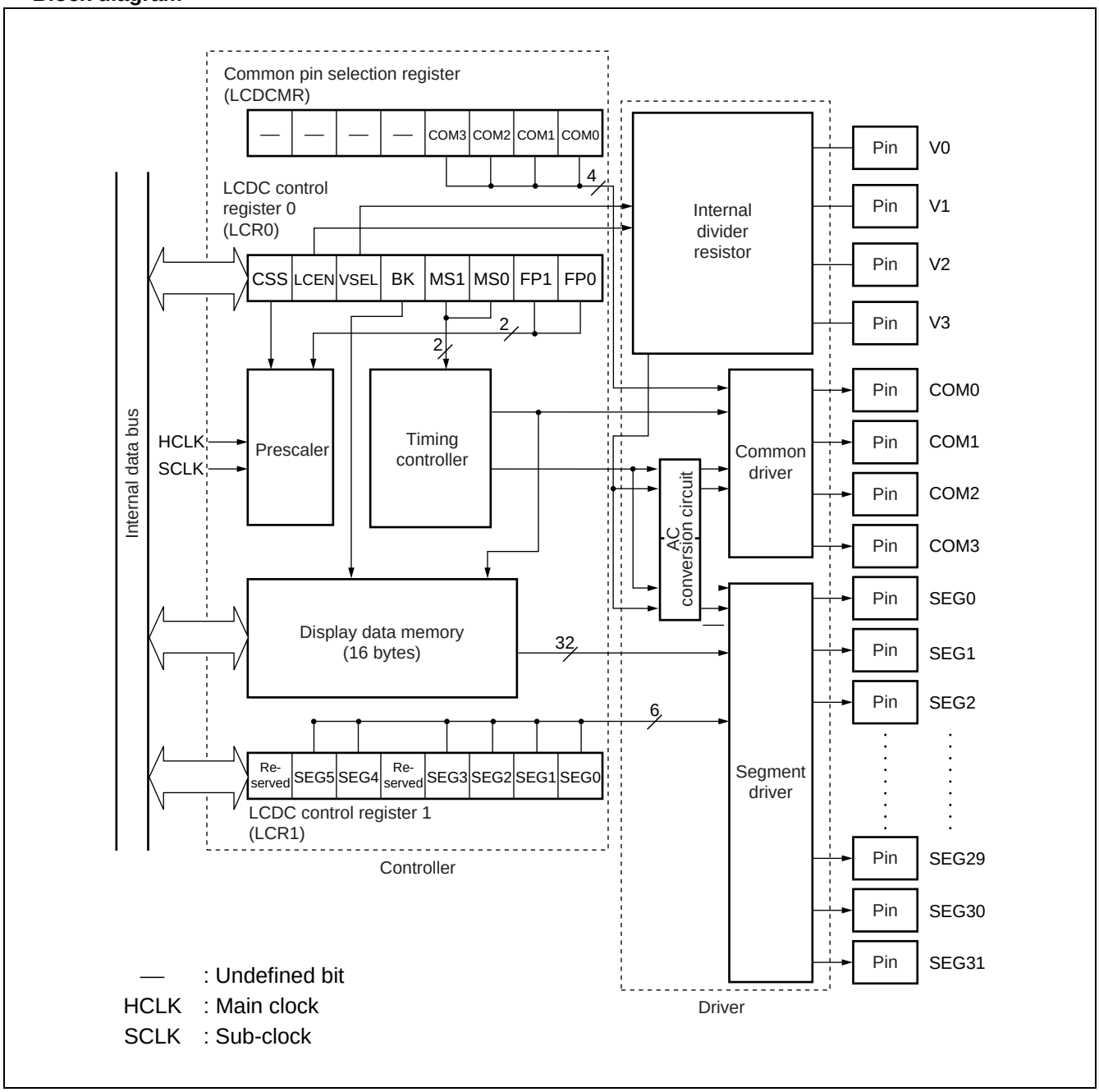
**• LCD controller/driver functions**

| | Function |
|---|---|
| Divider resistor for LCD drive power | • Either the internal resistor (approx. 100 kΩ) or an externally connected resistor can be selected. |
| Common outputs | • Max 4 outputs (The corresponding pins cannot be used as I/O ports when using an LCD.) |
| Segment outputs | • Max 32 outputs (of these, 24 pins can be used as I/O ports in blocks of 8 pins.) |
| Display data memory | • 16 bytes of RAM for internal display are provided |
| Duty | • 1/2, 1/3, or 1/4 can be selected. |
| Bias | • 1/3 only supported |
| Drive clock | • Either the oscillation clock (HCLK) or sub-clock (SCLK) can be used. |
| Interrupts | • None |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Bias, duty, and common output combinations**

| Bias | 1/2 Duty Output Mode | 1/3 Duty Output Mode | 1/4 Duty Output Mode |
|---|---|---|---|
| 1/3 bias | COM0 and COM1 outputs used | COM0 to COM2 outputs used | COM0 to COM3 outputs used |

• **Block diagram**



## 17. Communications Prescaler

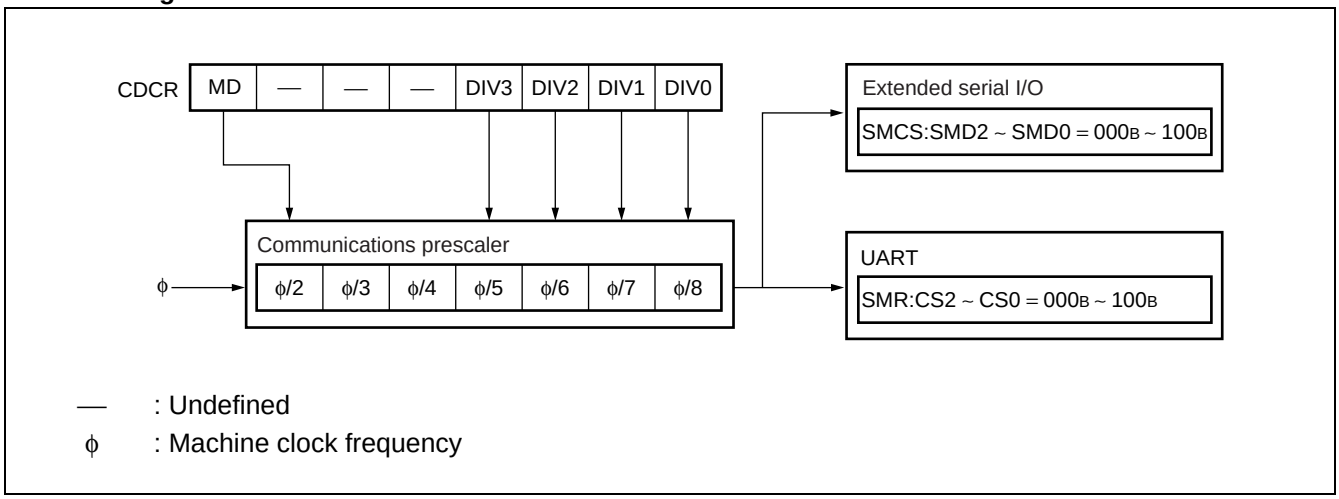
- Supplies the clock to the dedicated baud rate generator used by the UART (SCI) and extended I/O serial interfaces.
- By dividing the machine clock to produce the clock supply to the dedicated baud rate generator, the baud rate can be specified independently of the machine clock speed.
- The communications prescaler can divide the machine clock frequency $\phi$ by the following seven ratios to generate the clock supply to the dedicated baud rate generator and extended I/O serial interface :
  $\phi/2$, $\phi/3$, $\phi/4$, $\phi/5$, $\phi/6$, $\phi/7$, $\phi/8$

### • Communications prescaler functions

| | Function |
|---|---|
| Clock supply | • Dedicated baud rate generator for the UART (SCI) and the extended I/O serial interface. However, the same clock is supplied to both peripherals. |
| Divided clock frequency | • $\phi/2$, $\phi/3$, $\phi/4$, $\phi/5$, $\phi/6$, $\phi/7$, $\phi/8$ ($\phi$ : Machine clock frequency) |
| Interrupts | • None |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

Note : As the same output from the communications prescaler is supplied to both the UART (SCI) and the extended I/O serial interface, the transfer clock speed settings must be revised if the communications prescaler settings are changed.

### • Block diagram



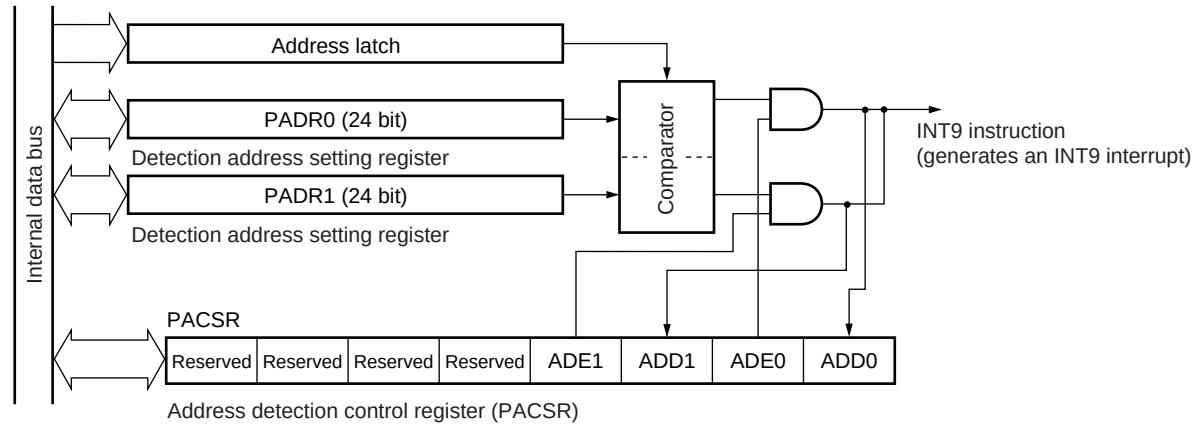
## 18. Address Match Detection Function

- If the program address during program execution matches the value set in one of the detection address setting registers (PADR) , the address match detection function replaces the instruction being executed with the INT9 instruction and executes the interrupt handler program.
- The address match detection function provides a simple method of correcting programming errors (patching) using RAM or similar.

**• Address match detection functions**

| | Function |
|---|---|
| No. of address settings | • Two channels (two addresses can be set) |
| Interrupts | • An interrupt is generated when the program address matches the detection address setting register. |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Block diagram**




Reserved : Always set to “0”.

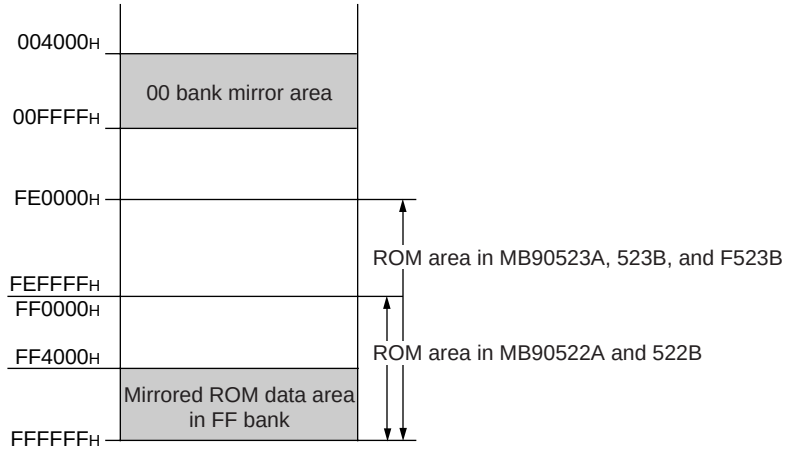
## 19. ROM Mirror Function Selection Module

The ROM mirror function selection module enables ROM data in FF bank to be read by accessing 00 bank.

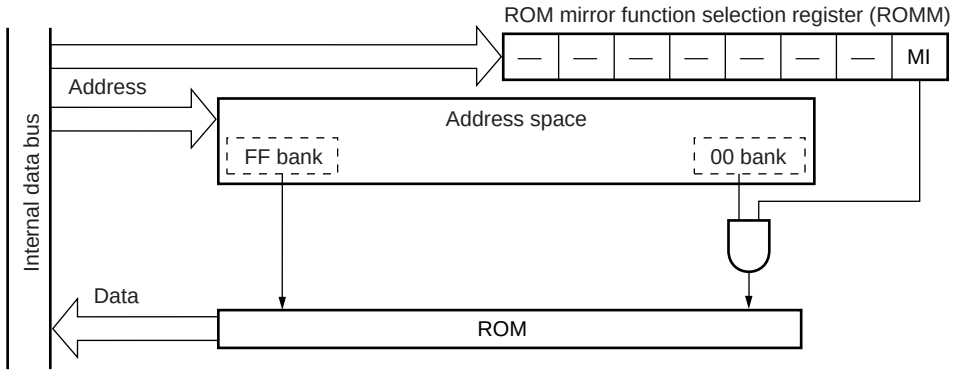
**• ROM mirror function selection module functions**

| | Function |
|---|---|
| Mirror setting address | • Data in FFFFFF$_H$ to FF4000$_H$ in FF bank can be read from 00FFFF$_H$ to 004000$_H$ in 00 bank. |
| Interrupts | • None |
| EI$^2$OS support | • Not supported by the extended intelligent I/O service (EI$^2$OS) . |

**• Relationship between addresses in the ROM mirror function**




**• Block diagram**



## 20. Low Power Consumption (Standby) Modes

The power consumption of F²MC-16LX devices can be reduced by various settings relating to the operating clock selection.

**• Functions of each CPU operation mode**

| CPU Operation Clock | Operation Mode | Explanation |
|---|---|---|
| PLL clock | Normal run | The CPU and peripheral functions operate using the oscillation clock (HCLK) multiplied by the PLL circuit. |
| | Sleep | The peripheral functions only operate using the oscillation clock (HCLK) multiplied by the PLL circuit. |
| | Pseudo-clock | The timebase timer only operates using the oscillation clock (HCLK) multiplied by the PLL circuit. |
| | Stop | The oscillation clock is stopped and the CPU and peripherals halt operation. |
| Main clock | Normal run | The CPU and peripheral functions operate using the oscillation clock (HCLK) divided by 2. |
| | Sleep | The peripheral functions only operate using the oscillation clock (HCLK) divided by 2. |
| | Stop | The oscillation clock is stopped and the CPU and peripherals halt operation. |
| Sub-clock | Normal run | The CPU and peripheral functions operate using the sub-clock (SCLK) . The oscillation clock stops. |
| | Sleep | The peripheral functions only operate using the sub-clock (SCLK) . The oscillation clock stops. |
| | Clock | The clock timer only operates using the sub-clock (SCLK) . The oscillation clock stops. |
| | Stop | The oscillation clock and sub-clock are stopped and the CPU and peripherals halt operation. |
| CPU intermittent operation | Normal run | The oscillation clock (HCLK) divided by 2 operates intermittently for fixed time intervals. |
| Hardware standby | Stop | The oscillation clock and sub-clock are stopped and the CPU and peripherals halt operation. |

## 21. Clock Monitor Function

The clock monitor function outputs the machine clock divided by a specified amount to the clock monitor pin (CKOT) .

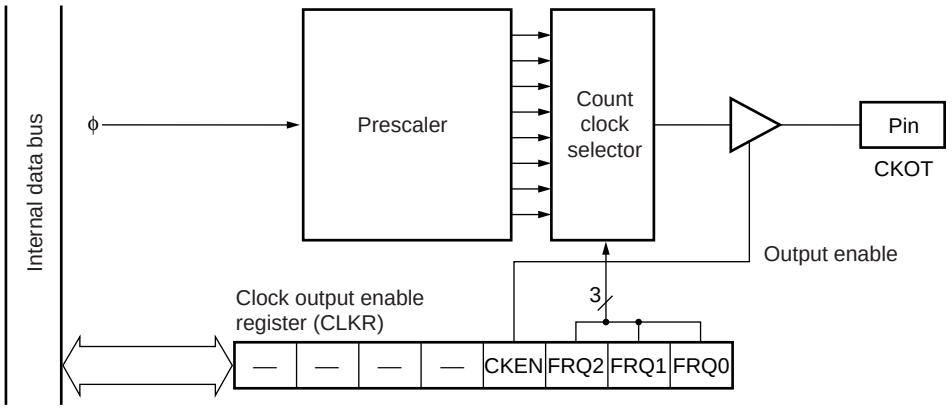
**• Clock monitor functions**

| | Function |
|---|---|
| Output frequency | • Machine clock divided by 2 to 32 (8 settings available) |
| Interrupts | • None |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

**• Output frequency of the clock monitor function**

| FRQ2 - 0 Bits | Machine Clock Divide Ratio | When ϕ = 16 MHz | | When ϕ = 8 MHz | | When ϕ = 4 MHz | |
|---|---|---|---|---|---|---|---|
| | | Period | Frequency | Period | Frequency | Period | Frequency |
| $000_B$ | $\phi/2^1$ | 125 ns | 8 MHz | 250 ns | 4 MHz | 500 ns | 2 MHz |
| $001_B$ | $\phi/2^2$ | 250 ns | 4 MHz | 500 ns | 2 MHz | 1.0 µs | 1 MHz |
| $010_B$ | $\phi/2^3$ | 500 ns | 2 MHz | 1.0 µs | 1 MHz | 2.0 µs | 500 kHz |
| $011_B$ | $\phi/2^4$ | 1.0 µs | 1 MHz | 2.0 µs | 500 kHz | 4.0 µs | 250 kHz |
| $100_B$ | $\phi/2^5$ | 2.0 µs | 500 kHz | 4.0 µs | 250 kHz | 8.0 µs | 125 kHz |
| $101_B$ | $\phi/2^6$ | 4.0 µs | 250 kHz | 8.0 µs | 125 kHz | 16.0 µs | 62.5 kHz |
| $110_B$ | $\phi/2^7$ | 8.0 µs | 125 kHz | 16.0 µs | 62.5 kHz | 32.0 µs | 31.25 kHz |
| $111_B$ | $\phi/2^8$ | 16.0 µs | 62.5 kHz | 32.0 µs | 31.25 kHz | 64.0 µs | 15.625 kHz |

**• Block diagram**




— : Undefined

ϕ : Machine clock frequency

## 22. 1 Mbit Flash Memory

- This section describes the flash memory on the MB90F523B and does not apply to evaluation products and MASK ROM versions.
- The flash memory is located in banks FE to FF in the CPU memory map.

**• Flash memory functions**

| | Function |
|---|---|
| Memory size | • 1 Mbit (128 KBytes) |
| Memory configuration | • 128 KWords × 8 bits or 64 KWords × 16 bits |
| Sector configuration | • 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes + 64 KBytes |
| Sector protect function | • Selectable for each sector |
| Programming algorithm | • Automatic programming algorithm (Embedded Algorithm* : Equivalent to MBM29F400TA) |
| Operation commands | • Compatible with JEDEC standard commands<br>• Includes an erase pause and restart function<br>• Data polling and toggle bit write/erase completion<br>• Erasing by sector available (sectors can be combined in any combination) |
| No. of write/erase cycles | • Min 10,000 guaranteed |
| Memory write/erase method | • Can be written and erased using a parallel writer (Minato Electronics model 1890A, Ando Denki AF9704, AF9705, AF9706, AF9708, and AF9709)<br>• Can be written and erased using a dedicated serial writer (YDC AF200, AF210, AF120, and AF110)<br>• Can be written and erased by the program |
| Interrupts | • Write and erase completion interrupts |
| EI²OS support | • Not supported by the extended intelligent I/O service (EI²OS) . |

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

**• Sector configuration of flash memory**

| Flash memory | CPU address | Writer address* |
|---|---|---|
| SA0 (64 Kbyte) | FE0000H<br>FEFFFH | 60000H<br>6FFFFH |
| SA1 (32 Kbyte) | FF0000H<br>FF7FFFH | 70000H<br>77FFFH |
| SA2 (8 Kbyte) | FF8000H<br>FF9FFFH | 78000H<br>79FFFH |
| SA3 (8 Kbyte) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA4 (16 Kbyte) | FFC000H<br>FEFFFFH | 7C000H<br>7FFFFH |

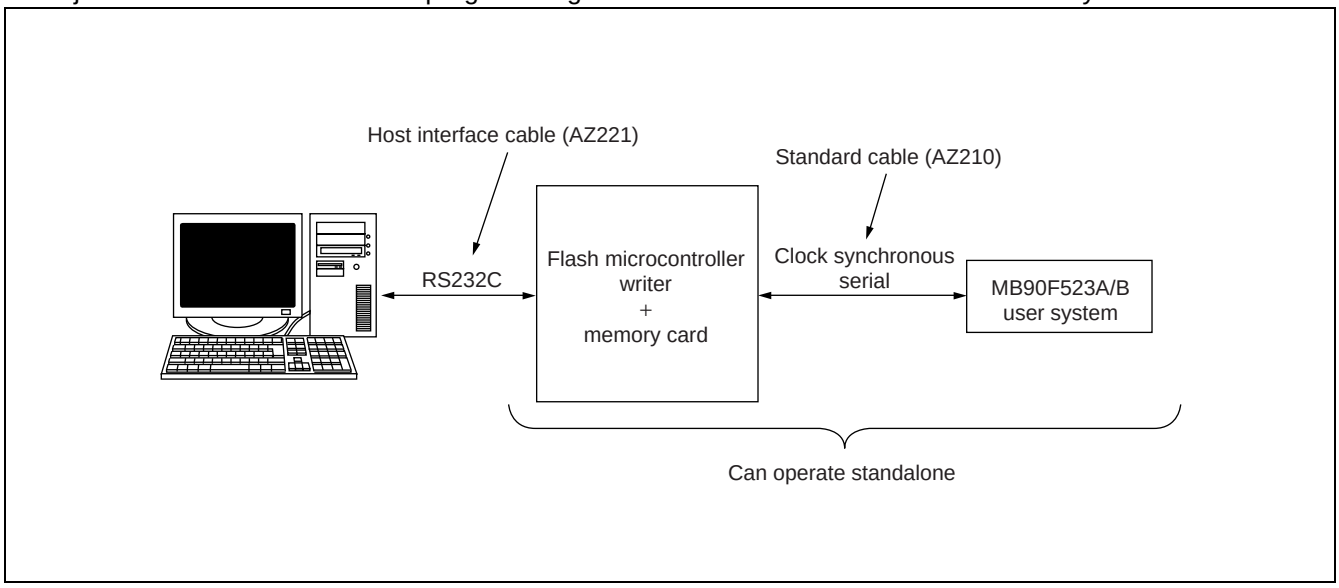
* : The writer address is the address to use instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing using a general-purpose parallel writer.

• **Pins used for Fujitsu standard serial on-board programming**

| Pin | Function | Explanation |
|---|---|---|
| MD2, MD1, MD0 | Mode pins | Setting MD2 = MD1 = 1, MD0 = 0 selects flash memory serial programming mode. |
| X0, X1 | Oscillation input pin | Flash memory serial programming mode uses the PLL clock with the multiplier set to 1 as the machine clock. Set the oscillation frequency used for serial programming to between 3 MHz and 16 MHz. |
| P00, P01 | Write program activation pins | Input P00 = 0 (“L” level) and P01 = 1 (“H” level) |
| RST | Reset pin | — |
| HST | Hardware standby pin | Input an “H” level during flash memory serial programming mode. |
| SIN0 | Serial data input pin | Uses the UART (SCI) in clock synchronous mode. |
| SOT0 | Serial data output pin | |
| SCK0 | Serial clock input pin | |
| C | C pin | Capacitor pin for power supply stabilization. Connect an external capacitor of approx. 0.1 μF. |
| $V_{CC}$ | Power supply voltage pins | If the user system can provide the programming voltage (5 V ± 10%) , do not need to connect to the flash microcontroller writer. |
| $V_{SS}$ | GND pin | Connect to common GND with the flash microcontroller writer. |

• **Overall configuration of connection between serial writer and MB90F523A**

Fujitsu standard serial on-board programming uses a flash microcontroller writer made by YDC.




Note : Contact YDC for details of the functions and operation of the flash microcontroller writer (AF220, AF210, AF120, or AF110) , standard connection cable (AZ210) , and connectors.

## ■ Electrical Characteristics\

### 1. Absolute Maximum Ratings

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *1 |
| | AVRH, AVRL | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *1 |
| | $DV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *4 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *5 |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *6 |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | *4 |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | *5 |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | –100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | –50 | mA | *6 |
| Power consumption | Pd | — | 400 | mW | MB90522A/523A/ F523B |
| | | — | 300 | mW | MB90522B/523B |
| Operating temperature | Ta | –40 | +85 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

*1 : $AV_{CC}$, AVRH, AVRL, and $DV_{CC}$ shall never exceed $V_{CC}$ . AVRH and AVRL shall never exceed $AV_{CC}$. Also, AVRL shall never exceed AVRH.

*2 : $V_{CC} \geq AV_{CC} \geq DV_{CC} \geq 3.0$ V.

*3 : $V_I$ and $V_O$ shall never exceed $V_{CC}$ + 0.3 V.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output current is the average current value for a single pin during a 100 ms period.

*6 : The total average current is the average current for all pins during a 100 ms period.

Note : Average output current = operating current × operating ratio

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | 3.0 | 5.5 | V | |
| Smoothing capacitor | $C_S$ | 0.1 | 1.0 | µF | |
| Operating temperature | Ta | −40 | +85 | °C | |

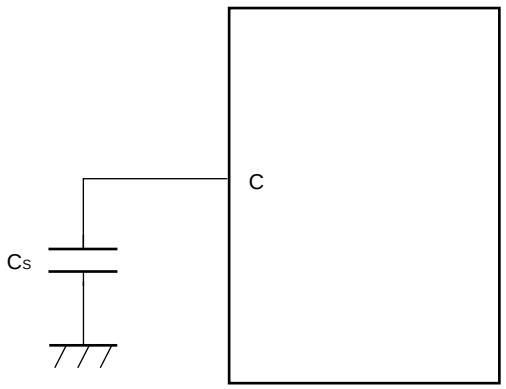
Note : Use a ceramic capacitor or other capacitor with equivalent frequency characteristics. The capacitance of the smoothing capacitor connected to the $V_{CC}$ pin must be greater than $C_S$.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

C pin diagram



### 3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0$ V ± 10%, $AV_{SS} = V_{SS} = DV_{SS} = 0.0$ V, Ta = –40 °C to +85 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHS}$ | P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7 | $V_{CC}$ = 3.0 V to 5.5 V | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHM}$ | MD0 to MD2 | | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{ILS}$ | P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7 | | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| | $V_{ILM}$ | MD0 to MD2 | | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | |
| "H" level output voltage | $V_{OH}$ | All output pins other than P90 to P97 | $V_{CC}$ = 4.5 V, $I_{OH}$ = –2.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | All output pins | $V_{CC}$ = 4.5 V, $I_{OL}$ = 2.0 mA | — | — | 0.4 | V | |
| Input leak current | $I_{IL}$ | All output pins other than P90 to P97 | $V_{CC}$ = 5.5 V, $V_{SS} < V_I < V_{CC}$ | – 5 | — | 5 | µA | |
| Open-drain output leak current | $I_{leak}$ | P90 to P97 output pins | — | — | 0.1 | 5 | µA | |
| Pull-up resistor | $R_{UP}$ | P00 to P07, P10 to P17 P40 to P47, MD0, MD1 | — | 50 | 100 | 200 | kΩ | |
| Pull-down resistor | $R_{DOWN}$ | MD2 | | 50 | 100 | 200 | kΩ | |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | For $V_{CC}$ = 5 V, internal frequency = 16 MHz, normal operation | — | 40 | 65 | mA | MB90522A/523A |
| | | | | — | 30 | 60 | mA | MB90F523B |
| | | | | — | 30 | 40 | mA | MB90522B/523B |

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = $DV_{SS}$ = 0.0 V, Ta = –40 °C to +85 °C)

| Parameter | Sym-bol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | For $V_{CC}$ = 5 V, internal frequency = 8 MHz, normal operation | — | 20 | 25 | mA | MB90522A/523A |
| | | | | — | 15 | 20 | mA | MB90F523B |
| | | | | — | 15 | 20 | mA | MB90522B/523B |
| | | | For $V_{CC}$ = 5 V, internal frequency = 16 MHz, A/D operation in progress | — | 50 | 70 | mA | MB90522A/523A |
| | | | | — | 45 | 65 | mA | MB90F523B |
| | | | | — | 35 | 45 | mA | MB90522B/523B |
| | | | For $V_{CC}$ = 5 V, internal frequency = 8 MHz, A/D operation in progress | — | 25 | 30 | mA | MB90522A/523A |
| | | | | — | 20 | 25 | mA | MB90F523B |
| | | | | — | 20 | 25 | mA | MB90522B/523B |
| | | | For $V_{CC}$ = 5 V, internal frequency = 16 MHz, D/A operation in progress | — | 55 | 70 | mA | MB90522A/523A |
| | | | | — | 50 | 70 | mA | MB90F523B |
| | | | | — | 40 | 50 | mA | MB90522B/523B |
| | | | For $V_{CC}$ = 5 V, internal frequency = 8 MHz, D/A operation in progress | — | 30 | 35 | mA | MB90522A/523A |
| | | | | — | 25 | 30 | mA | MB90F523B |
| | | | | — | 20 | 25 | mA | MB90522B/523B |
| | | | Writing or erasing flash memory | — | 50 | 75 | mA | MB90F523B |
| | $I_{CCS}$ | | For $V_{CC}$ = 5 V, internal frequency = 16 MHz, sleep mode | — | 8 | 15 | mA | MB90522A/523A |
| | | | | — | 15 | 20 | mA | MB90F523B/522B/523B |
| | | | For $V_{CC}$ = 5 V, internal frequency = 8 MHz, sleep mode | — | 7 | 10 | mA | MB90522A/523A |
| | | | | — | 12 | 18 | mA | MB90F523B/522B/523B |
| | $I_{CCL}$ | | For $V_{CC}$ = 5 V, internal frequency = 8 kHz, sub-clock mode, Ta = 25 °C | — | 0.1 | 1.0 | mA | MB90522A/523A/522B/523B |
| | | | | — | 4 | 7 | mA | MB90F523B |

*(Continued)*

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = $DV_{SS}$ = 0.0 V, Ta = –40 °C to +85 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CCLS}$ | $V_{CC}$ | For $V_{CC}$ = 5 V, internal frequency = 8 kHz, sub-sleep mode, Ta = 25 °C | — | 30 | 50 | µA | |
| | $I_{CCT}$ | | For $V_{CC}$ = 5 V, internal frequency = 8 kHz, clock mode, Ta = 25 °C | — | 15 | 30 | µA | |
| | $I_{CCH}$ | | Sleep mode, Ta = 25 °C | — | 5 | 20 | µA | |
| Input capacitance | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, C, $V_{CC}$, and $V_{SS}$ | — | — | 10 | 80 | pF | |
| LCD divider resistor | $R_{LCD}$ | V0 – V1, V1 – V2, V2 – V3 | — | 50 | 100 | 200 | kΩ | |
| Output impedance for COM0 to COM3 | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = 5.0 V | — | — | 2.5 | kΩ | |
| Output impedance for SEG00 to SEG31 | $R_{VSEG}$ | SEG00 to SEG31 | | — | — | 15 | kΩ | |
| LCDC leak current | $I_{LCDC}$ | V0 to V3, COM0 to COM3, SEG00 to SEG31 | — | — | — | ±5 | µA | |

* : Current values are provisional and are subject to change without notice to allow for improvements to the characteristics. The power supply current is measured with an external clock.

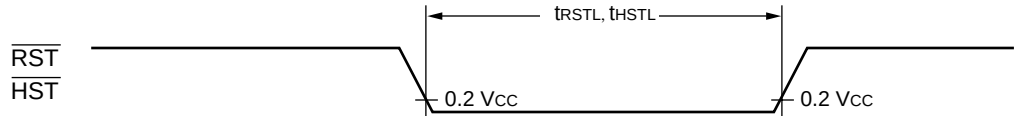
## 4. AC Characteristics

### (1) Reset and Hardware Standby Input Timings

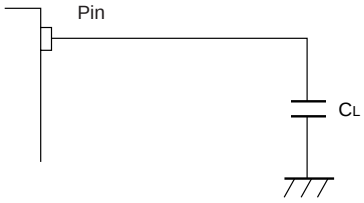
($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = $DV_{SS}$ = 0.0 V, Ta = –40 °C to +85 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 4 $t_{CP}$* | — | ns | |
| Hardware standby input time | $t_{HSTL}$ | $\overline{HST}$ | | 4 $t_{CP}$* | — | ns | |

* : See “ (3) Clock Timings” for more information about $t_{CP}$ (internal operating clock cycle time) .




**Measurement conditions for AC ratings**




$C_L$ is the load capacitance for the pin during testing.

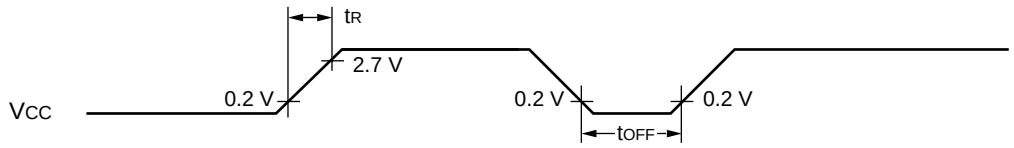
### (2) Power-On Reset

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

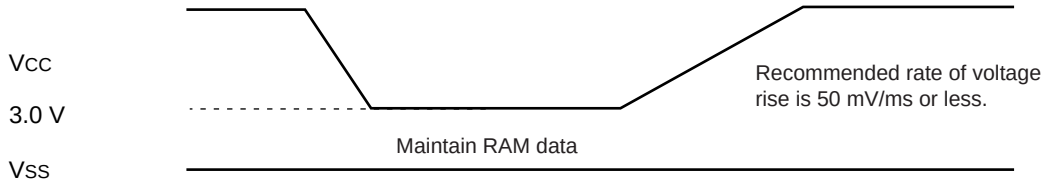
| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| Power supply rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | * |
| Power supply cutoff time | $t_{OFF}$ | $V_{CC}$ | | 4 | — | ms | For repeated operation |

* : $V_{CC}$ must be less than 0.2 V before power-on.

Notes : • The above rating values are for generating a power-on reset.
- When $\overline{HST}$ = "L", always apply the power supply in accordance with the above ratings regardless of whether a power-on reset is required.
- Some internal registers are only initialized by a power-on reset. Always apply the power supply in cordance with the above ratings if you wish to initialize these registers.




Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly as shown below. Also, changes to the supply voltage should be performed when the PLL clock is not in use. The PLL clock may be used, however, if the rate of voltage change is 1 V/s or less.

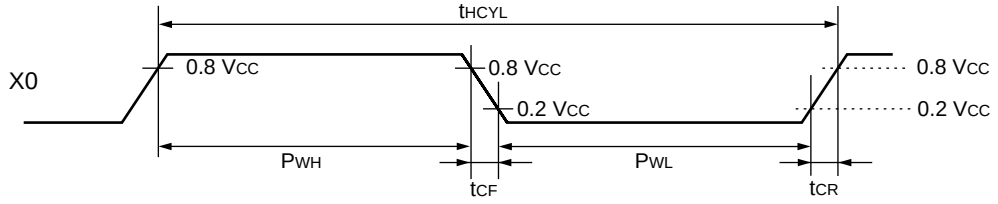


### (3) Clock Timings

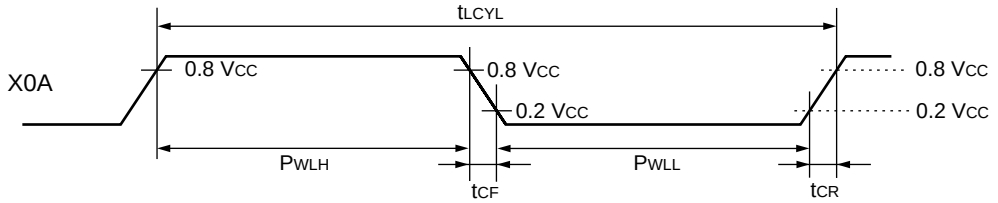
($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_C$ | X0, X1 | — | 3 | — | 16 | MHz | |
| | $F_{CL}$ | X0A, X1A | — | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | — | 62.5 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$ $P_{WL}$ | X0 | — | 10 | — | — | ns | Recommended duty ratio = 30% to 70% |
| | $P_{WLH}$ $P_{WLL}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rise/fall time | $t_{CR}$ $t_{CF}$ | X0 | — | — | — | 5 | ns | When using an external clock |
| Internal operating clock frequency | $f_{CP}$ | — | — | 1.5 | — | 16 | MHz | When using main clock |
| | $f_{LCP}$ | — | — | — | 8.192 | — | kHz | When using sub-clock |
| Internal operating clock cycle time | $t_{CP}$ | — | — | 62.5 | — | 666 | ns | When using main clock |
| | $t_{LCP}$ | — | — | — | 122.1 | — | µs | When using sub-clock |

**X0 and X1 clock timing**

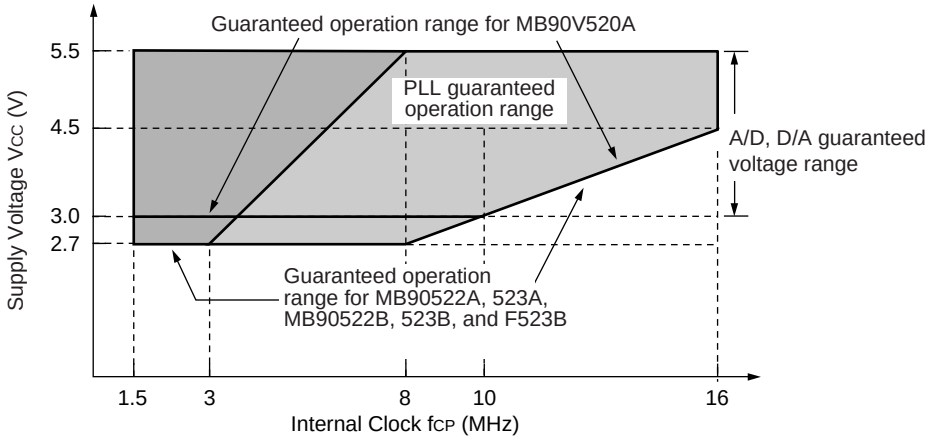



**X0A and X1A clock timing**

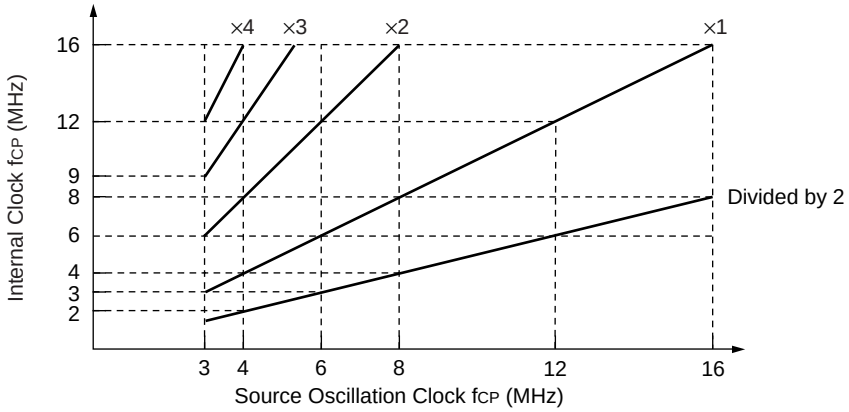


**PLL guaranteed operation range**

Relationship between internal operating clock frequency and power supply voltage



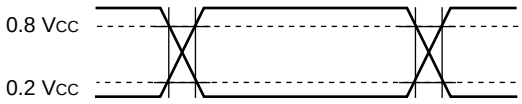

Relationship between oscillation frequency and internal operating clock frequency




The AC ratings are measured at the following reference voltages.

**Input signal waveform**

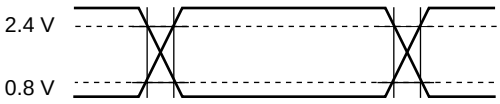
Hysteresis input pin




Pins other than hysteresis input or MD input pins


**Output signal waveform**

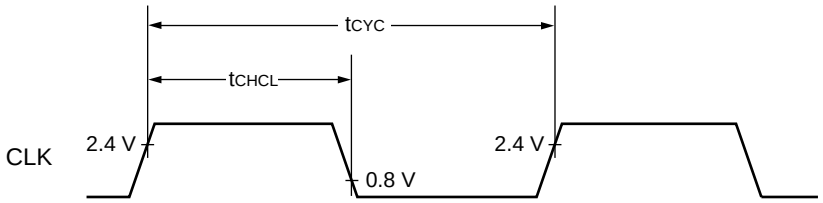
Output pin



### (4) Clock Output Timings

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| Cycle time | $t_{CYC}$ | CLK | $V_{CC} = 5.0\ V \pm 10\%$ | 62.5 | — | ns | |
| CLK ↑ → CLK ↓ | $t_{CHCL}$ | | | 20 | — | ns | |



### (5) UART (SCI) Timings

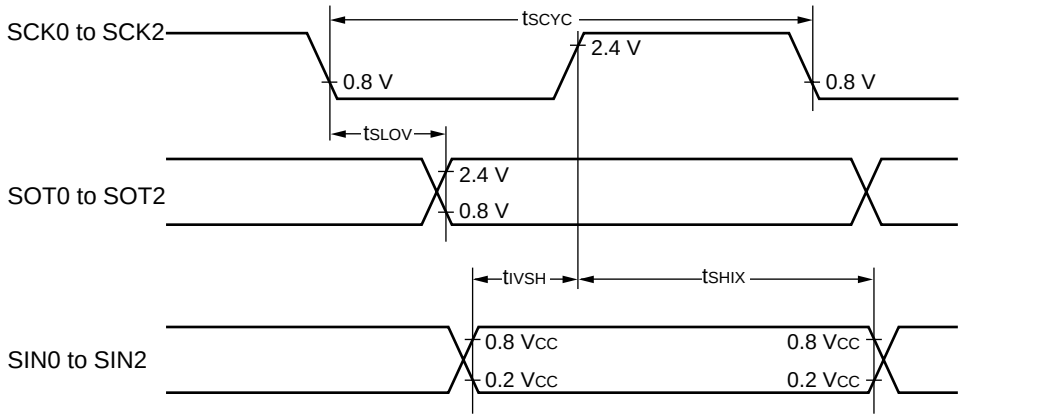
($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK2 | Internal shift clock mode, output pin load is $C_L$ = 80 pF + 1 TTL | 8 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK2<br>SOT0 to SOT2 | | −80 | 80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK2<br>SIN0 to SIN2 | | 100 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK2<br>SIN0 to SIN2 | | 60 | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0 to SCK2 | External shift clock mode, output pin load is $C_L$ = 80 pF + 1 TTL | 4 $t_{CP}$* | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK0 to SCK2 | | 4 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK2<br>SOT0 to SOT2 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK2<br>SIN0 to SIN2 | | 60 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK2<br>SIN0 to SIN2 | | 60 | — | ns | |

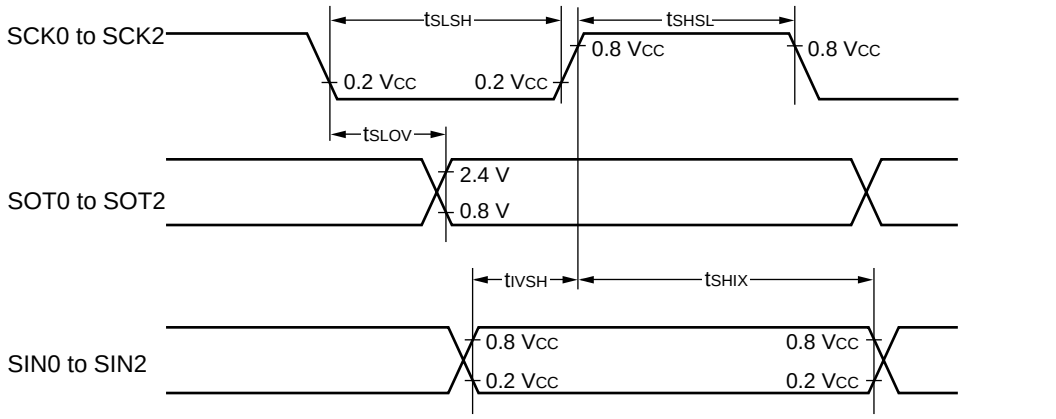
* : See “ (3) Clock Timings” for more information about $t_{CP}$ (internal operating clock cycle time) .

Notes : • These are the AC ratings for CLK synchronous mode.
• $C_L$ is the load capacitor connected to the pin for testing.

**Internal shift clock mode**




**External shift clock mode**

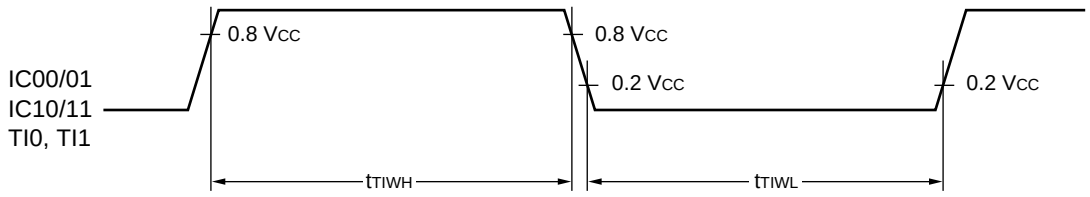


### (6) Timer Input Timings

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | IC00/01,<br>IC10/11<br>TI0, TI1 | — | 4 $t_{CP}$* | — | ns | |

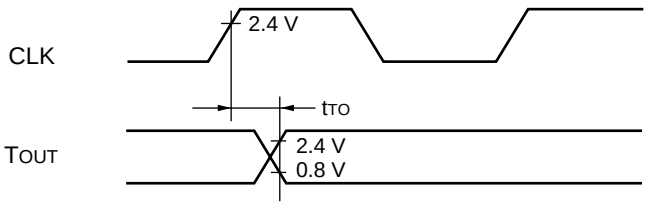
* : See “ (3) Clock Timings” for more information about $t_{CP}$ (internal operating clock cycle time) .




### (7) Timer Output Timings

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $Ta = -40\ °C$ to $+85\ °C$)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | | |
| CLK ↑ → $T_{OUT}$ change time | $t_{TO}$ | OUT0 to OUT7<br>PG00/01<br>PG10/11<br>TO0, TO1 | — | 30 | — | ns | |




($T_{OUT}$ : OUT0 to OUT7, PG00/01, PG10/11, TO0, TO1)

## 5. Electrical Characteristics for the A/D Converter

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = DV_{SS} = 0.0\ V$, $3.0\ V \le AVRH - AVRL$, $Ta = -40\ °C$ to $+85\ °C$)

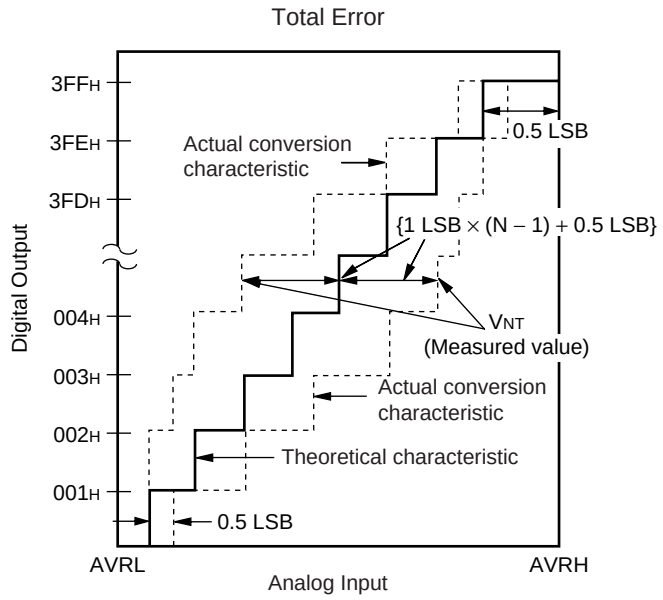
| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 8/10 | — | bit | |
| Total error | — | — | — | — | ±5.0 | LSB | |
| Linearity error | — | — | — | — | ±2.5 | LSB | |
| Differential linearity error | — | — | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ − 3.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 4.5 LSB | mV | |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH − 6.5 LSB | AVRH − 1.5 LSB | AVRH + 1.5 LSB | mV | |
| A/D conversion time | — | — | 163 tcp | — | — | ns | At machine clock = 16 MHz |
| Compare time | — | — | 99 tcp | — | — | ns | At machine clock = 16 MHz |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | AVRL | — | AVRH | V | |
| Reference voltage | — | AVRH | AVRL + 3.0 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH − 3.0 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 5 | — | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage supply current | $I_R$ | AVRH | — | 400 | — | µA | |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Variation between channels | — | AN0 to AN7 | — | — | 4 | LSB | |

* : Current when 8/10-bit A/D converter not used and CPU in stop mode ($V_{CC} = AV_{CC} = AVRH = 5.0\ V$)

Note : See " (3) Clock Timings" in "4. AC Ratings" for more information about $t_{CP}$ (internal operating clock cycle time) .

## 6. A/D Converter Glossary

| | | |
|---|---|---|
| Resolution | : | The change in analog voltage that can be recognized by the A/D converter. |
| Linearity error | : | The deviation between the actual conversion characteristics and the line linking the zero transition point (“00 0000 0000B” ⟷ “00 0000 0001B”) and the full scale transition point (“11 1111 1110B” ⟷ “11 1111 1111B”) . |
| Differential linearity error | : | The variation from the ideal input voltage required to change the output code by 1 LSB. |
| Total error | : | The total error is the difference between the actual value and the theoretical value. This includes the zero-transition error, full-scale transition error, and linearity error. |




$$1\ \text{LSB} = (\text{Theoretical value})\frac{\text{AVRH} - \text{AVRL}}{1024^{*}}\ [\text{V}]$$

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$V_{OT}$ (Theoretical value) = AVRL + 0.5 LSB [V]

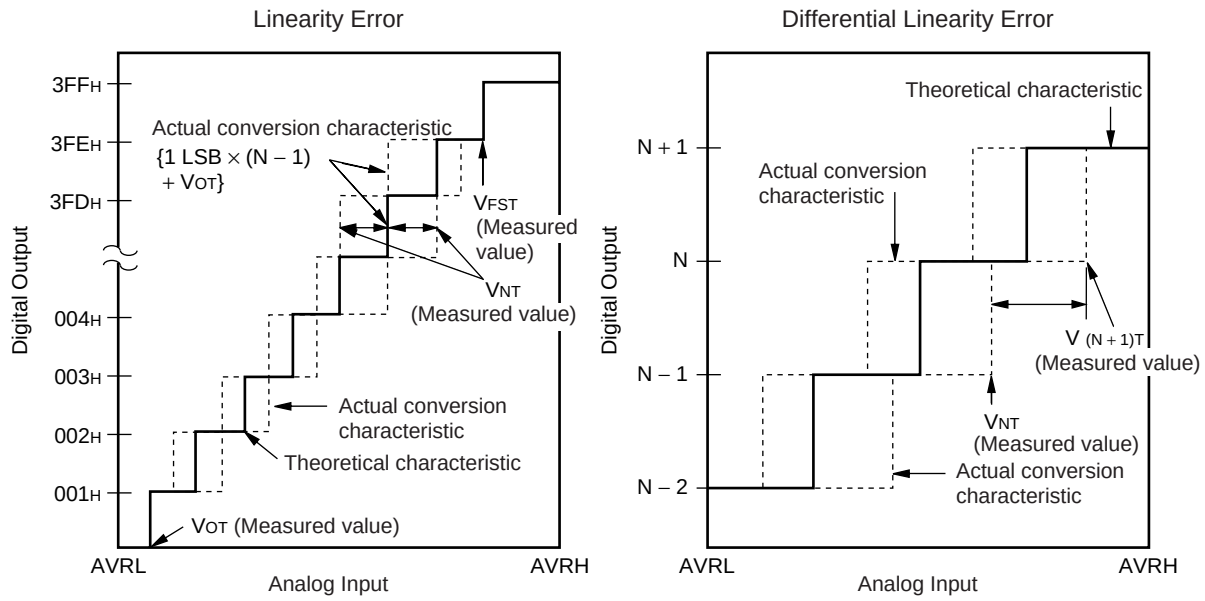
$V_{FST}$ (Theoretical value) = AVRH – 1.5 LSB [V]

$V_{NT}$ : Voltage at which digital output changes from (N – 1) to N

* : For 10-bit resolution, this value is 1024 ($2^{10}$) . For 8-bit resolution, this value is 256 ($2^{8}$) .

*(Continued)*

*(Continued)*




Linearity error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + V_{OT}\}}{1\ LSB}$ [LSB]

Differential linearity error for digital output N = $\frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1\ LSB$ [LSB]

1 LSB = $\frac{V_{FST} - V_{OT}}{1022^{*}}$ [V]

$V_{OT}$ : Voltage at which digital output changes from "$000_H$" to "$001_H$"
$V_{FST}$ : Voltage at which digital output changes from "$3FE_H$" to "$3FF_H$"

* : For 10-bit resolution, this value is 1022 ($2^{10} - 2$) . For 8-bit resolution, this value is 254 ($2^8 - 2$) .

## 7. Notes for A/D Conversion

The recommended external circuit impedance of analog inputs for MB90V520 is approximately 5 kΩ or less, that for MB90F523B is approximately 15.5 kΩ or less, and that for MB90522A/523A/522B/523B is approximately 10 kΩ or less.

If using an external capacitor, the capacitance should be several thousand times the level of the chip's internal capacitor to allow for the partial potential between the external and internal capacitance.

If the impedance of the external circuit is too high, the analog voltage sampling interval may be too short. (for sampling time = 4 µs, machine clock frequency = 16 MHz) .

- Block diagram of analog input circuit model


MB90522A/523A/522B/523B
$R_{ON}$ = 2.2 kΩ approx.
C = 45 pF approx.
MB90F523B
$R_{ON}$ = 2.6 kΩ approx.
C = 28 pF approx.

Note : The values listed are an indication only.

- **Error**

The relative error increases as |AVRH – AVRL| becomes smaller.

## 8. Electrical Characteristics for the D/A Converter

($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = $DV_{SS}$ = 0.0 V, Ta = –40 °C to +85 °C)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 8 | — | bit | |
| Differential linearity error | — | — | — | — | ±0.9 | LSB | |
| Absolute accuracy | — | — | — | — | ±1.2 | % | |
| Linearity error | — | — | — | — | ±1.5 | LSB | |
| Conversion time | — | — | — | 10 | 20 | µs | For load capacitance = 20 pF |
| Analog reference voltage | — | $DV_{CC}$ | $V_{SS}$ + 3.0 | — | $AV_{CC}$ | V | |
| Current consumption for reference voltage | $I_{DVR}$ | $DV_{CC}$ | — | 120 | 300 | µA | |
| | $I_{DVRS}$ | | — | — | 10 | µA | Stop mode |
| Analog output impedance | — | — | — | 20 | — | kΩ | |

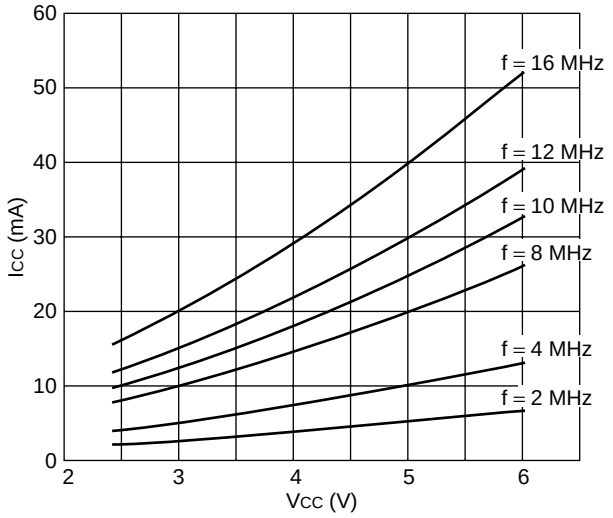
## 9. Flash Memory Program/Erase

| Parameter | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | Ta = + 25 °C $V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes 00H programming prior erasure |
| Chip erase time | | — | 5 | — | s | Excludes 00H programming prior erasure |
| Word (16-bit width) programming time | | — | 16 | 3,600 | µs | Excludes system-level overhead |
| Program/Erase cycle | — | 10,000 | — | — | cycle | |
| Data hold time | — | 100 K | — | — | h | |

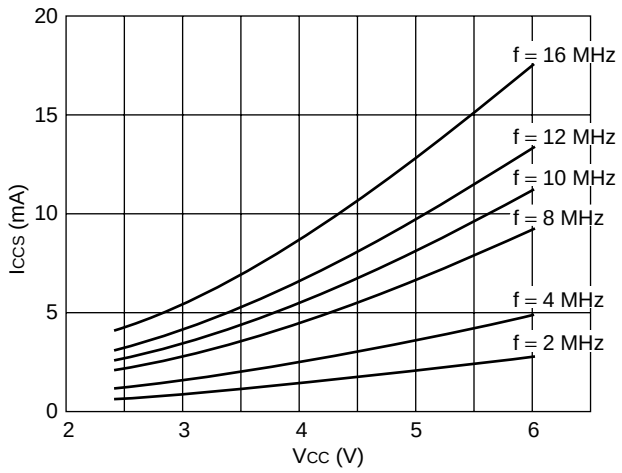
## ■ EXAMPLE CHARACTERISTICS

**Power supply current (MB90523A)**

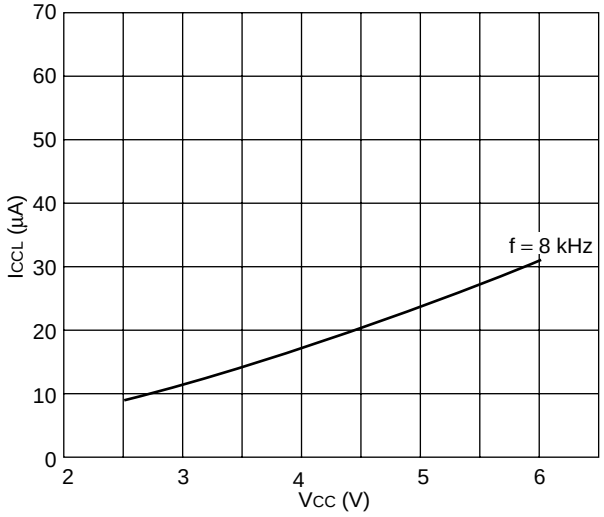
$I_{CC}$ – $V_{CC}$
Ta = +25 °C, External clock input



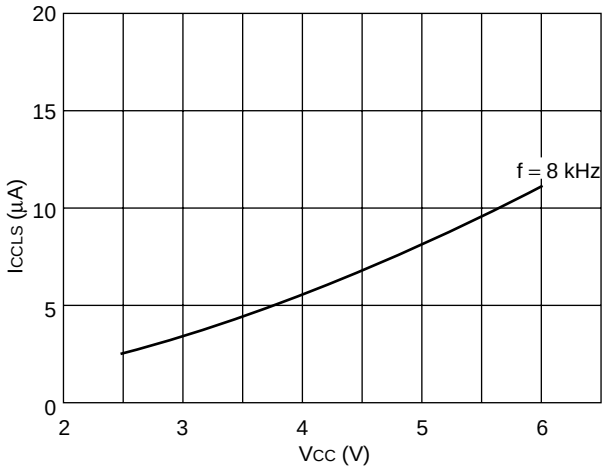

$I_{CCS}$ – $V_{CC}$
Ta = +25 °C, External clock input




$I_{CCL}$ – $V_{CC}$
Ta = +25 °C, External clock input




$I_{CCLS}$ – $V_{CC}$
Ta = +25 °C, External clock input

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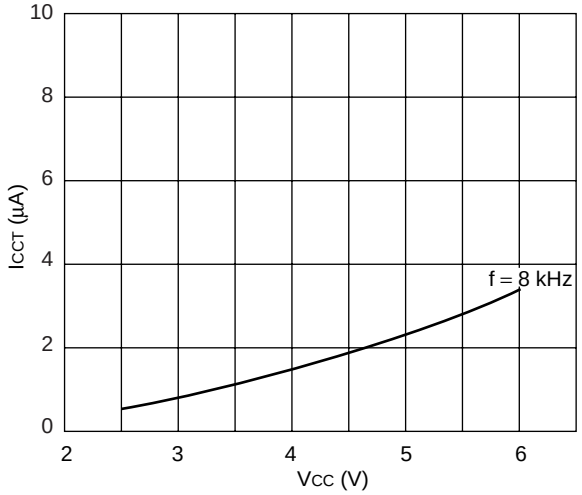
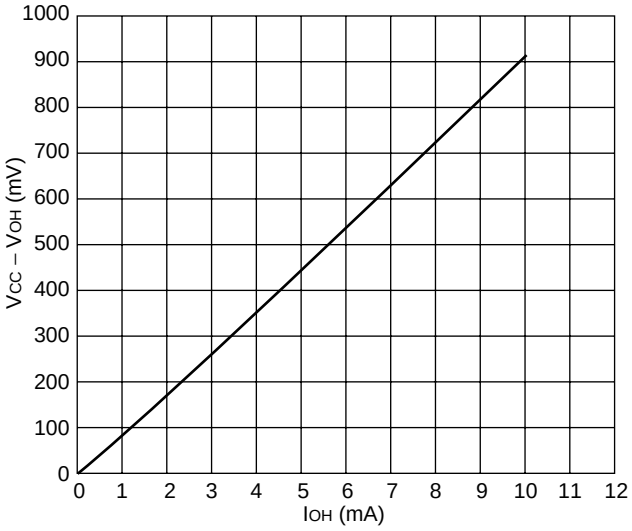
*(Continued)*

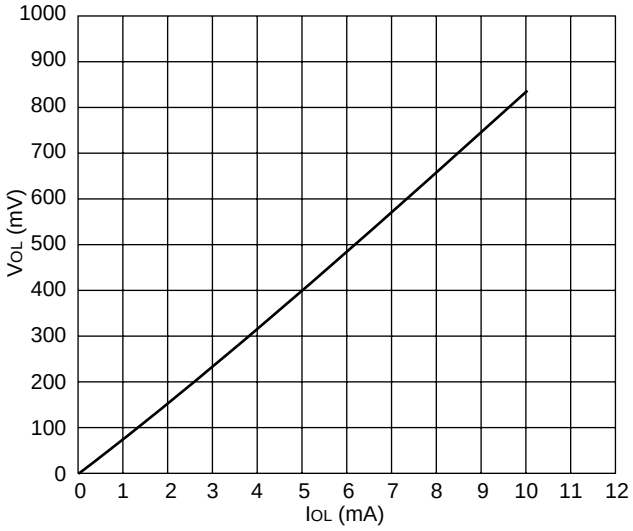
$I_{CCT}$ – $V_{CC}$
Ta = +25 °C, External clock input




Example MB90523A $V_{OH}$ – $I_{OH}$ Characteristics
Ta = +25 °C, $V_{CC}$ = 4.5 V




Example MB90523A $V_{OL}$ – $I_{OL}$ Characteristics
Ta = +25 °C, $V_{CC}$ = 4.5 V



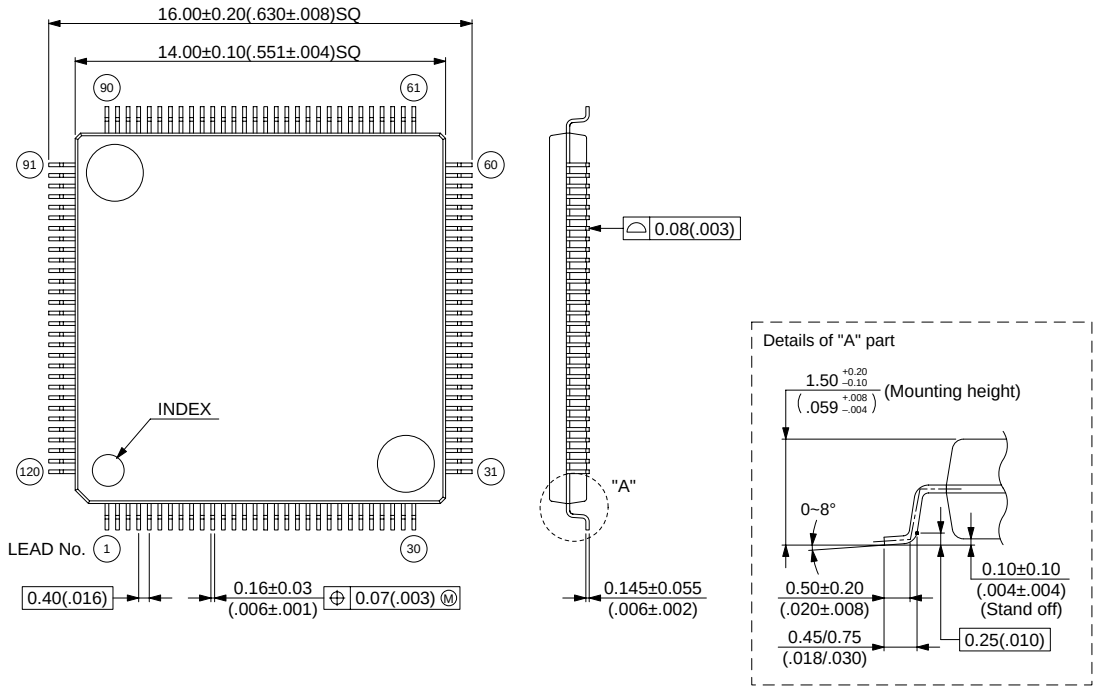
## ■ ORDERING INFORMATION

| Part No. | Package | Remarks |
|---|---|---|
| MB90522APFF<br>MB90523APFF<br>MB90522BPFF<br>MB90F523BPFF | 120-pin, Plastic LQFP<br>(FPT-120P-M05) | |
| MB90522APFV<br>MB90523APFV<br>MB90522BPFV<br>MB90F523BPFV | 120-pin, Plastic QFP<br>(FPT-120P-M13) | |

## ■ PACKAGE DIMENSIONS

120-pin Plastic LQFP
(FPT-120P-M05)

* : Pins width and pins thickness include plating thickness.





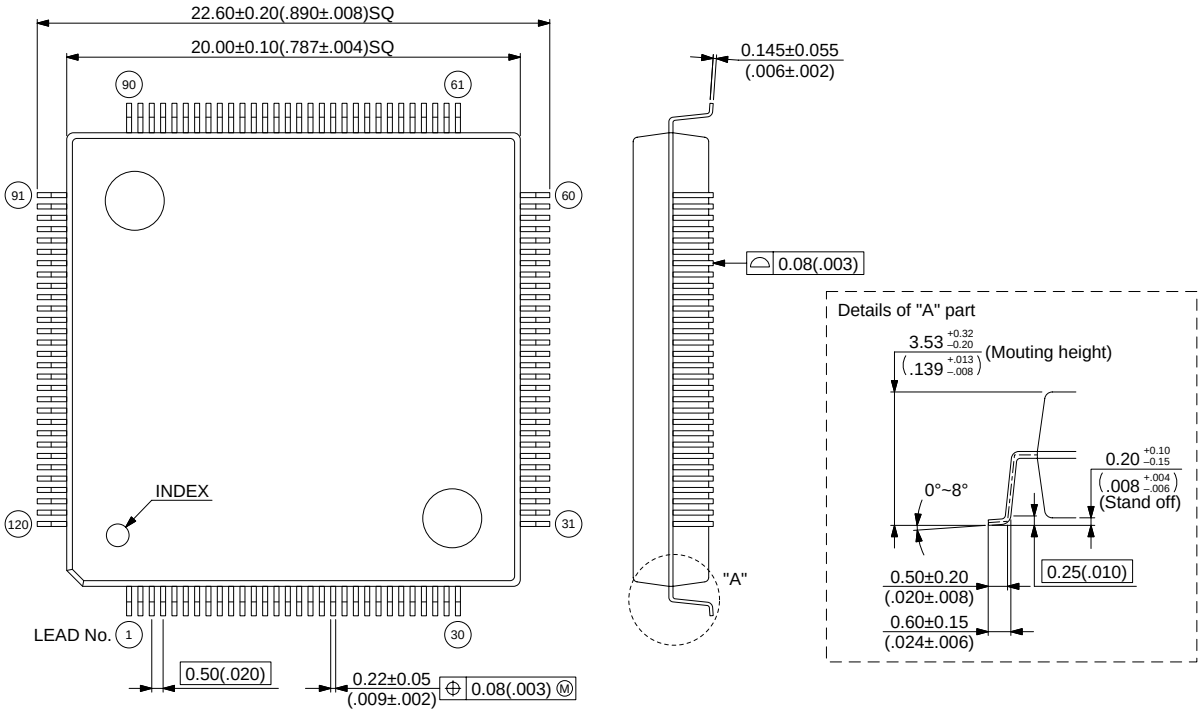

Dimensions in mm (inches)

*(Continued)*

*(Continued)*

120-pin Plastic QFP
(FPT-120P-M13)

* : Pins width and pins thickness include plating thickness.






Dimensions in mm (inches)

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